# ADC08161 500 ns A/D Converter with S/H Function and 2.5V Bandgap Reference

**Check for Samples: ADC08161**

## FEATURES

- **No external clock required**
- **Analog input voltage range from GND to $V^+$**
- **2.5V bandgap reference**

## APPLICATIONS

- **Mobile telecommunications**
- **Hard-disk drives**
- **Instrumentation**
- **High-speed data acquisition systems**

## DESCRIPTION

**This product is on Lifetime Buy and is NOT RECOMMENDED for new designs.**

Using a patented multi-step A/D conversion technique, the 8-bit ADC08161 CMOS A/D converter offers 500 ns conversion time, internal sample-and-hold (S/H), a 2.5V bandgap reference, and dissipates only 100 mW of power. The ADC08161 performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LBSs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, this part has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

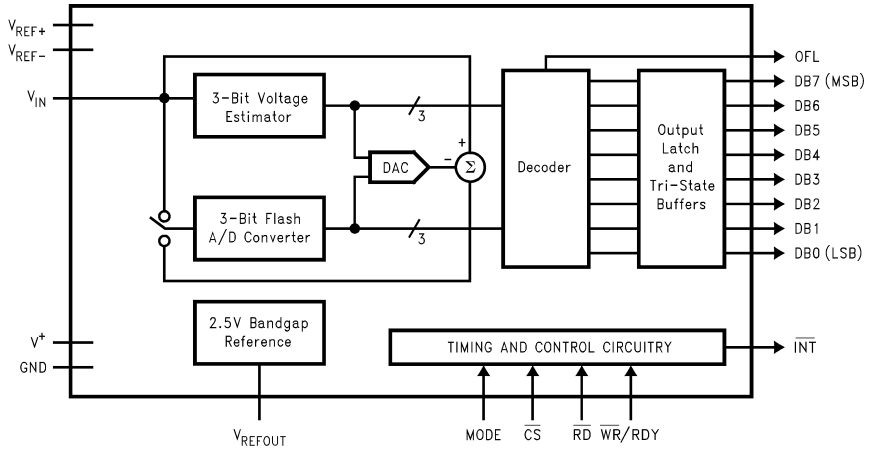
**Table 1. Key Specifications**

| | VALUE | UNIT |
|---|---|---|
| Resolution | 8 | Bits |
| Conversion time ($t_{CONV}$) | 560 ($\overline{WR}$-$\overline{RD}$ Mode) | ns max |
| Full power bandwidth | 300 | kHz (typ) |
| Throughput rate | 1.5 | MHz min |
| Power dissipation | 100 | mW max |
| Total unadjusted error | ±½ LSB and ±1 LSB max | |

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Block Diagram




## Connection Diagram

### Wide-Body Small-Outline Package

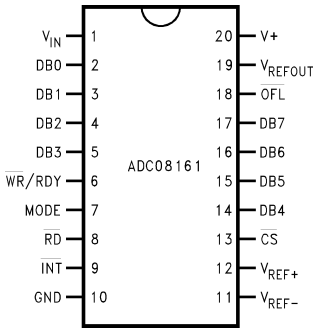



**Figure 1. See NS Package Number M20B**

### Pin Descriptions

| | |
|---|---|
| $V_{IN}$ | This is the analog input. The input range is GND–50 mV = $V_{INPUT}$ = $V^+$ + 50 mV. |
| DB0–DB7 | TRI-STATE® data outputs—bit 0 (LSB) through bit 7 (MSB). |
| $\overline{WR}$ /RDY | **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)<br>**$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the rising edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (Figure 7 Figure 8 Figure 9).<br>**$\overline{RD}$ Mode** (Logic low applied to MODE pin)<br>**RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and returns high at the end of conversion. |
| MODE | **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$** ) selection input– This pin is pulled to a logic low through an internal 50 µA current sink when left unconnected.<br>**$\overline{RD}$ Mode** is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.<br>**$\overline{WR}$-$\overline{RD}$ Mode** is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data. |

## Pin Descriptions (continued)

| | |
|---|---|
| $\overline{RD}$ | **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin)<br>This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (Figure 7 Figure 8 Figure 9).<br>**$\overline{RD}$ Mode** (logic low on the MODE pin)<br>With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (Figure 6 Figure 10). |
| $\overline{INT}$ | This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$. |
| GND | This is the power supply ground pin. The ground pin should be connected to a “clean” ground reference point. |
| $V_{REF-}$, $V_{REF+}$ | These are the reference voltage inputs. They may be placed at any voltage between GND - 50 mV and $V^+$ + 50 mV, but $V_{REF+}$ must be greater than $V_{REF-}$. Ideally, an input voltage equal to $V_{REF-}$ produces an output code of 0, and an input voltage greater than $V_{REF+}$ - 1.5 LSB produces an output code of 255.<br>For the ADC08161 an input voltage that exceeds $V^+$ by more than 100 mV or is below GND by more than 100 mV will create conversion errors. |
| $\overline{CS}$ | This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals. |
| $\overline{OFL}$ | Overflow Output. If the analog input is higher than $V_{REF+}$, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08161s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read. |
| $V^+$ | Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 µF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible. |
| $V_{REFOUT}$ | The internal bandgap reference's 2.5V output is available on this pin. Use a 220 µF bypass capacitor between this pin and analog ground. |

## Absolute Maximum Ratings (1) (2)

| | |
|---|---|
| Supply Voltage ($V^+$) | 6V |
| Logic Control Inputs | −0.3V to $V^+$ + 0.3V |
| Voltage at Other Inputs and Outputs | −0.3V to $V^+$ + 0.3V |
| Input Current at Any Pin (3) | 5 mA |
| Package Input Current (3) | 20 mA |
| Power Dissipation (4) | 875 mW |
| Lead Temperature (5) | |
| (Vapor Phase, 60 sec.) | +215°C |
| (Infrared, 15 sec.) | +220°C |
| Storage Temperature | −65°C to +150°C |
| ESD Susceptibility (6) | 750V |

(1) All voltages are measured with respect to the GND pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) When the input voltage ($V_{IN}$) at any pin exceeds the power supply voltage ($V_{IN}$ < GND or $V_{IN}$ > $V^+$), the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current specification limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.
(4) The power dissipation of this device under normal operation should never exceed 875 mW (Quiescent Power Dissipation + TTL Loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (e.g., when any input or output exceeds the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$ (maximum junction temperature), $\theta_{JA}$ (package junction to ambient thermal resistance), and $T_A$ (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX}$ = 105°C and $\theta_{JA}$ = 85°C/W.
(5) See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

## Operating Ratings (1)

| | |
|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
| ADC08161CIWM | $-40°C \le T_A \le 85°C$ |
| Supply Voltage, ($V^+$) | 4.5V to 5.5V |

(1) All voltages are measured with respect to the GND pin, unless otherwise specified.

## Converter Characteristics

The following specifications apply for $\overline{RD}$ Mode, $V^+$ = 5V, $V_{REF+}$ = 5V, and $V_{REF-}$ = GND unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$ = 25°C.

| Symbol | Parameter | Conditions | Typical (1) | Limits (2) | Units (Limit) |
|---|---|---|---|---|---|
| INL | Integral Non Linearity | $V_{REF}$ = 5V | | **±1** | LSB (max) |
| TUE | Total Unadjusted Error (3) | $V_{REF}$ = 5V | | **±1** | LSB (max) |
| INL | Integral Non Linearity | $V_{REF}$ = 2.5V | | **±1** | LSB (max) |
| TUE | Total Unadjusted Error | $V_{REF}$ = 2.5V | | **±1** | LSB (max) |
| | Missing Codes | $V_{REF}$ = 5V | | **0** | Bits (max) |
| | | $V_{REF}$ = 2.5V | | **0** | Bits (max) |
| | Reference Input Resistance | | 700 | **500** | Ω (min) |
| | | | 700 | **1250** | Ω (max) |
| $V_{REF+}$ | Positive Reference Input Voltage | | | **$V_{REF-}$** | V (min) |
| | | | | **$V^+$** | V (max) |
| $V_{REF-}$ | Negative Reference Input Voltage | | | **GND** | V (min) |
| | | | | **$V_{REF+}$** | V (max) |
| $V_{IN}$ | Analog Input Voltage | (4) | | **GND − 0.1** | V (min) |
| | | | | **$V^+$ + 0.1** | V (max) |
| | On-Channel Input Current | On Channel Input = 5V, | | | |
| | | Off Channel Input = 0V | −0.4 | **−20** | µA (max) |
| | | (5) | | | |
| | | On Channel Input = 0V, | | | |
| | | Off Channel Input = 5V | −0.4 | **−20** | µA (max) |
| | | (5) | | | |
| PSS | Power Supply Sensitivity | All Codes Tested, $V_{REF}$ = 4.75V, $V^+$ = 5V ±5%, | ±1/16 | **±½** | LSB (max) |
| | Effective Bits | $V_{IN}$ = 4.85 $V_{p-p}$ , $f_{IN}$ = 20 Hz to 20 kHz | 7.8 | | Bits |
| | Full-Power Bandwidth | $V_{IN}$ = 4.85 $V_{p-p}$ | 300 | | kHz |
| THD | Total Harmonic Distortion | $V_{IN}$ = 4.85 $V_{p-p}$, $f_{IN}$ = 20 Hz to 20 kHz | 0.5 | | % |
| S/N | Signal-to-Noise Ratio | $V_{IN}$ = 4.85 $V_{p-p}$, $f_{IN}$ = 20 Hz to 20 kHz | 50 | | dB |
| IMD | Intermodulation Distortion | $V_{IN}$ = 4.85 $V_{p-p}$ $f_{IN}$ = 20 Hz to 20 kHz | 50 | | dB |
| $C_{VIN}$ | Analog Input Capacitance | | 25 | | pF |

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are to AOQL (Average Output Quality Level).
(3) Total unadjusted error includes offset, full-scale, and linearity errors.
(4) Two on-chip diodes are tied to each analog input and are reversed biased during normal operation. One is connected to $V^+$ and the other is connected to GND. They will become forward biased and conduct when an analog input voltage is equal to or greater than one diode drop above $V^+$ or below GND. Therefore, caution should be exercised when testing with $V^+$ = 4.5V. Analog inputs with magnitudes equal to 5V can cause an input diode to conduct, especially at elevated temperatures. This can create conversion errors for analog signals near full-scale. The specification allows 50 mV forward bias on either diode; e.g., the output code will be correct as long as the analog input signal does not exceed the supply voltage by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. An absolute analog input signal voltage range of 0V ≤ $V_{IN}$ ≤ 5V can be achieved by ensuring that the minimum supply voltage applied to $V^+$ is 4.950V over temperature variations, initial tolerance, and loading.
(5) Off-channel leakage current is measured on the on-channel selection.

## AC Electrical Characteristics

The following specifications apply for $V^+$ = 5V, $t_r = t_f$ = 10 ns, $V_{REF+}$ = 5V, $V_{REF-}$ = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$ = 25°C.

| Symbol | Parameter | Conditions | Typical (1) | Limit (2) | Units (Limit) |
|---|---|---|---|---|---|
| $t_{\overline{WR}}$ | Write Time | Mode Pin to $V^+$ (Figure 7 Figure 8 Figure 9) | 100 | **100** | ns (min) |
| $t_{\overline{RD}}$ | Read Time (Time from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{RD}$ ) | Mode Pin to $V^+$, (Figure 7) | 350 | **350** | ns (min) |
| $t_{RDW}$ | $\overline{RD}$ Width | Mode Pin to GND (Figure 10 ) | 200<br>400 | **250**<br>**400** | ns (min)<br>ns (max) |
| $t_{CONV}$ | $\overline{WR}$ -$\overline{RD}$ Mode Conversion Time ($t_{WR} + t_{RD} + t_{ACC1}$) | Mode Pin to $V^+$, (Figure 7 ) | 500 | **560** | ns (max) |
| $t_{CRD}$ | $\overline{RD}$ Mode Conversion Time | Mode Pin to GND, (Figure 6 ) | 655 | **900** | ns (max) |
| $t_{ACCO}$ | Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid) | $C_L \le$ 100 pF, Mode Pin to GND (Figure 6 ) | 640 | **900** | ns (max) |
| $t_{ACC1}$ | Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid) | Mode Pin to $V^+$, $t_{RD} \le t_{INTL}$ (Figure 7 ) | | | |
| | | $C_L$ = 10 pF | 45 | | ns |
| | | $C_L \le$ 100 pF | 50 | **110** | ns (max) |
| | | $t_{RD} > t_{INTL}$, (Figure 8 Figure 10) | | | |
| $t_{ACC2}$ | Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid) | $C_L \le$ 10 pF | 25 | | ns |
| | | $C_L$ = 100 pF | 30 | **55** | ns (max) |
| $t_{1H}$, $t_{0H}$ | TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State) | $R_L$ = 3 kΩ, $C_L$ = 10 pF (Figure 6 Figure 7 Figure 8 Figure 9 Figure 10) | 30 | **60** | ns (max) |
| $t_{\overline{INTL}}$ | Delay from Rising Edge of$\overline{WR}$ to Falling Edge of $\overline{INT}$ | Mode Pin = $V^+$, $C_L$ = 50 pF (Figure 8 Figure 9) | 520 | **690** | ns (max) |
| $t_{\overline{INTH}}$ | Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$ | $C_L$ = 50 pF, (Figure 6 Figure 7 Figure 8 Figure 10) | 50 | **95** | ns (max) |
| $t_{\overline{INTH}}$ | Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$ | $C_L$ = 50 pF, (Figure 9) | 45 | **95** | ns (max) |
| $t_{RDY}$ | Delay from $\overline{CS}$ to RDY | Mode Pin = 0V, $C_L$ = 50 pF, $R_L$ = 3 kΩ, (Figure 6) | 25 | **45** | ns (max) |
| $t_{ID}$ | Delay from $\overline{INT}$ to Output Valid | $R_L$ = 3 kΩ, $C_L$ = 100 pF (Figure 9) | 0 | **15** | ns (max) |
| $t_{RI}$ | Delay from $\overline{RD}$ to $\overline{INT}$ | Mode Pin = $V^+$, $t_{RD} \le t_{INTL}$ (Figure 7) | 60 | **115** | ns (max) |
| $t_N$ | Time between End of $\overline{RD}$ and Start of New Conversion | (Figure 6 Figure 7 Figure 8 Figure 9 Figure 10) | 50 | **50** | ns (min) |
| $t_{\overline{CSS}}$ | $\overline{CS}$ Setup Time | (Figure 6 Figure 7 Figure 8 Figure 9 Figure 10) | 0 | **0** | ns (max) |
| $t_{\overline{CSH}}$ | $\overline{CS}$ Hold Time | (Figure 6 Figure 7 Figure 8 Figure 9 Figure 10) | 0 | **0** | ns (max) |

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are to AOQL (Average Output Quality Level).

## DC Electrical Characteristics

The following specifications apply for $V^+$ = 5V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$ = 25°C.

| Symbol | Parameter | Conditions | Typical (1) | Limit (2) | Units (Limit) |
|---|---|---|---|---|---|
| $V_{IH}$ | Logic “1” Input Voltage | $V^+$ = 5.5 V | | | |
| | | $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins | | **2.0** | V (min) |
| | | Mode Pin | | **3.5** | |
| $V_{IL}$ | Logic “0” Input Voltage | $V^+$ = 4.5V | | | |
| | | $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins | | **0.8** | V (max) |
| | | Mode Pin | | **1.5** | |
| $I_{IH}$ | Logic “1” Input Current | $V_H$ = 5V | | | |
| | | $\overline{CS}$, $\overline{RD}$, A0, A, A2 Pins | 0.005 | **1** | |
| | | $\overline{WR}$ Pin | 0.1 | **3** | µA (max) |
| | | Mode Pin | 50 | **200** | |
| $I_{IL}$ | Logic “0” Input Current | $V_L$ = 0V | | | |
| | | $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, A1, A2 | −0.005 | −2 | µA (max) |
| | | Mode Pins | | | |
| $V_{OH}$ | Logic “1” Output Voltage | $V^+$ = 4.75V | | | |
| | | $I_{OUT}$ = −360 µA | | **2.4** | V (min) |
| | | DB0–DB7, $\overline{OFL}$, $\overline{INT}$ | | | |
| | | $I_{OUT}$ = −10 µA | | **4.5** | V (min) |
| | | DB0–DB7, $\overline{OFL}$, $\overline{INT}$ | | | |
| $V_{OL}$ | Logic “0” Output Voltage | $V^+$ = 4.75V | | | |
| | | $I_{OUT}$ = 1.6 mA | | **0.4** | V (max) |
| | | DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY | | | |
| $I_O$ | TRI-STATE Output Current | $V_{OUT}$ = 5.0V | 0.1 | **3** | µA (max) |
| | | DB0–DB7, RDY | | | |
| | | $V_{OUT}$ = 0V | −0.1 | **−3** | µA (max) |
| | | DB0–DB7, RDY | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V DB0–DB7, $\overline{OFL}$, $\overline{INT}$ | −26 | **−6** | mA (min) |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = 5V DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY | 24 | **7** | mA (min) |
| $I_C$ | Supply Current | $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 | 11.5 | **20** | mA (max) |
| $C_{OUT}$ | Logic Output Capacitance | | 5 | | pF |
| $C_{IN}$ | Logic Input Capacitance | | 5 | | pF |

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are to AOQL (Average Output Quality Level).

## Bandgap Reference Electrical Characteristics

The following specifications apply for $V^+$ = 5V unless otherwise specified. **Boldface limits apply for $T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J$ = 25°C.

| Symbol | Parameter | Conditions | Typical (1) | Limits (2) | Units (Limit) |
|---|---|---|---|---|---|
| $V_{REFOUT}$ | Internal Reference Output Voltage | | | **2.5 ± 2.0%** | V (max) |
| $\Delta V_{REF}/\Delta T$ | Internal Reference Temperature Coefficient | | 40 | | ppm/°C |
| $\Delta V_{REF}/\Delta I_L$ | Internal Reference Load Regulation | Sourcing (0 ≤ $I_L$ ≤ +10 mA) | 0.01 | **0.1** | %/mA (max) |
| | Line Regulation | 4.75V ≤ $V^+$ ≤ 5.25V | 0.5 | **6.0** | mV (max) |
| $I_{SC}$ | Short Circuit Current | $V_{REV}$ = 0V | 35 | | mA (max) |
| $\Delta V_{REF}/\Delta_t$ | Long Term Stability | | 200 | | ppm/kHr |
| | Start-Up Time | $V^+$: 0V→5V, $C_L$ = 220 µF | 40 | | ms |

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are to AOQL (Average Output Quality Level).

## TRI-STATE Test Circuit and Waveforms

**Figure 2. $t_{1H}$**

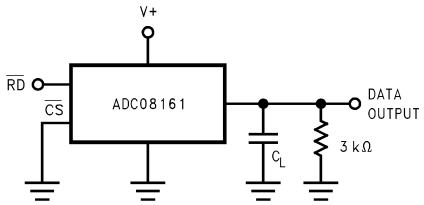
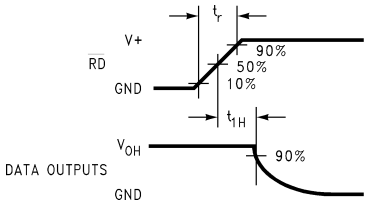



**Figure 3. $t_{1H}$, $C_L$ = 10 pF**




$t_r$ = 10 ns

**Figure 4. $t_{0H}$**

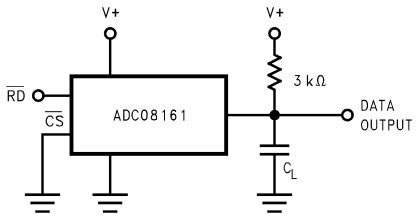
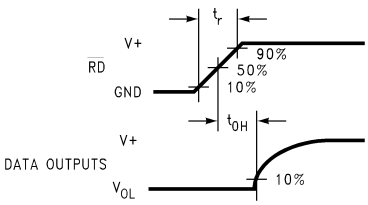



**Figure 5. $t_{0H}$, $C_L$ = 10 pF**




$t_r$ = 10 ns

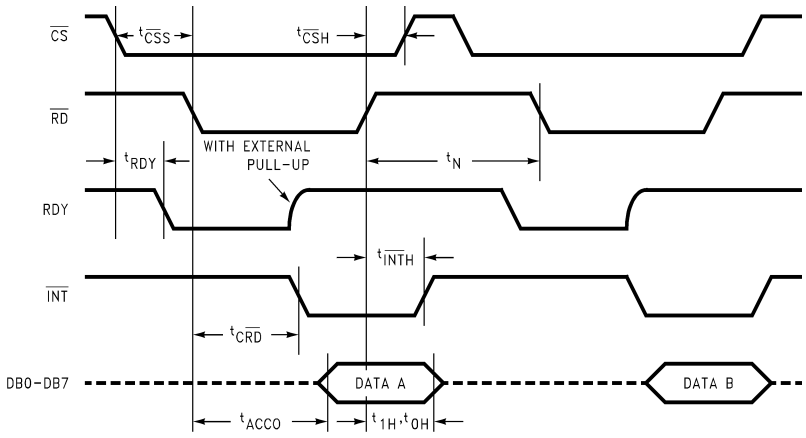



**Figure 6. $\overline{RD}$ Mode (Mode Pin is Low)**

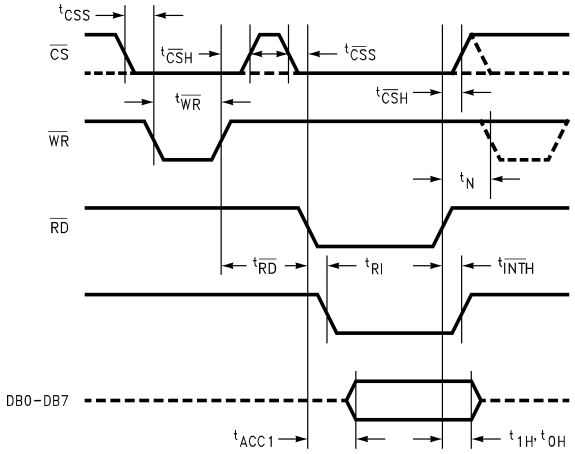



**Figure 7. $\overline{WR}$-$\overline{RD}$ Mode with $t_{RD} \leq t_{INTL}$ (Mode Pin is High)**

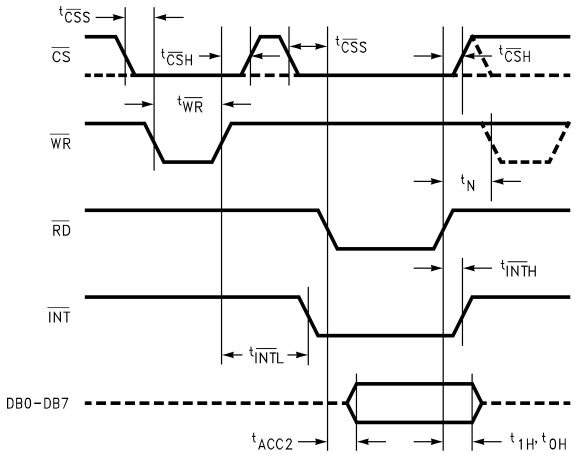



**Figure 8. $\overline{WR}$-$\overline{RD}$ Mode with $t_{RD} > t_{INTL}$ (Mode Pin is High)**

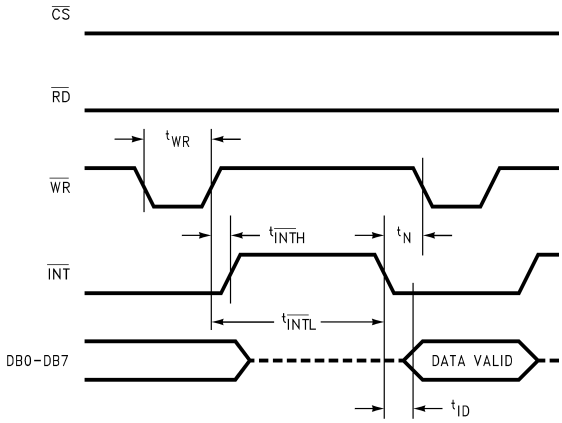



**Figure 9. WR-RD Mode Reduced Interface System Connection with CS = RD = 0 (Mode Pin is High)**

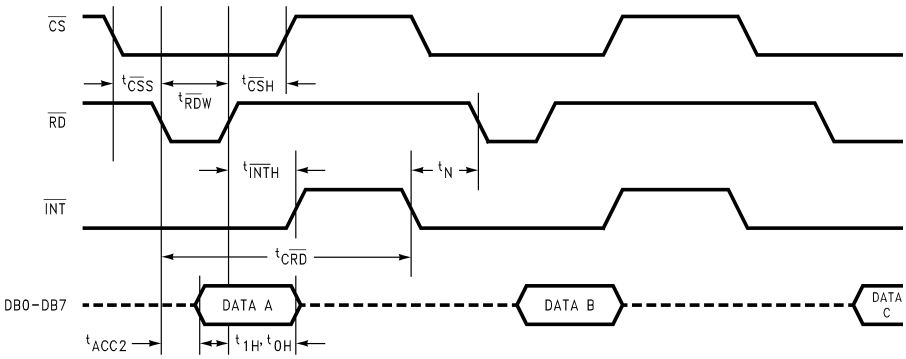
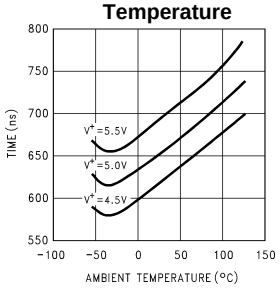


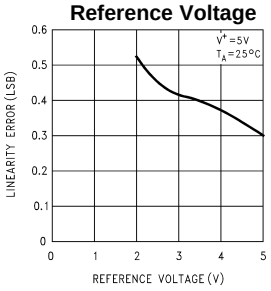

**Figure 10. RD Mode (Pipeline Operation); $t_{RDW}$ must be between 200 ns and 400 ns. (Mode Pin is Low)**

## Typical Performance Characteristics

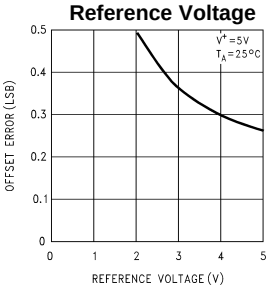
**$t_{CRD}$ vs Temperature**



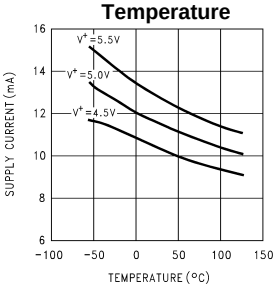

**Linearity Error vs Reference Voltage**



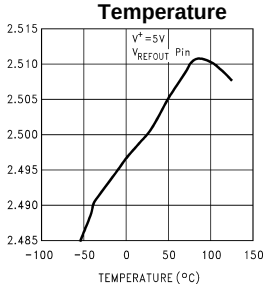

**Offset Error vs Reference Voltage**



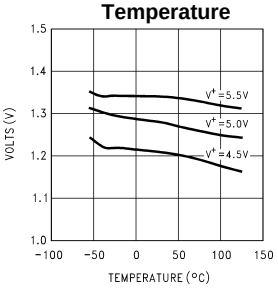

**Supply Current vs Temperature**



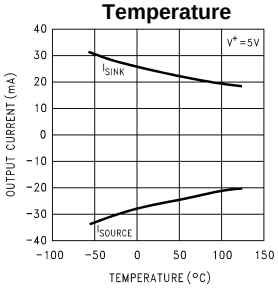

**Reference Output Voltage vs Temperature**




**Logic Threshold vs Temperature**




**Output Current vs Temperature**



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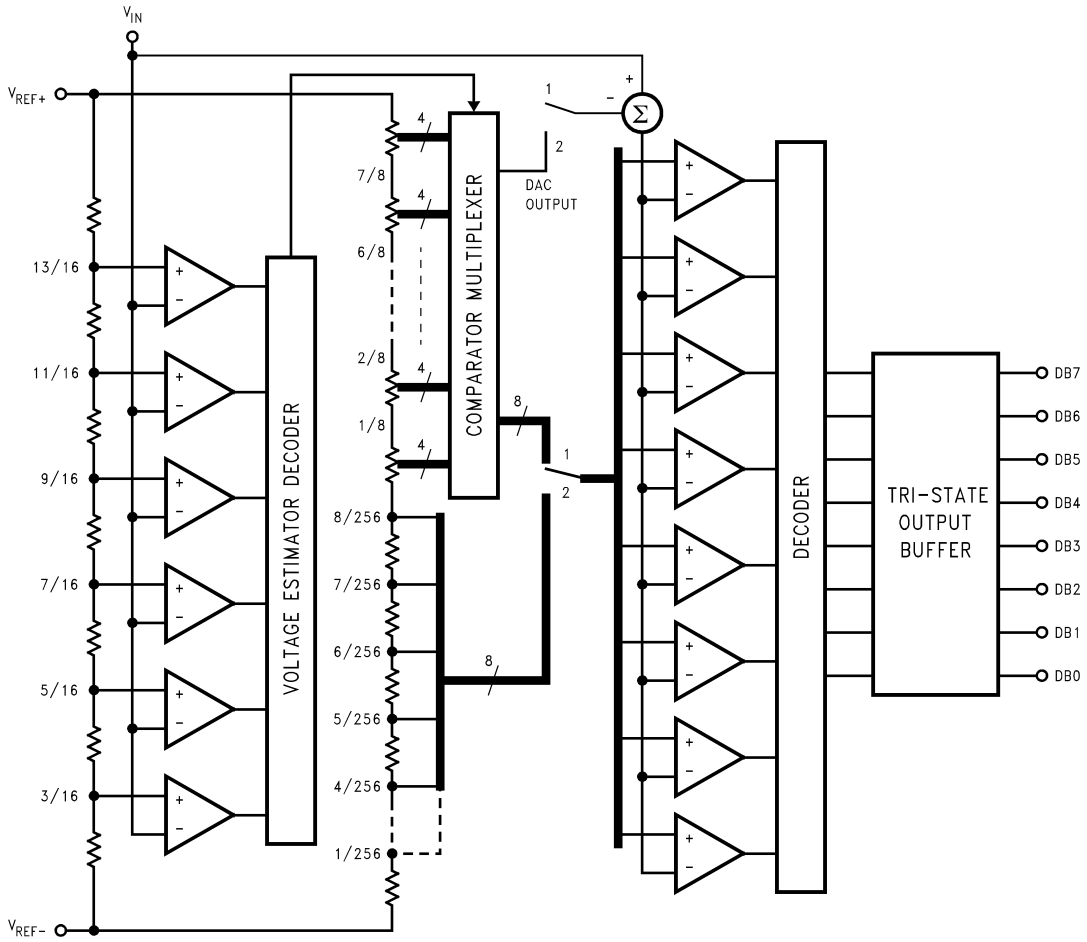


**Figure 11. Block Diagram of the ADC08161 Multi-Step Flash Architecture**

### 1.0 FUNCTIONAL DESCRIPTION

The ADC08161 performs an 8-bit analog-to-digital conversion using a multi-step flash technique. The first flash generates the five most significant bits (MSBs) and the second flash generates the three least significant bits (LSBs). Figure 11 shows the major functional blocks of the ADC08161 multi-step flash converter. It consists of an over-encoded 2½-bit Voltage Estimator, an internal DAC with two different voltage spans, a 3-bit half-flash converter and a comparator multiplexer.

The resistor string near the center of the block diagram in Figure 11 forms the internal main DAC. Each of the eight resistors at the bottom of the string is equal to 1/256 of the total string resistance. These resistors form the **LSB Ladder** and have a voltage drop of 1/256 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remaining resistors make up the **MSB Ladder** . They are made up of eight groups of four resistors connected in series. Each MSB Ladder section has ⅛ of the total reference voltage across it. Within a given MSB Ladder section, each of the MSB resistors has 8/256, or 1⁄32 of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB Ladders. Through the Comparator Multiplexer these tap points can be connected, in groups of eight, to the eight comparators shown at the right of Figure 11. This function provides the necessary reference voltages to the comparators during each flash conversion.

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The six comparators, seven-resistor string (estimator DAC), and Estimator Decoder at the left of Figure 11 form the Voltage Estimator. The estimator DAC connected between $V_{REF+}$ and $V_{REF-}$ generates the reference voltages for the six Voltage Estimator comparators. These comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is then used to control the Comparator Multiplexer, connecting the appropriate MSB Ladder section to the eight flash comparators. Only 14 comparators, six in the Voltage Estimator and eight in the flash converter, are needed to achieve the full eight-bit resolution, instead of 32 comparators that would be needed by traditional half-flash methods.

A conversion begins with the Voltage Estimator comparing the analog input signal against the six tap voltages on the estimator DAC. The estimator decoder then selects one of the groups of tap points along the MSB Ladder. These eight tap points are then connected to the eight flash comparators. For example, if the analog input signal applied to $V_{IN}$ is between 0 and 3/16 of $V_{REF}$ ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the eight tap points between 8/256 and 2/8 of $V_{REF}$ and connects them to the eight flash comparators. The first flash conversion is now performed, producing the five MSBs of data.

The remaining three LSBs are generated next using the same eight comparators that were used for the first flash conversion. As determined by the results of the MSB flash, a voltage from the MSB Ladder equivalent to the magnitude of the five MSBs is subtracted from the analog input voltage as the upper switch is moved from position one to position two. The resulting remainder voltage is applied to the eight flash comparators and, with the lower switch in position two, compared with the eight tap points from the LSB Ladder.

By using the same eight comparators for both flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard half-flash techniques.

Voltage Estimator errors as large as 1/16 of $V_{REF}$(16 LSBs) will be corrected since the flash comparators are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if 7/16 $V_{REF}$ < $V_{IN}$ < 9/16 $V_{REF}$ the Voltage Estimator's comparators tied to the tap points below 9/16 $V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The eight flash comparators will be placed at the MSB Ladder tap points between ⅜ $V_{REF}$ and ⅝ $V_{REF}$. The overlap of 1/16 $V_{REF}$ on each side of the Voltage Estimator's span will automatically correct an error of up to 16 LSBs (16 LSBs = 312.5 mV for $V_{REF}$ = 5V). If the first flash conversion determines that the input voltage is between ⅜ $V_{REF}$ and 4/8 $V_{REF}$ − LSB/2, the Voltage Estimator's output code will be corrected by subtracting "1". This results in a corrected value of "01". If the first flash conversion determines that the input voltage is between 8/16 $V_{REF}$ − LSB/2 and ⅝ $V_{REF}$, the Voltage Estimator's output code remains unchanged.

After correction, the 2-bit data from both the Voltage Estimator and the first flash conversion are decoded to produce the five MSBs. Decoding is similar to that of a 5-bit flash converter since there are 32 tap points on the MSB Ladder. However, 31 comparators are not needed since the Voltage Estimator places the eight comparators along the MSB Ladder where reference tap voltages are present that fall above and below the magnitude of $V_{IN}$. Comparators are not needed outside this selected range. If a comparator's output is a "0", all comparators above it will also have outputs of "0" and if a comparator's output is a "1", all comparators below it will also have outputs of "1".

## 2.0 DIGITAL INTERFACE

The ADC08161 has two basic interface modes which are selected by connecting the **MODE** pin to a logic high or low.

### *2.1 $\overline{RD}$ Mode*

With a logic low applied to the **MODE** pin, the converter is set to **Read** mode. In this configuration (Figure 6), a complete conversion is done by pulling $\overline{RD}$ low, and holding low, until the conversion is complete and output data appears. This typically takes 655 ns. The $\overline{INT}$ (interrupt) line goes low at the end of conversion. A typical delay of 50 ns is needed between the rising edge of $\overline{CS}$ (after the end of a conversion) and the start of the next conversion (by pulling $\overline{RD}$ low). The RDY output goes low after the falling edge of $\overline{CS}$ and goes high at the end-of-conversion. It can be used to signal a processor that the converter is busy or serve as a system Transfer Acknowledge signal.

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### *2.2 $\overline{RD}$ Mode Pipelined Operation*

Applications that require shorter $\overline{RD}$ pulse widths than those used in the **Read** mode as described above can be achieved by setting $\overline{RD}$'s width between 200 ns–400 ns (Figure 10). $\overline{RD}$ pulse widths outside this range will create conversion linearity errors. These errors are caused by exercising internal interface logic circuitry using $\overline{CS}$ and/or $\overline{RD}$ during a conversion.

When $\overline{RD}$ goes low, a conversion is initiated and the data from the previous conversion is available on the DB0–DB7 outputs. Reading DB0–DB7 for the first two times after power-up produces random data. The data will be valid during the third $\overline{RD}$ pulse that occurs after the first conversion.

### *2.3 $\overline{WR}$-$\overline{RD}$ ($\overline{WR}$ then $\overline{RD}$ ) Mode*

The ADC08161 is in the **$\overline{WR}$-$\overline{RD}$ mode** with the **MODE** pin tied high. A conversion starts on the rising edge of the $\overline{WR}$ signal. There are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for the $\overline{INT}$ output to go low before reading the conversion result (Figure 8). Typically, $\overline{INT}$ will go low 690 ns, maximum, after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 350 ns (Figure 7). If $\overline{RD}$ is pulled low before $\overline{INT}$ goes low, $\overline{INT}$ will immediately go low and data will appear at the outputs. This is the fastest operating mode ($t_{RD} \leq t_{INTL}$) with a conversion time, including data access time, of 560 ns. Allowing 100 ns for reading the conversion data and the delay between conversions gives a total throughput time of 660 ns (throughput rate of 1.5 MHz).

### *2.4 $\overline{WR}$-$\overline{RD}$ Mode with Reduced Interface System Connection*

$\overline{CS}$ and $\overline{RD}$ can be tied low, using only $\overline{WR}$ to control the start of conversion for applications that require reduced digital interface while operating in the **WR-RD mode** (Figure 9). Data will be valid approximately 705 ns following $\overline{WR}$'s rising edge.

## 3.0 REFERENCE INPUTS

The ADC08161's two $V_{REF}$ inputs are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{REF+}$and $V_{REF-}$. Transducers that have outputs that minimum output voltages above GND can also be compensated by connecting $V_{REF-}$ to a voltage that is equal to this minimum voltage. By reducing $V_{REF}$ ($V_{REF} = V_{REF+} – V_{REF-}$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF}$ = 2.5V, then 1 LSB = 9.8 mV). The reference arrangement also facilitates ratiometric operation and in may cases the power supply can be used for transducer power as well as the $V_{REF}$ source. Ratiometric operation is achieved by connecting $V_{REF-}$ to GND and connecting $V_{REF+}$ and a transducer's power supply input to $V^+$. The ADC08161s accuracy degrades when $V_{REF+} – |V_{REF-}|$ is less than 2.0V.

The voltage at $V_{REF-}$ sets the input level that produces a digital output of all zeroes. Through $V_{IN}$ is not itself differential, the reference design affords nearly differential-input capability for some measurement applications. Figure 12 shows one possible differential configuration.

It should be noted that, while the two $V_{REF}$ inputs are fully differential, the digital output will be zero for any analog input voltage if $V_{REF-} \geq V_{REF+}$.

## 4.0 ANALOG INPUT AND SOURCE IMPEDANCE

The ADC08161's analog input circuitry includes an analog switch with an “on” resistance of 70Ω and a 1.4 pF capacitor (Figure 12). The switch is closed during the A/D's input signal acquisition time (while $\overline{WR}$ is low when using the $\overline{WR}$-$\overline{RD}$ Mode). A small transient current flows into the input pin each time the switch closes. A transient voltage, whose magnitude can increase as the source impedance increases, may be present at the input. So long as the source impedance is less than 500Ω, the input voltage transient will not cause errors and need not be filtered.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (100 ns maximum). A signal source with a high output impedance should have its output buffered with an operational amplifier. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

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Some suggested input configurations using the internal 2.5V reference, an external reference, and adjusting the input span are shown in Figure 16.

Correct conversion results will be obtained for input voltages greater than GND − 100 mV and less than $V^+$ + 100 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than $V^+$, or more than 300 mV lower than GND. The current flowing through any analog input pin should be limited to 5 mA or less to avoid permanent damage to the IC if an analog input pin is forced beyond these voltages. The sum of all the overdrive currents into all pins must be less than 20 mA. Some sort of protection scheme should be used when the input signal is expected to extend more than 300 mV beyond the power supply limits. A simple protection network using resistors and diodes is shown in Figure 17.

## 5.0 INHERENT SAMPLE-AND-HOLD

An important benefit of the ADC08161's input architecture is the inherent sample-and-hold (S/H) and its ability to measure relatively high speed signals without the help of an external S/H. In a non-sampling converter, regardless of its speed, the input must remain stable to at least ½ LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion.

The ADC08161 is suitable for DSP-based systems because of the direct control of the S/H through the $\overline{WR}$ signal. The $\overline{WR}$ input signal allows the A/D to be synchronized to a DSP system's sampling rate or to other ADC08161s.

The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

## 6.0 INTERNAL BANDGAP REFERENCE

The ADC08161 has an internal bandgap 2.5V reference that can be used as the $V_{REF+}$ input. A parallel combination of a 0.1 µF ceramic capacitor and a 220 µF tantalum capacitor should be used to bypass the $V_{REFOUT}$ pin. This reduces possible noise pickup that could cause conversion errors.

## 7.0 LAYOUT, GROUNDS, AND BYPASSING

In order to ensure fast, accurate conversions from the ADC08161, it is necessary to use appropriate circuit board layout techniques. Ideally, the analog-to-digital converter's ground reference should be low impedance and free of noise from other parts of the system. Digital circuits can produce a great deal of noise on their ground returns and, therefore, should have their own separate ground lines. Best performance is obtained using separate ground planes should be provided for the digital and analog parts of the system.

The analog inputs should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., an input filter capacitor) connected across the inputs should be returned to a very clean ground point. Incorrectly grounding the ADC08161 may result in reduced conversion accuracy.

The $V^+$ supply pin, $V_{REF+}$, and $V_{REF-}$ (if not grounded) should be bypassed with a parallel combination of a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor placed as close as possible to the pins using short circuit board traces. See Figure 16 Figure 17.

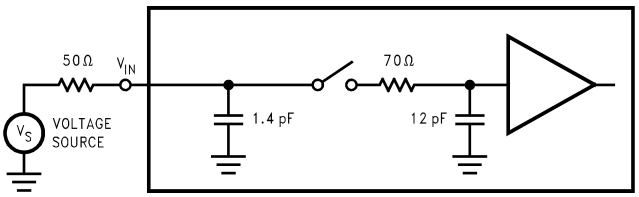


**Figure 12. ADC08161 Equivalent Input Circuit Model**

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**Figure 13. Internal Reference 2.5V Full-Scale (Standard Application)**

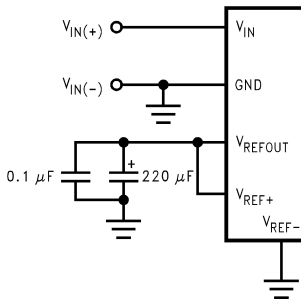



**Figure 14. Power Supply as Reference**

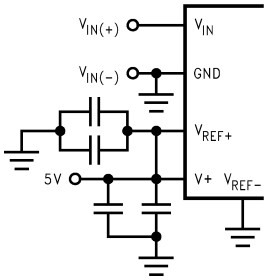
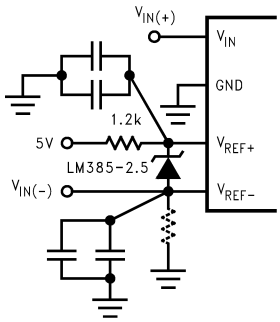



**Figure 15. Input Not Referred to GND**




*Signal source driving $V_{IN}(-)$ must be capable of sinking 5 mA.

**Figure 16. Analog Input Options**

**Note:** Bypass capacitors consist of a 0.1 µF ceramic in parallel with a 10 µF bead tantalum, unless otherwise specified.

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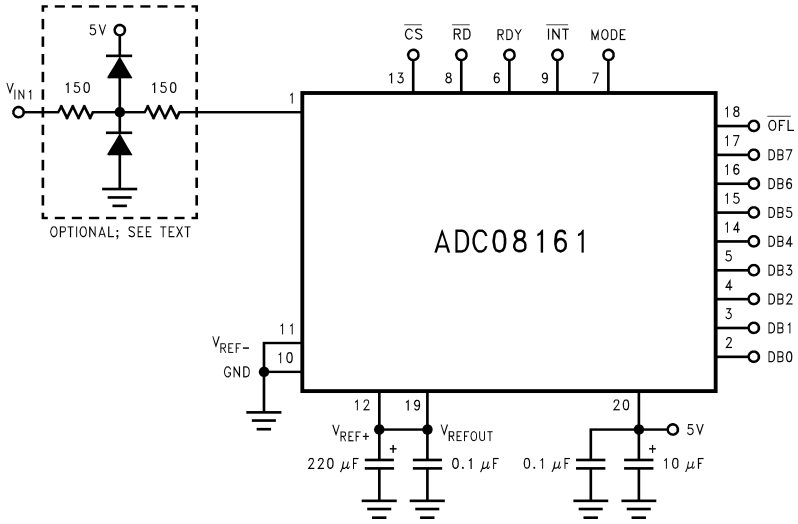


**Figure 17. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. $V_{REF-}$ should be bypassed to analog ground using multiple capacitors if it is not grounded (See Section 7.0 "LAYOUT, GROUNDS, and BYPASSING"). $V_{IN1}$ is shown with an optional input protection network.**

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