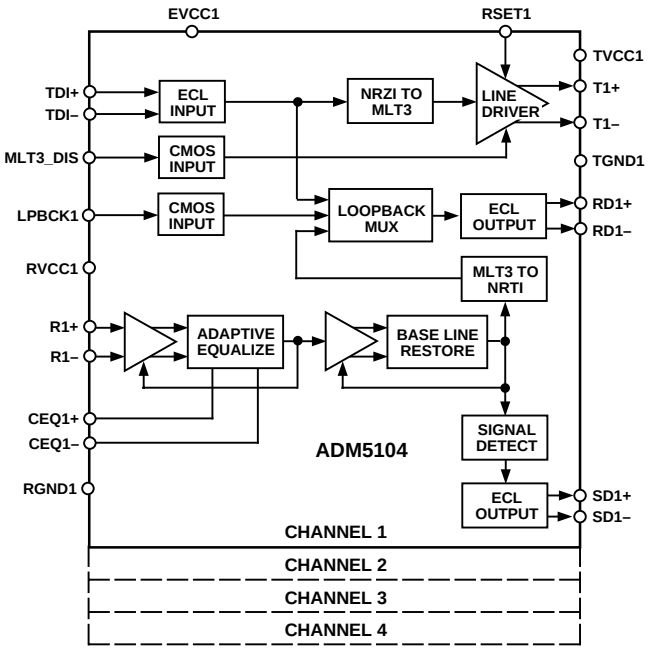
Low Power Quad NRZ to Transformer Fast Ethernet 110Base-TX Transceiver

ADM5104

FEATURES

Four 100 TX to Match One Quad Transformer
Compliant to 802.3u 110Base-TX
Equalization and Base Line Wander Correction
Low Power, Typ 300 mW per Channel
Differential Transformer Interface for Transmit and Receive Channels
NRZ PECL ASIC Interface
Loopback and Power-Down Modes
Resistor Programmed Drive Currents
Adaptive Equalizer Capacitively Adjustable

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM5104 is a four-channel 110Base-TX transceiver for multichannel Fast Ethernet interfaces. For minimum pin count and power, the 125 MHz differential PECL interface is well matched to digital controller ASICs. With a four-channel transformer, this transceiver manages the high speed analog transmission and the equalization and detection of the MLT3 TX signal over 100 meters of Category 5 UTP. Including the PECL and transformer loads, the chip power level is typically less than 1 1/2 W for all four channels in an 80-terminal TQFP.

APPLICATIONS

Intelligent Hubs, Repeaters
Multichannel 100 TX interfaces

PRODUCT HIGHLIGHTS

1. Specified for 5 V supplies.
2. Low power and compact package for four channels.
3. Complete analog I/O silicon to NRZ interface.
4. IEEE 802.3 Compliant 110Base-TX.

REV. 0

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ADM5104–SPECIFICATIONS (EVCCn = TVCCn = RVCCn = +5.0 V, T_A + T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RECEIVER					
Input Signal Range	764			mV p-p	0 to 110 M UTP#5 (140)
			1.06	V p-p	
Differential Input Voltage			2.1	V	Differential Input Voltage
	10.0			kΩ	Differential Input Resistance
Transitionless Data Run			400	Bit Periods	
Equalizer Time Constant			1000	ms	Ceq-0.1 µF
RECEIVER OUTPUT LEVELS					
Output Logic High, V_{OH}	–1.2			PECL V	RDn+, RDn–
		–1.0		PECL V	
			–0.7	PECL V	
Output Logic Low, V_{OL}	–2.0			PECL V	RDn+, RDn–
		–1.8		PECL V	
			–1.7	PECL V	
Output Drive		50		Ω	
Rise and Fall Times		1.0		ns	10%–90% PECL Levels 50 Ω Loads, No Cap
SIGNAL DETECT					
Trip Level	200			mV p-p	2^{23} – 1 PRN, 0 M Cable
		350		mV p-p	
Release Level		750		mV p-p	2^{23} – 1 PRN, 0 M Cable
			1000	mV p-p	
Response Time		12.9		µs	30 M Cable From Receiver Input to Active/Inactive
SDOUT Output Logic High, V_{OH}	–1.2			PECL V	SDn+, SDn–
		–1.0		PECL V	
			–0.7	PECL V	
SDOUT Output Logic Low, V_{OL}	–2.0			PECL V	SDn+, SDn–
		–1.8		PECL V	
			–1.7	PECL V	
TRANSMITTER LINE DRIVER					
Differential Input	150			mV	Output Current Variation < 1%
			1000	mV	
Common-Mode Input Voltage	2			V	
			V_{CC} – 1	V	
Output Current Levels MLT3		0, 20, 40		mA	Into 50 Ω
Output Current Variation			5	%	1% Resistor to Ground at RSETn = 2.2 kΩ
Common-Mode Current		2.5		%	Percentage of Output Drive Current with 50 Ω Loads
Rise and Fall Times		3.0		ns	10 %–90% MLT3 Levels 100 Ω Loads at T+ and T–
Rise and Fall Times		4.0		ns	10 %–90% MLT3 Levels 100 Ω through Xformer Loads
Output Jitter		750		ps	
INPUT CONTROL SIGNALS					
Input Logic Low, V_{IL}			0.8	V	LPBCKn, MLT3_DISn
Input Logic High, V_{IH}	2			V	
LPBCK On to RECEIVER Output Delay		150		ns	Filtered Input Pin
LPBCK Off to RECEIVER Output Delay		150		ns	Filtered Input Pin
LPBCK On to XMITTER Output Balance		150		ns	Filtered Input Pin
LPBCK Off to XMITTER Output Active		150		ns	Filtered Input Pin
MLT3_DIS On to XMITTER Output Off		150		ns	Filtered Input Pin
MLT3_DIS Off to XMITTER Output Active		350		ns	Filtered Input Pin
POWER REQUIREMENTS					
Power Voltage Supply	4.5			V	
Power Voltage Supply			5.5	V	
Total Power In Chip			1.6	Watts	125 MHz @ 5.5 V
Typical Power In Chip		1.3		Watts	125 MHz @ 25°C, V_{CC} = 5.0 V
		80		mA	From VCC into Chip Core
		160		mA	From VCC into PECL Outputs
		80		mA	From Chip Core to GND
		160		mA	From Xmitter Line Driver Outputs to GND
OPERATING TEMPERATURE RANGE	0		+70	°C	Ambient

ABSOLUTE MAXIMUM RATINGS

ORDERING GUIDE

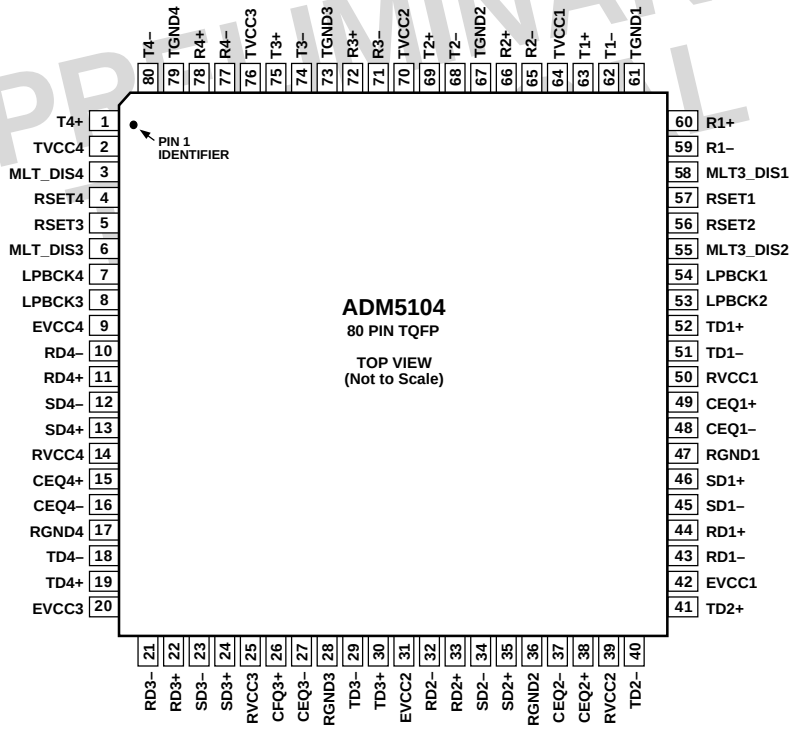
Model	Temperature Range	Package Description	Package Option
ADM5104?	0°C to 70°C	Thin Quad Flatpack (TQFP)	ST-80

ST = Surface Mount.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM5104 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NOTES ON QUAD PMD PINOUT

T*+, T*– are the Line Driver outputs to the Transformer.
R*+, R*– are the Receiver inputs from the Transformer.

TVCC1–4 and TGND1–4 are the Supplies to the Line Drivers.

RSET1–4 are the pins to which Precision Resistors are tied to set the Line Driver Output Levels.

CEQ*+, CEQ*– are the pins across which the Equalizer Loop Filter Caps are connected.

RVCC1–4 and RGND1–4 are the Supplies to the Receivers/Equalizers.

TD*+, TD*– are ECL inputs that Transmit Data from the PHY.
RD*+, RD*– are ECL outputs that send Receive Data to the PHY.

SD*+, SD*– are ECL outputs that send Signal Detect Data to the PHY.

EVCC1–4 are the Supplies for the ECL Output Pins.

LPBCK* are CMOS inputs that enable Loopback Mode.

MLT3_DIS* are CMOS inputs three-states the MLT# Line Drivers.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	T4+	Line Driver Collector Output Channel 4
2	TVCC4	Channel 4 Driver Supply To Transformer
3	MLT3_DIS4	Channel 4 Disable to High Impedance
4	RSET4	Output Current Set Channel 4
5	RSET3	Output Current Set Channel 3
6	MLT3_DIS3	Channel 3 Disable to High Impedance
7	LPBCK4	Loopback Channel 4
8	LPBCK3	Loopback Channel 3
9	EVCC4	ECL Supply On Channel 4
10	RD4–	ECL Receive Data To The PHY Channel 4
11	RD4+	ECL Receive Data To The PHY Channel 4
12	SD4–	Signal Detect Channel 4
13	SD4+	Signal Detect Channel 4
14	RVCC4	Receiver/Equalizer Supply Channel 4
15	CEQ4+	Equalizer Loop Filter Capacitor Channel 4
16	CEQ4–	Equalizer Loop Filter Capacitor Channel 4
17	RGND4	Receiver Supply Ground Channel 4
18	TD4–	ECL Transmit Data From the PHY Channel 4
19	TD4+	ECL Transmit Data From the PHY Channel 4
20	EVCC3	ECL Supply On Channel 3
21	RD3–	ECL Receive Data To The PHY Channel 3
22	RD3+	ECL Receive Data To The PHY Channel 3
23	SD3–	Signal Detect Channel 3
24	SD3+	Signal Detect Channel 3
25	RVCC3	Receiver/Equalizer Supply Channel 3
26	CEQ3+	Equalizer Loop Filter Capacitor Channel 3
27	CEQ3–	Equalizer Loop Filter Capacitor Channel 3
28	RGND3	Receiver Supply Ground Channel 3
29	TD3–	ECL Transmit Data From the PHY Channel 3
30	TD3+	ECL Transmit Data From the PHY Channel 3
31	EVCC2	ECL Supply On Channel 2
32	RD2–	ECL Receive Data To The PHY Channel 2
33	RD2+	ECL Receive Data To The PHY Channel 2
34	SD2–	Signal Detect Channel 2
35	SD2+	Signal Detect Channel 2
36	RGND2	Receiver Supply Ground Channel 2
37	CEQ2–	Equalizer Loop Filter Capacitor Channel 2
38	CEQ2+	Equalizer Loop Filter Capacitor Channel 2
39	RVCC2	Receiver/Equalizer Supply Channel 2
40	TD2–	ECL Transmit Data From the PHY Channel 2
41	TD2+	ECL Transmit Data From the PHY Channel 2
42	EVCC1	ECL Supply On Channel 1
43	RD1–	ECL Receive Data To The PHY Channel 1
44	RD1+	ECL Receive Data To The PHY Channel 1
45	SD1–	Signal Detect Channel 1
46	SD1+	Signal Detect Channel 1
47	RGND1	Receiver Supply Ground Channel 1
48	CEQ1–	Equalizer Loop Filter Capacitor Channel 1
49	CEQ1+	Equalizer Loop Filter Capacitor Channel 1
50	RVCC1	Receiver/Equalizer Supply Channel 1
51	TD1–	ECL Transmit Data From the PHY Channel 1
52	TD1+	ECL Transmit Data From the PHY Channel 1
53	LPBCK2	Loopback Channel 2
54	LPBCK1	Loopback Channel 1

Pin No.	Mnemonic	Description
55	MLT3_DIS2	Channel 2 Disable to High Impedance
56	RSET2	Output Current Set Channel 2
57	RSET1	Output Current Set Channel 1
58	MLT3_DIS1	Channel 1 Disable to High Impedance
59	R1–	Differential Receiver Input Channel 1
60	R1+	Differential Receiver Input Channel 1
61	TGND1	Channel 1 Driver Ground
62	T1–	Line Driver Collector Output Channel 1
63	T1+	Line Driver Collector Output Channel 1
64	TVCC1	Channel 1 Driver Supply To Transformer
65	R2–	Differential Receiver Input Channel 2
66	R2+	Differential Receiver Input Channel 2
67	TGND2	Channel 2 Driver Ground
68	T2–	Line Driver Collector Output Channel 2
69	T2+	Line Driver Collector Output Channel 2
70	TVCC2	Channel 2 Driver Supply To Transformer
71	R3–	Differential Receiver Input Channel 3
72	R3+	Differential Receiver Input Channel 3
73	TGND3	Channel 3 Driver Ground
74	T3–	Line Driver Collector Output Channel 3
75	T3+	Line Driver Collector Output Channel 3
76	TVCC3	Channel 3 Driver Supply To Transformer
77	R4–	Differential Receiver Input Channel 4
78	R4+	Differential Receiver Input Channel 4
79	TGND4	Channel 4 Driver Ground
80	T4–	Line Driver Collector Output Channel 4

PRODUCT DESCRIPTION

The ADM5104 provides a single chip solution for interfacing four 110Base-TX ports to four Category #5 Unshielded Twisted Pair (UTP) cables. Four channel MII with timing to PMD transceiver and ASICs will complete four PHY channels for repeaters/hubs. The IC provides four independent PMD transceivers with separate transmit line drivers and receiver buffers with line equalization and baseline restoration. Each channel has signal multiplexers that allow the user to independently perform loopback, signal detect and equalization compensation.

The line equalization and baseline restoration block compensates for up to 140 M Category #5 UTP and transformer, respectively. This block has a signal detect output SDOUTn that, when low, indicates a loss of input signal at Rn±.

The line driver has a differential ECL input stage that provides a controlled current output to match driving Category #5 UTP cable. A single resistor for each channel, from the line driver output current control pin to ground, controls the output current. The user has the option to disable the line driver output. A signal multiplexer allows the user to loopback the line driver to the receiver on each respective channel for test purposes.

THEORY OF OPERATION

Line Drivers

The line drivers accept differential input data between 100 mV and 1.0 V peak (ac coupled or ECL common mode), and transmits the 125 MHz MLT3 data signal through a transformer and up to 100 M of Category #5 Unshielded Twisted Pair cable (UTP #5) per EIA586A, 802.3 110Base-TX requirements. The user sets the output current, I_{OUT}, between 4 mA and 40 mA (cable removed and 100 Ω resistor across the transformer) with a single resistor. A 2.0 V p-p output signal is obtained with an I_{OUT} of 20 mA, corresponding to an Rtxampset = 2280 Ω. Generally, IOUT = 22.3/Rtxampset.

The line driver does not share any power supplies or biases with other blocks or channels in the ADM5104. This, and techniques used to stabilize the effective beta of transistors during switching, keep output common-mode current to <3%.

Receiver (Equalizer, Baseline Restoration and Loss of Signal Detect Circuits)

Each of the four receivers processes an MLT3 data stream from a transformer and up to 140 M of Category # 5 Unshielded Twisted Pair cable (UTP#5). The receiver (Figure 1) consists of an adaptive equalizer, a baseline restore loop, and a loss of signal (LOS) detector. The adaptive equalizer compensates for intersymbol interference and distortion caused by the cable. The baseline restore loop corrects for baseline wander due to the coding and transformer. The LOS detector indicates a cable break.

The incoming data chooses either the high pass path, shown as E(s), the straight path, or some combination of both. The strength of each path is determined by the control variable, x.

The loop works by comparing the amplitude of the equalizer output to the expected value. If the amplitude is too small, the signal is under-equalized and the control variable x is decreased to choose more of the high pass path. The signal is equalized when the output amplitude equals the reference value. The time constant of the loop is slow enough so that the equalization remains constant if the signal amplitude decreases due to the absence of transitions.

The baseline restore loop compensates for the baseline wander caused by the transformer (ac coupling) used to terminate the cable. This loop adjusts the slice levels of the data signal for lengthy transitionless data runs to ensure that no bit errors are made upon new transitions. This loop also compensates for a dc offset that could be created by the transformer processing unbalanced data signal patterns (baseline wander). The circuit works by subtracting the comparator input signal from the output signal. The error signal output of the subtracter is added in, to offset the incoming signal to keep the average value equal to the average output. If the equalizer output goes to zero, this loop will servo the comparator input to the last logic level.

The LOS detector monitors the output amplitude of the equalizer and trips when it falls below a predetermined threshold. The low-pass filter is slow enough so that the detector will not trip for less than 800 missing edges.

PECL Output Compatibility with Fast Ethernet PHY Interface IC Inputs

The PECL outputs (RDn±) are more than adequate for driving interface IC PECL inputs. This is demonstrated on the comparison of the PECL output specifications and an interface IC PECL input dc characteristics, given below.

The PECL output levels, specified in single-ended terms over 0°C to 70°C (V_{OH} and V_{OL}), should not be taken at face value. Since the output signals that V_{OH} and V_{OL} refer to are processed

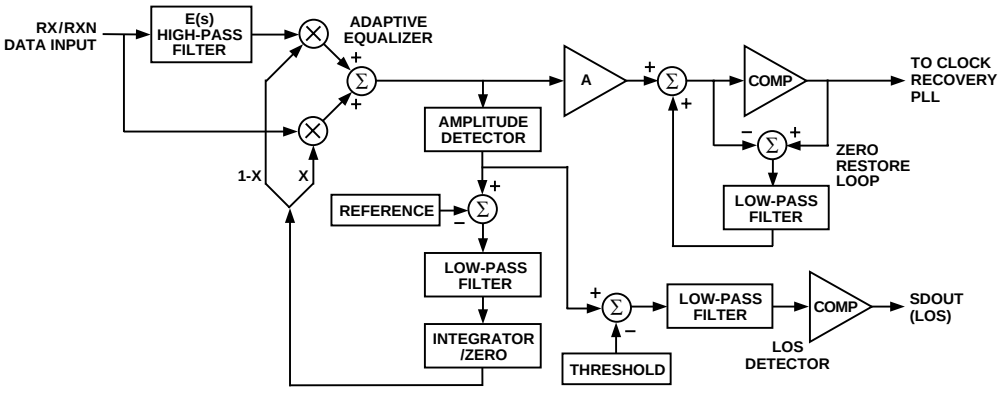


Figure 1. Receiver Diagram

differentially (typically the interface IC "self-biased" PECL Inputs require ac coupling), the differential voltage swing between V_{OH} and V_{OL} determine compatibility. Yet, simply combining the V_{OH} min specification with the V_{OL} max specification confuses a compatibility analysis since both V_{OH} and V_{OL} track with temperature. This means that V_{OH} min and V_{OL} max do not occur simultaneously, but at opposite temperature extremes (refer to Figure 2). Note that the different voltage swing (V_{OH} – V_{OL}) remains ≥0.93 V over temperature.

Test results of identical PECL outputs over temperature reveal that minimum differential voltage swings at –40°C and at +85°C equal 0.72 V and 0.81 V, respectively (with 6 sigma confidence).

Typical interface IC PECL inputs have V_{IH} min and V_{IL} max dc specifications that require differential drive (V_{IH} min – V_{IL} max) ≥0.4 V to ≥0.6 V. The ADM5104 PECL outputs have the differential swing (0.72 V minimum) to drive these inputs with sufficient margin.

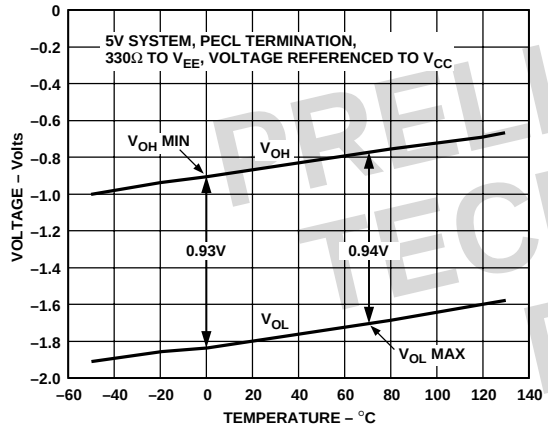


Figure 2. PECL Output Levels Chart

5 V PECL to 3.3 V PECL Interface Analysis

The following three equations need to be satisfied for this interface (in the following example Rh = Resistor connected to PECL 5, Rm = Resistor connected between termination line and destination pin, and Rl = Resistor connected to ground):

1. Termination Impedance must match trace impedance:

   $Termination\ Impedance = (Rh \times [Rm + Rl])/(Rh + Rm + Rl) = 50\ \Omega$

2. Resistors need to provide the correct voltage levels:

   $(Vsource - Vterm\_destination)/Rm = Vterm\_destination/Rl$

   where: $Vsource$ = 3.67 V (PECL 5 V midpoint) and

   $Vterm\_destination$ = 2.0 V (PECL 3.3 V midpoint).

3. Desired driver current of 25 mA:

   $Idrive = ([4 - Vdest\_high])/Rm) - ([5 - 4]/Rh)$,

   where: $Vdest\_high = (4 \times Rl)/(Rm + Rl)$ and Idrive = 0.025

The midpoints are used to ensure that the waveforms are centered at the critical levels. The waveform is attenuated at the destination because of the voltage divider. Rounding the resistor values to the nearest standard 5% resistors results in circuit of Figure x. A 3.2 V to 4.0 V input swing into this circuit creates an output swing between 1.8 V and 2.2 V.

Figure x.

3.3 V PECL to 5 V PECL Interface Analysis

The common-mode rejection area of the ADM5104 line receiver input requires the input signal voltage swing to be above 2.6 V. This is lower that standard PECL and helps simplify the termination resistor network (less drive current is required). In the following example: Rh = Resistor connected to PECL 5 V, Rm = Resistor connected between termination line and destination pin, and Rl = Resistor connected to ground. The following three equations need to be satisfied for this interface:

1. The voltage swings need to be centered at the correct voltage levels:

   $(5 - Vmid\_destination)/Rh =$

   $(Vmid\_destination - Vmid\_source)/Rm$

   where: $Vmid\_destination$ = 3.0 V and

   $Vmid\_source$ = 2.0 V.

2. Termination Impedance must match trace impedance:

   $Termination\ Impedance =$

   $(Rl \times [Rm + Rh])/(Rh + Rm + Rl) = 50\ \Omega$

3. The voltage for the driver should be within 5% of 1.7 V for the proper swing:

   $Vsource = (5 \times Rl)/(Rh + Rm + Rl)$

   where: $Vsource$ = 1.7 V

Using the equations and rounding the resistor values to the nearest standard 5% resistor results in the circuit of Figure x. This circuit will result in a source voltage swing between 1.66 V and 2.4 V, and a destination voltage swing between 2.79 V and 3.28 V. This exceeds the minimum required voltage swing sufficient margin.

4. Also, the current required by the driver must be less than 17 mA:

   $Idrive = (2.4/Rl) - ([5 - Vterm\_destination\_high]/Rh)$

Figure x.

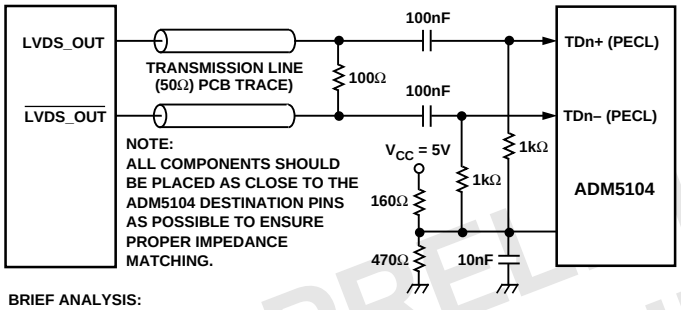
In this case, the current of the driver is 15 mA.

PECL interface to IEEE LVDS levels

The ADM5104 high speed inputs and outputs operate at PECL levels. ASICs in a 3.3 V CMOS that use IEEE LVDS levels (Low Voltage Differential Signal) for its high speed digital outputs and inputs should refer to the following paragraphs and to Figures 3 and 4 for the description of the interface to the ADM5104.

LVDS to PECL Conversion

LVDS levels from the ASIC can be shifted to PECL levels to the ADM5104 using capacitive coupling (Figure 3). This scheme assumes the LVDS output drives the "long" portion on the transmission line. The passive shifting and termination network is located as close to the PECL input as possible.

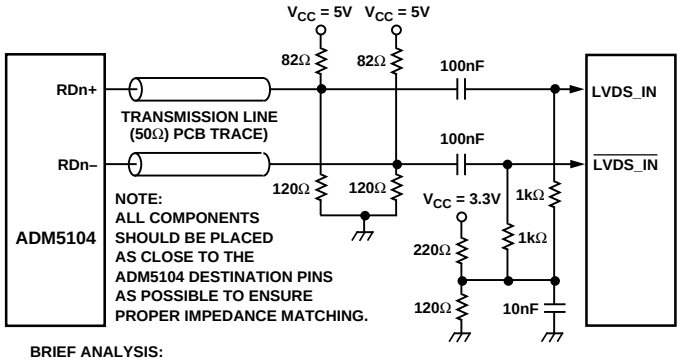


BRIEF ANALYSIS:
1. TERMINATION IS DONE BY THE 100Ω RESISTOR BETWEEN THE DIFFERENTIAL LINES.
2. THE 100nF CAPACITORS PROVIDE AC COUPLING TO THE PHY ASIC OUTPUT.
3. THE RESISTOR DIVIDER GENERATES THE NEW OFFSET VOLTAGE (VBB, IN CENTER BETWEEN PECL VIH AND VIL) OF APPROXIMATELY 3.7V.
4. THE TWO 1kΩ RESISTORS ARE USED FOR DECOUPLING THE TWO SIGNALS.
5. PECL COMMON-MODE VOLTAGE SUPPLIED EXTERNALLY. COMPONENTS ARE NOT REQUIRED.

Figure 3. LVDS to PECL Conversion

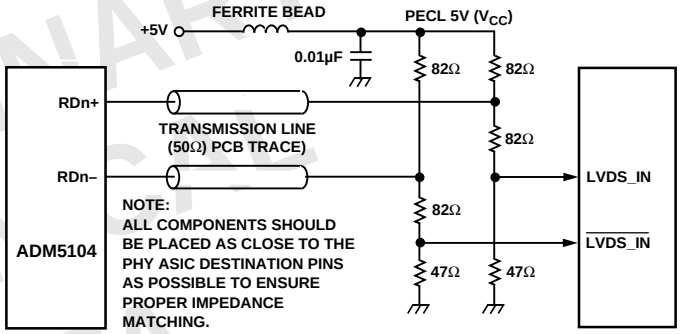
PECL to LVDS Conversion

PECL levels from the ADM5104 can be shifted to LVDS levels of a 3.3 V ASIC using either ac coupling or dc coupling (Figures 4a and 4b). These schemes assume that the PECL output drives the "long" portion of the transmission line. The passive shifting and termination network is located as close to the LVDS input as possible.



BRIEF ANALYSIS:
1. TERMINATION IS DONE BY A PARALLEL THEVEVIN SCHEME.
2. THE 100nF CAPACITORS PROVIDE AC COUPLING.
3. THE RESISTOR DIVIDER NETWORK FIXES NEW OFFSET VOLTAGE AT 1.2V.

a.



BRIEF ANALYSIS:
1. SHIFTING NETWORK BASED ON THEVENIN SCHEME WITH LOWER RESISTOR REPLACED BY DIVIDER.
2. COMMON MODE VOLTAGE TRANSFORMED FROM 3.7V DOWN TO 1.4V.
3. DIFFERENTIAL VOLTAGE SWING ATTENUATED FROM 600mV MINIMUM (PECL) TO 220mV MINIMUM FOR LVDS.

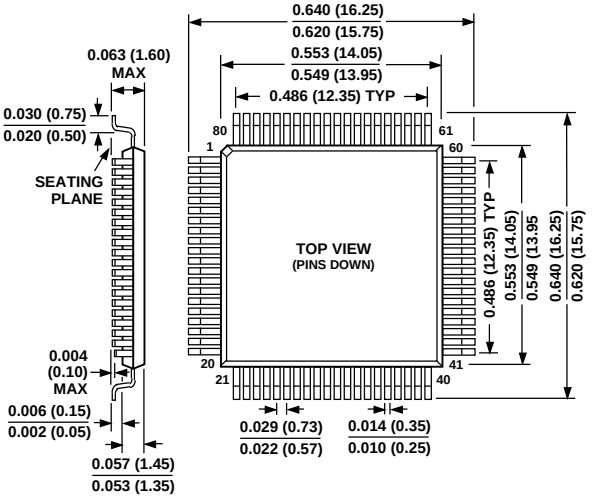
b.

Figure 4. PECL to LVDS Conversion

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

80-Terminal Plastic Thin Quad Flatpack (TQFP)
(ST-80)



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