

Microprocessors Supervisory Circuit in 4-Lead SOT-143

ADM811/ADM812

FEATURES

Superior Upgrade for MAX811/MAX812 Specified Over Temperature Low Power Consumption (5 μA Typ) Precision Voltage Monitor: +3 V, +3.3 V, +5 V Options Reset Assertion Down to 1 V V_{CC} 140 ms Min Power-On Reset Logic Low RESET Output (ADM811) Logic High RESET Output (ADM812) Built-In Manual Reset

APPLICATIONS

Microprocessor Systems Controllers Intelligent Instruments Automotive Systems Safety Systems Portable Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM811/ADM812 are reliable voltage monitoring devices suitable for use in most voltage monitoring applications.

The ADM811/ADM812 are designed to monitor five different voltages, each allowing for a 5% or 10% degradation of standard PSU voltages before a reset occurs. These voltages have been selected for the effective monitoring of +3 V, +3.3 V and +5 V supply voltage levels.

Included in this circuit is a debounced Manual Reset input. Reset can be activated using an electrical switch (or an input from another digital device) or by a degradation of the supply voltage. The Manual Reset function is very useful especially if the circuit in which the ADM811/ADM812 is operating enters into a state that can only be detected by the user. Allowing the user to manually reset a system can reduce the damage or danger that could be otherwise caused by an out-of-control or locked up system.



Figure 1. Typical Operating Circuit

REV.0

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ADM811/ADM812—SPECIFICATIONS ($V_{CC} = Full Operating Range, T_A = T_{MIN}$ to T_{MAX} , V_{CC} typ = +5 V for L/M, +3.3 V for T/S, +3 V for R Models unless otherwise noted)

| Parameter | Min | Тур | Max | Units | Test Conditions/Comments |
|--------------------------------------|----------------------|------|------------------------|------------|----------------------------------------------------------------------------------------------------------------|
| SUPPLY | | | | | |
| Voltage | 1.0 | | 5.5 | V | $T_A = 0^{\circ}C$ to $+70^{\circ}C$ |
| C C | 1.2 | | | V | $T_{A}^{-} = -40^{\circ}C \text{ to } +85^{\circ}C$ |
| Current | | 8 | 15 | μA | $V_{CC} < +5.5 \text{ V}, \text{ADM81}_L/M, \text{I}_{OUT} = 0 \text{ A}$ |
| | | 5 | 10 | μA | $V_{CC} < +3.6 \text{ V}, \text{ADM81}_R/S/T, I_{OUT} = 0 \text{ A}$ |
| RESET VOLTAGE THRESHOLD | | | | | |
| ADM81_L | 4.54 | 4.63 | 4.72 | V | $T_A = +25^{\circ}C$ |
| ADM81_L | 4.50 | | 4.75 | V | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ |
| ADM81_M | 4.30 | 4.38 | 4.46 | V | $T_A = +25^{\circ}C$ |
| ADM81_M | 4.25 | 1150 | 4.50 | v | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ |
| ADM81_T | 3.03 | 3.08 | 3.14 | v | $T_A = +25^{\circ}C$ |
| ADM81 T | 3.00 | 5.00 | 3.15 | v | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ |
| ADM81_S | 2.88 | 2.93 | 2.98 | v | $T_A = +25^{\circ}C$ |
| ADM81_S | 2.85 | 2.95 | 3.00 | v | $T_A = +25$ C $T_A = -40^{\circ}$ C to $+85^{\circ}$ C |
| ADM81_S ADM81_R | 2.58 | 2.63 | 2.68 | V | $T_{A} = -40$ C to +85 C $T_{A} = +25^{\circ}$ C |
| — | | 2.05 | | VV | |
| ADM81_R | 2.55 | | 2.70 | V | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ |
| RESET THRESHOLD | | | | 10.0 | |
| TEMPERATURE COEFFICIENT | | 30 | | ppm/°C | |
| V _{CC} TO RESET/RESET DELAY | | 40 | | μs | V_{OD} = 125 mV, ADM81_L/M |
| | | 20 | | μs | V_{OD} = 125 mV, ADM81_R/S/T |
| RESET ACTIVE TIMEOUT PERIOD | 140 | | 560 | ms | $V_{CC} = V_{TH(MAX)}$ |
| | 300 | | 700 | ms | (ADM811-3T Only) |
| MANUAL RESET | | | | | |
| Minimum Pulsewidth | 10 | | | μs | |
| Glitch Immunity | | 100 | | ns | |
| RESET/RESET Propagation Delay | | 0.5 | | μs | |
| Pull-Up Resistance | 10 | 20 | 30 | kΩ | |
| The Manual Reset Circuit Will Act On | 10 | 20 | 50 | | |
| An Input Rising Above | 2.3 | | | V | $V_{CC} > V_{TH(MAX)}$, ADM81_L/M |
| An Input Falling Below | 2.5 | | 0.8 | v | $V_{CC} > V_{TH(MAX)}, ADM81_L/M$ |
| An Input Rising Above | $0.7 \times V_{CC}$ | | 0.0 | v | $V_{CC} > V_{TH(MAX)}, ADM81_R/S/T$ |
| An Input Falling Below | 0.7 × VCC | | $0.25 \times V_{CC}$ | V | $V_{CC} > V_{TH(MAX)}, ADM81_R/S/T$ $V_{CC} > V_{TH(MAX)}, ADM81_R/S/T$ |
| | | | 0.2J × V _{CC} | v | $V_{\rm CC} > V_{\rm TH(MAX)}, AD WOT_NS/1$ |
| RESET Output Voltage | | | 0.2 | X 7 | $\mathbf{X} = \mathbf{X}$ $\mathbf{I} = 1 2 \cdots \mathbf{A}$ |
| Low (ADM812R/S/T) | | | 0.3 | V | $V_{CC} = V_{TH(MAX)}$, $I_{SINK} = 1.2 \text{ mA}$ |
| Low (ADM812L/M) | 0.0.17 | | 0.4 | V | $V_{CC} = V_{TH(MAX)}$, $I_{SINK} = 3.2 \text{ mA}$ |
| High (ADM812R/S/T/L/M) | 0.8 V _{CC} | | 0.0 | V | $1.8 \text{ V} < \text{V}_{\text{CC}} < \text{V}_{\text{TH(MIN)}}, \text{I}_{\text{SOURCE}} = 150 \mu\text{A}$ |
| Low (ADM811R/S/T) | | | 0.3 | V | $V_{CC} = V_{TH(MIN)}$, $I_{SINK} = 1.2 \text{ mA}$ |
| Low (ADM811L/M) | | | 0.4 | V | $V_{CC} = V_{TH(MIN)}, I_{SINK} = 3.2 \text{ mA}$ |
| Low (ADM811R/S/T/L/M) | | | 0.3 | V | $V_{CC} > 1.0 \text{ V}, \text{ I}_{\text{SINK}} = 50 \ \mu\text{A}$ |
| High (ADM811R/S/T) | $0.8 V_{CC}$ | | | V | $V_{CC} > V_{TH(MAX)}$, $I_{SOURCE} = 500 \ \mu A$ |
| High (ADM811L/M) | V _{CC} -1.5 | | | V | $V_{CC} > V_{TH(MAX)}$, $I_{SOURCE} = 800 \ \mu A$ |

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(Typical values are at $T_A = +25^{\circ}C$ unless otherwise noted)

Terminal Voltage (With Respect to Ground)

| V_{CC} |
|--------------------------------------------------------------------------------------------------------------------------------------|
| All Other Inputs $\dots \dots \dots$ |
| Input Current |
| V _{CC} |
| $\overline{\mathrm{MR}}$ 20 mA |
| Output Current |
| RESET, RESET 20 mA |
| Power Dissipation ($T_A = +70^{\circ}C$) |
| RT-4, SOT-143 200 mW |
| Derate by 4 mW/°C above +70°C |
| θ_{JA} Thermal Impedance |
| |

| Operating Temperature Range40°C to +85°C |
|--------------------------------------------|
| Storage Temperature Range65°C to +160°C |
| Lead Temperature (Soldering, 10 sec)+300°C |
| Vapor Phase (60 sec)+215°C |
| Infrared (15 secs)+220°C |
| ESD Rating 3 kV |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ADM811/ADM812

PIN FUNCTION DESCRIPTIONS

| Pin | Mnemonic | Function |
|-----|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | GND | 0 V. Ground reference for all signals. |
| 2 | RESET (ADM811) | Active Low Logic Output. RESET remains low while V_{CC} is below the reset threshold or when \overline{MR} is low, RESET then remains low for at least 140 ms (at least 300 ms for the ADM811-3T) after V_{CC} rises above the reset threshold. |
| 2 | RESET (ADM812) | Active High Logic Output. RESET remains high while V_{CC} is below the reset threshold or when \overline{MR} is low, RESET then remains high for 240 ms (typical) after V_{CC} rises above the reset threshold. |
| 3 | MR | Manual Reset. This active low debounced input will ignore input pulses of 100 ns or less (typical) and is guaranteed to accept input pulses of greater than 10 μ s. Leave floating when not used. |
| 4 | V _{CC} | +3 V, +3.3 V or +5 V monitored supply voltage. |

PIN CONFIGURATION

| GND 1 | ADM811/ ADM812 | ₄ v _{cc} |
|---------------|----------------------------|-------------------|
| RESET/RESET 2 | TOP VIEW (Not to Scale) | 3 MR |

ORDERING GUIDE

| Model* | Reset Threshold | Temperature Range | Brand Information | Quantity |
|-------------------|--------------------|------------------------------------|----------------------|-------------|
| ADM811LART-REEL | 4.63 V | -40°C to +85°C | MBV | 10K |
| ADM811LART-REEL-7 | 4.63 V | -40° C to $+85^{\circ}$ C | MBV | 3K |
| ADM811MART-REEL | 4.38 V | -40° C to $+85^{\circ}$ C | MBT | 10K |
| ADM811MART-REEL-7 | 4.38 V | -40° C to $+85^{\circ}$ C | MBT | 3K |
| ADM811TART-REEL | 3.08 V | -40°C to +85°C | MBG | 10 K |
| ADM811TART-REEL-7 | 3.08 V | -40° C to $+85^{\circ}$ C | MBG | 3K |
| ADM811-3TART-REEL | 3.08 V | -40° C to $+85^{\circ}$ C | MB3 | 10K |
| ADM811-3TART-RL7 | 3.08 V | -40° C to $+85^{\circ}$ C | MB3 | 3K |
| ADM811SART-REEL | 2.93 V | -40°C to +85°C | MBE | 10 K |
| ADM811SART-REEL-7 | 2.93 V | -40° C to $+85^{\circ}$ C | MBE | 3K |
| ADM811RART-REEL | 2.63 V | -40° C to $+85^{\circ}$ C | MBB | 10K |
| ADM811RART-REEL-7 | 2.63 V | -40°C to +85°C | MBB | 3K |
| ADM812LART-REEL | 4.63 V | -40°C to +85°C | MCV | 10K |
| ADM812LART-REEL-7 | 4.63 V | –40°C to +85°C | MCV | 3K |
| ADM812MART-REEL | 4.38 V | -40°C to +85°C | MCT | 10K |
| ADM812MART-REEL-7 | 4.38 V | -40°C to +85°C | MCT | 3K |
| ADM812TART-REEL | 3.08 V | –40°C to +85°C | MCG | 10K |
| ADM812TART-REEL-7 | 3.08 V | -40°C to +85°C | MCG | 3K |
| ADM812SART-REEL | 2.93 V | -40°C to +85°C | MCE | 10K |
| ADM812SART-REEL-7 | 2.93 V | –40°C to +85°C | MCE | 3K |
| ADM812RART-REEL | 2.63 V | -40°C to +85°C | MCB | 10K |
| ADM812RART-REEL-7 | 2.63 V | –40°C to +85°C | MCB | 3K |

*Only available in reels. Parts in **bol**d are ex-stock, please contact factory for availability.

ADM811/ADM812—Typical Performance Characteristics



Figure 2. Supply Current vs. Temperature (ADM81_R/S/T)



Figure 3. Power-Down RESET Delay vs. Temperature (ADM81_R/S/T)



Figure 4. Power-Up Reset Timeout vs. Temperature



Figure 5. Supply Current vs. Temperature (ADM81_L/M)



Figure 6. Power-Down RESET Delay vs. Temperature (ADM81_L/M)



Figure 7. Reset Threshold Deviation vs. Temperature

CIRCUIT INFORMATION RESET THRESHOLDS

The reset output provides a $\overline{\text{RESET}}$ (for the ADM811) or a RESET (for the ADM812) output to the microprocessor whenever the V_{CC} input is below the reset threshold. The actual reset threshold is dependent on whether a L, M, T, S or R suffix is used. Please refer to Table I.

Table I. Reset Threshold Options

| Model | RESET Threshold |
|--------------|--------------------|
| ADM811LART | 4.63 V |
| ADM811MART | 4.38 V |
| ADM811TART | 3.08 V |
| ADM811-3TART | 3.08 V |
| ADM811SART | 2.93 V |
| ADM811RART | 2.63 V |
| ADM812LART | 4.63 V |
| ADM812MART | 4.38 V |
| ADM812TART | 3.08 V |
| ADM812SART | 2.93 V |
| ADM812RART | 2.63 V |

Parts in bold type are ex-stock, please contact factory for availability.

RESET OUTPUT

On power-up and after V_{CC} rises above the reset threshold, an internal timer holds the reset output active for 240 ms (typical). This is intended as a power-on reset signal for the processor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset output is similarly activated and remains active for 240 ms (typical) after the supply recovers. This allows time for the power supply and microprocessor to stabilize.

The ADM811 provides an active low reset output ($\overline{\text{RESET}}$) while the ADM812 provides an active high output (RESET).

During power-down of the ADM811, the $\overline{\text{RESET}}$ output remains valid (low) with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the supply falls and also ensures that no spurious activity can occur via the μ P as it powers up.

MANUAL RESET

The ADM811/ADM812 is equipped with a manual reset input. This input is designed to operate in a noisy environment where unwanted glitches could be induced. These glitches could be produced by the bouncing action of a switch contact or where a Manual Reset switch may be located some distance away from the circuit (the cabling of which may pickup noise).

The Manual Reset input is guaranteed to ignore logically valid inputs which are faster than 100 ns and accept inputs longer in duration than 10 μ s.

GLITCH IMMUNITY

The ADM811/ADM812 contain internal filtering circuitry providing glitch immunity from fast transient glitches on the power supply line.



Figure 8. Power Fail RESET Timing

INTERFACING TO OTHER DEVICES Output

The ADM811/ADM812 series is designed to integrate with as many devices as possible. One feature of the ADM811/ ADM812 is the reset output, which is directly proportional to V_{CC} (this is guaranteed only while V_{CC} is greater than 1 V). This enables the part to be used in both 3 V and 5 V or any nominal voltage within the minimum and maximum specifications for V_{CC} .

THE BENEFITS OF A VERY ACCURATE RESET THRESHOLD

Because the ADM811/ADM812 series can operate effectively even when there are large degradations of the supply voltages, the possibility of a malfunction during a power failure is greatly reduced. Another advantage of the ADM811/ADM812 series is its very accurate internal voltage reference circuit. Combined, these benefits produce an exceptionally reliable Microprocessor Supervisory Circuit.



Figure 9. Ensuring a Valid \overline{RESET} Output Down to $V_{cc} = 0 V$

ENSURING A VALID RESET OUTPUT DOWN TO $V_{CC} = 0 V$

When V_{CC} falls below 0.8 V, ADM811s RESET no longer sinks current. Therefore, a high impedance CMOS logic input connected to RESET may drift to undetermined logic levels. To eliminate this problem a 100 k Ω resistor should be connected from RESET to ground.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

4-Lead Plastic Surface Mount Package (SOT-143)

