Multiphase IMVP-IV Core Controller for Mobile CPUs

ADP3205

FEATURES

Pin Programmable 1-, 2-, or 3-Phase Operation
Excellent Static and Dynamic Current Sharing
Superior Load Transient Response when Used with ADOPT™ Optimal Positioning Technology
Noise-Blanking for Speed and Stability
Synchronous Rectification Control for Optimized Light Load Efficiency
Soft DAC Output Voltage Transition for VID Change
Cycle-by-Cycle Current Limiting
Latched or Hiccup Current Overload Protection
Masked Power Good during Output Voltage Transients
Soft Start-Up without Power-On In-Rush Current Surge
2-Level Overvoltage and Reverse-Voltage Protection

APPLICATIONS

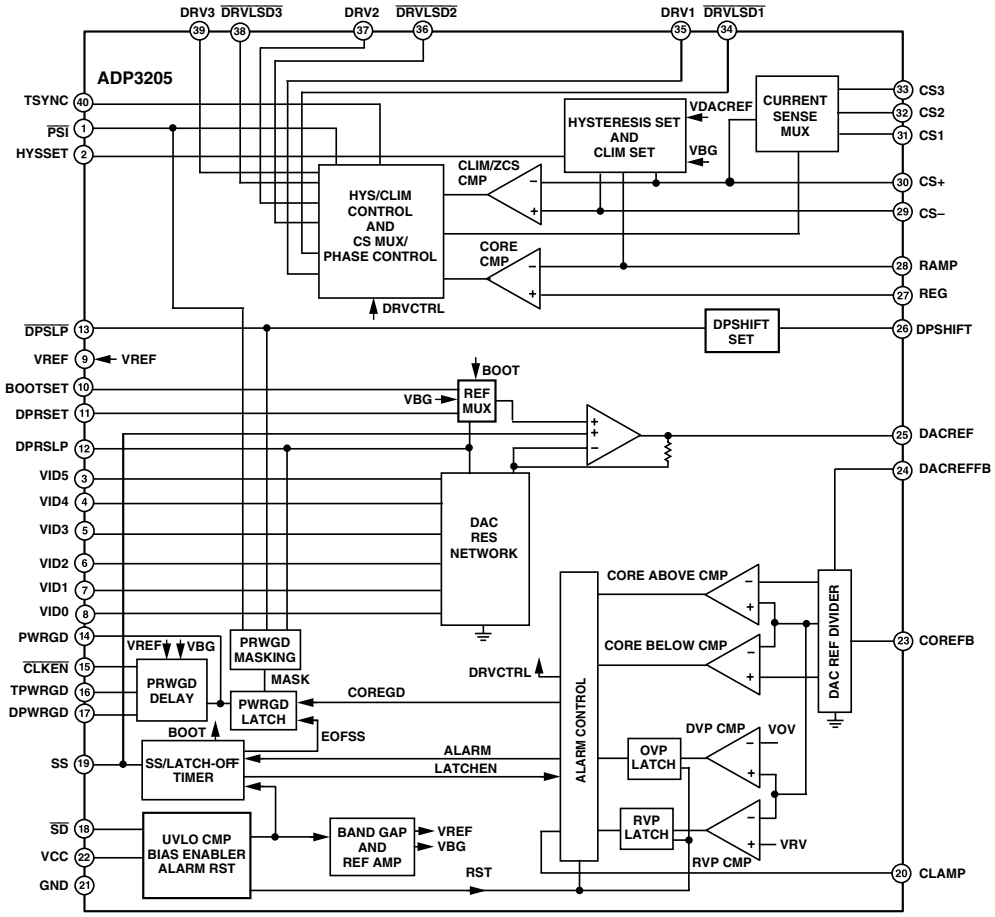
IMVP-IV CPU Core DC-to-DC Converters
Programmable Output Power Supplies

GENERAL DESCRIPTION

The ADP3205 is a 1-, 2-, or 3-phase hysteretic peak current mode dc-to-dc buck converter controller dedicated to powering a mobile processor's core. The chip optimized low voltage design runs from the 3.3 V system supply. The chip contains a precision 6-bit DAC whose nominal output voltage is set by VID code. The ADP3205 features high speed operation to allow a minimized inductor size that results in the fastest possible change of current to the output. To further minimize the number of output capacitors, the converter features active voltage positioning enhanced with ADOPT optimal compensation to ensure a superior load transient response. The output signals interface with ADP3415 MOSFET drivers, which that are optimized for high speed and high efficiency. The ADP3205 is capable of providing synchronous rectification control to extend battery lifetime in light load conditions.

The ADP3205 is specified over the extended commercial temperature range of 0°C to 100°C and is available in a 40-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective companies.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703 **© 2003 Analog Devices, Inc. All rights reserved.**

ADP3205–SPECIFICATIONS[1]

($0°C < T_A < 100°C$, High (H) = V_{CC}, Low (L) = 0 V, V_{CC} = 3.3 V, $\overline{SD}$ = H, $V_{COREFB} = V_{REFFB} = V_{DAC} (\equiv V_{DACREF})$, $V_{REG} = V_{CS-} = V_{VID}$ = 1.25 V, $R_{DACREFFB}$ = 50 Ω, $C_{DACREFFB}$ = 680 nF, $R_{DRV1} = R_{DRV2} = R_{DRV3}$ =100 kΩ, $C_{DRV1} = C_{DRV2} = C_{DRV3}$ = 10 pF, C_{SS} = 0.047 μF, R_{PWRGD} = 3 kΩ to V_{CC}, R_{CLAMP} = 5.1 kΩ to V_{CC}, HYSSET, DPSHIFT is open, $\overline{DPSLP}$ = H, DPRSLP = L, VBOOTSET = 1.0 V, VDPRSET = 1.0 V, unless otherwise noted.) Current sunk by a pin has a positive sign; current sourced by a pin has a negative sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY UVLO SHUTDOWN						
Normal Supply Current	I_{CC}			7	11	mA
UVLO Supply Current	$I_{CC(UVLO)}$				450	μA
Shutdown Supply Current	I_{CCSD}	$\overline{SD}$ = L, 3.0 V ≤ V_{CC} ≤ 3.6 V		60		μA
UVLO Threshold		$\overline{SD}$ = H				
	V_{CCH}	V_{CC} Ramping Up, V_{SS} = 0 V			2.95	V
	V_{CCL}	V_{CC} Ramping Down	2.65			V
		V_{SS} Floating				
UVLO Hysteresis[2]	V_{CCHYS}		50			mV
Shutdown Threshold ($\overline{SD}$ CMOS Input)	V_{SDTH}			$V_{CC}/2$		V
CORE FEEDBACK POWER GOOD						
Core Feedback Threshold Voltage	$V_{COREFBTH}$	0.7 V < V_{DAC} < 1.708 V				
		V_{COREFB} Ramping Up	1.12 V_{DAC}		1.14 V_{DAC}	
		V_{COREFB} Ramping Down	1.10 V_{DAC}		1.12 V_{DAC}	
		V_{COREFB} Ramping Up	0.88 V_{DAC}		0.90 V_{DAC}	
		V_{COREFB} Ramping Down	0.86 V_{DAC}		0.88 V_{DAC}	
Power Good Output Voltage	V_{PWRGD}	$V_{COREFB} = V_{DAC}$	0.95 V_{CC}		V_{CC}	V
(Open-Drain Output)		V_{COREFB} = 0.8 V_{DAC}	0		0.8	V
Masking Time	$t_{PWRGD, MSK}$[3]	V_{CC} = 3.3 V	80	200		μs
CLOCK ENABLER						
Output Voltage	V_{CLKENH}	V_{CC} = 3.0 V, $I_{\overline{CLKEN}}$ = –10 μA	2.5		3.0	V
	V_{CLKENL}	V_{CC} = 3.6 V, $I_{\overline{CLKEN}}$ = +10 μA	0		0.4	V
Delay Time (PWRGD to $\overline{CLKEN}$)	t_{DCLKEN}			10		μs
DELAYED POWER GOOD						
Output Current	$I_{DPWRGDH}$	V_{CC} = 3.0 V, Off		±0.1		μA
(Open-Drain Output)	$I_{DPWRGDL}$	V_{CC} = 3.6 V, On	1.0			mA
POWER GOOD DELAY TIMER						
Timing Threshold	$V_{TPWRGDTH}$			1.2		V
Input Current	I_{TPWRGD}	V_{TPWRGD} = 3 V		0.1		μA
Input Resistance	R_{TPWRGD}	V_{TPWRGD} = 1.3 V		320		Ω
SOFT START/LATCH-OFF TIMER						
Charge Current	I_{SS}	V_{SS} = 0.5 V		–32		μA
Discharge Current		V_{SS} = 0.5 V		+0.7		μA
Soft-Start Enable Threshold	V_{SSEN}	V_{REG} = 1.25 V,				
		$V_{RAMP} = V_{COREFB}$ = 1.27 V				
		V_{SS} Ramping Down		200	300	mV
		V_{SS} Ramping Up[2]		150		mV
Soft-Start Termination Threshold	V_{SSTERM}	$V_{RAMP} = V_{COREFB}$ = 1.27 V				
		V_{SS} Ramping Up	1.70	2.00	2.25	V
FIXED REFERENCE						
Output Voltage	V_{REF}	–10 μA ≤ I_{VREF} ≤ 10 μA	1.666	1.700	1.734	V
VID PROGRAMMED DAC						
REFERENCE						
VID Input Threshold (MOS Inputs)	$V_{VID0..5}$			0.5		V
Output Voltage	V_{DAC}	See VID Code Table I	0.700		1.708	V
Static Tolerance (at a Given VID)	$\Delta V_{DAC}/V_{DAC}$					
		1.708 V ≥ V_{DAC} ≥ 0.860 V	–1.0		+1.0	%
		0.844 V ≥ V_{DAC} ≥ 0.700 V	–8.4		+8.4	mV
Settling Time	t_{DACS}[4]	C_{DACREF} = 10 nF		3.5		μs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC REFERENCE FEEDBACK						
Input Resistance	$R_{DACREFFB}$			80		kΩ
CORE COMPARATOR						
Input Offset Voltage (Ramp–Reg)	V_{COREOS}	V_{REG} = 1.25 V		±0.5	±4	mV
Input Bias Current	I_{REG}, I_{RAMP}	V_{REG} = V_{RAMP} = 1.25 V		±1		µA
Output Voltage	V_{DRV_H}	V_{CC} = 3.0 V	2.5			V
(DRV1, DRV2, and DRV3)	V_{DRV_L}	V_{CC} = 3.6 V			0.8	V
Propagation Delay Time	$t_{RMPODRV\_PD}$[5]	T_A = 25°C		60		ns
(RAMP–DRV1, RAMP–DRV2, RAMP–DRV3)				70		ns
Rise and Fall Time	t_{DRV_R}[6]			8		ns
(DRV1, DRV2, and DRV3)	t_{DRV_F}[6]			9		ns
Noise Blanking Time	t_{BLNK}	DRV L-H Transition		80		ns
		DRV H-L Transition		140		ns
CURRENT SENSE MULTIPLEXER						
Trans-Resistance	$R_{CS1–CS+}$	MUX Switch Is ON		150		Ω
	$R_{CS2–CS+}$	MUX Switch Is OFF		10		MΩ
	$R_{CS3–CS+}$					
Common-Mode Voltage Range	V_{CSCMR}	V_{CS1} = V_{CS2} = V_{CS3}	0		2	V
CURRENT LIMIT COMPARATOR						
Input Offset Voltage	V_{CLIMOS}	$V_{CS–}$ = 1.25 V		±2.5		mV
Input Bias Current	I_{CS+}, $I_{CS–}$	V_{CS+} = 1.25 V		–3	–5	µA
Propagation Delay Time	t_{CLPD}[5]	T_A = 25°C		65		ns
				85		ns
HYSTERESIS SETTING						
Hysteresis Current	I_{RAMP_H}	V_{REG} = 1.25 V				
	$–I_{CSP\_H}$	V_{COREFB} = V_{RAMP} = 1.23 V				
		I_{HYSSET} = 100 µA	–85	–100	–115	µA
		I_{HYSSET} = 10 µA		–10		µA
		V_{RAMP} = 1.27 V				
		I_{HYSSET} = 100 µA	85	100	115	µA
		I_{HYSSET} = 10 µA		10		µA
Hysteresis Reference Voltage	V_{HYSSET}			V_{DAC}		V
CURRENT LIMIT SETTING						
Limit Setting Current	$I_{CS–}$	V_{RAMP} = 1.23 V				
		V_{REG} = $V_{CS–}$ = V_{COREFB} = 1.25 V				
		V_{CS+} = 1.23 V				
		I_{HYSSET} = 100 µA	–268	–310	–335	µA
		I_{HYSSET} = 10 µA		–31.5		µA
		V_{CS+} = 1.27 V				
		I_{HYSSET} = 100 µA	–178	–208	–225	µA
		I_{HYSSET} = 10 µA		–21.5		µA
DEEP SLEEP SHIFT SETTING AND CONTROL						
DPSHIFT Inner Resistance	$R_{DPSHIFT}$	$\overline{DPSLP}$ = L		140		Ω
		$\overline{DPSLP}$ = H		10		MΩ
$\overline{DPSLP}$ Control Threshold (CMOS Input)	$V_{DPSLPTH}$			V_{CC}/2		V
DEEPER SLEEP VOLTAGE SETTING AND CONTROL[7]						
Input Current	I_{DPRSET}	V_{DPRSET} = 1.0 V		±0.1		µA
DPRSET Gain (DPRSET–DACREF)	A_{DPR}			1.09		V/V
DPRSLP Control Threshold (CMOS Input)	$V_{DPRSLPTH}$			V_{CC}/2		V

SPECIFICATIONS (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BOOT VOLTAGE SETTING						
Input Current	$I_{BOOTSET}$	$V_{BOOTSET}$ = 1.0 V		±0.1		µA
BOOTSET Gain (BOOTSET–DACREF)	A_{BOOT}			1.09		V/V
LOW-SIDE DRIVE CONTROL						
Output Voltage (CMOS Output)	$V_{\overline{DRVLSD1,2,3}}$	DPRSLP = H	0		0.4	V
		DPRSLP = L	0.7 V_{CC}		V_{CC}	V
Output Current	$I_{\overline{DRVLSD1,2,3}}$	DPRSLP = H, V_{DRVLSD} = 1.5 V	2			mA
		DPRSLP = L, V_{DRVLSD} = 1.5 V	–0.8			mA
POWER STATE INDICATOR						
$\overline{PSI}$ Control Threshold (MOS Input)	$V_{\overline{PSI}}$		0.30	0.5	0.70	V
SYNCHRONOUS TIMER						
Timing Threshold	V_{TSYNTH}			1.2		V
Input Current	I_{TSYNC}	V_{TSYNC} = 1.7 V DRV1 or DRV2 or DRV3 = L		±0.1		µA
Input Resistance	R_{TSYNC}	V_{TSYNC} = 1.3 V DRV1 or DRV2 or DRV3 = H		670		Ω
OVER/REVERSE VOLTAGE PROTECTION						
Overvoltage Threshold	$V_{COREFB, OVP}$	V_{COREFB} Rising		1.9		V
Reverse-Voltage Threshold	$V_{COREFB, RVP}$	V_{COREFB} Falling		–0.3		V
Output Voltage (Open-Drain Output)	V_{CLAMP}		0.7 V_{CC}		V_{CC}	V
Output Current	I_{CLAMP}	V_{COREFB} = V_{DAC}, V_{CLAMP} = 1.5 V			10	µA
		V_{COREFB} = 2.2 V, V_{CLAMP} = 0.8 V	1	6		mA

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]Guaranteed by design. Not production tested.

[3]Two test conditions: 1)PWRGD is OK but forced to fail by applying an out-of-the-CoreGood-window voltage ($V_{COREFB, BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) to the COREFB pin right after DPRSLP has been asserted/deasserted. PWRGD should not fail immediately only with the specified blanking delay time. 2) PWRGD is forced to fail ($V_{COREFB, BAD}$ = 1.0 V at V_{VID} = 1.25 V setting) but gets into the CoreGood-window ($V_{COREFB, GOOD}$ = 1.25 V) right after DPRSLP has been asserted/deasserted. PWRGD should not go high immediately only with the specified blanking delay time.

[4]Measured from 50% of VID code transition amplitude to the point where V_{DACREF} settles within ±1% of its steady state value.

[5]40 mV p-p amplitude impulse with 20 mV overdrive. Measured from the input threshold intercept point to 50% of the output voltage swing.

[6]Measured between the 30% and 70% points of the output voltage swing.

[7]DPRSLP circuit meets the minimum 30 ns DPRSLPVR signal assertion requirement; guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage (V_{CC}) . . . . . –0.3 V to +7 V
All Other Inputs/Outputs . . . . . –0.3 V to V_{CC} + 0.3 V
Operating Ambient Temperature Range . . . . . 0°C to 100°C
Junction Temperature Range . . . . . 0°C to 150°C
Junction-to-Ambient Thermal Resistance . . . . . 98°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

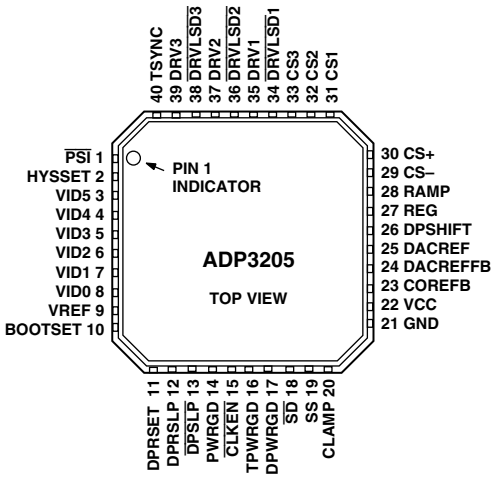
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Quantity per Reel
ADP3205JCP-Reel	0°C to 100°C	LFCSP-40	CP-40	2500

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3205 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$\overline{\text{PSI}}$	Power Status Indicator. This is a digital input pin that is driven low when the CPU enters into either deep sleep or deeper sleep modes. The drive signal is normally a PSB level CMOS signal, but the chip is also capable of handling V_{CC} level logic signals. The $\overline{\text{PSI}}$ signal is indicative of a light load condition, and because of that, it is used for enabling discontinuous current mode operation. Combined with the $\overline{\text{STPCPU}}$ and DPRSLPVR signals, the $\overline{\text{PSI}}$ signal can control power good masking. The $\overline{\text{PSI}}$ signal, and consequently the generated masking signal, carries the necessary masking time determined by system signal specification.
2	HYSSET	Hysteresis Set. This is an analog I/O pin whose output is a fixed voltage reference and whose input current is programmed by an external resistance to ground. The current is used in the IC to set the hysteretic currents for the core comparator and the current limit comparator. Modification of the resistance will affect both the hysteresis of the feedback regulation and the current limit set point and hysteresis.
3–8	VID[5:0]	Voltage Identification. These are the VID inputs for logic control of the programmed reference voltage that appears at the DACREF pin, and, via external component configuration, is used for setting the output voltage regulation point. The VID code sets the DAC output voltage directly except in deeper sleep mode and bootset mode, where the DPRSET or BOOTSET voltage determines it. The VID signals are normally PSB level CMOS signals, but the chip is also capable of handling V_{CC} level logic signals.
9	VREF	Reference Voltage Pin. This pin provides a VREF reference voltage to set the boot voltage and the deeper sleep voltages.
10	BOOTSET	Boot Voltage Set. This is a high impedance analog input pin. At power-up, the DACREF voltage ramps up, by default, to a boot voltage determined by this pin. The pin voltage can be set by an external resistor divider that is driven by the fixed VREF reference voltage. There is a nonunit gain from the BOOTSET pin to the DACREF output.
11	DPRSET	Deeper Sleep Voltage Set. This is a high impedance analog input pin. In deeper sleep mode, the DACREF voltage is determined by this pin. The pin voltage can be set by an external resistor divider that is driven by the VREF pin's reference voltage. There is a nonunit gain from the BOOTSET pin to the DACREF output.
12	DPRSLP	Deeper Sleep Control (Active High). This is a digital input pin that is driven by the system's DPRSLPVR signal. Its active high state corresponds to deeper sleep mode operation. When it is activated, the signal controls the DACREF amplifier output voltage by disconnecting the DAC resistor network from the DACREF amplifier and using it as a unity gain buffer. When it is deactivated, the DAC resistor network connection is restored, and the voltage level is determined by the external VID code. The DPRSLPVR signal is also used to initiate a PWRGD masking period to disable its response to a pending dynamic core voltage change triggered by a DACREF voltage transition.
13	$\overline{\text{DPSLP}}$	Deep Sleep Control (Active Low). This is a digital input pin that is driven by the system's $\overline{\text{STPCPU}}$ signal, which, in its active low state, corresponds to deep sleep mode of operation.
14	PWRGD	Power Good (Active High). This is an open-drain output pin which, via the assistance of an external pull-up resistor tied to V_{CC}, indicates that the core voltage is within the specified tolerance of the VID programmed value. PWRGD is deactivated (pulled low) when the IC is either disabled, in UVLO mode, or starting up, or the COREFB voltage is out of the core power good window. The open-drain output allows external wired ANDing (logical NORing) with other open-drain/collector power good indicators.

PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Function
15	$\overline{\text{CLKEN}}$	Clock Enable. This is an active low, V_{CC} level logic output signal. It is used to enable the CPU's clock generator module. The signal is asserted low with some internally set delay after all the wired-ANDed, open-drain power good signals (PWRGD of the core controller, of the PSB, and of the MCH chipset converters) report power is okay by allowing the common PWRGD node voltage to go high.
16	TPWRGD	Power Good Delay Time Set. This is an analog input-output pin that is used to set the delay time from the shared PWRGD signal assertion to DPWRGD assertion. The delay time is set by the external RC network. The R resistor is connected from the pin to the VREF reference pin and provides charge current into the C capacitor connected from the pin to GND. The charge period starts when PWRGD asserts high and terminates when the pin voltage reaches the TPWRGD threshold. Due to the band gap referenced termination and target thresholds, the delay accuracy practically depends only on the accuracy of the external RC components. In case of power good failure, DPWRGD deasserts low without any delay relative to PWRGD deassertion.
17	DPWRGD	Delayed Power Good Output. This is an open-drain digital output pin that requires an external pull-up resistor. The pin active high assertion indicates that the delay of the merged power good signals is expired and the CPU reset period can be terminated.
18	$\overline{\text{SD}}$	Shutdown (Active Low). This is a digital input pin that is driven by a system signal (VR-ON), which, in its active low state, shuts down the IC operation, placing the IC in its lowest quiescent current state for maximum power savings.
19	SS	Soft Start. This is an analog I/O pin whose output is a controlled current source used to charge or discharge an external grounded capacitor and whose input is the detected voltage that is indicative of elapsed time. The pin controls the soft-start time of the IC and also times the delay before the chip latches off following a current overload event.
20	CLAMP	Clamp Output (Active High). This is an open-drain output pin, which, via the assistance of an external pull-up resistor, indicates that the core voltage should be clamped for its protection. To allow the highest level of protection, the CLAMP signal is developed using both a redundant reference and a redundant feedback path with respect to those of the main regulation loop. The signal is timed out using the soft-start capacitor, so an external current protection mechanism (e.g., fuse or ac adapter's current limit) should be tripped within ~3 times the programmed soft-start time (e.g., 5 ms to 10 ms). In a preferred and more conservative configuration, the core voltage is clamped by an external FET. The initial protection function is served when it is activated by detection of either an overvoltage or a reverse-voltage condition on the COREFB pin. A backup protection function due to loss of the latched signal at IC power-off is served by connecting the pull-up resistor to a system "ALWAYS" regulator output (e.g., V5_ALWAYS). If an external FET is used, this implementation will keep the core voltage clamped until the ADP3205 has the power reapplied, thus keeping protection for the CPU even after a hard failure (e.g., a shorted top or bottom FET) caused power-down and restart.
21	GND	Ground
22	VCC	Power Supply. This should be connected to the system's 3.3 V power supply output.
23	COREFB	Core Feedback. This is a high impedance analog input pin that is used to monitor the output voltage for setting the proper state of the PWRGD and CLAMP pins. It is generally recommended to RC-filter the ripple and noise from the monitored core voltage, as suggested by the application schematic.
24	DACREFFB	Reference Feedback Input. This is an input pin for the core power good reference resistor divider. The pin is normally driven with a slew rate controlled version of the DACREF output voltage. The slew rate control can be achieved by the use of a low impedance RC network.
25	DACREF	Digital-to-Analog Converter Reference Output. This output voltage is the VID controlled reference voltage whose primary function is to determine the output voltage regulation point. During soft start, the reference output voltage tracks the ramping up SS voltage up to the BOOTSET pin determined level. It stays there until soft start times out. When soft start is terminated, DACREF ramps up or down to the VID code determined level.
26	DPSHIFT	Deep Sleep Shift. This is an analog I/O pin whose output is the DACOUT reference voltage and whose input is a current that is programmed by external resistors to ground. The current is used to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{DPSLP}}$ signal. When activated, the added offsetting current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to deep sleep mode of CPU operation. The use of the DACREF voltage as the reference for offset current generation makes the DPSHIFT to be a fixed percentage of the VID setting, as required by IMVP specifications.
27	REG	Regulation Voltage Summing Input. This is a high impedance analog input pin into which the voltage reference of the feedback loop allows the summing of both the DACREF voltage and the core voltage for programming the output resistance of the core voltage regulator. This is also the pin at which an optimized transient response can be tailored using Analog Devices' patented ADOPT compensation technique.

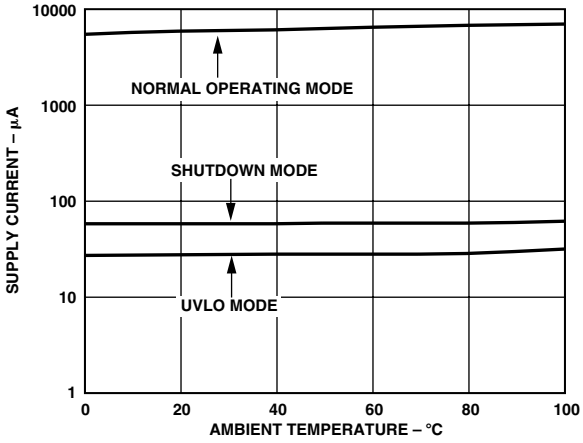
PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Function
28	RAMP	Regulation Ramp Feedback Input. The RAMP pin voltage is compared against the REG pin for cycle-by-cycle switching response. Several switched current sources also appear at this input, the cycle-by-cycle hysteresis-setting switched current programmed by the HYSSET pin, and the deep sleep shift current programmed by the DPSHIFT pin. The external resistive termination at this pin sets the magnitude of the hysteresis applied to the regulation loop.
29	CS–	Current Limit Negative Sense. This is a high impedance analog input pin that is normally Kelvin connected via a current-limit programming resistor to the negative node of the current sense resistor(s). A hysteretically controlled current—three times the current programmed at the HYSSET pin—also flows out of this pin and develops a current-limit-setting voltage across the current limit programming resistor that must then be matched by the inductor current flowing in the current sensing resistor in order to trigger the current limit function. When triggered, the current flowing out of this pin is reduced to two-thirds of its previous value, twice the HYSSET current, producing hysteresis in the current limiting function.
30	CS+	Current Limit Positive Sense. This is a high impedance analog input pin that is multiplexed between either of the current-sense inputs during the high state of the DRV pin of the respective channel. During the common off time of the channels, the pin's voltage reflects the average current of the channels. The multiplexed current sense signal is passed to the core comparator through an external resistive termination connected from this pin to the RAMP pin. The external (RAMP) resistor sets the magnitude of the hysteresis applied to the regulation loop.
31	CS1	Current Sense Channel 1. This is a high impedance analog input pin that is used to provide negative feedback of the current information for the first channel.
32	CS2	Current Sense, Channel 2. This is a high impedance analog input pin that is used to provide negative feedback of the current information for the second channel. The pin is also used to determine whether the chip is acting as a single or multiphase controller. If the CS2 pin is tied to V_{CC} but not to a sense resistor, three-phase operation is disabled. In this condition, the second phase output signal (DRV2) is not switching but stays static low; the first and third phase output signals (DRV1 and DRV3) are switching in-phase. It is the user's discretion to use only one of the two signals or both to drive a single- or dual-channel power stage.
33	CS3	Current Sense, Channel 3. This is a high impedance analog input pin that is used to provide negative feedback of the current information for the third channel. The pin is also used to determine whether the chip is acting as a dual- or three-phase controller. If the pin is tied to V_{CC} but not to a sense resistor, three-phase operation is disabled; the chip works as a dual-phase controller. In this condition, the third phase's drive signal (DRV3) is not switching but stays static low.
34, 36, 38	$\overline{\text{DRVLSD1}}$, $\overline{\text{DRVLSD2}}$, $\overline{\text{DRVLSD3}}$	Drive-Low Shutdown (Active Low). These are digital output pins which, in active state, indicate that the bottom FETs of the core regulator should be disabled. In the suggested application schematic, these pins are directly connected to the pin named similarly on the ADP3415 ICs. The ADP3205 achieves high conversion efficiency in light load conditions by using these pins for synchronous rectification control. During high-to-low voltage conversions and during overvoltage protection, the pin's voltage is always set high. During reverse-voltage protection, the pin's voltage is low.
35, 37, 39	DRV1, DRV2, DRV3	Drive Output 1, 2, and 3. These are digital output pins that are used to command the state of the switched nodes via the drivers and the power switches. They have to be connected to the driver inputs of the appropriate channels.
40	TSYNC	Synchronous Rectifier On-Time Setting. This is an analog input-output pin. In light load condition, i.e., when the $\overline{\text{PSI}}$ signal is asserted low and when the on-time of any of the active phases terminates, a timer common for all the phases is started. While the timer is active, the bottom MOSFET of the appropriate channel is kept turned on. When the timer times out, the bottom MOSFET of the relevant channel also gets turned off. If the timer is set right, the bottom MOSFET turn-off happens at the zero current crossing moment, and the ideal diode operation occurs. The delay time is set by the external RC network. The R resistor is connected from the pin to the VREF reference pin and provides charge current into the C capacitor connected from the pin to GND. The charge period starts when the active phase on-time terminates and the bottom MOSFET of the same phase turns on. The timer times out when the C capacitor voltage reaches the TSYNC pin threshold. Due to the band gap referenced termination threshold and the charge-target threshold, the TSYNC time accuracy practically depends only on the accuracy of the external RC components. Nonsynchronous operation can be disabled by shorting the TSYNC pin to GND.

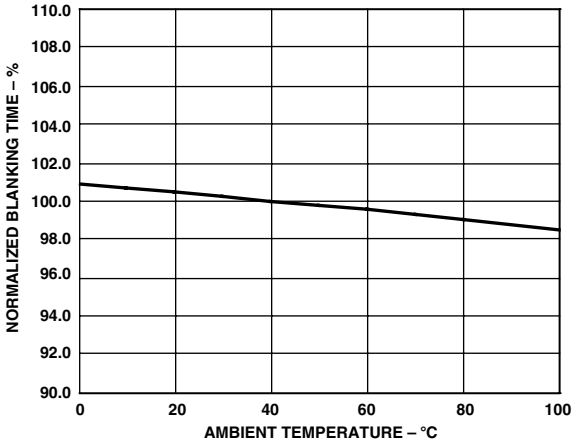
Table I. VID Code (V_{CCCORE} vs. VID)

VID						V_{CCCORE}	VID						V_{CCCORE}
5	4	3	2	1	0	(V)	5	4	3	2	1	0	(V)
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

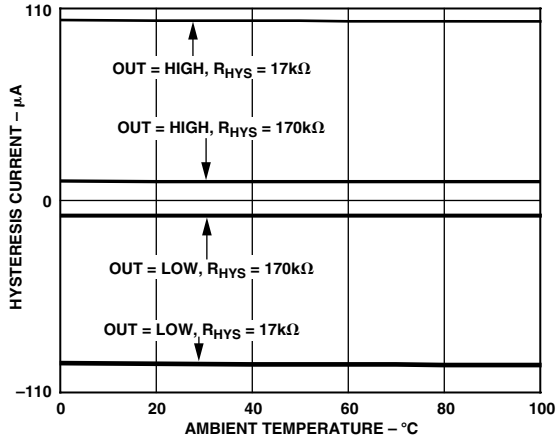
ADP3205–Typical Performance Characteristics



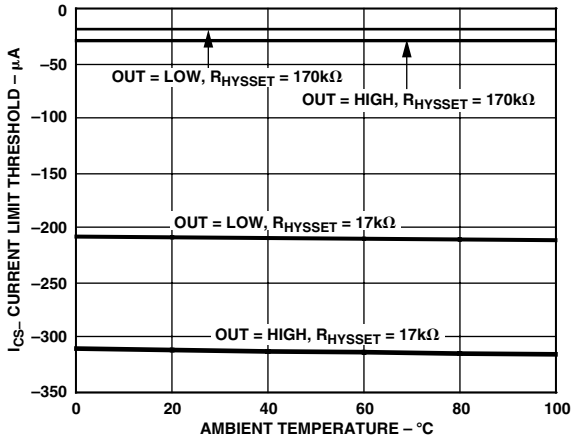
TPC 1. Supply Current vs. Temperature



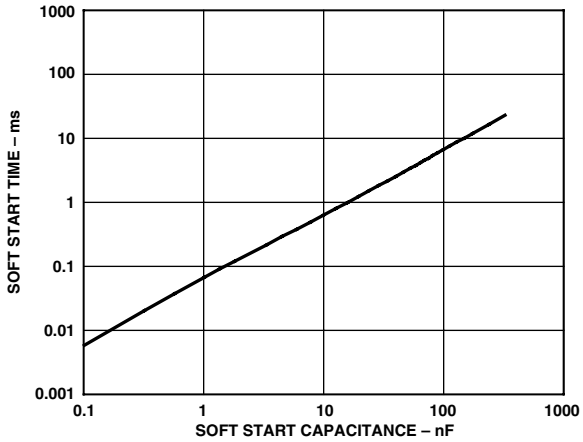
TPC 4. PWRGD Blanking Time vs. Temperature, Normalized to 25°C



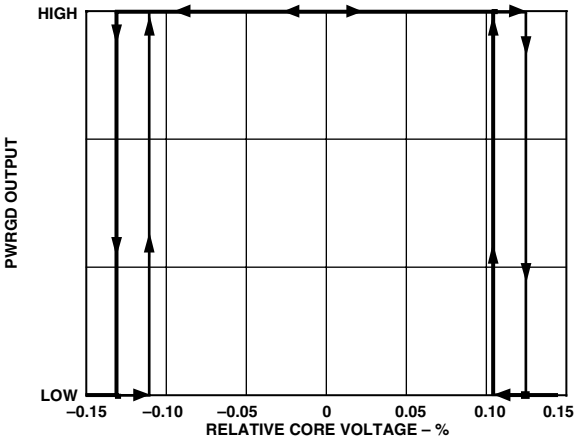
TPC 2. Core Hysteresis Current vs. Temperature



TPC 5. Current Limit Threshold vs. Temperature



TPC 3. Soft Start Timing vs. Timing Capacitor



TPC 6. Power Good vs. Relative Core Temperature

THEORY OF OPERATION

Theoretical Background

Featuring a new proprietary single or multiple phase buck converter hysteretic control architecture developed by Analog Devices, Inc., the ADP3205 is the optimal core voltage control solution for IMVP-IV Intel® mobile microprocessors.

The theoretical background for single and multiple phase dc-to-dc converters using the ADP3205 for Intel mobile CPUs is presented below. The ADP3205 features multiphase ripple regulators (also called hysteretic regulators), which allow employing the ADOPT (Analog Devices' Optimal Voltage Positioning) technique to implement the desired output voltage and load line, both statically and dynamically, as required by Intel's IMVPs specifications.

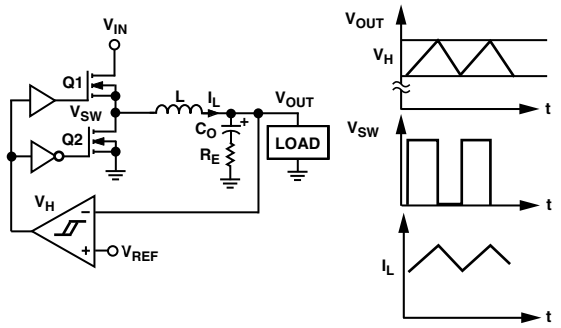


Figure 1. Conventional Hysteretic Regulator and Its Characteristic Waveforms

Figure 1 shows the conventional single-phase hysteretic regulator and the characteristic waveforms. The operation is as follows. During the time the upper transistor, Q1, is turned on, the inductor current, I_L, and also the output voltage, V_{OUT}, increase. When V_{OUT} reaches the upper threshold of the hysteretic comparator, Q1 is turned off, Q2 is turned on, and the inductor current and output voltage begin to decrease. The cycle repeats after V_{OUT} reaches the lower threshold of the hysteretic comparator.

Since there is no voltage-error amplifier in the hysteretic regulator, its response to any change in the load current or the input voltage is virtually instantaneous. Therefore, the hysteretic regulator represents the fastest possible dc-to-dc converter control technique. A disadvantage of the conventional hysteretic regulator is that its frequency varies proportionally with the ESR, R_E, of the output capacitor. Since the initial value is often poorly controlled, and the ESR of electrolytic capacitors also changes with temperature and age, practical ESR variations can easily lead to a frequency variation in the order of one to three. However, a modification of the hysteretic topology eliminates the dependence of the operating frequency on the ESR. In addition, the modification allows the optimal implementation, ADOPT, of Intel's IMVP-IV load-line specifications.

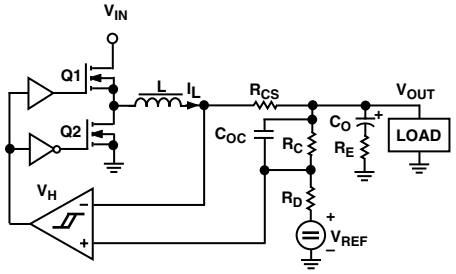


Figure 2. Modified Hysteretic Regulator with ADOPT

The implementation requires adding a resistive divider (R_C and R_D) between the reference voltage and the output, and connecting the tap of the divider to the noninverting input of the hysteretic comparator. A capacitor, C_{OC}, is placed across the upper member (R_C) of the divider.

It is easily shown that the output impedance of the converter can be no less than the ESR of the output capacitor. A straightforward derivation demonstrates that the output impedance of the converter can be minimized to equal the ESR, R_E, when the following two equations are valid (neglecting PCB trace resistance for now):

$$\frac{R_D}{R_C} = \frac{R_E - R_{CS}}{R_{CS}} \tag{1}$$

and

$$C_{OC} = \frac{C_O R_E^{\,2}}{R_{CS} R_D} \tag{2}$$

From (2), the series resistance is:

$$R_{CS} = \frac{R_E}{1 + \dfrac{R_D}{R_C}} \tag{3}$$

This is the ADOPT configuration and design procedure that allows the maximum possible ESR to be used while meeting a given load-line specification.

It can be seen from Equation 3 that unless R_D is zero or R_C is infinite, R_{CS} will be always smaller than R_E. An advantage of the circuit of Figure 2 is that if we select the ratio R_D/R_C well above unity, the additional dissipation introduced by the series resistance R_{CS} will be negligible. Another interesting feature of the circuit in Figure 2 is that the ac voltage across the two inputs of the hysteretic comparator is now equal only to the ac voltage across R_{CS}. This is due to the presence of the capacitor C_{OC}, which effectively couples the ac component of the output voltage to the noninverting input voltage of the comparator. Since the comparator sees only the ac voltage across R_{CS}, in the circuit of Figure 2, the dependence of the switching frequency on the ESR of the output capacitor is completely eliminated. Equation 4 presents the expression for the switching frequency.

$$f = \frac{R_{CS}}{L V_H} \frac{\left(V_{IN} - V_{OUT}\right) V_{OUT}}{V_{IN}} \tag{4}$$

Multiphase converters have certain, very important advantages, including reduced rms current in the input filter capacitor (allowing the use of a smaller and less expensive device), distributed heat dissipation (reducing the hot-spot temperature and increasing reliability), higher total power capability, increased equivalent frequency without increased switching losses (allowing the use of smaller equivalent inductances and thereby shortening the load transient time), and reduced ripple current in the output capacitor (reducing the output ripple voltage and allowing the use of smaller and less expensive output capacitors). Also, they have some disadvantages that should be considered when choosing the number of phases. Those disadvantages include the need for more switches and output inductors than in a single-phase design (leading to higher cost than a single-phase solution, at least below a certain power level), more complex control, and the possibility of uneven current sharing among the phases.

The ADP3205 controller alleviates two of the above disadvantages of multiphase converters. It presents a simple and cost-effective control solution and provides perfect current sharing among the phases. A simplified block diagram of a three-phase converter

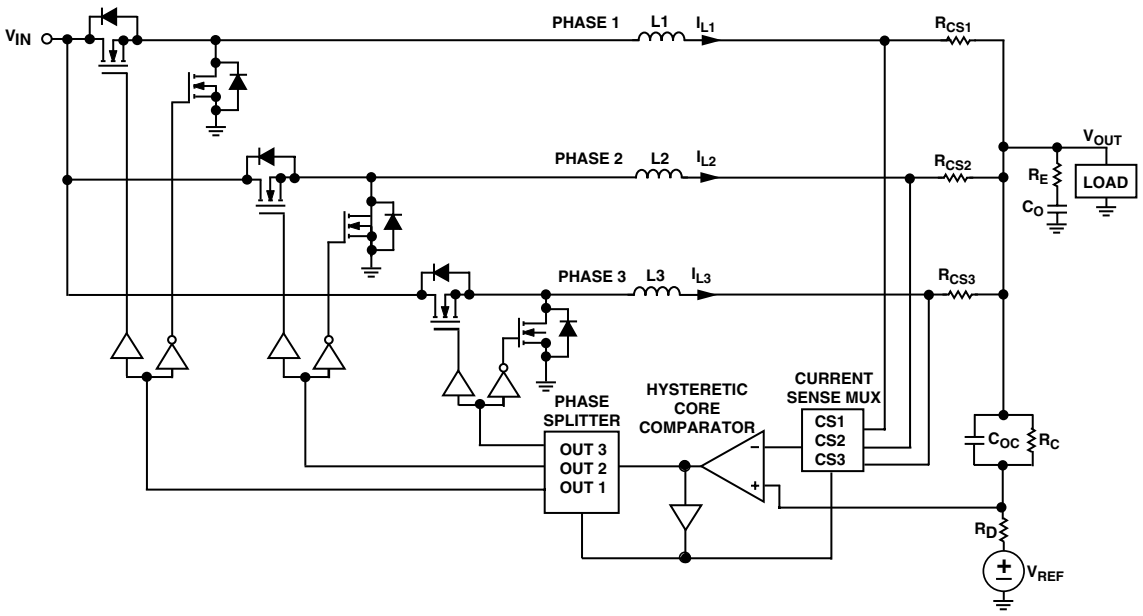


Figure 3. 3-Phase Modified Hysteretic Regulator with ADOPT

using the control principle implemented with the ADP3205 is shown in Figure 3.

As Figure 3 shows, in the multiphase configuration the ripple current signal is multiplexed from all phases. During the on-time of any given phase, its current is compared to the upper threshold of the hysteretic comparator. When the current reaches the upper threshold, the control FET of that phase is turned off. During the common off time of all phases, their currents are averaged and compared to the lower threshold. When the averaged phase current reaches the lower threshold, the hysteretic comparator changes state again and turns on the control FET of the next phase, as selected by the phase splitter logic. This control concept ensures that the peak currents of all phases will be the same, and therefore, the phase currents will be perfectly balanced. The ADOPT compensation can be used the same way as in the single-phase version previously discussed.

Implementation of Multiphase Hysteretic Control and ADOPT

With a properly applied ADOPT capacitor, C_C, the ADP3205 implements hysteretic control of ripple current. The resistor from the HYSSET pin to ground sets up a current that is switched bidirectionally into a resistor interconnected between the RAMP and CS+ pins. The switching of this current sets the hysteretic control signal for the ripple current. By setting the HYSSET pin voltage equal to the DACREF voltage, the ripple current is set proportional to the V_{CORE} voltage. In this way, the ADP3205 keeps switch frequency constant at different V_{CORE} voltages.

When more than one phase is used, the ripple current signals from the CS1, CS2, and CS3 pins are multiplexed. During the on-time of any given phase, its current is compared to the upper threshold of the hysteretic control. During the common off-time of all phases, their currents are averaged and compared to the lower threshold of the hysteretic control.

The ADOPT compensation provides the optimum output voltage containment within a specified voltage window or along a specified load-line using the fewest possible number of output capacitors. Figure 4 shows the step-off load transient of the application circuit in Figure 13.

At a certain CPU core voltage, the inductor ripple current is kept constant while the output voltage is regulated with fully programmable voltage positioning parameters that can be tuned to optimize the design for any particular CPU regulation specifications. By controlling the ripple current rather than the ripple voltage, the frequency variations associated with changes in output impedance for standard ripple regulators do not appear.

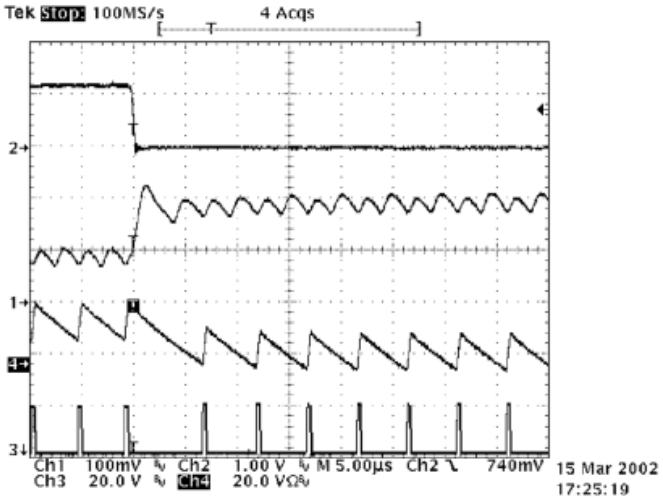


Figure 4. Step Load Transient

- Ch 1: V_{CORE} (1.0 V offset)
- Ch 2: Load current signal (load current step from 32 A to 7 A)
- Ch 3: SW node voltage
- Ch 4: Current of inductor (20 A/div)

Command the MOSFET Driver

Driving of the individual phase is accomplished by using external MOSFET drivers, such as the ADP3415. Each phase owns two PWM interface pins: the DRV and DRVLSD. The top MOSFET is turned on when the DRV pin is high; the bottom MOSFET is turned on when the DRV pin is low and the DRVLSD pin is high. The DRVLSD pin commands to turn off the bottom MOSFET at light load current condition to achieve high power conversion efficiency as well as at reverse voltage protection.

Current Sensing, Current Sharing, and Current Limit

Accurate current sensing is needed to accomplish output voltage positioning accurately, which, in turn, is required both to meet specification and to allow the minimum number of output capacitors to be used to contain transients. A current sense resistor is used between each inductor and the output capacitors. To allow the control to operate without amplifiers, a negative feedback signal is multiplexed from the inductor, or the upstream, side of the current sense resistors, and a positive feedback signal for load-line tuning is multiplexed from the output or downstream side.

Static and dynamic current sharing is achieved by keeping the voltage across the sense resistor of each phase identical. Since all the phases are sharing one hysteretic comparator, the IC parasitic mismatch between phases is minimized, leading to good performance in current sharing.

The current programmed at the HYSSET pin and a resistor from the CS– pin to the common node of the current sense resistors set the peak current limit. If the current limit threshold is triggered, the top MOSFET of that phase is turned off immediately by setting the DRV pin low. Thus, cycle-by-cycle peak current limit is achieved. Also a hysteresis is applied to the current limit threshold so that hysteretic control is maintained during the current limited operation.

Soft Start and Power-On Sequence

Soft start is implemented by forcing the DACREF voltage to track the SS pin voltage at power-on. A capacitor from the SS pin to ground programs the soft start time.

The power-on sequence of the ADP3205 is illustrated in Figure 5. The 3.3 V for the ADP3205 and 5.0 V for the MOSFET driver are required to be established before the system $\overline{SD}$ signal enables the ADP3205. The SS pin voltage increases linearly. The ADP3205 regulates the V_{CORE} voltage to follow the DACREF voltage. The DACREF voltage rises to V_{BOOT}, which is programmed at the BOOTSET pin, and stays there while the SS pin voltage continues to rise. When the SS pin voltage hits V_{SSTERM}, the ADP3205 will set PWRGD (power good signal) by checking whether the V_{CORE} voltage is within the good window of the DACREFFB voltage. The $\overline{CLKEN}$ will be asserted 10 µs after the assertion of PWRGD. The PWRGD is an open-collector pin. Power good signals from the MCH and VTT rail can pull this pin to low. 3 ms to 10 ms later, the DPWRGD (the IMVP-IV power good) signal is asserted. This 3 ms to 10 ms delay is programmed by a resistor and a capacitor on the TPWRGD pin.

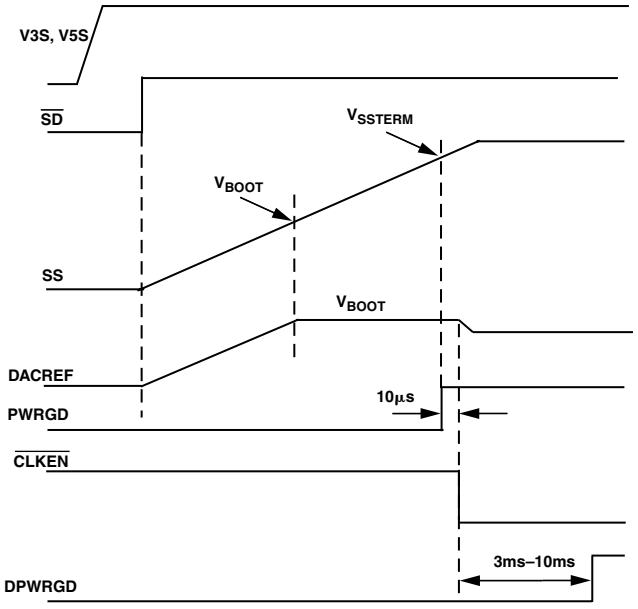


Figure 5. Power-On Sequence

Soft V_{CORE} Transient

During the transient between two CPU core voltages, such as the transient between deep sleep mode and deeper sleep mode, soft transient of V_{CORE} is implemented to reduce inrush current of the inductor and of MOSFETs as well as to reduce audio noise of input capacitors and inductors. An RC filter between the DACREF pin and the DACREFFB pin programs the duration of the soft transition.

The following two waveforms (Figures 6a and 6b) demonstrate that the soft V_{CORE} transition greatly reduces inrush current in the inductor. In a conventional V_{CORE} transient arrangement, the transient is completed in a short period of time, less than 20 µs, resulting in huge inductor current, which is only limited by the peak current limiter. In a soft V_{CORE} transient arrangement, the transient duration is programmed to be about 60 µs by the RC filter on the DACREF pin. As a result, the current stress to inductors, MOSFETs, and sense resistors is greatly reduced.

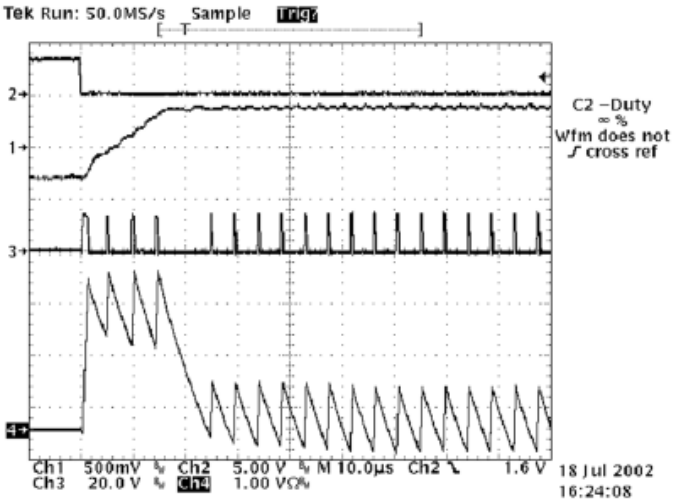


Figure 6a. Conventional V_{CORE} Transient

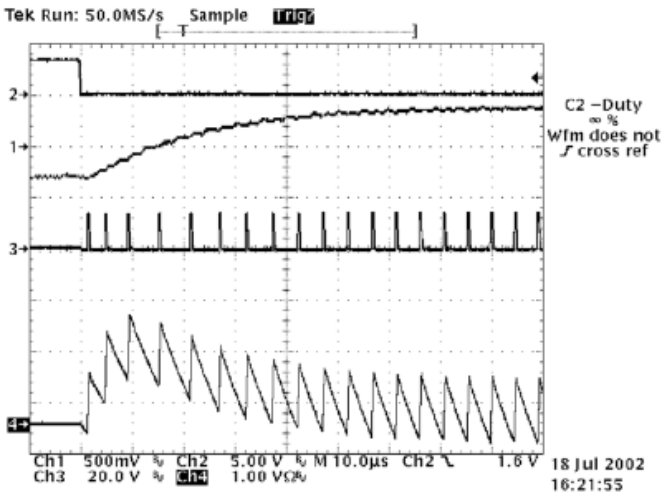


Figure 6b. Soft V_{CORE} Transient

- Ch 1: V_{CORE} (1 V offset)
- Ch 2: Current in inductor (10 A/div)
- Ch 3: DPRSLP signal
- Ch 4: Switch node

Output Voltage Programming

In the IMVP-IV specification, the output voltage is a function of both the system operating mode and the core current, according to a specified load line.

The nominal core voltage is set up at the DACREF pin, which is programmed in the following way:

- Deeper Sleep Mode: V_{DACREF} = 1.094 V_{DPRSET}
- Boot Up: V_{DACREF} = 1.094 $V_{BOOTSET}$
- All Other Conditions: V_{DACREF} is set by the VID Code

The voltages of the DPRSET and the BOOTSET pins are programmed by resistor dividers from a 1.7 V reference voltage provided at the VREF pin.

In deep sleep mode (the $\overline{\text{DPSLP}}$ pin is low), the CPU core voltage has to be offset by a dc value specified as a percentage of the DAC REF voltage in the IMVP-IV specification. This voltage offset is programmed by a resistor connected between the DSHIFT pin and the REG pin.

$\overline{\text{PSI}}$ and Power-Saving Operation

In deep sleep (C3) and deeper sleep (C4) mode, if the $\overline{\text{PSI}}$ signal from the CPU is asserted (low), indicating low CPU current, the ADP3205 switches into power-saving operation.

In power-saving operation, the bottom MOSFET is turned off before the inductor current becomes negative. As a result, the dc-to-dc converter runs in the discontinuous current mode. In discontinuous current operation mode, the ADP3205 keeps peak current proportional to the V_{CORE} voltage by setting the HYSSET pin voltage equal to that of the DACREF pin.

$$i_{PEAK} = \frac{2I_{HYSSET}R_A}{R_{CS}} = \frac{2V_{DACREF}R_A}{R_{HYSSET}R_{CS}} \quad (5)$$

The time period that the bottom FET is ON is also proportional to the peak current.

$$T_{SYNC} = \frac{i_{PEAK}L}{V_{CORE}} \quad (6)$$

Therefore, the time period, T_{SYNC} that the bottom MOSFET is ON is independent of V_{CORE} and battery voltage, assuming V_{CORE} = V_{DACREF}.

The ADP3205 programs T_{SYNC} with an RC circuit at the TSYNC pin, as shown in the system schematic in Figure 11, Figure 12, and Figure 13. The waveforms of power-saving operation are shown in Figure 7. The capacitor C_{SYNC} is discharged to zero voltage when the DRV pin of any of the phases is high. When the DRV pin goes low, C_{SYNC} starts charging up to the reference voltage through the R_{SYNC} resistor. When the voltage on the TSYNC pin hits the threshold V_{TSYNTH}, the ADP3205 sets the $\overline{\text{DRVLSD}}$ of the same phase low. The time period the bottom FET is on, T_{SYNC}, can be calculated as follows:

$$T_{SYNC} = R_{SYNC} \times C_{SYNC} \times \ln\left(\frac{1}{1 - \frac{V_{TSYNTH}}{V_{REF}}}\right) \quad (7)$$

where V_{REF} =1.7 V, V_{TSYNTH} = 1.2 V. The above formula can be simplified to:

$$T_{SYNC} = 1.22R_{SYNC}C_{SYNC} \quad (8)$$

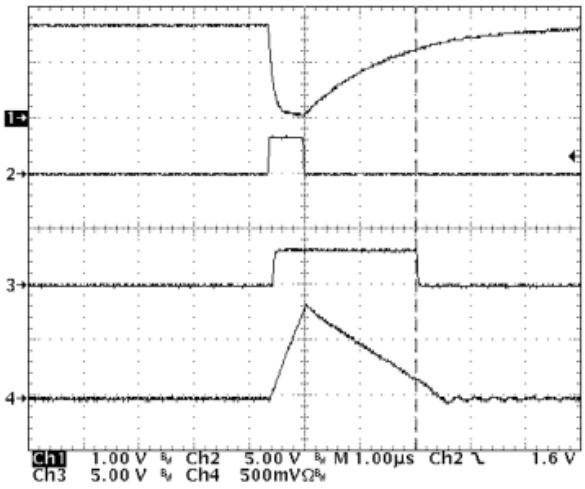


Figure 7. Power-Saving Mode Operation

- Ch 1: TSYNC pin voltage
- Ch 2: DRV pin voltage
- Ch 3: $\overline{\text{DRVLSD}}$ pin voltage
- Ch 4: Inductor current (5 A/div)

Usually, some margin is used to set TSYNC shorter than calculated by the above formula. The margin guarantees that the bottom MOSFET is turned off before the inductor current goes negative. Turning off the bottom MOSFET at the positive inductor current avoids the turn-on loss and EMI noise.

During the V_{CORE} voltage transient, such as switching the event from deeper sleep to deep sleep, this power-saving mode is disabled and the $\overline{\text{PSI}}$ signal is asserted to guarantee fast transition.

PROTECTION FEATURES

The ADP3205 provides comprehensive redundant protection features of OVP, RVP, and OCP to protect the CPU core as well as the power stage of the dc-to-dc converter from damage in various harsh conditions, as might be induced by a component or connection failure in the power stage or system.

Overvoltage Protection (OVP)

The CPU core voltage is monitored via the COREFB pin. OVP is triggered when the voltage of the COREFB pin is over 1.9 V.

Primary overvoltage protection is achieved by activating the crowbar function of the bottom MOSFETs via their driver ADP3415. The ADP3205 commands the MOSFET drivers to enter crowbar state by setting all the DRV pins low and setting all the $\overline{\text{DRVLSD}}$ pins high.

Meanwhile, the ADP3205 provides a redundant overvoltage protection feature via its CLAMP pin, which is an open-drain output pin. The CLAMP pin defaults to a low state at normal condition. If the OVP is triggered, the CLAMP pin is switched and pulled high by external pull-up resistors. The CLAMP pin is used to drive the gate of a power MOSFET whose drain-source is connected across the CPU core voltage and the CPU ground. Turning on this MOSFET will clamp the CPU core voltage to essentially zero, thus preventing further energy from being applied to the CPU core.

Once the OVP is triggered, the ADP3205 will latch itself in the OVP state, even after the system $\overline{\text{SD}}$ signal goes low. The latch is reset only by removing the V_{CC} power of the ADP3205 or recycling the $\overline{\text{SD}}$ signal to high again.

Reverse-Voltage Protection (RVP)

The RVP is implemented in the ADP3205 in the same architecture of the OVP function. RVP is triggered when the voltage on the COREFB pin is lower than –300 mV.

To prevent the CPU core voltage from being further negative, the ADP3205 commands the MOSFET drivers to turn off all the bottom MOSFETs by forcing all the DRV pins and the $\overline{\text{DRVLSD}}$ pins low.

Meanwhile, the CLAMP pin of the ADP3205 switches to high (pulled high by the external pull-up resistors). The clamp MOSFET whose drain-source is connected across the CPU core voltage is turned on. Thus, the CPU core voltage is quickly reset to essentially zero.

The ADP3205 will latch itself in the RVP state, even after the system $\overline{\text{SD}}$ signal goes low. The RVP latch is reset only by removing the V_{CC} power of the ADP3205 or recycling the $\overline{\text{SD}}$ signal to high again.

Overcurrent Protection (OCP)

When an overload or short happens at the output, the V_{CORE} voltage will drop out of the regulation window due to the cycle-by-cycle peak current limitation.

The ADP3205 enters hiccup mode after the V_{CORE} voltage drops out of the regulation window (power good fails). The frequency of the hiccup mode is controlled by the capacitance on the SS pin. If the overload or short on the output is removed, the ADP3205 can return to normal operation.

An external application circuit (a small-signal diode and resistor) can be used to clamp the SS pin voltage to obtain latched overcurrent protection as shown in Figure 11, Figure 12, and Figure 13.

Undervoltage Lockout

The ADP3205 includes an undervoltage lockout (UVLO) circuit to ensure that if V_{CC} is too low to maintain proper operation, the IC will remain off and in a low current state.

APPLICATION INFORMATION

The power stage must be planned before designing the control circuitry. The most important fundamental choice is how many parallel phases will be used. This choice depends on a number of factors, the most important of which is the thermal design, which is strongly affected by the choice of the power MOSFET switches and their mounting and thermal performance, the airflow, and so on. It is beyond the scope of this data sheet to provide a quantitative trade-off analysis. Historically, 14 A to 18 A per phase is an optimal maximization against the cost of adding another phase.

Inductor Selection

The inductor is selected based on two criteria: minimization of the output capacitors and trade-off between the power conversion efficiency and the size/cost of the power stage.

For the IMVP specifications on ripple voltage in both static and load transient operation, the optimized inductance should be the one that minimizes the output capacitance to meet both specifications. If the inductance is too small, the ripple current is high, and therefore, the output ripple voltage will be too high. To keep the output ripple voltage within the "ripple regulation window," more output capacitors are required. On the other hand, during step load transient, if the inductance is too large, the rate at which current can change is too slow, so more output capacitors would need to be added simply to hold up the output voltage while the inductors have time to respond.

Small inductance means large ripple current at a certain switch frequency. As a result, the turn-off loss of the top MOSFET increases as well as the conduction loss in MOSFETs and inductors. However, larger inductance potentially leads to a larger size footprint of the inductor and more output capacitors.

The selection of the inductance is an iterative process. A good initial value of the inductance is the one resulting in peak-to-peak ripple current of 50% of the maximum dc current per phase.

Output Capacitors

The output capacitor requirement is forced by the IMVP specifications on V_{CORE} voltage ripple in steady-state and transient. Under the existing cost structure, the most popular solution is the combination of MLCCs and specialty polymer capacitors. The combination provides both low ESR and large capacitance at relatively low cost.

During steady-state, due to the lower ESR effect, the V_{CORE} ripple is closer to a sinusoidal wave rather than triangle wave. Therefore, the steady-state V_{CORE} ripple can be estimated by the following equation:

$$V_{RPP} = Z_{CE} \frac{\left(1 - n_{PH} \times D\right) V_{CORE}}{f_S L} \quad (9)$$

Where V_{RPP} stands for the peak-to-peak ripple voltage, n_{PH} is the number of phases, L is the inductance of each phase, f_S is the switch frequency of each phase, and Z_{CE} is the impedance of the combined output capacitors at the ripple frequency, which equals the switch frequency times the number of phases. Also, D is the duty cycle of each phase.

Even under the extreme dynamic condition of a maximum load step (up or down) in the CPU current demand, the V_{CORE} voltage is still required to be within the window specified by IMVP. Since the ADP3205 can respond essentially as fast as possible, the undershoot and overshoot of V_{CORE} is mainly determined by the output capacitors. Usually, the worst dynamic is the overshoot during a step-off load from the maximum load current to minimum load current. Therefore, the minimum output capacitance is determined by having this worst-case overshoot within the specification window.

Input Capacitors

Use an input capacitance to output the current ratio of approximately 2 μF/A. Input capacitors are most effective in their filtering function when distributed evenly among the MOSFETs of parallel power phases and connected in close proximity to the MOSFETs on the power and ground planes. Very high frequency performance is needed, so MLCCs are a popular choice. The rms current rating of the input capacitors should be sufficient for the maximum input ripple current of the power stage, which is given by

$$I_{INRMS} = I_{OMAX} \times \sqrt{D\left(\frac{1}{n_{PH}} - D\right)} \quad (10)$$

where n_{PH} is the number of phases (that are operated out of phase), D is the duty ratio, and I_{OMAX} is the maximum output current. Duty cycle D, which equals V_O/V_{IN}, should be chosen at the worst-case condition for the input ripple current. The condition where V_{IN} is closest to $2 \times V_O \times n_{PH}$, even with three phases, is still typically the minimum input voltage at which the maximum load is allowed.

Antiparallel Schottky Diode

External antiparallel Schottky diodes (across the bottom MOSFET) may help improve efficiency a small amount (< ~1%) depending on their forward voltage drop compared to the MOSFET's body diode at a given current; a MOSFET with a built-in antiparallel Schottky is more effective. For an external Schottky, it should be placed next to the SR MOSFET or it may not be effective at all.

Clamp MOSFET and Connection

For a less comprehensively protective but also less costly solution, the CLAMP pin may be used to latch the disconnection of input power. The latch should be powered whenever any input power source is present. Typically, such a latching circuit is already present in a system design, so it becomes only a matter of allowing the CLAMP pin to also trigger the latch. In this configuration, the latched off-state of the system would be indicative of a system failure. The OV/RV protective means is provided by not allowing the continued application of energy to the CPU core. The design objective should be to ensure that the CPU core could safely absorb the remaining energy in the power converter, since this energy is not clamped as in the preferred configuration.

Control Design

Due to the substantial tightening of the CPU voltage regulation specifications, it has become important to preserve every millivolt of accuracy by considering second order regulation offset effects when selecting components. Therefore, the detailed design of a multiphase converter with the ADP3205 is rather complex. A design aid using the Mathcad™ program by Mathsoft™ has been developed. Please contact ADI for further information.

PCB LAYOUT AND COMPONENT PLACEMENT

The CPU core power supply must be carefully considered as part of the total system functional block placement and layout strategy. A good layout helps to increase power conversion efficiency, improve thermal management, and achieve better noise immunity of the control circuits.

Overall Placement

The ADP3205 sends digital signals to the drivers and interfaces with digital system signals, but it must sense very small analog signals with great precision: the output voltage error and the current signals. So the optimal placement of the ADP3205 is near the output and the current sense resistors, away from noise sources (e.g., switching power circuits). An ideal overall placement is illustrated in Figure 8. The ADP3205 sits immediately beside the sense resistors, while the power stage is around symmetrically. A sufficient number of vias should be placed immediately beside the downstream of the sense resistors, in order to conduct the high current from the power stage to the CPU pins. The ground area of each phase is placed near the ADP3205 side, so that the ADP3205 is isolated from the switching noise of the power stage.

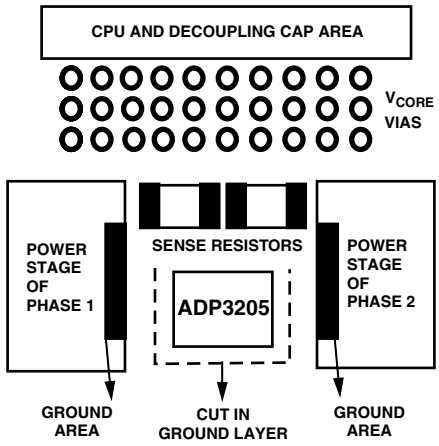


Figure 8. Overall Placement Example 1

Noise immunity can be improved by the use of a devoted signal ground plane for the ADP3205 and its surrounding components. If such a ground plane can be used, connect it into the main ground plane with several vias near the vicinity of the output capacitors. A cut around ADP3205 on the ground plan, as shown in Figure 8, serves the same purpose of a signal ground.

If the ideal recommended placement cannot be accommodated, care should be taken to keep the ADP3205 and surrounding components away from the radiation sources (e.g., from power inductors) and to keep the capacitive coupling away from noisy power nodes. If possible, please avoid the situation where the power stage stands between the sense resistors and the ADP3205. It is difficult to route the current sense trace if the current sense resistors and the ADP3205 are isolated by the noisy power stage. Again, a dedicated ground or ground cut is needed to avoid ground noise.

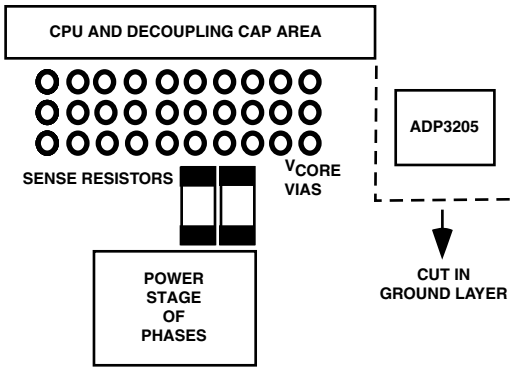


Figure 9. Overall Placement Example 2

Current Sense Resistors

1. Considering the high current levels at full load, the placement of the current sense resistors should be as close as possible to the CPU.
2. The voltage V_{CORE} is measured at the downstream heads of the sense resistors. Due to the high density current on the sense resistors' heads, it is required to join the two heads of the sense resistors as close as possible. The PCB traces from the sense resistors should be Kelvin connected as shown in Figure 10. If vias are used in the sensing signal traces, avoid power current passing the sensing signal vias.
3. For the two V_{CORE} traces from the downstream heads, it is essential to keep them symmetrical before they are joined together. Asymmetrical traces may lead to asymmetrical ac ripple in V_{CORE}. If space is available, make two long traces to the V_{CORE} signals before they are joined together.

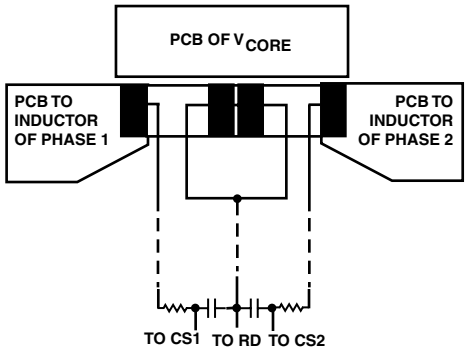


Figure 10. Kelvin Connection of Current Sensing Traces

4. The RC filter used for the current sense signal should be located near the control components; this filters out the effect of both the current sense resistors' parasitic inductance and the noise picked up along the routing of the signal. The former is achieved by having the time constant of the RC filters approximately matched to that of the sense resistors and is important for maintaining the accuracy of the current signal.
5. Absolutely avoid crossing any signal lines over the switching power path loop, described in the overall placement. If critical signal lines (e.g., signals from the current sense resistors leading back to the ADP3205) must cross through power circuitry, a signal ground plane is required to be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals.

MOSFET Driver

The drivers, unlike the control, should be located near the power MOSFETs that they drive. This separation of control and driver makes it possible for the optimal placement of the functional blocks of the CPU core power supply. Locate the ADP3415 near the MOSFETs so the loop inductance in the path of the top gate drive returned to the SW pin is small, and similarly for the bottom gate drive whose return path is the ground plane. The GND pin should have at least one very close via into the ground plane.

CPU and Power Stage

1. While HF bypass capacitors, i.e., small MLCCs, must be located directly under and within the CPU mounting area (as dictated in CPU system design manuals), even larger MLCCs and polarized bulk capacitors of the CPU core power supply must be located in close proximity to the CPU, i.e., around the periphery of the CPU. The physical area of the loop enclosed in the electrical path through the input bypass capacitors and around through the top and bottom MOSFETs (drain-source) should be small and wide. This is the switching power path loop.
2. There should be at least one solid ground plane interconnecting the CPU ground pins, the bypass and bulk capacitors, and the power delivery stage.
3. There must be a minimum of one solid power plane interconnecting the CPU core pins, the bypass and bulk capacitors, and the current sense resistors from which current is delivered from the several phases.
4. More ground and power planes can help in three ways: reducing copper resistance that degrades static and dynamic regulation, shielding of sensitive signal lines, and thermal performance. Don't let any PCB layers around the CPU remain unused; fill them with copper and use them for any or all of these purposes.
5. Make provisions for thermal management of all the MOSFETs. Heavy copper and wide traces to ground and power planes will help to pull the heat out. Heat sinking by a metal tap soldered in the power plane near the MOSFETs will help.
6. The CPU may be the number one power dissipator in the system, but it has a fan that is usually devoted to cooling the CPU. The CPU power delivery stage is the number two power dissipator in the PC system at maximum load. It has no devoted fan. Any airflow can help it. Channel the airflow across the CPU power delivery stage also, or even the reverse side of the PCB from where the power MOSFETs are mounted. Make sure the CPU is upstream in the airflow path so that the power delivery stage heat does not warm the air that cools the CPU.
7. Space must be allocated in the PCB layers for power flow vias. Vias interfere with signal lines from the CPU, but many vias are needed to minimize inductance and resistance in the power current path and for reducing thermal resistance to the copper power planes. It is best to locate the CPU power stage in a location where it is not necessary to pass many signals to the CPU pins. This technique will also leave available space on signal layers of the PCB near the power stage, so they can be used for extra power planes instead.

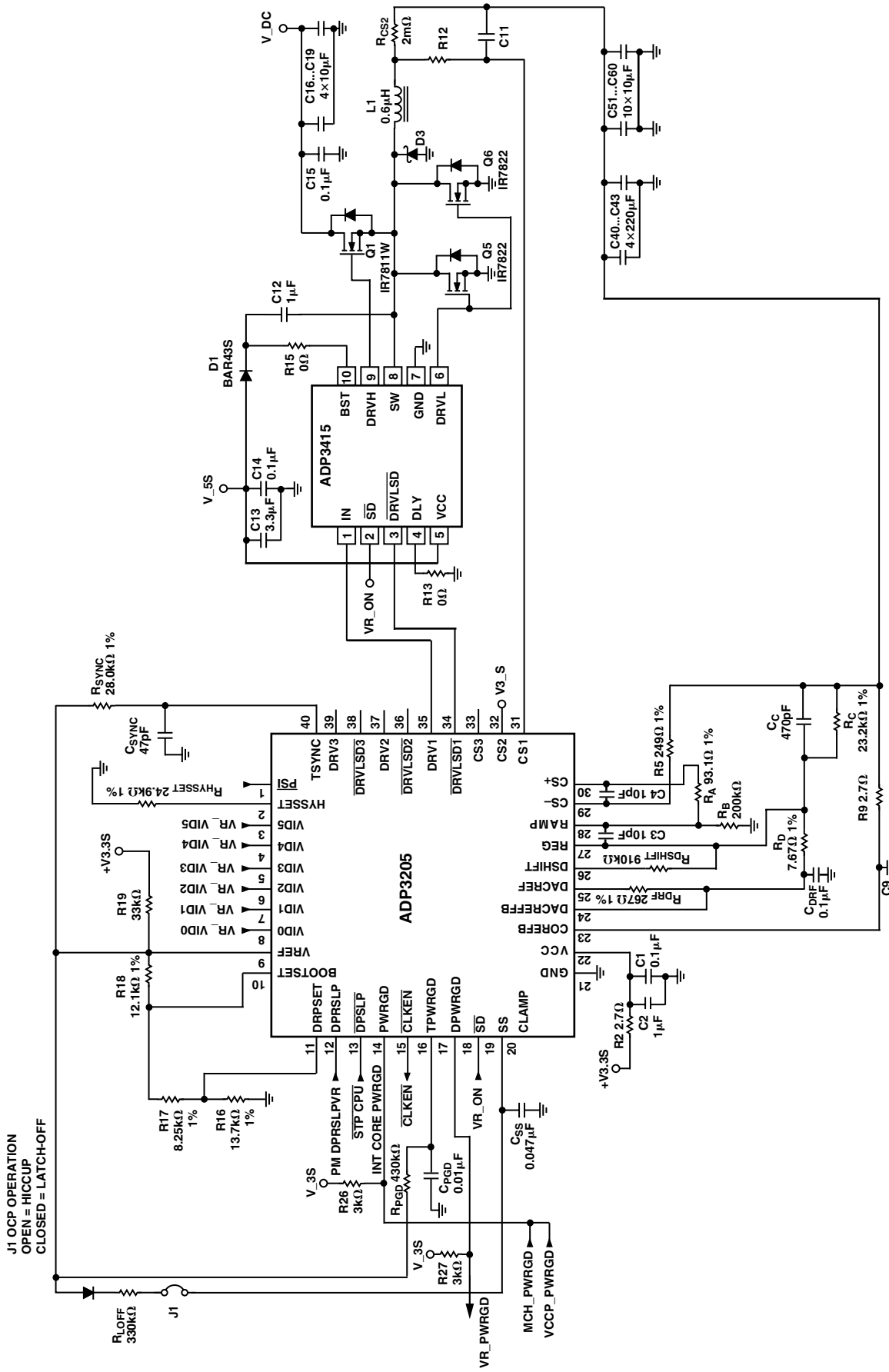


Figure 11. Typical Application for 1-Phase 12 A Load

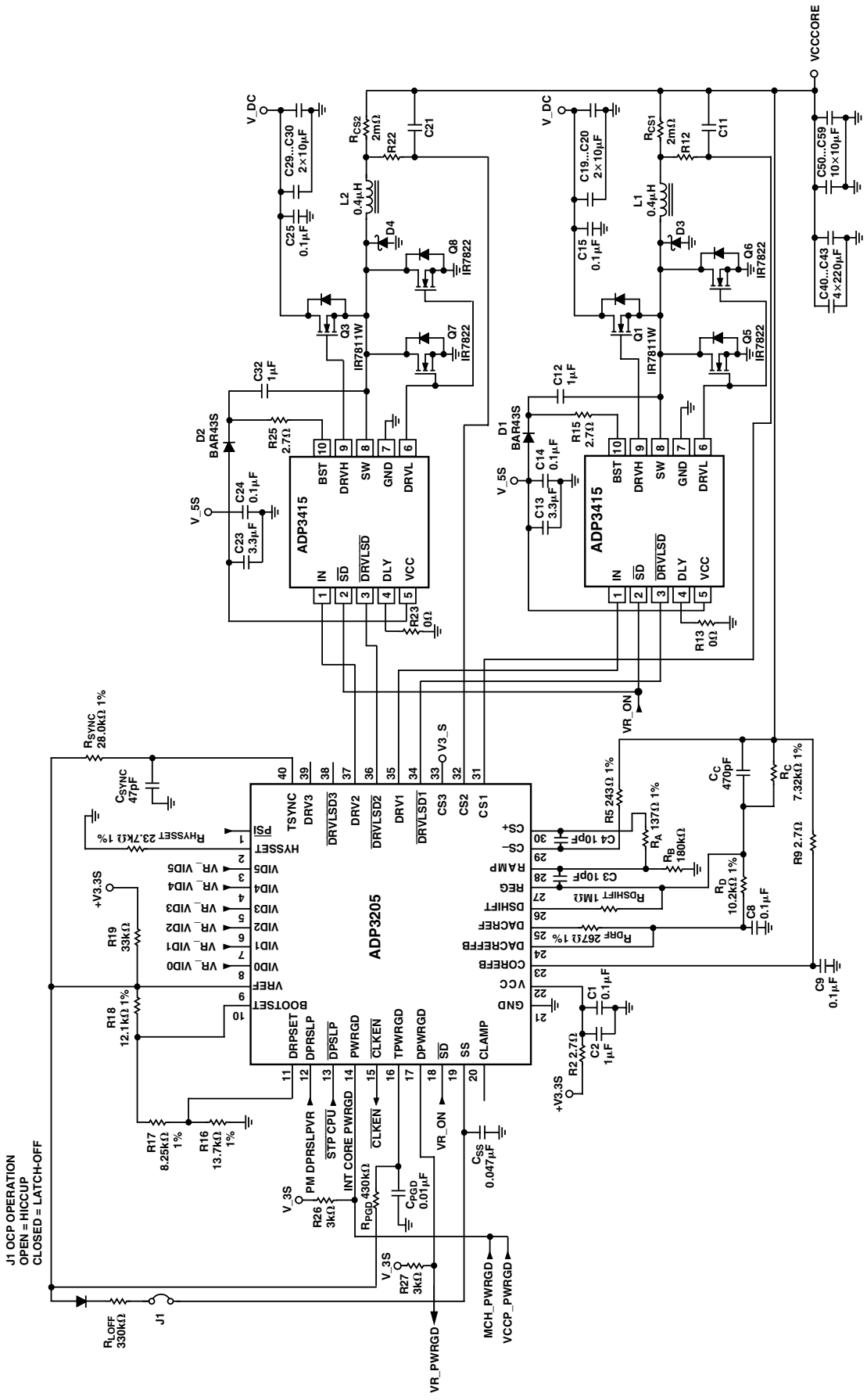


Figure 12. Typical Application for 2-Phase 25 A Load

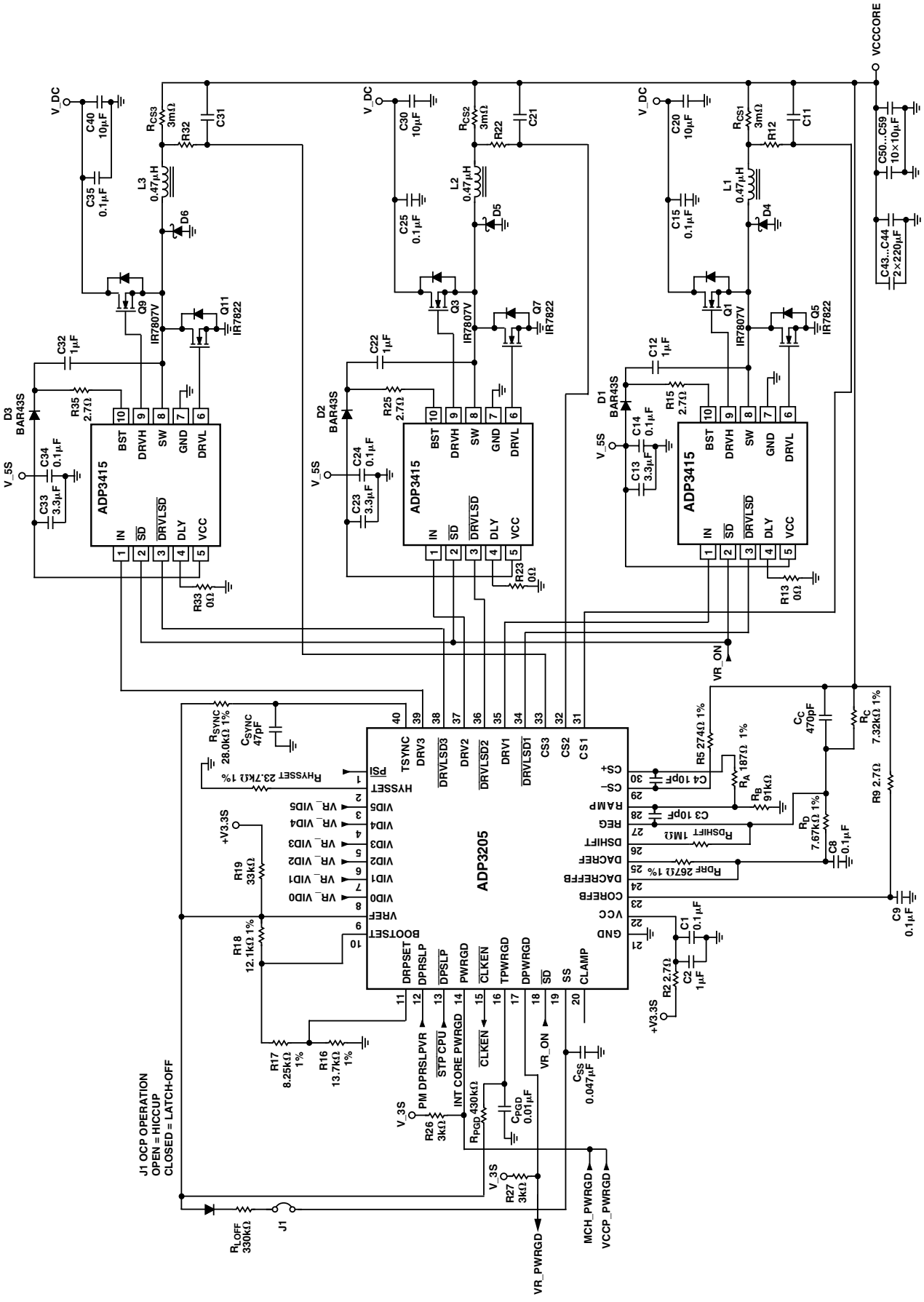
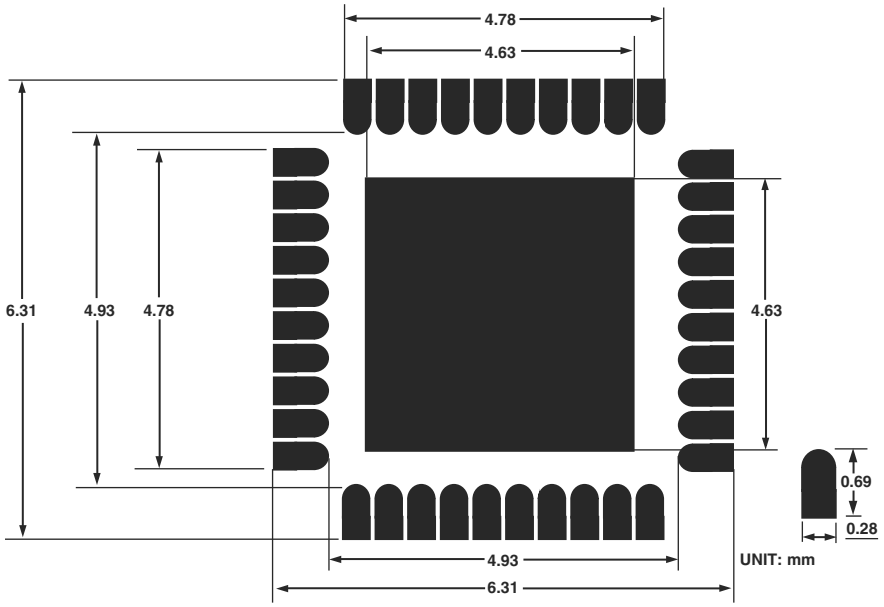


Figure 13. Typical Application for 3-Phase 25 A Load

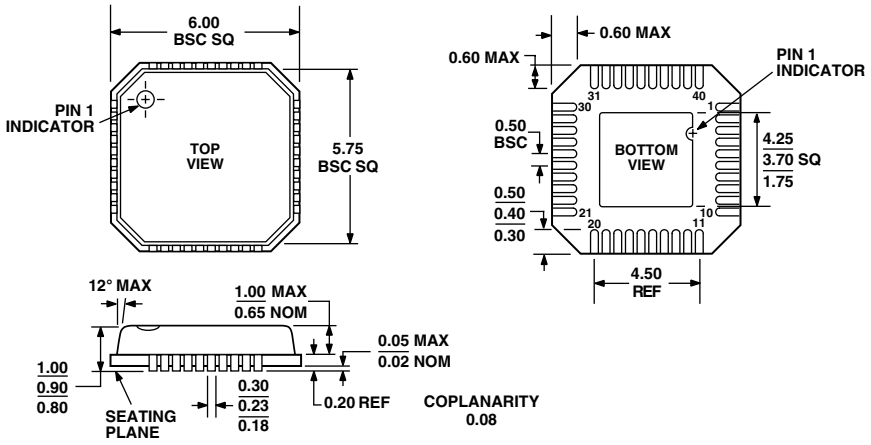


1. The central square-shaped pad is optional. If the pad is used, the exposed lead-frame paddle on the bottom of the package should be soldered to it to improve solder-joint reliability. The pad can be left floating or can be connected to V_{CC}, but should never be grounded. If the pad is omitted, any wiring and/or vias in the area underneath the package should be properly protected with electrically isolating coating to prevent shorts between the wires/vias caused by the package's metal paddle.
2. The size of the central square-shaped pad can match the package exposed paddle size of 4.25mm × 4.25mm, but it is recommended to be oversized to maximum 4.63mm × 4.63mm to improve placement alignment.

Figure 14. Recommended PCB Footprint

OUTLINE DIMENSIONS

40-Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body
(CP-40)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

Note: Soldering the exposed metal paddle on the bottom of the package to the square pattern shown on the recommended PCB footprint drawing (Figure 14) improves thermal resistance and solder-joint reliability.