Dual Channel 14-/16-Bit 250Msps Analog-to-Digital Converters

Check for Samples: ADS42JB49, ADS42JB69

FEATURES

- **Dual Channel**
- **14/16-Bit Resolution**
- **Maximum Clock Rate: 250 Msps**
- **JESD204B Serial Interface**
  - **Subclass 0,1, 2 Compliant up to 3.125Gbps**
  - **2 to 4 Lanes Supporting up to 250Msps**
- **Analog Input Buffer with High Impedance Input**
- **Flexible Input Clock Buffer with divide by 1,2,4**
- **2Vpp and 2.5Vpp Differential Full-Scale Input (SPI programmable)**
- **64-Pin QFN Package (9x9mm)**
- **Power Dissipation: 775mW/ch**
- **Aperture Jitter: 85fs rms**
- **Channel Isolation: 100dB**
- **Performance at f_{in} = 170 MHz at 2Vpp,-1dBFS**
  - **SNR: 73.3 dBFS**
  - **SFDR: 89 dBc HD2,3**
    100 dBc non HD2,3
- **Performance at f_{in} = 170 MHz at 2.5Vpp,-1dBFS**
  - **SNR: 74.9 dBFS**
  - **SFDR: 86 dBc HD2,3**
    97 dBc non HD2,3

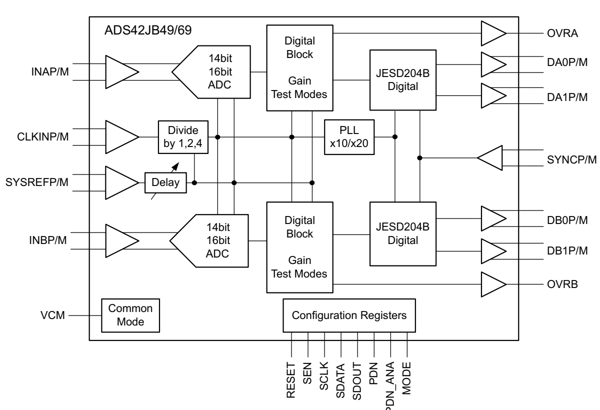
Interface Option	14-Bit	16-Bit
DDR/QDR LVDS	ADS42LB49	ADS42LB69
JESD204B	ADS42JB49	ADS42JB69

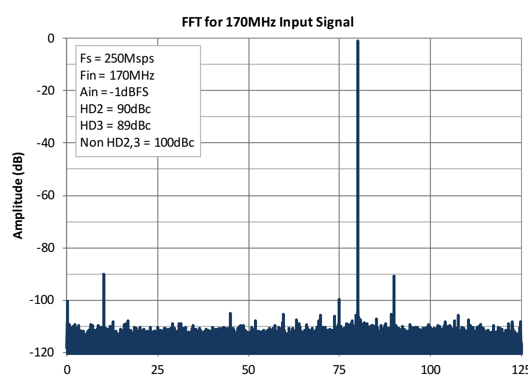
APPLICATIONS

- **Multicarrier, Multimode Cellular Receivers**
- **Radar and Smart Antenna Arrays**
- **Broadband Wireless**
- **Communications Test Equipment**
- **Microwave Receivers**
- **Software Defined Radios**

DESCRIPTION

The ADS42JB49/69 are a family of high linearity dual channel 14 and 16-bit, 250 MSPS analog-to-digital converters (ADC). The ADS42xB49/69 family supports the JESD204B serial interface with data rates up to 3.125Gbps as well as DDR and QDR LVDS interfaces. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A sampling clock divider allows more flexibility for system clock architecture design. The ADS42JB49/69 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with low power consumption.



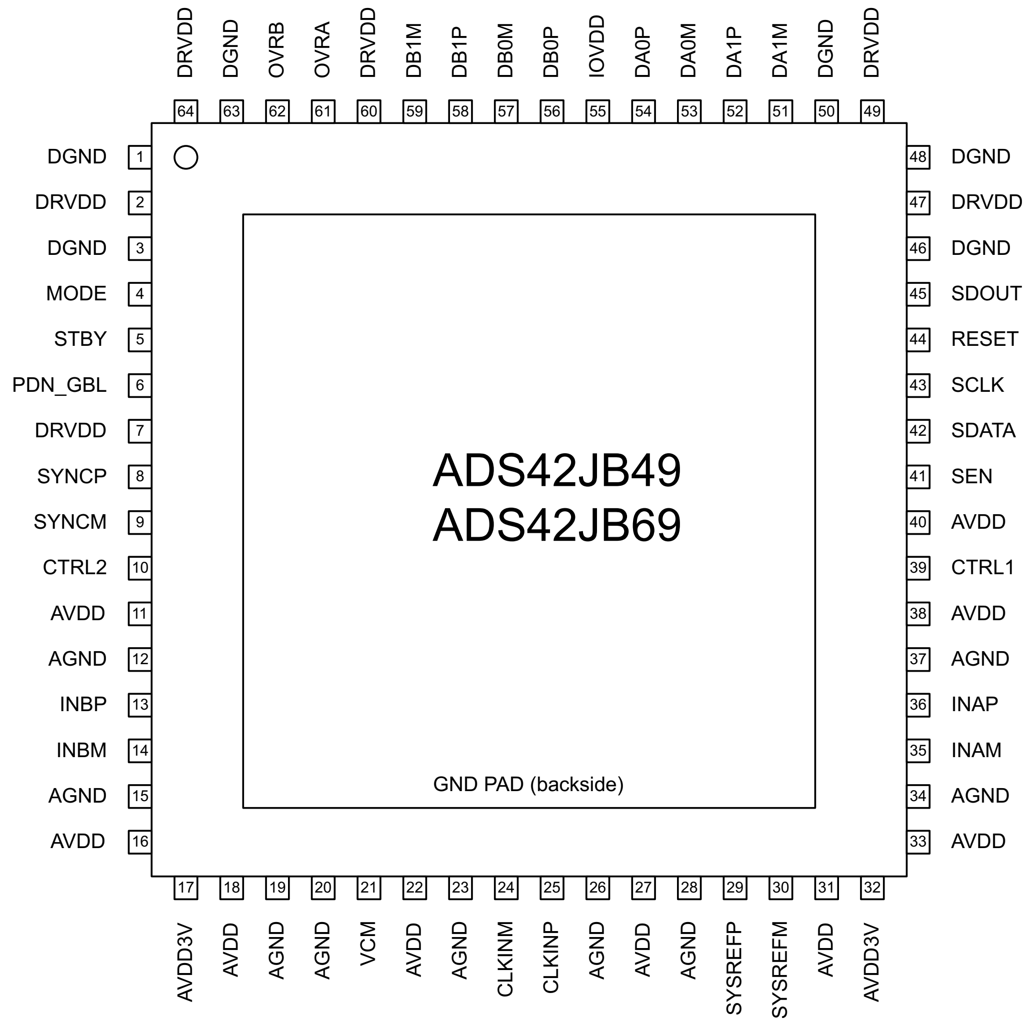


PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PINOUT INFORMATION



PIN ASSIGNMENTS – JESD204B OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT/REFERENCE			
INAP/M	36, 35	I	Differential analog input for channel A
INBP/M	13, 14	I	Differential analog input for channel B
VCM	21	O	Common mode voltage for analog inputs, 1.9V
CLOCK/SYNC			
CLKINP/M	25, 24	I	Differential clock input for ADC
SYSREFP/M	29, 30	I	External sync input
CONTROL/SERIAL			
RESET	44	I	Hardware reset. Active high. This pin has an internal 150kΩ pull-down resistor.
SCLK	43	I	Serial interface clock input
SDATA	42	I	Serial interface data input.

PIN ASSIGNMENTS – JESD204B OUTPUT INTERFACE (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SEN	41	I	Serial interface enable
SDOUT	45	O	Serial interface data output
PDN_GBL	6	I	Global power down. Active high with internal pulldown resistor
STBY	5	I	Standby. Active high with internal pulldown resistor
MODE	4	I	Connect to GND
CTRL1	39	I	Power down control
CTRL2	10	I	Power down control
DATA INTERFACE			
DA[0,1]P/M	54, 53, 52, 51	O	JESD204B Serial data output for channel A
DB[0,1]P/M	56, 57, 58, 59	O	JESD204B Serial data output for channel B
SYNCP/M	8, 9	I	Synchronization input for JESD204B port
OVRA	61	O	Overrange indication channel A
OVRB	62	O	Overrange indication channel B
POWER SUPPLY			
AVDD3V	17, 32	I	Analog 3.3V for analog buffer
AVDD	11, 16, 18, 22, 27, 31, 33, 38, 40	I	Analog 1.8V power supply
DRVDD	2, 7, 47, 49, 60, 64	I	Digital 1.8V power supply
IOVDD	55	I	Digital 1.8V power supply for the JESD204B transmitter
AGND	12, 15, 19, 20, 23, 26, 28, 34, 37	I	Analog ground
DGND	1, 3, 46, 48, 50, 63	I	Digital ground

PRODUCT PREVIEW

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/ BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS42JB49	QFN-64	RGC	–40C to 85C	GREEN (RoHS & no Sb/Br)	NiPdAu	ADS42JB49	ADS42JB49IRGC	Tape and Reel
ADS42JB69						ADS42JB69	ADS42JB69IRGC	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE MIN	VALUE MAX	UNIT
Supply voltage range, AVDD3V		–0.3	3.6	V
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, DRVDD		–0.3	2.1	V
Supply voltage range, IOVDD		–0.3	2.1	V
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INA/BP, INA/BM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3V	V
	SYNCP, SYNCM	–0.3	AVDD + 0.3V	V
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3V	V
	SCLK, SEN, SDATA, RESET, PDN, PDN_ANA, MODE	–0.3	3.9	V
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J			125	°C
Storage temperature range		–65	150	°C
ESD, Human Body Model			2	kV

THERMAL INFORMATION

THERMAL METRIC(1)		ADS42JB69 QFN (64-PIN)	UNITS
T_J	Maximum junction temperature	125	°C
θ_{JA}	Junction-to-ambient thermal resistance(2)	23.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	8.8	
θ_{JB}	Junction-to-board thermal resistance(4)	3.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	3.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	??	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS – ADS42JB69

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
ADC Clock Frequency					250	MSPS
Resolution			16			Bits
SUPPLY						
AVDD3V			3.15	3.3	3.45	V
AVDD, DRVDD			1.7	1.8	1.9	V
POWER SUPPLY						
I_{AVDD3V}	3.3V Analog supply current	V_{IN} = Fullscale, f_{IN} = 100 MHz		267		mA
I_{AVDD}	1.8V Analog supply current			143		mA
I_{DRVDD}	1.8V Digital supply current			193		mA
I_{IOVDD}	I/O Voltage supply current			35		mA
P_{dis}	Total power dissipation			1.55		W
Global power down dissipation				30		mW
Wake up time from global power down				TBD		µs
Standby power down dissipation				450		mW
Wake up time from standby power down				TBD		µs

ELECTRICAL CHARACTERISTICS – ADS42JB49

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
ADC Clock Frequency					250	MSPS
Resolution			14			Bits
SUPPLY						
AVDD3V			3.15	3.3	3.45	V
AVDD, DRVDD			1.7	1.8	1.9	V
POWER SUPPLY						
I_{AVDD3V}	3.3V Analog supply current	V_{IN} = Fullscale, f_{IN} = 100 MHz		267		mA
I_{AVDD}	1.8V Analog supply current			143		mA
I_{DRVDD}	1.8V Digital supply current			193		mA
I_{IOVDD}	I/O Voltage supply current			35		mA
P_{dis}	Total power dissipation			1.55		W
Global power down dissipation				30		mW
Wake up time from global power down				TBD		µs
Standby power down dissipation				450		mW
Wake up time from standby power down				TBD		µs

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ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ANALOG INPUTS					
Differential input full-scale			2.0		Vpp
Input common mode voltage			1.85 ± tbd		V
Input resistance	Differential at DC		TBD		Ω
Input capacitance	Each input to GND		TBD		pF
VCM common mode voltage output			1.85		V
Analog input bandwidth (3dB)			650		MHz
CLOCK INPUT					
Input clock frequency				1000	MHz
Input clock amplitude			1.5		Vpp
Input clock duty cycle			50%		
Internal clock biasing			1.4		V

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ELECTRICAL CHARACTERISTICS – ADS42JB69 (16-BIT)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Analog Input Full Scale				2.0			2.5		Vpp
DYNAMIC AC CHARACTERISTICS									
SNR	Signal to Noise Ratio	f_{IN} = 10 MHz		74.1			75.8		dBFS
		f_{IN} = 70 MHz		73.9			75.6		
		f_{IN} = 100 MHz		73.7			75.5		
		f_{IN} = 170 MHz	70.8	73.3			74.9		
		f_{IN} = 210 MHz		73.0			74.5		
SFDR	Spur Free Dynamic Range (including second and third harmonic distortion)	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	81	89			86		
		f_{IN} = 210 MHz		89			85		
HD2	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	81	90			90		
		f_{IN} = 210 MHz		89			85		
HD3	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	81	89			86		
		f_{IN} = 210 MHz		89			86		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion)	f_{IN} = 10 MHz		100			100		dBc
		f_{IN} = 70 MHz		100			100		
		f_{IN} = 100 MHz		100			100		
		f_{IN} = 170 MHz	87	100			97		
		f_{IN} = 210 MHz		100			96		
IMD3		F_{in} = 99 and 101 MHz		TBD			TBD		dBFS
	Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		100			100		dB

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ELECTRICAL CHARACTERISTICS – ADS42JB49 (14-BIT)

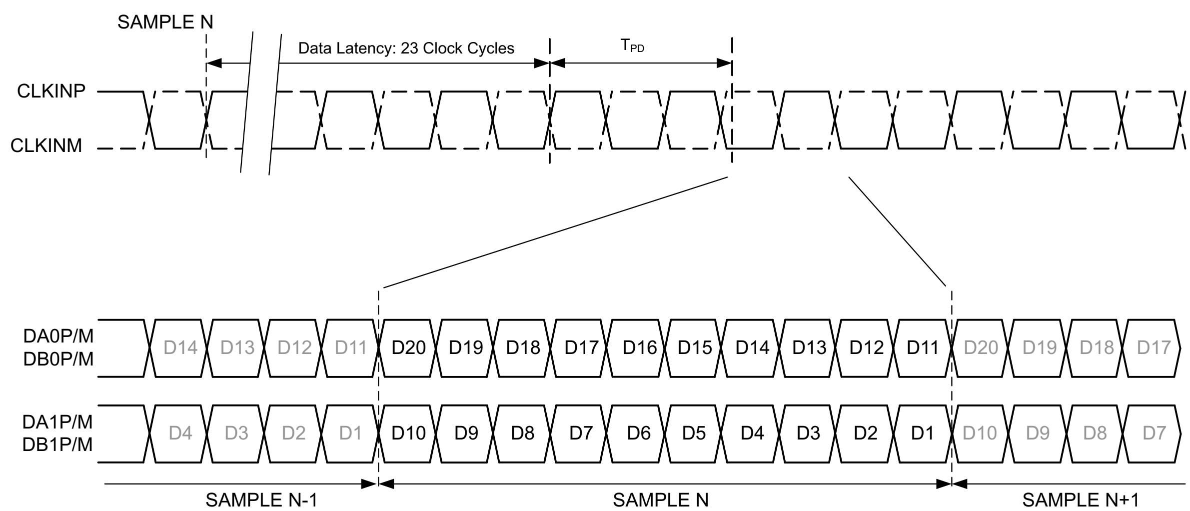
Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Analog Input Full Scale				2.0			2.5		Vpp
DYNAMIC AC CHARACTERISTICS									
SNR	Signal to Noise Ratio	f_{IN} = 10 MHz		72.6			74.3		dBFS
		f_{IN} = 70 MHz		72.4			74.1		
		f_{IN} = 100 MHz		72.2			74.0		
		f_{IN} = 170 MHz	69.5	71.9			73.4		
		f_{IN} = 210 MHz		71.5			73.0		
SFDR	Spur Free Dynamic Range (including second and third harmonic distortion)	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	79	89			86		
		f_{IN} = 210 MHz		89			85		
HD2	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	79	90			90		
		f_{IN} = 210 MHz		89			85		
HD3	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	79	89			86		
		f_{IN} = 210 MHz		89			86		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion)	f_{IN} = 10 MHz		100			100		dBc
		f_{IN} = 70 MHz		100			100		
		f_{IN} = 100 MHz		100			100		
		f_{IN} = 170 MHz	87	100			97		
		f_{IN} = 210 MHz		100			96		
IMD3		F_{in} = 99 and 101 MHz		TBD			TBD		dBFS
	Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		100			100		dB

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
SAMPLE TIMING CHARACTERISTICS						
rms	Aperture Jitter	Sample uncertainty		85		fs rms
	Data Latency	ADC sample to digital output (incl JESD204B interface)		23		Clock Cycles
		ADC sample to digital output (incl. JESD204B interface) – digital gain enabled		27		
	Fast Over-range (OVR) Latency	ADC sample to fast OVR output		9		Clock Cycles
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over		TBD		ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		TBD		ns



ELECTRICAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
DIGITAL INPUTS – RESET, SCLK, SEN, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE						
	High-level input voltage	All digital inputs support 1.8V and 3.3V logic levels.	1.2			V
	Low-level input voltage				0.4	V
	High-level input current			50		µA
	Low-level input current			–50		µA
	Input capacitance			4		pF
DIGITAL OUTPUTS – SDOUT, OVRA, OVRB						
	High-level output voltage		DRVDD-0.1	DRVDD		V
	Low-level output voltage				0.1	V
DIGITAL INPUTS – SYNCP/M, SYSREFP/M						
	High-level input voltage			1.3		V
	Low-level input voltage			0.5		V
V_{CM}	Input common mode voltage			0.9		V
t_{S_SYNC}		Referenced to rising edge of input clock	400		400 + T_{CLKIN}/2	ps
t_{H_SYNC}		Referenced to rising edge of input clock	100			ps
t_{S_SYSREF}		Referenced to rising edge of input clock	400		400 + T_{CLKIN}/2	ps
t_{H_SYSREF}		Referenced to rising edge of input clock	100			ps
DIGITAL OUTPUTS – JESD204B Interface: DA[0,1], DB[0,1]		**50Ω single ended external termination to IOVDD**				
	High-level output voltage			IOVDD		V
	Low-level output voltage			IOVDD-0.4		V
$\lvert V_{OD} \rvert$	Output differential voltage			0.4		V
V_{OCM}	Output common mode voltage			IOVDD-0.2		V
	Transmitter short circuit current	Transmitter terminals shorted to any voltage between –0.25V and 1.45V	–90		50	mA
	Single ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF
UI	Unit interval	2.5Gbps		400		ps
	Rise/fall times	5pF single-ended load capacitance to ground		106		ps
	Serial output data rate			2.5	3.125	Gbps

PRODUCT PREVIEW

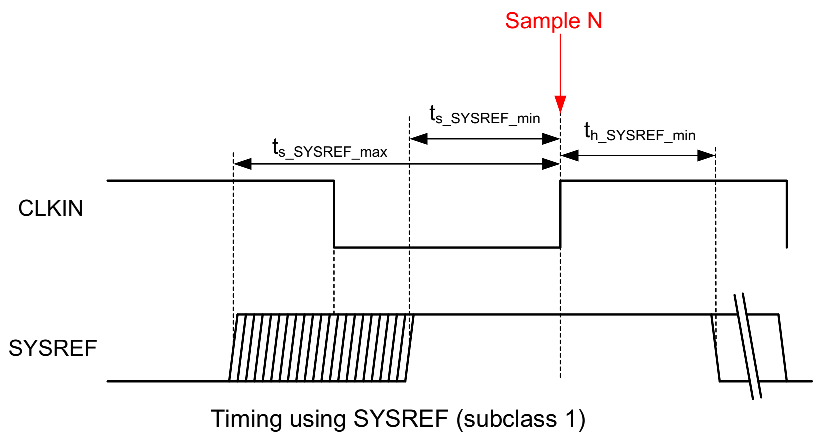


Figure 1. Timing using SYSREF (subclass 1)

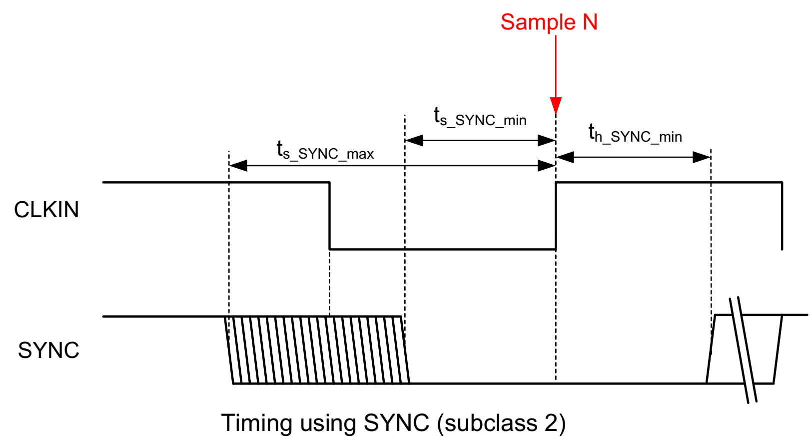


Figure 2. Timing using SYNC (subclass 2)

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS – ADS42JB69

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, -1dBFS differential input, 65k-point FFT, unless otherwise noted.

FFT FOR 10 MHz INPUT SIGNAL (FS = 2.0 Vpp)

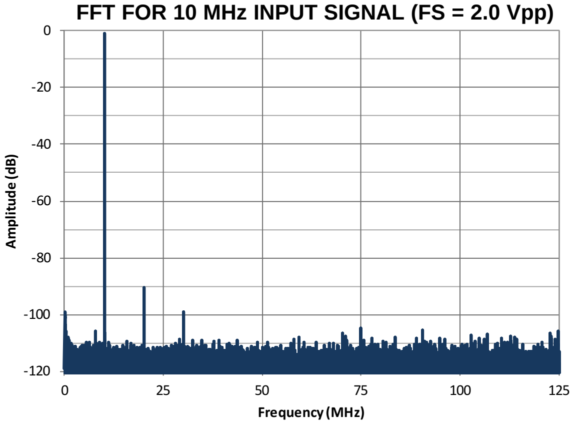


Figure 3.

FFT FOR 100 MHz INPUT SIGNAL (FS = 2.0 Vpp)

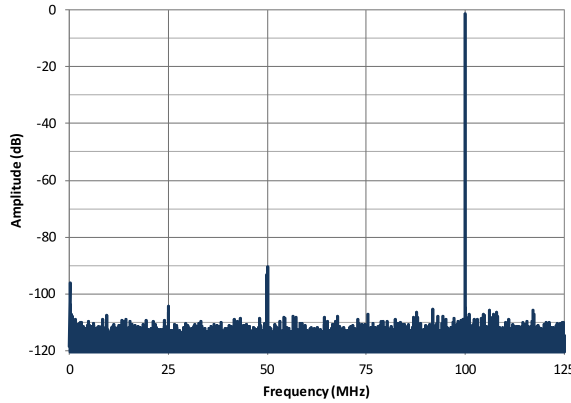


Figure 4.

FFT FOR 170 MHz INPUT SIGNAL (FS = 2.0 Vpp)

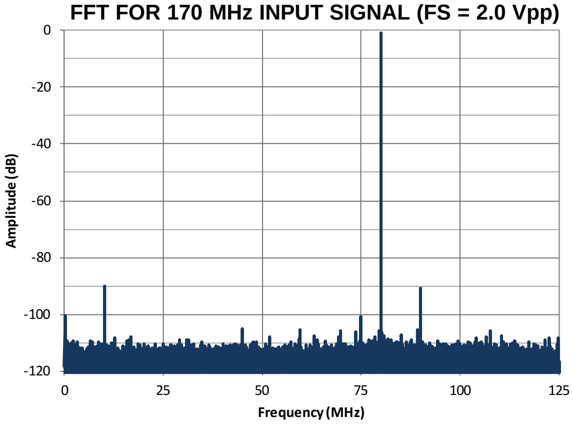


Figure 5.

POWER CONSUMPTION vs SAMPLING RATE

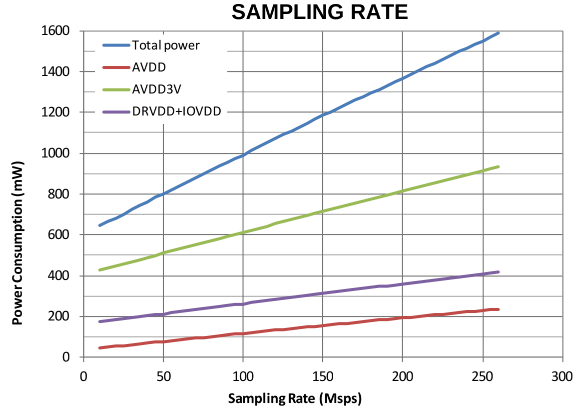


Figure 6.

SNR (dBFS) vs INPUT FREQUENCY

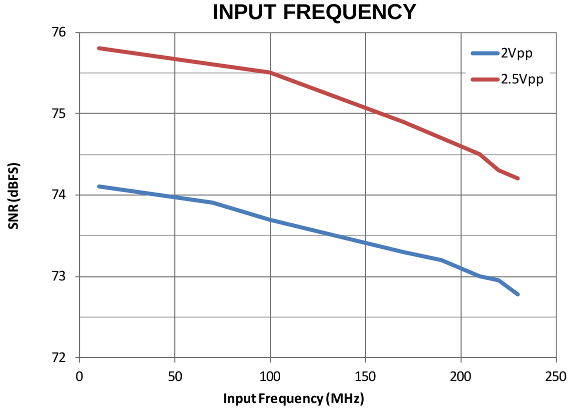


Figure 7.

SFDR (dBc) vs INPUT FREQUENCY

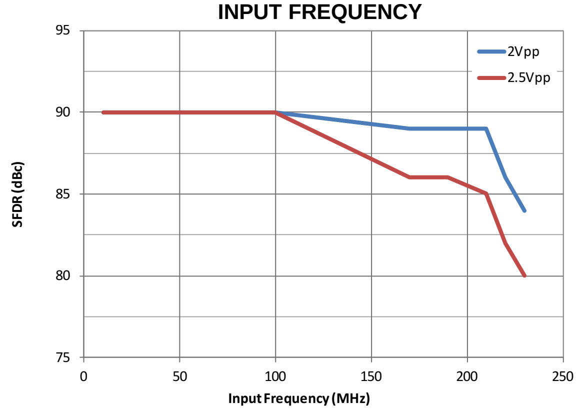


Figure 8.

TYPICAL CHARACTERISTICS – ADS42JB69 (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, -1dBFS differential input, 65k-point FFT, unless otherwise noted.

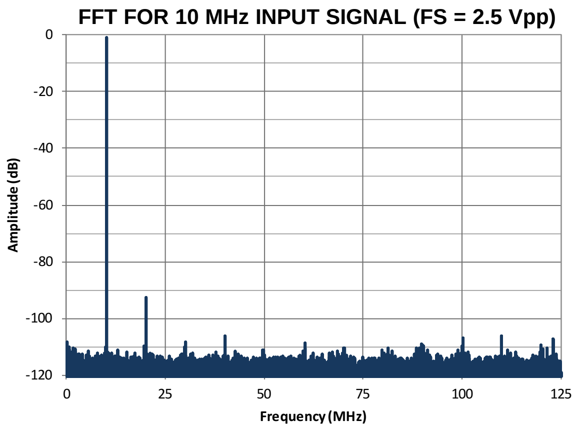


Figure 9.

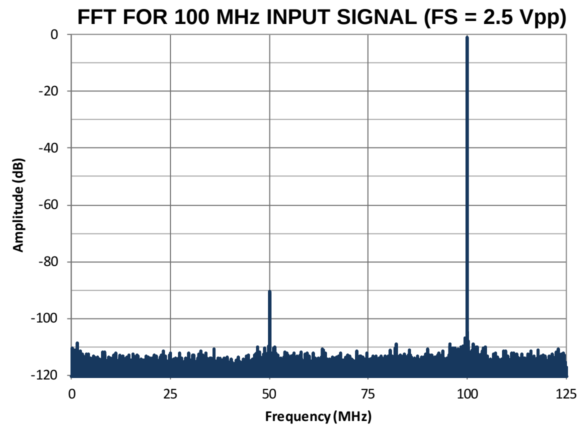


Figure 10.

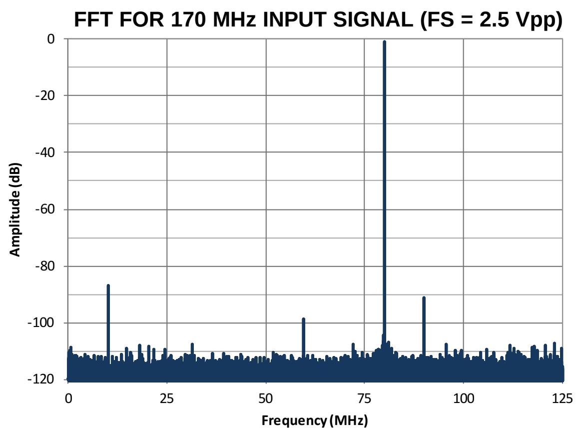


Figure 11.

PRODUCT PREVIEW

DEVICE CONFIGURATION

The ADS42JB49/ADS42JB69 can be configured using a serial programming interface, as described below. In addition, the device has three dedicated parallel pins (STBY, CTRL1 and CTRL2) for controlling the power down modes.

DETAILS OF SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and SDOUT (serial interface data output) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns, as shown in Figure 12; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 08h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

Serial Register Write

The internal register of the ADS42JB49/ADS42JB69 can be programmed following these steps:

1. Drive SEN pin low
2. Set the R/W bit to ‘0’ (bit A7 of the 8 bit address)
3. Set bit A6 in the address field to ‘0’
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content has to be written
5. Write 8 bit data which is latched in on the rising edge of SCLK.

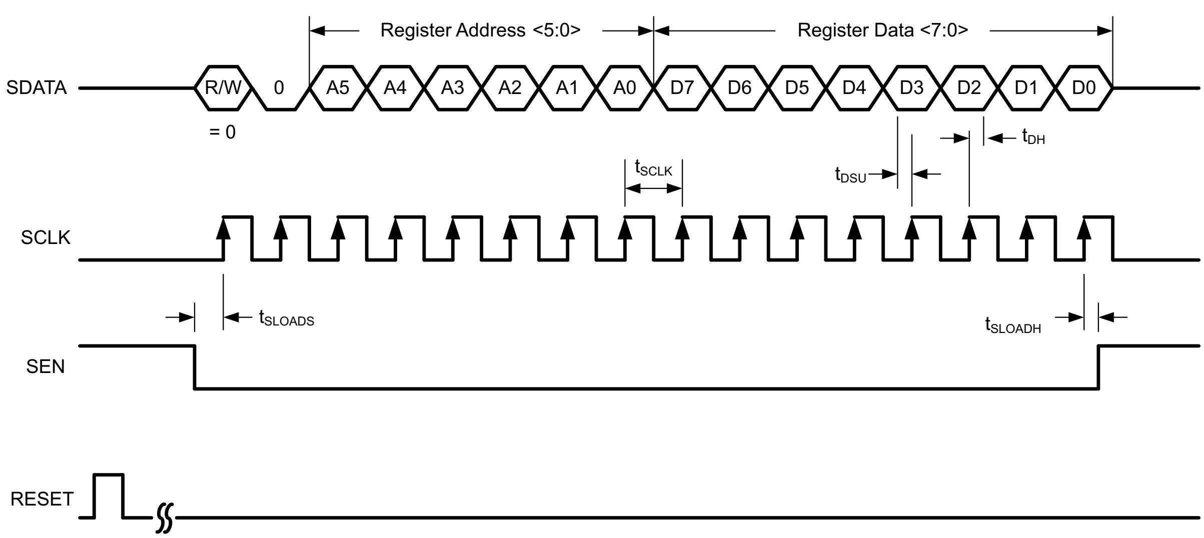


Figure 12. Serial Register Write Timing Diagram

Table 1. Reset Timing (only when Serial Interface is Used)(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/t_{SCLK})	>DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: TMIN = –40°C to TMAX = +85°C, AVDD3V = 3.3V, AVDD, DRVDD = 1.9V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 15).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.

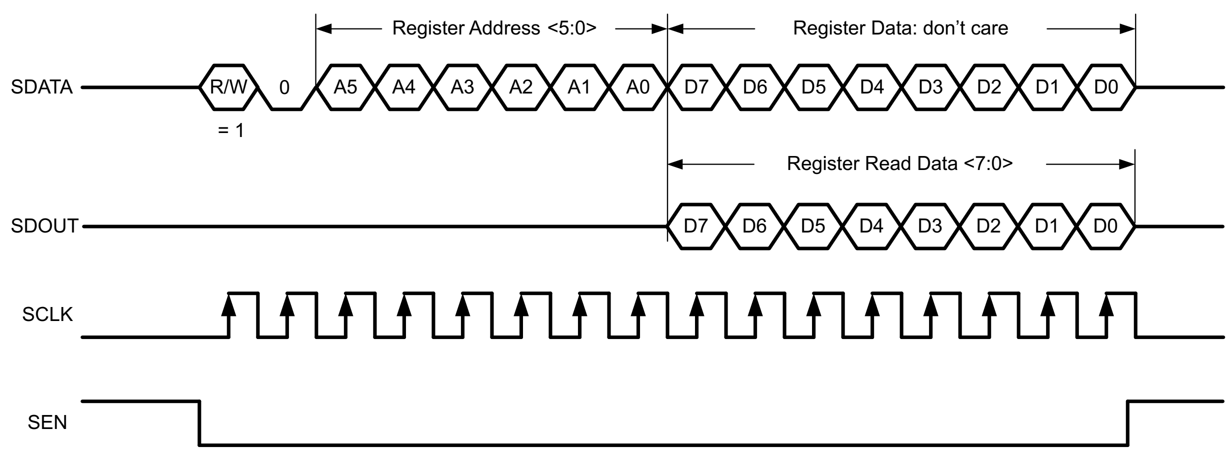


Figure 13. Serial Register Readout Timing Diagram

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SUMMARY OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
6	0	0	0	0	0	0	CLK DIV	
7	0	0	0	0	0	SYSREF DELAY		
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	1	0	0	RESET
B	CHA GAIN					CHA GAIN EN	0	0
C	CHBGAIN					CHB GAIN EN	0	0
D	0	0	0	0	0	0	0	FAST OVR EN
F	CHA TEST PATTERNS				CHB TEST PATTERNS			
10	CUSTOM PATTERN (15:8)							
11	CUSTOM PATTERN (15:8)							
12	CUSTOM PATTERN (15:8)							
13	CUSTOM PATTERN (15:8)							
1F	FAST OVR THRESHOLD							
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LAN ALIGN	FRAME ALIGN	TX LINK CONFIG DATA0
27	0	0	0	0	0	0	CTRLK	CTRLF
2B	SCRAMBLE EN	0	0	0	0	0	0	0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME
2D	0	0	0	FRAMES PER MULTIFRAME				
30	SUBCLASS			0	0	0	0	0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		

DESCRIPTION OF SERIAL INTERFACE REGISTERS

Register Address	Register Data							
A7-A0 IN HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
6	0	0	0	0	0	0	CLK DIV	

Default: 00h

D1-D0 **CLK DIV** Internal clock divider for input sample clock

00 /1 (clock divider bypassed)

01 /2

10 /1

11 /4

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
7	0	0	0	0	0	0	SYSREF DELAY	

Default: 00h

D2-D0 **SYSREF DELAY** Controls the delay of the SYNC input with respect to input clock in 60ps steps

000	0 ps delay	100	240 ps delay
001	60 ps delay	101	300 ps delay
010	120 ps delay	110	360 ps delay
011	180 ps delay	111	420 ps delay

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	1	0	0	RESET

Default: 00h

D7 **PDN CHA** Power down channel A

0 normal operation

1 power down

D6 **PDN CHB** Power down channel B

0 normal operation

1 power down

D6 **STBY** Dual ADC is placed into standby mode

0 normal operation

1 power down

D5 **STBY** Digital output data format

0 2s complement

1 offset binary

D3 **Must be set to 1**

D0 **RESET** Software reset applied

This bit resets all internal registers to the default values and self-clears to ‘0’

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Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
B	CHA GAIN					CHA GAIN EN	0	0

Default: 00h

D7-D3 **CHA GAIN** Digital Gain for channel A (must set CHA GAIN EN bit first (D2))

Register Value	Digital Gain	Max Input Voltage		Register Value	Digital Gain	Max Input Voltage (Vpp)
00000	0 dB	**2.0 Vpp**		01010	1.5 dB	1.7 Vpp
00001	–2.7 dB	2.7 Vpp		01011	2 dB	1.6 Vpp
00010	–2.3 dB	2.6 Vpp		01100	2.5 dB	1.5 Vpp
00011	–2.0 dB	**2.5 Vpp**		01101	3 dB	1.4 Vpp
00100	–1.5 dB	2.4 Vpp		01110	3.5 dB	1.3 Vpp
00101	–1.0 dB	2.2 Vpp		01111	4 dB	1.25 Vpp
00110	–0.5 dB	2.1 Vpp		10000	4.5 dB	1.2 Vpp
00111	0 dB	**2.0 Vpp**		10001	5 dB	1.1 Vpp
01000	0.5 dB	1.9 Vpp		10010	5.5 dB	1.05 Vpp
01001	1 dB	1.8 Vpp		10011	6 dB	1.0 Vpp

D2 **CHA GAIN EN** Digital Gain enable bit for channel A

0 Digital gain disabled

1 Digital gain disabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
C	CHB GAIN					CHB GAIN EN	0	0

Default: 00h

D7-D3 **CHB GAIN** Digital Gain for channel B (must set CHA GAIN EN bit first (D2))

Register Value	Digital Gain	Max Input Voltage		Register Value	Digital Gain	Max Input Voltage (Vpp)
00000	0 dB	**2.0 Vpp**		01010	1.5 dB	1.7 Vpp
00001	–2.7 dB	2.7 Vpp		01011	2 dB	1.6 Vpp
00010	–2.3 dB	2.6 Vpp		01100	2.5 dB	1.5 Vpp
00011	–2.0 dB	**2.5 Vpp**		01101	3 dB	1.4 Vpp
00100	–1.5 dB	2.4 Vpp		01110	3.5 dB	1.3 Vpp
00101	–1.0 dB	2.2 Vpp		01111	4 dB	1.25 Vpp
00110	–0.5 dB	2.1 Vpp		10000	4.5 dB	1.2 Vpp
00111	0 dB	**2.0 Vpp**		10001	5 dB	1.1 Vpp
01000	0.5 dB	1.9 Vpp		10010	5.5 dB	1.05 Vpp
01001	1 dB	1.8 Vpp		10011	6 dB	1.0 Vpp

D2 **CHB GAIN EN** Digital Gain enable bit for channel B

0 Digital gain disabled

1 Digital gain disabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
D	0	0	0	0	0	0	0	FAST OVR EN

D0 **FAST OVR EN** Selects if normal OVR or fast OVR signal gets presented on OVR pins

0 normal OVR on OVR pins

1 fast OVR on OVR pins

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
F	CHA TEST PATTERNS				CHB TEST PATTERNS			

Default: 00h

D7-D4	**CHA TEST PATTERNS**	ChA test pattern programmability
0000	Normal Operation	
0001	Outputs all 0s	
0010	Outputs all 1s	
0011	Outputs toggle pattern:	Output data are an alternating sequence of *1010101010101010* and *0101010101010101*
0100	Output digital ramp:	output data increments by one LSB every clock cycle from code 0 to 65535
0101	Increment pattern:	pattern gets incremented by step size set in custom pattern 1 (0x10 and 0x11, 16bit)
0110	Single pattern:	output data is custom pattern 1 (0x10 and 0x11)
0111	Double pattern:	output data alternates between custom patter 1 and custom pattern 2
1000	Deskew pattern:	output data is 0xAAAA
1001	SYNC pattern:	output data is 0xFFFF
1010	PRBS pattern:	output data is PRBS
1011	8P sine:	output data is a 8 point sine wave
D3-D0	**CHB TEST PATTERNS**	ChB test pattern programmablility
0000	Normal Operation	
0001	Outputs all 0s	
0010	Outputs all 1s	
0011	Outputs toggle pattern:	Output data are an alternating sequence of *1010101010101010* and *0101010101010101*
0100	Output digital ramp:	output data increments by one LSB every clock cycle from code 0 to 65535
0101	Increment pattern:	pattern gets incremented by step size set in custom pattern 1 (0x10 and 0x11, 16bit)
0110	Single pattern:	output data is custom pattern 1 (0x10 and 0x11)
0111	Double pattern:	output data alternates between custom patter 1 and custom pattern 2
1000	Deskew pattern:	output data is 0xAAAA
1001	SYNC pattern:	output data is 0xFFFF
1010	PRBS pattern:	output data is PRBS
1011	8P sine:	output data is a 8 point sine wave

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
10	CUSTOM PATTERN 1 (15:8)							

Default: 00h

D7-D0 **CUSTOM PATTERN 1 (15:8)** Set the custom pattern 1 (15:8) using these bits for both channels

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Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
11	CUSTOM PATTERN 1 (7:0)							

Default: 00h

D7-D0 **CUSTOM PATTERN 1 (7:0)** Set the custom pattern 1 (7:0) using these bits for both channels

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
12	CUSTOM PATTERN 2 (15:8)							

Default: 00h

D7-D0 **CUSTOM PATTERN 2 (15:8)** Set the custom pattern 2 (15:8) using these bits for both channels

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
13	CUSTOM PATTERN 2 (7:0)							

Default: 00h

D7-D0 **CUSTOM PATTERN 2 (7:0)** Set the custom pattern 2 (7:0) using these bits for both channels

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
1F	FAST OVR THRESHOLD							

Default: FFh

D7-D0 **FAST OVR THRESHOLD**

The ADS42JB49/ADS42JB69 has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered 9 output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 255). After reset, when FAST OVR EN is set, the default value of the FAST OVR THRESHOLD bits is 255 (decimal).

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Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRANE ALIGN	TX LINK CONFIG DATA

Default: 00h

D7-D6 **SERDES TEST PATTERN** Sets test patterns in the transport layer of the JESD204B interface

00 normal operation

01 Outputs clock pattern: Output is 10101010 pattern

10 Encoded pattern: Output is 1111111100000000

11 PRBS sequence: Output is 2^{15} - 1

D5 **IDLE SYNC** Sets output pattern when SYNC is high

0 Sync code is k28.5 (0xBCBC)

1 Sync code is 0xBC50

D4 **TESTMODE EN** Generates long transport layer test pattern mode according to 5.1.63 clause of JESD204B specification

0 test mode disbled

1 test mode enabled

D3 **FLIP ADC DATA**

0 normal operation

1 output data order is reversed: MSB – LSB

D2 **LANE ALIGN** Inserts lane alignment character (K28.3) for the receiver to align to lane boundary per section 5.3.3.5 of the JESD204B specification.

0 normal operation

1 inserts lane alignment characteris

D1 **FRAME ALIGN** Inserts frame alignment character (K28.7) for the receiver to align to frame boundary per section 5.3.3.4 of the JESD204B specification.

0 normal operation

1 inserts frame alignment characters

D0 **TX LINK CONFIG DATA** Disables sending initial link alignment (ILA) sequence when SYNC is de-asserted 0 normal operation

0 normal operation

1 ILA disabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
27	0	0	0	0	0	0	CTRL K	CTRL F

Default: 00h

D1 **CTRL K** Enable bit for number of frames per multi frame

0 Default is 17 (10x mode) or 9 (20x mode) frames per multi frame

1 Frames per multi frame can be set in register 0x2D

D0 **CTRL F** Enable bit for number of octets per frame

0 Default is F = 1 10x mode using 2 lanes per ADC

1 Octets per frame can be specified in 0x2C

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Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
28	SCRAMBLE EN	0	0	0	0	0	0	0

Default: 00h

D7 **SCRAMBLE EN** Scramble enable bit in the JESD204B interface

0 Scrambling disabled

1 Scrambling enabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME

Default: 00h

D7-D0 **OCTETS PER FRAME** Sets number of octets per frame (F)

0 10x mode using 2 lanes per ADC

1 20x mode using 1 lane per ADC

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
2D	0	0	0	FRAMES PER MULTIFRAME				

Default: 00h

D4-D0 **FRAMES PER MULTIFRAME** Sets number of frames per multi frame

After reset, the default settings for frames per multi-frame are:

10x K = 16

20x K = 8

For each mode, K should not be set to a lower value.

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
30	SUBCLASS			0	0	0	0	0

Default: 40h

D7-D5 **SUBCLASS** Sets JESD204B subclass

000 Subclass 0 backward compatibility with JESD204A

001 Subclass 1 deterministic latency using SYSREF signal

010 Subclass 2 deterministic latency using SYNC detection

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Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			

Default: 00h

D7 **SYNC REQ** Generates synchronization request

0 normal operation

1 generate sync request

D6 **LMFC RESET MASK** Mask LMFC reset coming to digital

0 normal operation

1 ignores LMFC reset

D3-D0 **OUTPUT CURRENT SEL** Changes JESD output buffer current.

0000	16 mA	1000	8 mA
0001	15 mA	1001	7 mA
0010	14 mA	1010	6 mA
0011	13 mA	1011	5 mA
0100	20 mA	1100	12 mA
0101	19 mA	1101	11 mA
0110	18 mA	1110	10 mA
0111	17 mA	1111	9 mA

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		

Default: 00h

D7-D5 **LINK LAYER TESTMODE** Generates pattern according to clause 5.3.3.8.2 of the JESD204B document

000 normal ADC data

001 D21.5 (high frequency jitter pattern)

010 K28.5 (mixed frequency jitter pattern)

011 Repeat initial lane alignment (generate K28.5 character and repeat lane alignment sequences continuously)

100 12 octet RPAT jitter pattern

D4 **LINK LAYER RPAT** Changes the running disparity in modified RPAT pattern test mode (only when link layer test mode = 100)

0 normal operation

1 changes disparity

D2-D0 **PULSE DET MODES** selects different detection modes for SYSREF (subclass 1) and SYNC (subclass2)

D2	D1	D0	Functionality
0	Don't care	0	Allow all pulses to reset input clock dividers
1	Don't care	0	Do not allow reset of analog clock dividers
Don't care	0 ≥ 1 transition	1	Allow one pulse immediately after the 0 ≥ 1 transition to reset the divider

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Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
38	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

Default: 00h

D7 **FORCE LMFC COUNT** Force LMFC ount

0 normal operation

1 enables using different starting value for LMFC counter

D6-D2 **LMFC COUNT INIT** SYSREF coming to the digital block will reset the LMFC count to 0 and K28.5 will stop coming when the LMFC count reaches 31. The initial value to which LMFC count resets to can be set using LMFC COUNT INIT. This way the Rx can get synchronized early since it will get the LANE ALIGNMENT SEQUENCE early. Register bit FORCE LMFC COUNT must be enabled.

D1-D0 **RELEASE ILANE SEQ** Delays the generation of lane alignment sequence by 0, 1, 2 or 3 multi frames after code group synchronization.

00 0

01 1

10 2

11 3

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FEATURES

ANALOG INPUTS

The ADS42JB49/69 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50Ω matching for RF applications

The buffer also helps to isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to 1.85V using 5kΩ resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5V) and (VCM – 0.5V), resulting in a 2Vpp (default) differential input swing. The input sampling circuit has a 3dB bandwidth that extends up to 650MHz. Figure 14 shows an equivalent circuit for the analog inputs.

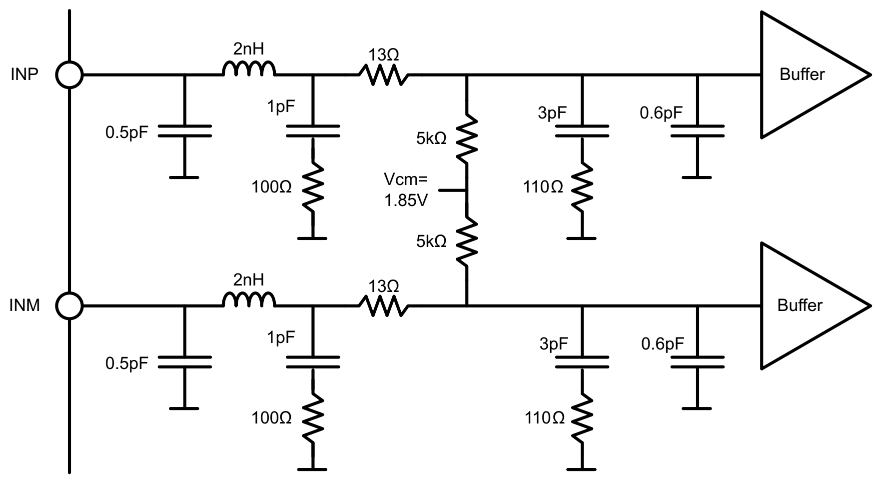

Figure 14. Analog Inputs

DIGITAL GAIN

The input full-scale amplitude can be selected between 1Vpp to 2.7Vpp (default is 2Vpp) by choosing the appropriate digital gain setting via SPI register write. This provides an option to trade off SNR for SFDR performance. A larger input full-scale increases SNR performance (2.5Vpp recommended for maximum SNR) while reduced input swing typically results in better SFDR performance.

DIGITAL GAIN	MAX INPUT VOLTAGE
-2 dB	2.5 Vpp
-1 dB	2.2 Vpp
0 dB (default)	2.0 Vpp
1 dB	1.8 Vpp
2 dB	1.6 Vpp
3 dB	1.4 Vpp
4 dB	1.25 Vpp
5 dB	1.1 Vpp
6 dB	1.0 Vpp

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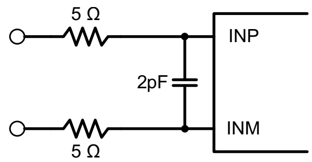
ANALOG INPUT DRIVING CIRCUIT

For maximum SFDR performance it is recommended to place a 5Ω resistor in series with the inputs and a 2pF shunt capacitor at the analog inputs. This circuit helps absorb some of the residual sampling glitches and improves HD2 and HD3 performance over a very wide input frequency range.



OVER-RANGE INDICATION

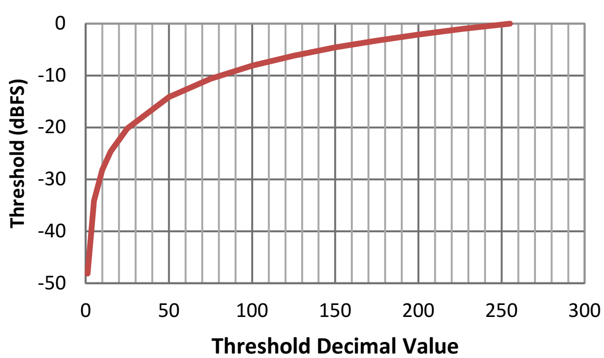
The ADS42JB49/69 provides two different overrange indications. The normal OVR (default) is triggered if the final 16 bit data output exceeds the maximum code value. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 9 clock cycles enabling a quicker reaction to an overrange event.

By default the normal overrange indication is output on the OVRA and OVRB pins. Using the SPI register map, the fast OVR indication can be presented on the overrange pins instead.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered 9 output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] / 255). After reset, when FAST OVR EN is set, the default value of the FAST OVR THRESHOLD bits is 255 (decimal).

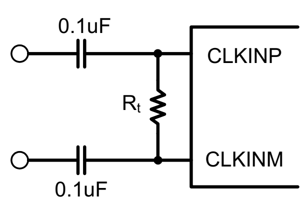
The full-scale is including digital gain – for example with +1dB digital gain the full-scale value is reduced from 2Vpp to 1.8Vpp.

In terms of full scale input, the fast OVR threshold can be calculated as: 20*log(<FOVR Threshold>/255).



CLOCK INPUTS

The ADS42JB49/69 clock input can be driven differentially with a sine wave, LVPECL or LVDS source with little or no difference in performance. The common mode voltage of the clock input is set to 1.4V using internal 5kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close as possible to the clock inputs in order to minimize signal reflections and jitter degradation.



SNR AND CLOCK JITTER

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 96dB for a 16bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2} \quad (1)$$

The SNR limitation due to sample clock jitter can be calculated as following:

$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{in} \times T_{Jitter}) \quad (2)$$

The total clock jitter (TJitter) has three components – the internal aperture jitter (85fs for ADS42JB49/69) which is set by the noise of the clock input buffer, the external clock jitter and the jitter from the analog input signal. It can be calculated as following:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2 + (T_{Jitter,Analog\_input})^2} \quad (3)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter.

The ADS42JB49/69 has a thermal noise of 74.1dBFS and internal aperture jitter of 85fs. The SNR depending on amount of external jitter for different input frequencies is shown in Figure 15.

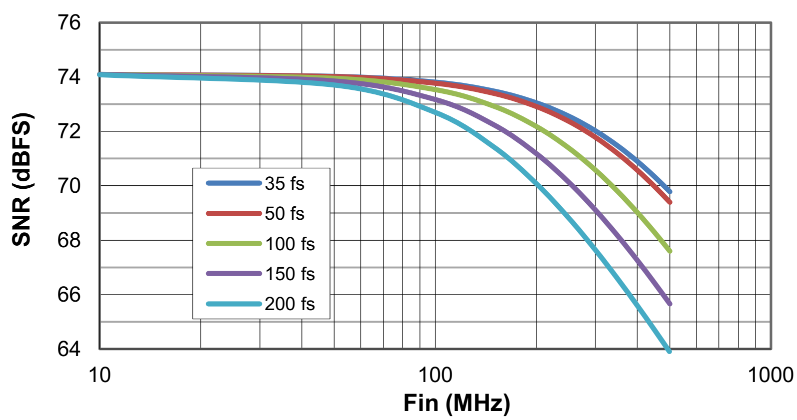


Figure 15. SNR vs Input Frequency and External Clock Jitter

INPUT CLOCK DIVIDER

The ADS42JB49/69 is equipped with an internal divider on the clock input. This allows operation with a faster input clock simplifying the system clock distribution design. The clock divider can be bypassed (/1) for operation with a 250MHz clock while /2 option supports a maximum input clock of 500MHz and the /4 option a maximum input clock frequency of 1GHz.

PRODUCT PREVIEW

POWER DOWN CONTROL

The power down functions of the ADS42JB49/69 can be controlled either through the parallel control pins (STBY, PDN_GBL, CTRL1 and CTRL2) or through a SPI register setting.

STBY places the device in standby power down mode. PDN_GBL places the device in global power down mode.

Table 2. Power Down Control

CTRL1	CTRL2	DESCRIPTION
Low	Low	Normal operation
High	Low	ChA powered down
Low	High	ChB powered down
High	High	Global power don

JESD204B INTERFACE

The ADS42JB49/69 supports device subclass 0, 1 and 2 with a maximum output data rate of 3.125 Gbps for each serial transmitter.

An external SYSREF (subclass 1) or SYNC (subclass 2) signal is used to align all internal clock phases and the local multi frame clock to a specific sampling clock edge. This allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

Depending on the ADC sampling rate, the JESD204B output interface can be operated with either 1 or 2 lanes per single ADC or 2,3 or 4 lanes per dual ADC. The JESD204B setup and configuration of the frame assembly parameters is handled via SPI interface.

The JESD204B transmitter block consists of the transport layer, the data scrambler and the link layer.

The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are being transmitted. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally data from the transport layer can be scrambled.

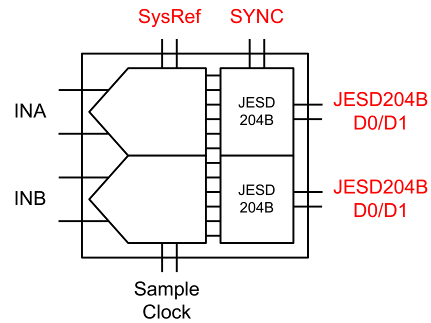


Figure 16. JESD204B Interface

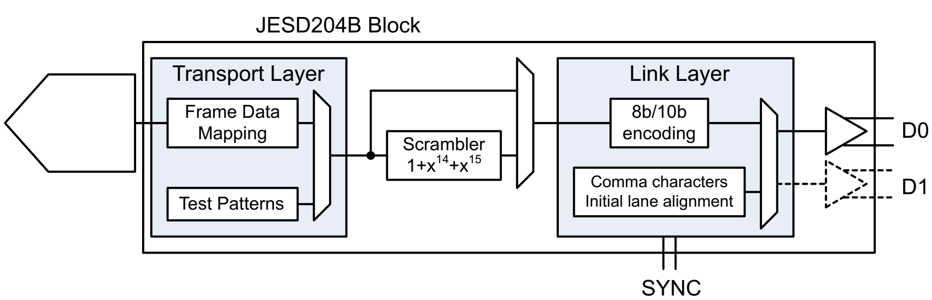


Figure 17. JESD204B Block

JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by asserting the SYNC signal. Upon detecting a logic high on the SYNC input pins, the ADS42JB49/ADS42JB69 starts transmitting comma (K28.5) characters to establish code group synchronization.

Once synchronization is completed the receiving device de-asserts the SYNC signal and the ADS42JB49/ADS42JB69 starts the initial lane alignment sequence with the next local multi frame clock boundary. The ADS42JB49/ADS42JB69 transmits 4 multi-frames each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the 2nd multi-frame also contains the JESD204 link configuration data.

JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADS42JB49/ADS42JB69 supports a clock output, encoded and a PRBS (2^{15} – 1) pattern. They can be enabled via SPI register write and are located in address 0x26 bits D7-D6.

PRODUCT PREVIEW

JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link
- M is the number of converters for device
- F is the number of octets per frame clock period
- S is the number of samples per frame

Table 3 lists the available JESD204B formats and valid ranges for the ADS42JB49/ADS42JB69. The ranges are limited by the maximum ADC sample frequency and the Serdes line rate.

Table 3. JESD240B Ranges

L	M	F	S	Max ADC Sampling Rate (Msps)	Max f_{SERDES} (Gsps)
4	2	1	1	250	2.5
2	2	2	1	156.25	3.125

The detailed frame assembly for dual channel mode is shown in Figure 18.

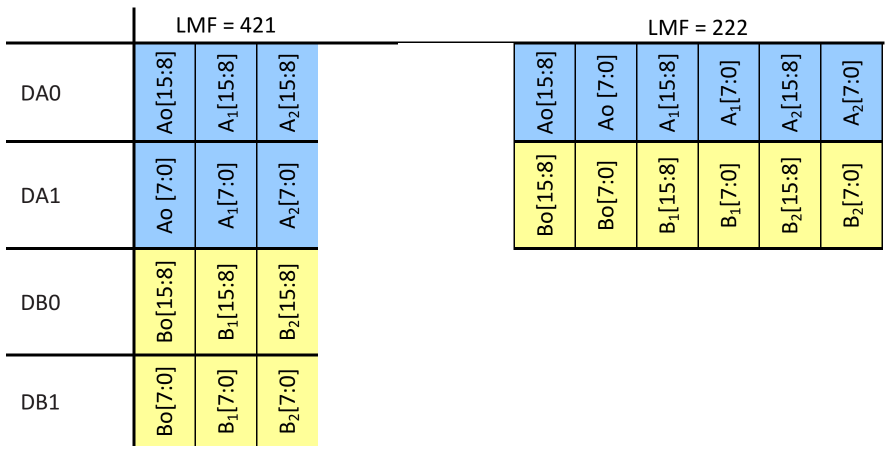


Figure 18. Frame Assembly for Dual Channel Mode

Digital Outputs

The JESD204B transmitter of the ADS42JB49/69 uses differential CML output drivers. The CML output current is programmable from 5mA to 20mA using the SPI register settings.

The output driver expects to drive a differential 100 Ω load impedance and the termination resistors should be placed as close to the receiver inputs as possible to avoid unwanted reflections and signal distortion. Since JESD204B employs 8b/10b encoding, the output data stream is DC-balanced and AC coupling can be used avoiding the need to match up common mode voltages between transmitter and receivers. The termination resistors should be connected to the termination voltage as shown in Figure 19.

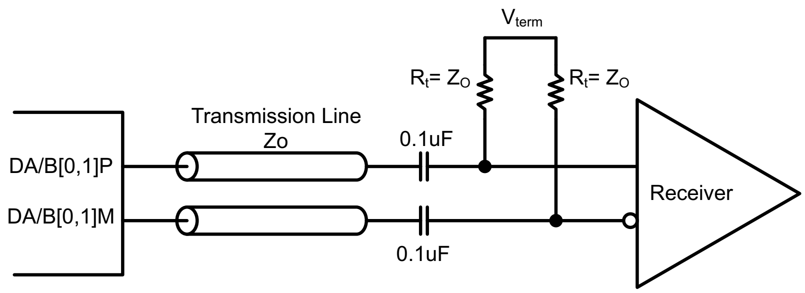


Figure 19. Digital Outputs

Figure 20 shows the data eye measurements of the ADS42JB69 JESD204B transmitter against the JESD204B transmitter mask at 2.5Gbps (10x mode) and 3.125Gbps (20x mode).

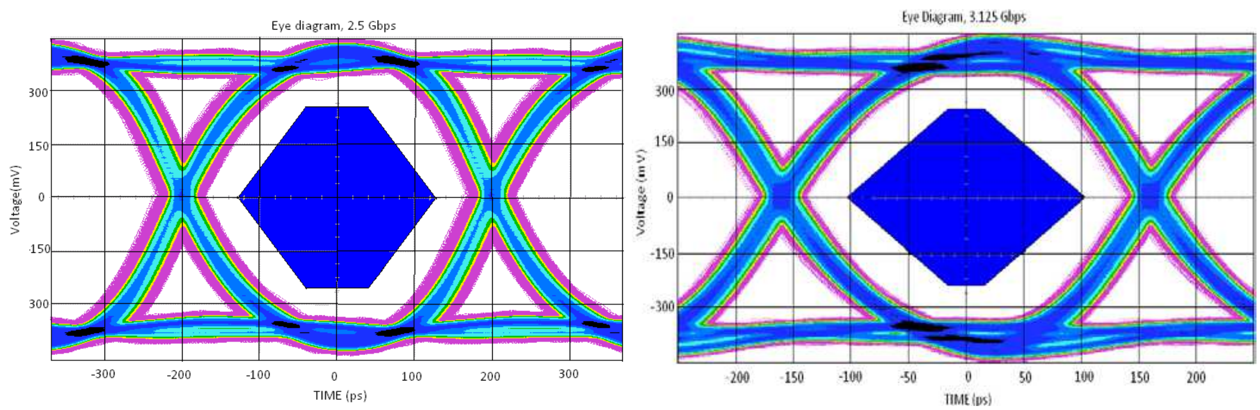


Figure 20. Data Eye Measurements

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS42JB49IRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI	
ADS42JB49IRGCT	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI	
ADS42JB69IRGC25	PREVIEW	VQFN	RGC	64	25	TBD	Call TI	Call TI	
ADS42JB69IRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI	
ADS42JB69IRGCT	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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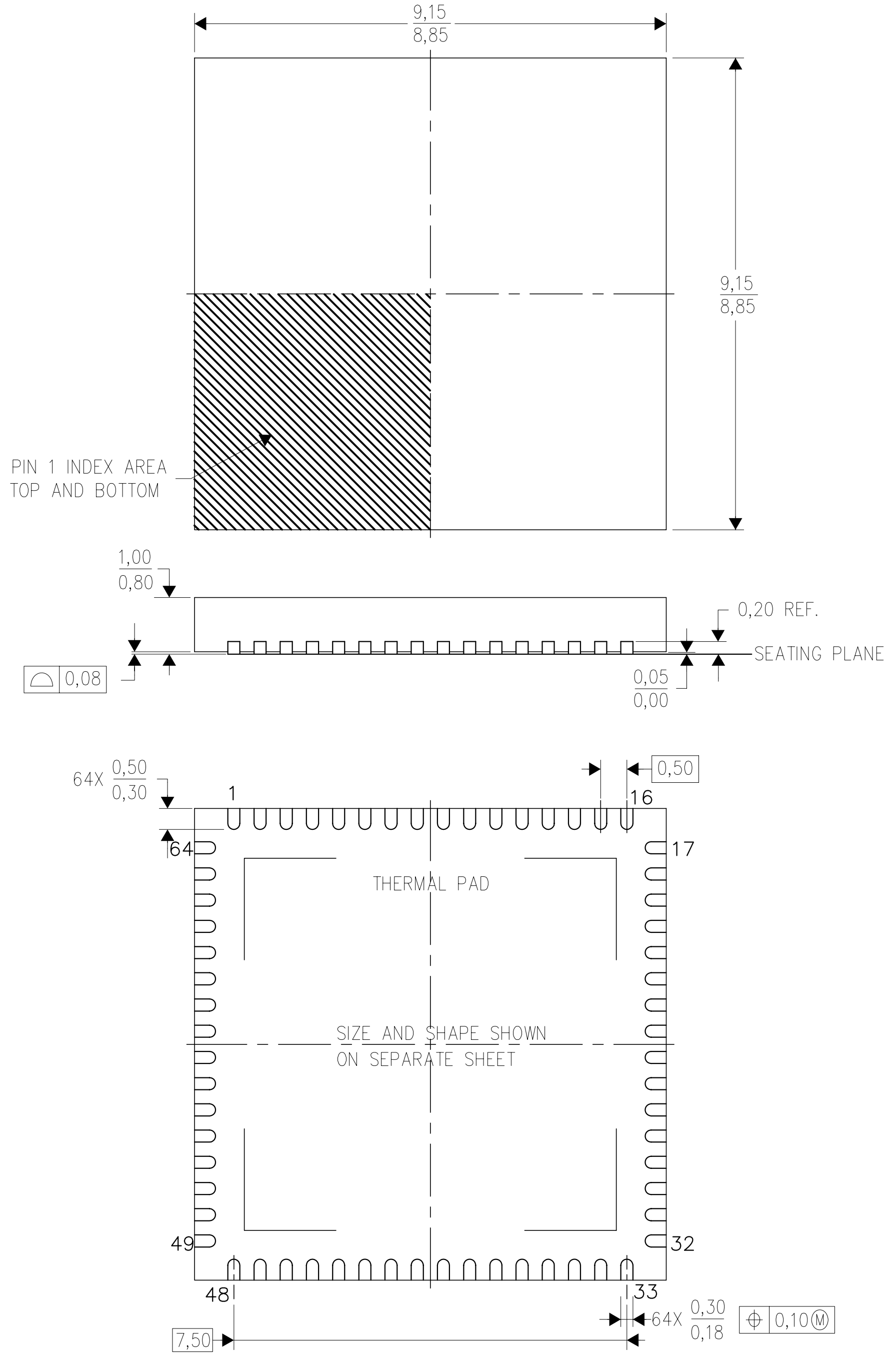
RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



4204106/F 11/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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