Dual Channel 14-/16-Bit 250Msps Analog-to-Digital Converters

Check for Samples: ADS42LB49, ADS42LB69

FEATURES

- **Dual Channel**
- **14/16-Bit Resolution**
- **Maximum Clock Rate: 250 Msps**
- **Analog Input Buffer with High Impedance Input**
- **Flexible Input Clock Buffer with divide by 1,2,4**
- **2Vpp and 2.5Vpp Differential Full-Scale Input (SPI programmable)**
- **DDR or QDR LVDS Interface**
- **64-Pin QFN Package (9x9mm)**
- **Power Dissipation: 740mW/ch**
- **Aperture Jitter: 85fs**
- **Channel Isolation: 100dB**
- **Performance at f_{in} = 170 MHz at 2Vpp,-1dBFS**
  - **SNR: 73.3 dBFS**
  - **SFDR: 89 dBc HD2,3**
    100 dBc non HD2,3
- **Performance at f_{in} = 170 MHz at 2.5Vpp,-1dBFS**
  - **SNR: 74.9 dBFS**
  - **SFDR: 86 dBc HD2,3**
    97 dBc non HD2,3

Interface Option	14-Bit	16-Bit
DDR/QDR LVDS	ADS42LB49	ADS42LB69
JESD204B	ADS42JB49	ADS42JB69

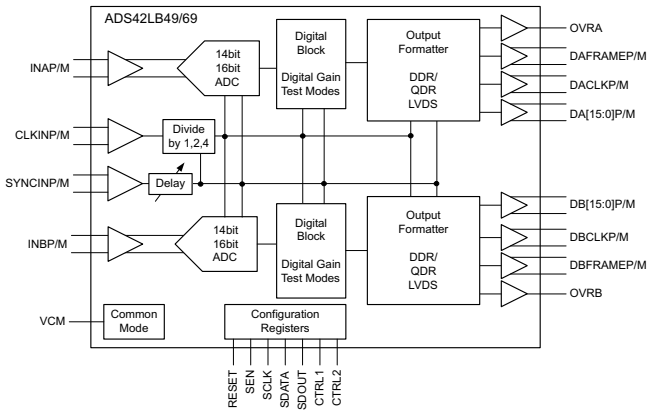
PRODUCT PREVIEW

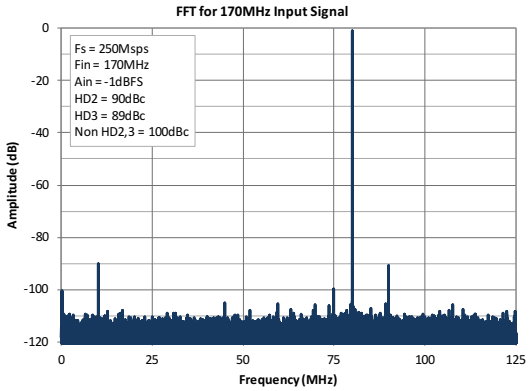
APPLICATIONS

- **Multicarrier, Multimode Cellular Receivers**
- **Radar and Smart Antenna Arrays**
- **Broadband Wireless**
- **Communications Test Equipment**
- **Microwave Receivers**
- **Software Defined Radios**

DESCRIPTION

The ADS42LB49/69 are a family of high linearity dual channel 14 and 16-bit, 250 MSPS analog-to-digital converters (ADC). The ADS42xB49/69 family supports the JESD204B serial interface with data rates up to 3.125Gbps as well as DDR and QDR LVDS interfaces. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A sampling clock divider allows more flexibility for system clock architecture design. The ADS42LB49/69 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with low power consumption.





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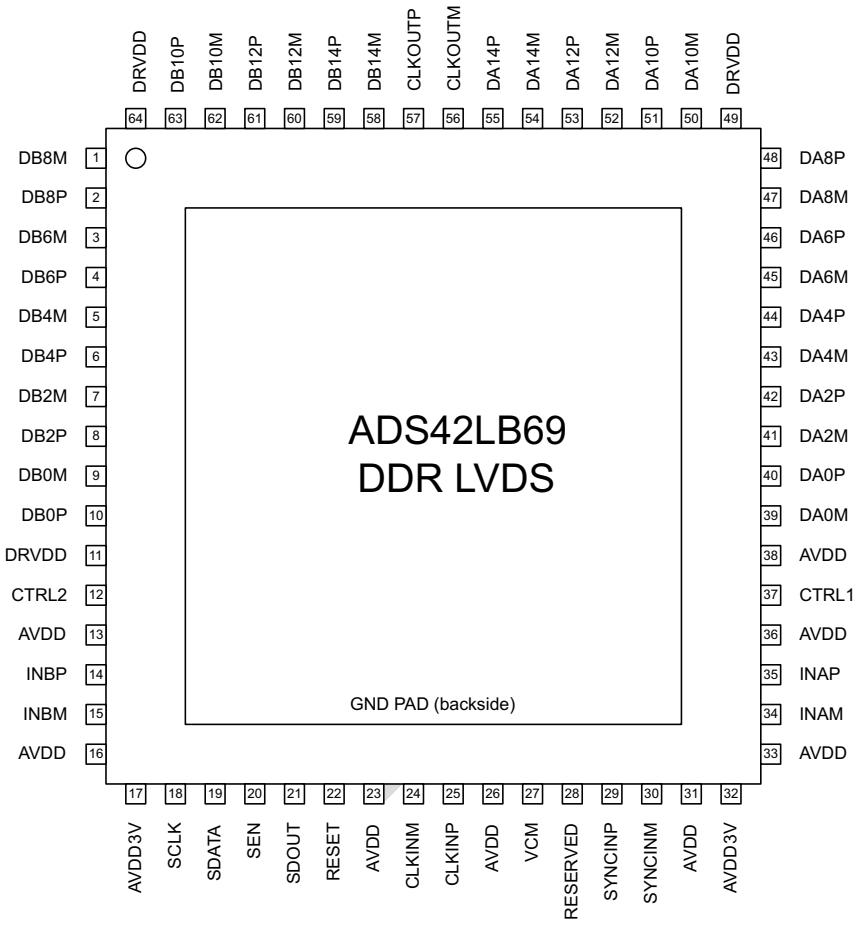
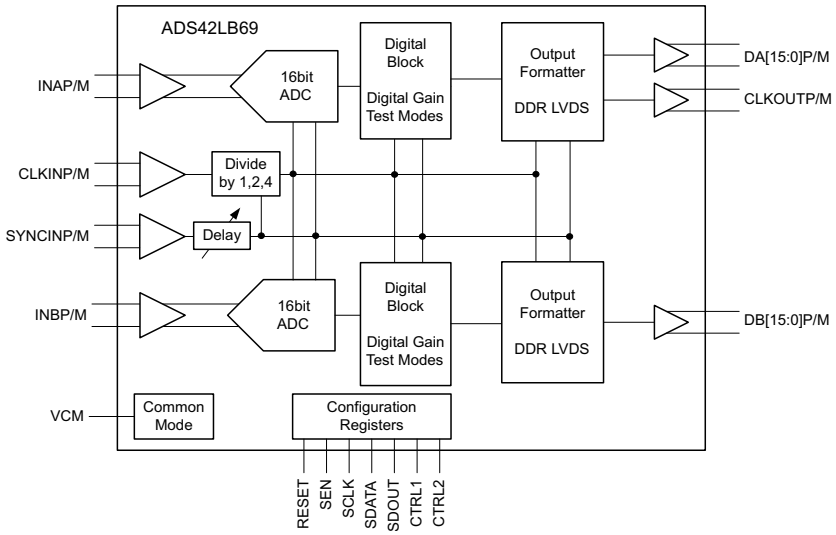
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PINOUT INFORMATION – ADS42LB69 DDR LVDS





PRODUCT PREVIEW

PIN ASSIGNMENTS – ADS42LB69 DDR LVDS OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT/REFERENCE			
INAP/M	36, 35	I	Differential analog input for channel A
INBP/M	14, 15	I	Differential analog input for channel B
VCM	27	O	Common mode voltage for analog inputs, 1.85V
CLOCK/SYNC			
CLKINP/M	25, 24	I	Differential clock input for ADC
SYNCINP/M	29, 30	I	External sync input
CONTROL/SERIAL			
RESET	22	I	Hardware reset. Active high. This pin has an internal 150kΩ pull-down resistor.
SCLK	18	I	Serial interface clock input
SDATA	19	I	Serial interface data input.
SEN	20	I	Serial interface enable
SDOUT	21	O	Serial interface data output
CTRL1	37	I	Power down control
CTRL2	12	I	Power down control
Reserved	28	–	Do not connect
DATA INTERFACE			
DA[14..0]P/M	40,39,42,41,44,43,46,45,48,47,51,50,53,52,55,54	O	DDR LVDS output interface for channel A
DB[14..0]P/M	9,10,7,8,5,6,3,4,1,2,62,63,60,61,58,59	O	DDR LVDS output interface for channel B
CLKOUTP/M	57, 56	O	Differential LVDS output clock
POWER SUPPLY			
AVDD3V	17, 32	I	Analog 3.3V for analog buffer
AVDD	13,16,23,26,31,33,36,38	I	Analog 1.8V power supply
DRVDD	11,49,64	I	Digital 1.8V power supply
GND	Power pad	I	Ground

PRODUCT PREVIEW

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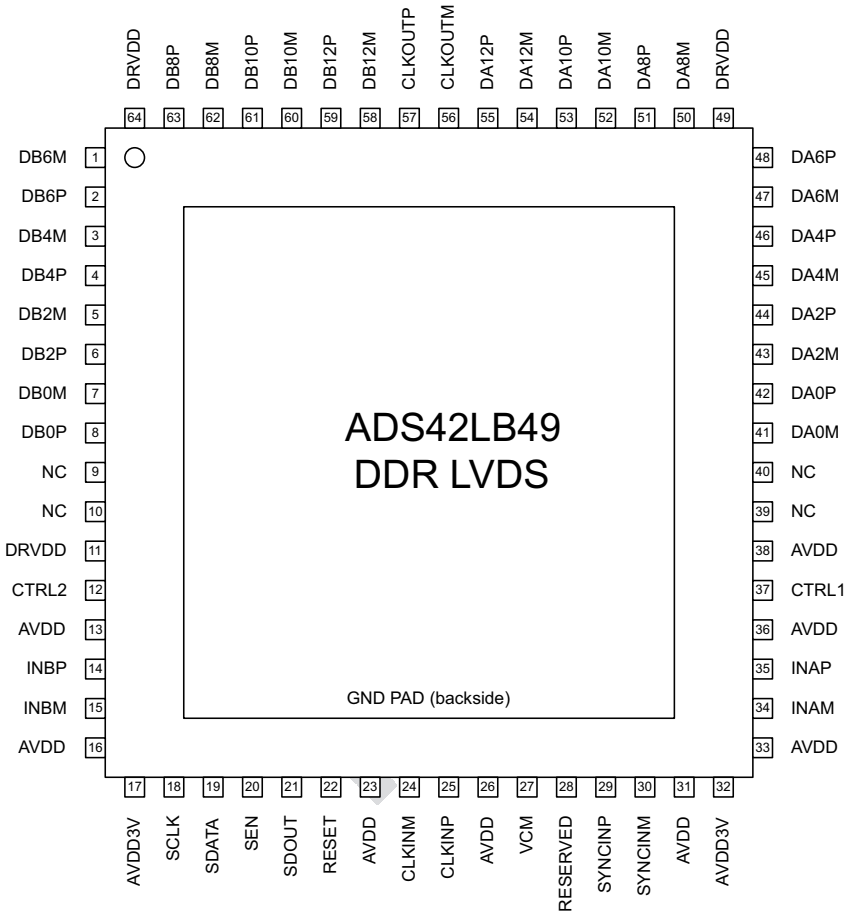
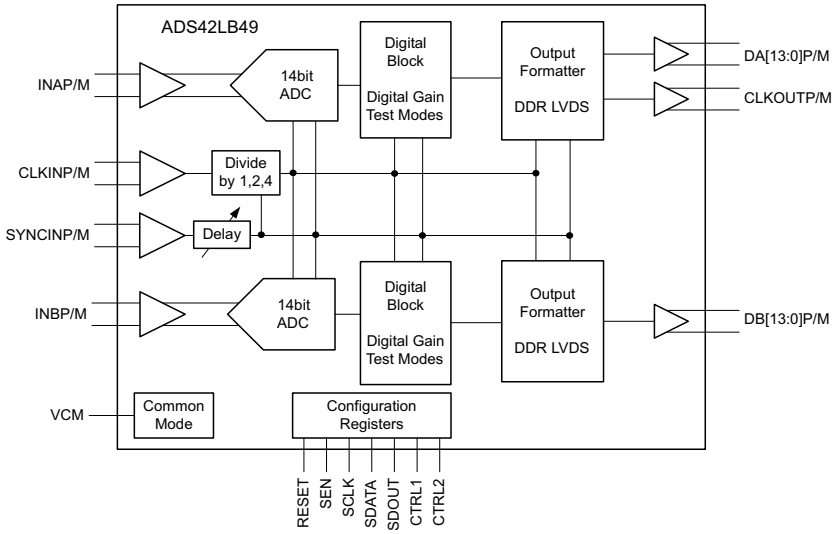
PINOUT INFORMATION – ADS42LB49 DDR LVDS





PIN ASSIGNMENTS – ADS42LB49 DDR LVDS OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT/REFERENCE			
INAP/M	35, 35	I	Differential analog input for channel A
INBP/M	14, 15	I	Differential analog input for channel B
VCM	27	O	Common mode voltage for analog inputs, 1.85V
CLOCK/SYNC			
CLKINP/M	25, 24	I	Differential clock input for ADC
SYNCINP/M	29, 30	I	External sync input
CONTROL/SERIAL			
RESET	22	I	Hardware reset. Active high. This pin has an internal 150kΩ pull-down resistor.
SCLK	18	I	Serial interface clock input
SDATA	19	I	Serial interface data input.
SEN	20	I	Serial interface enable
SDOUT	21	O	Serial interface data output
CTRL1	37	I	Power down control
CTRL2	12	I	Power down control
Reserved	28	–	Do not connect
NC	9,10,39,40	–	Do not connect
DATA INTERFACE			
DA[14..0]P/M	42,41,44,43,46,45,48,47,51,50,53,52,55,54	O	DDR LVDS output interface for channel A
DB[14..0]P/M	7,8,5,6,3,4,1,2,62,63,60,61,58, 59	O	DDR LVDS output interface for channel B
CLKOUTP/M	57, 56	O	Differential LVDS output clock
POWER SUPPLY			
AVDD3V	17, 32	I	Analog 3.3V for analog buffer
AVDD	13,16,23,26,31,33,36,38	I	Analog 1.8V power supply
DRVDD	11,49,64	I	Digital 1.8V power supply
GND	Power pad	I	Ground

PRODUCT PREVIEW

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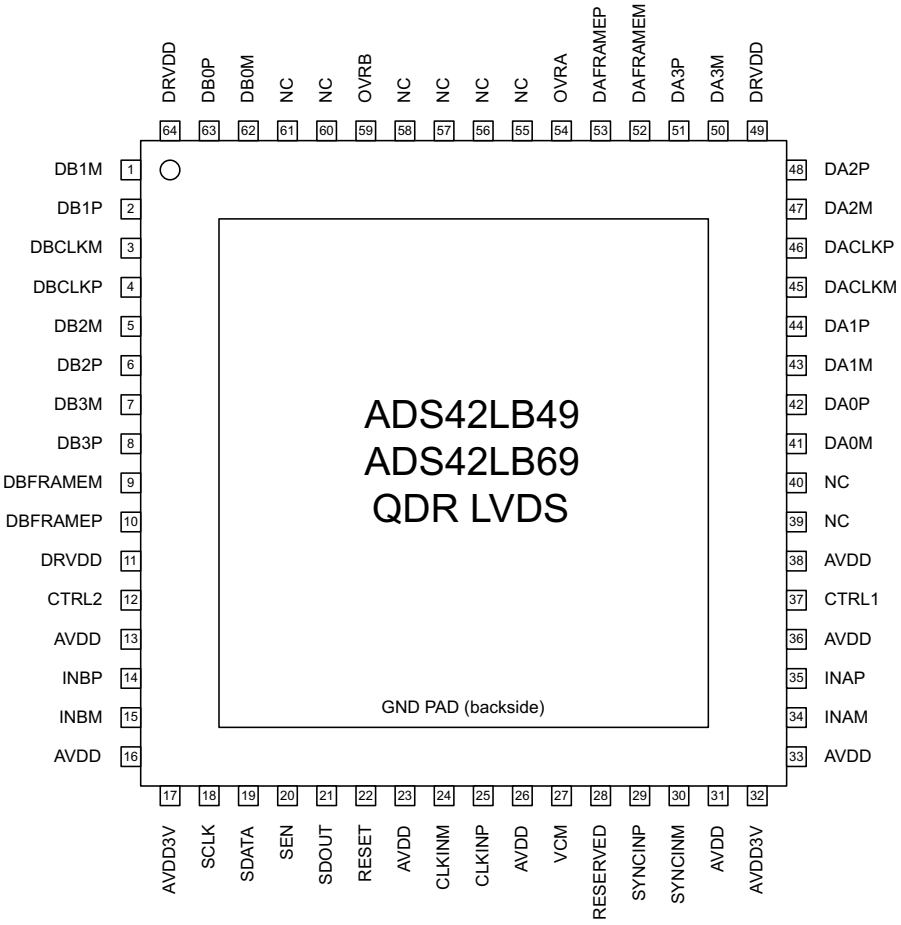
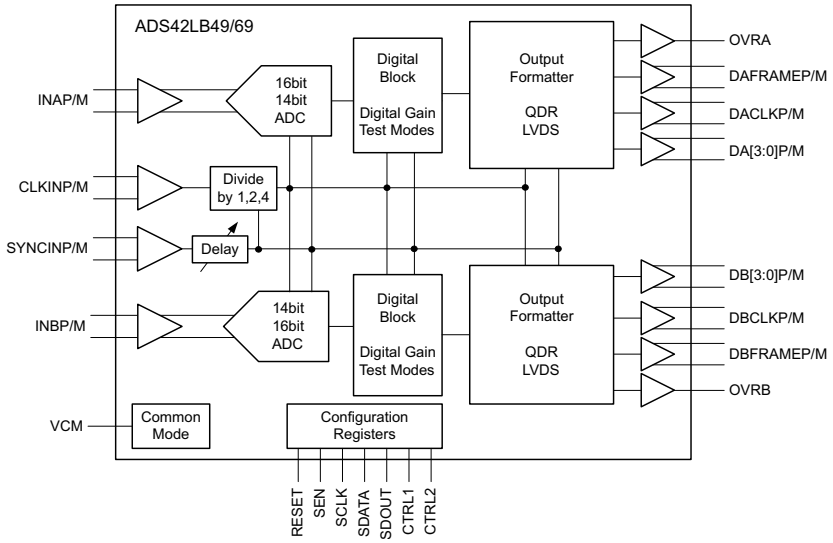
PINOUT INFORMATION – QDR LVDS





PIN ASSIGNMENTS – QDR LVDS OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT/REFERENCE			
INAP/M	35, 34	I	Differential analog input for channel A
INBP/M	14, 15	I	Differential analog input for channel B
VCM	27	O	Common mode voltage for analog inputs, 1.9V
CLOCK/SYNC			
CLKINP/M	25, 24	I	Differential clock input for ADC
SYNCINP/M	29, 30	I	External sync input
CONTROL/SERIAL			
RESET	22	I	Hardware reset. Active high. This pin has an internal 150kΩ pull-down resistor.
SCLK	18	I	Serial interface clock input
SDATA	19	I	Serial interface data input.
SEN	20	I	Serial interface enable
SDOUT	21	O	Serial interface data output
CTRL1	37	I	Power down control
CTRL2	12	I	Power down control
Reserved	28	–	Do not connect
NC	39,40,55,56,57,58 ,60,61	–	Do not connect
DATA INTERFACE			
DA[3..0]P/M	51,50,48,47,44,43 ,42,41	O	4bit QDR LVDS output interface for channel A
DACLKP/M	46,45	O	Differential output clock for channel A
DAFRAMEP/M	53,52		Differential frame clock output for channel A
OVRA	54	O	Overrange indication channel A
DB[3..0]P/M	8,7,6,5,2,1,63,62		4bit QDR LVDS output interface for channel B
DBCLKP/M	4, 3		Differential output clock for channel A
DBFRAMEP/M	10, 9		Differential frame clock output for channel A
OVRB	59	O	Overrange indication channel A
POWER SUPPLY			
AVDD3V	17, 32	I	Analog 3.3V for analog buffer
AVDD	13,16,23,26,31,33 ,36,38	I	Analog 1.8V power supply
DRVDD	11,49,64	I	Digital 1.8V power supply
GND	Power pad	I	Ground

PRODUCT PREVIEW

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS42LB49	QFN-64	RGC	–40°C to 85°C	GREEN (RoHS & no Sb/Br)	NiPdAu	ADS42LB49	ADS42LB49IRGC	Tape and Reel
ADS42LB69						ADS42LB69	ADS42LB69IRGC	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range, AVDD3V		–0.3	3.6	V
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, DRVDD		–0.3	2.1	V
Supply voltage range, IOVDD		–0.3	2.1	V
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INA/BP, INA/BM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3V	V
	SYNCINP, SYNCINM	–0.3	AVDD + 0.3V	V
	SCLK, SEN, SDATA, RESET, PDN, PDN_ANA, MODE	–0.3	3.9	V
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J			125	°C
Storage temperature range		–65	150	°C
ESD, Human Body Model			2	kV

THERMAL INFORMATION

THERMAL METRIC(1)		ADS42JB69 QFN (64-PIN)	UNITS
T_J	Maximum junction temperature	125	°C
θ_{JA}	Junction-to-ambient thermal resistance(2)	23.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	8.8	
θ_{JB}	Junction-to-board thermal resistance(4)	3.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	3.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	??	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS – ADS42LB69

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
ADC Clock Frequency					250	MSPS
Resolution			16			Bits
SUPPLY						
AVDD3V			3.15	3.3	3.45	V
AVDD, DRVDD			1.7	1.8	1.9	V
POWER SUPPLY						
I_{AVDD3V}	3.3V Analog supply current	V_{IN} = Fullscale, f_{IN} = 100MHz		267		mA
I_{AVDD}	1.8V Analog supply current			143		mA
I_{DRVDD}	1.8V Digital supply current			193		mA
P_{dis}	Total power dissipation			1.48		W
Global power down dissipation				30		mW
Wake up time from global power down				TBD		µs
Standby power down dissipation				450		mW
Wake up time from standby power down				TBD		µs

ELECTRICAL CHARACTERISTICS – ADS42LB49

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
ADC Clock Frequency					250	MSPS
Resolution			14			Bits
SUPPLY						
AVDD3V			3.15	3.3	3.45	V
AVDD, DRVDD			1.7	1.8	1.9	V
POWER SUPPLY						
I_{AVDD3V}	3.3V Analog supply current	V_{IN} = Fullscale, f_{IN} = 100MHz		267		mA
I_{AVDD}	1.8V Analog supply current			143		mA
I_{DRVDD}	1.8V Digital supply current			193		mA
P_{dis}	Total power dissipation			1.48		W
Global power down dissipation				30		mW
Wake up time from global power down				TBD		µs
Standby power down dissipation				450		mW
Wake up time from standby power down				TBD		µs

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ANALOG INPUTS					
Differential input full-scale			2.0		Vpp
Input common mode voltage			1.85 ± tbd		V
Input resistance	Differential at DC				Ω
Input capacitance	Each input to GND				pF
VCM common mode voltage output			1.85		V
Analog input bandwidth (3dB)			650		MHz
CLOCK INPUT					
Input clock frequency				1000	MHz
Input clock amplitude			1.5		Vpp
Input clock duty cycle			50%		
Internal clock biasing			1.4		V

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS – ADS42LB69 (16-BIT)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Analog Input Full Scale				2.0			2.5		Vpp
DYNAMIC AC CHARACTERISTICS									
SNR	Signal to Noise Ratio	f_{IN} = 10 MHz		74.1			75.8		dBFS
		f_{IN} = 70 MHz		73.9			75.6		
		f_{IN} = 100 MHz		73.7			75.5		
		f_{IN} = 170 MHz	70.8	73.3			74.9		
		f_{IN} = 210 MHz		73.0			74.5		
SFDR	Spur Free Dynamic Range (including second and third harmonic distortion)	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	81	89			86		
		f_{IN} = 210 MHz		89			85		
HD2	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	81	90			90		
		f_{IN} = 210 MHz		89			85		
HD3	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	81	89			86		
		f_{IN} = 210 MHz		89			86		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion)	f_{IN} = 10 MHz		100			100		dBc
		f_{IN} = 70 MHz		100			100		
		f_{IN} = 100 MHz		100			100		
		f_{IN} = 170 MHz	87	100			97		
		f_{IN} = 210 MHz		100			96		
IMD3		F_{in} = 99 and 101 MHz		TBD			TBD		dBFS
	Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		100			100		dB

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS – ADS42LB49 (14-BIT)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Analog Input Full Scale				2.0			2.5		Vpp
DYNAMIC AC CHARACTERISTICS									
SNR	Signal to Noise Ratio	f_{IN} = 10 MHz		72.6			74.3		dBFS
		f_{IN} = 70 MHz		72.4			74.1		
		f_{IN} = 100 MHz		72.2			74.0		
		f_{IN} = 170 MHz	69.5	71.9			73.4		
		f_{IN} = 210 MHz		71.5			73.0		
SFDR	Spur Free Dynamic Range (including second and third harmonic distortion)	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	79	89			86		
		f_{IN} = 210 MHz		89			85		
HD2	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	79	90			90		
		f_{IN} = 210 MHz		89			85		
HD3	Harmonic Distortion	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz	79	89			86		
		f_{IN} = 210 MHz		89			86		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion)	f_{IN} = 10 MHz		100			100		dBc
		f_{IN} = 70 MHz		100			100		
		f_{IN} = 100 MHz		100			100		
		f_{IN} = 170 MHz	87	100			97		
		f_{IN} = 210 MHz		100			96		
IMD3		F_{in} = 99 and 101 MHz		TBD			TBD		dBFS
	Crosstalk	With a full-scale 170 MHz signal on aggressor and no signal on victim channel		100			100		dB

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
SAMPLE TIMING CHARACTERISTICS						
rms	Aperture Jitter	Sample uncertainty		85		fs rms
	Data Latency	ADC sample to digital output (incl JESD204B interface)		14		Clock Cycles
		ADC sample to digital output (digital gain enabled		18		
	Fast Over-range (OVR) Latency	ADC sample to fast OVR output		9		Clock Cycles

ELECTRICAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD3V = 3.3V, AVDD/DRVDD = 1.8V

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
DIGITAL INPUTS – RESET, SCLK, SEN, SDATA, CTRL1, CTRL2						
	High-level input voltage	All digital inputs support 1.8V and 3.3V logic levels.	1.3			V
	Low-level input voltage				0.4	V
	High-level input current			10		µA
	Low-level input current			–10		µA
	Input capacitance			4		pF
DIGITAL OUTPUTS – SDOUT, OVRA, OVRB						
	High-level output voltage		DRVDD-0.1	DRVDD		V
	Low-level output voltage			0	0.1	V
DIGITAL INPUTS – SYNCINP/M						
	High-level input voltage			1.3		V
	Low-level input voltage			0.5		V
V_{CM}	Input common mode voltage			0.9		V
t_{S_SYNCIN}		Referenced to rising edge of input clock	400		400 + T_{CLKIN} /2	ps
t_{h_SYNCIN}		Referenced to rising edge of input clock	100			

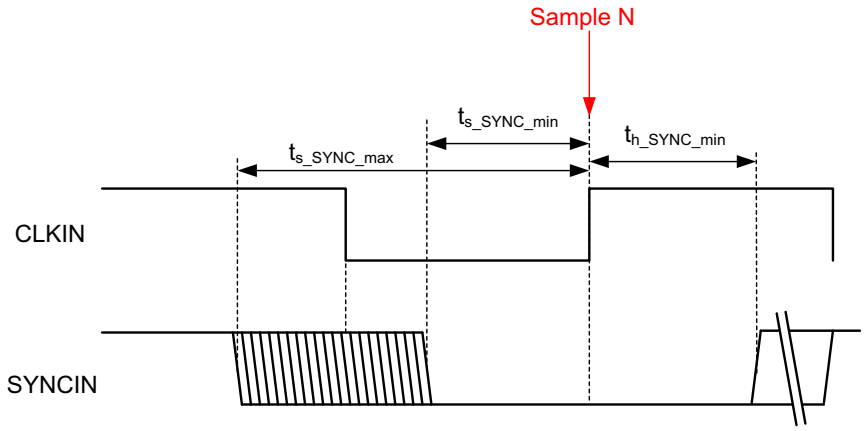


Figure 1. Timing using SYSREF (subclass 1)

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD3V = 3.3V, AVDD/DRVDD = 1.8V

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS – DDR LVDS Interface: DA[14..0], DB[14..0], CLKOUT			**With an external 100Ω termination**			
	High-level output voltage	Standard swing LVDS	270	350	430	mV
	Low-level output voltage	Standard swing LVDS	–430	–350	–270	mV
V_{OCM}	Output common mode voltage		0.85	1.05	1.25	V
t_{SU}	Data setup time	Data valid to zero-crossing of CLKOUTP		800		ps
t_H	Data hold time	Zero-crossing of CLKOUTP to data becoming invalid		800		ps
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over		TBD		ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		TBD		ns

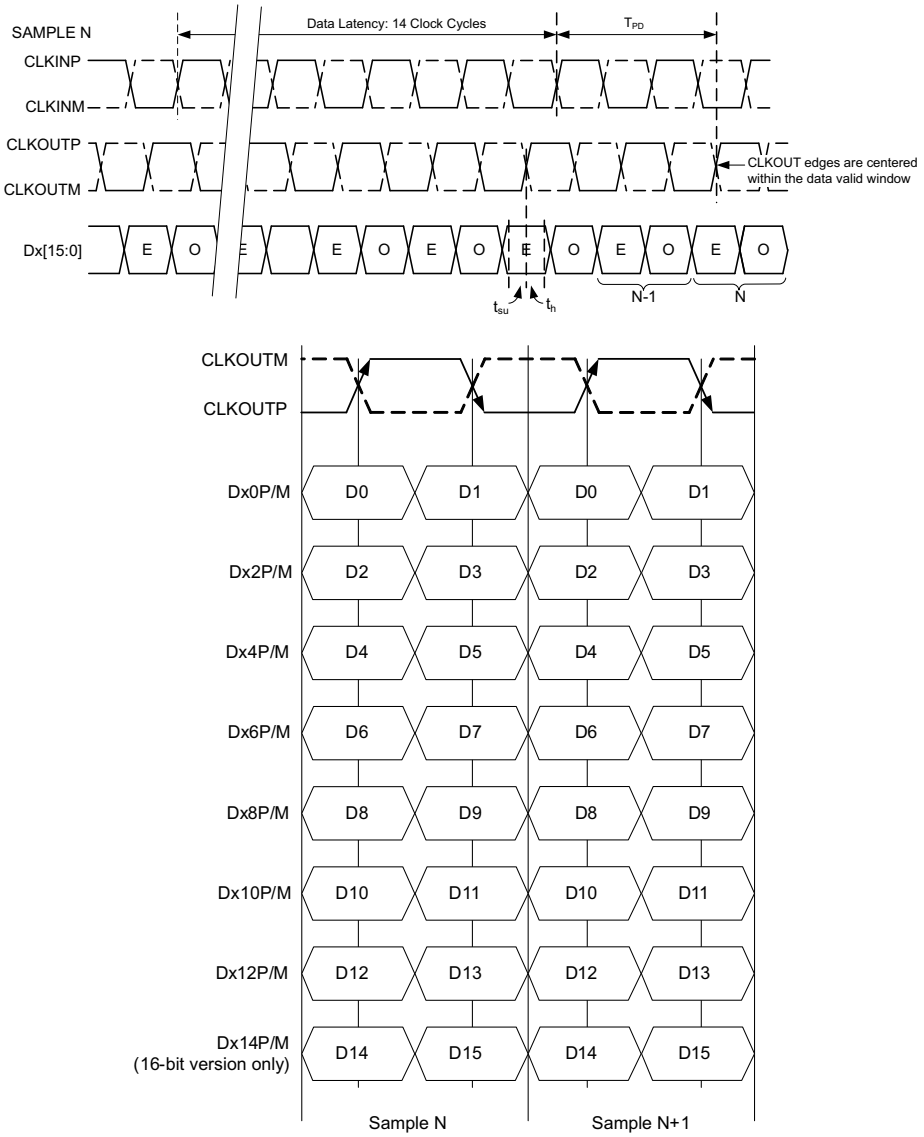


Figure 2. Timing Diagram – DDR LVDS Output

ELECTRICAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD3V = 3.3V, AVDD/DRVDD = 1.8V

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS – QDR LVDS Interface: DA[3..0], DACLK, DAFRAME, DB[3..0], DBCLK, DBFRAME			**With an external 100Ω termination**			
V_{ODH}	High-level output voltage	Standard swing LVDS	270	350	430	mV
V_{ODL}	Low-level output voltage	Standard swing LVDS	–430	–350	–270	mV
V_{OCM}	Output common mode voltage		0.85	1.05	1.25	V
t_{SU}	Data setup time	Data valid to zero-crossing of DxCLKP	TBD	400		ps
t_H	Data hold time	Zero-crossing of DxCLKP to data becoming invalid	TBD	400		ps
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over		TBD		ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		TBD		ns

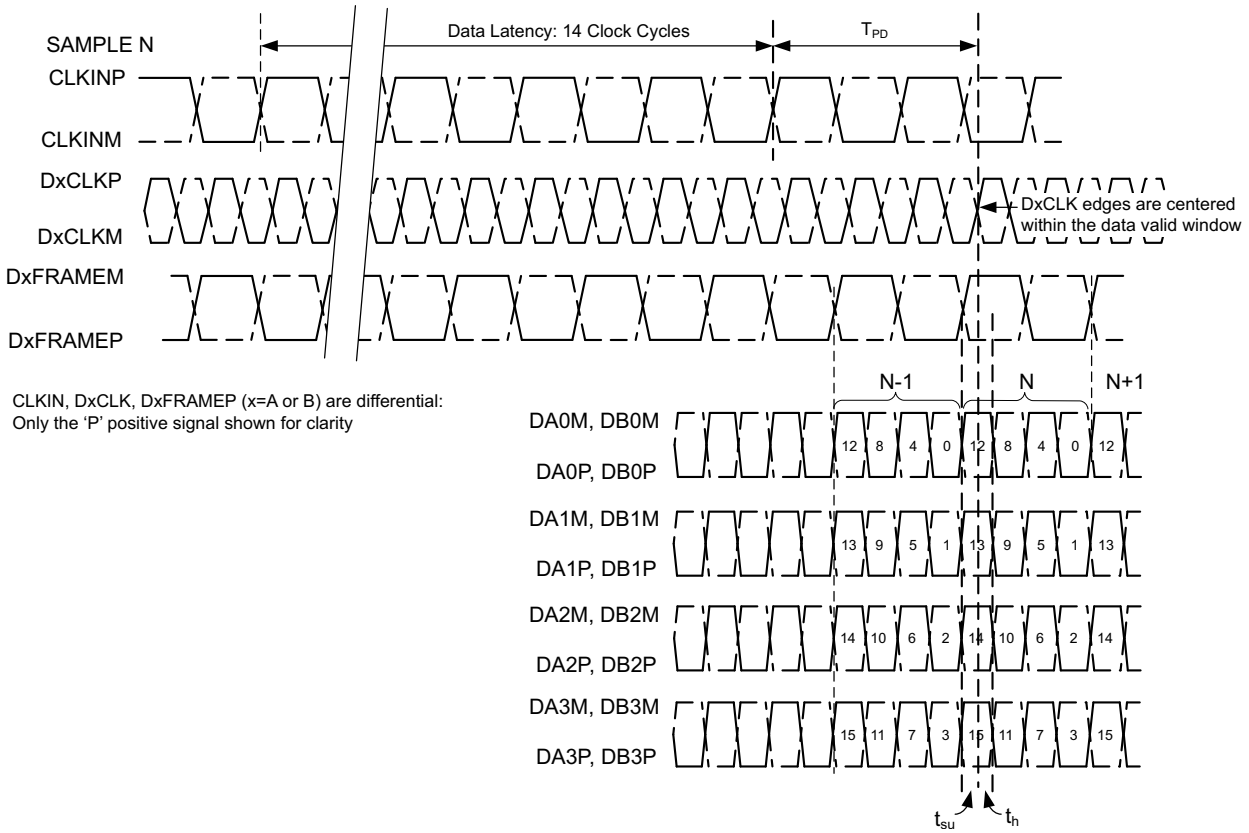


Figure 3. Timing Diagram – QDR LVDS Output

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS – ADS42LB69

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, -1dBFS differential input, 65k-point FFT, unless otherwise noted.

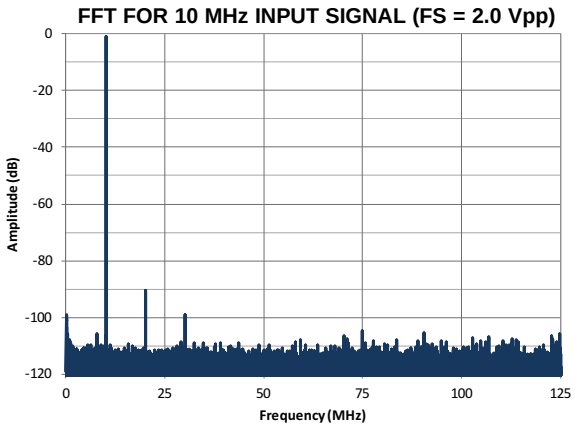


Figure 4.

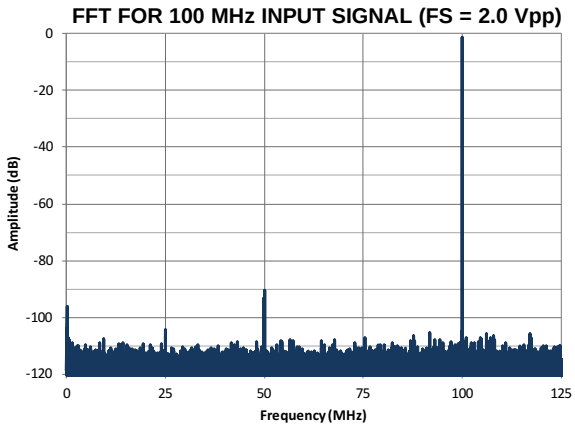


Figure 5.

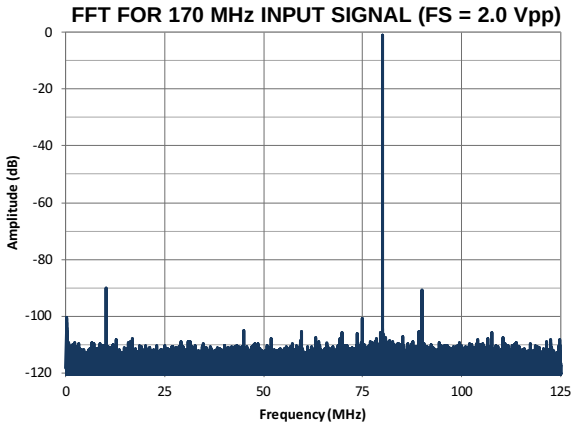


Figure 6.

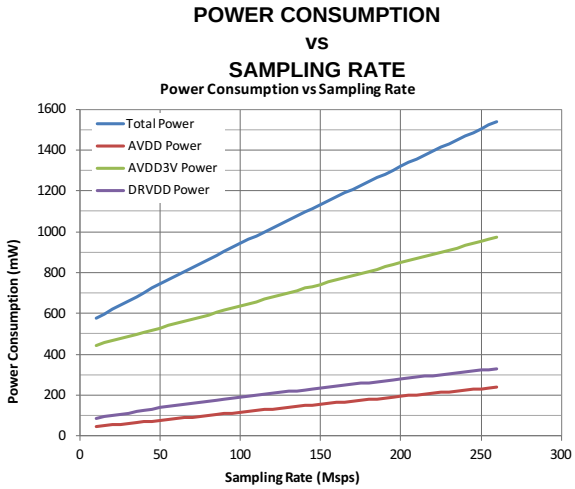


Figure 7.

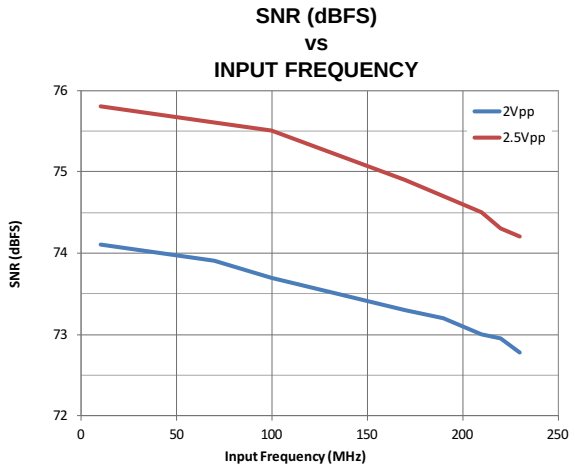


Figure 8.

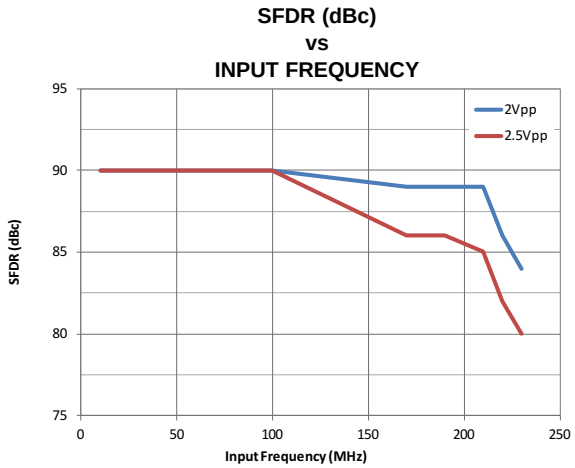


Figure 9.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS – ADS42LB69 (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 250Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD = 1.8V, -1dBFS differential input, 65k-point FFT, unless otherwise noted.

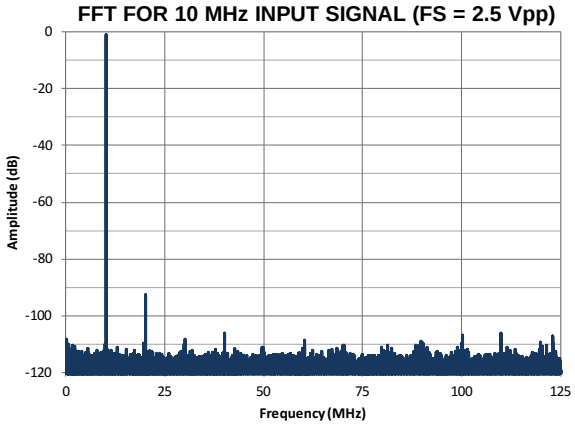


Figure 10.

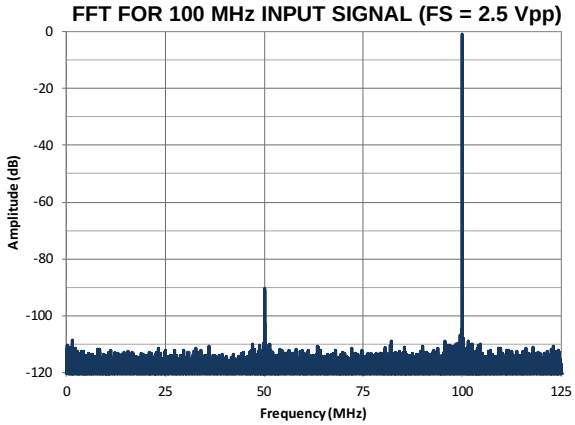


Figure 11.

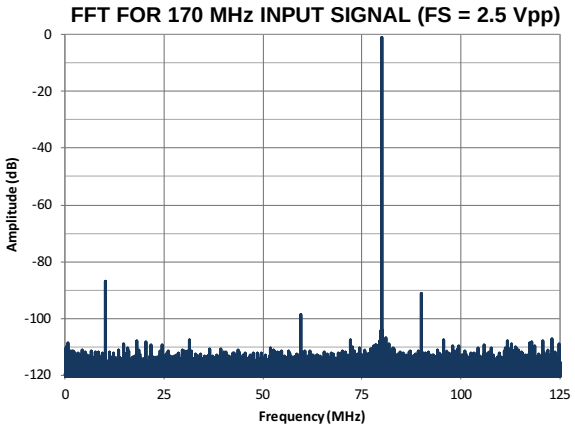


Figure 12.

PRODUCT PREVIEW

DEVICE CONFIGURATION

The ADS42LB49/ADS42LB69 can be configured using a serial programming interface, as described below. In addition, the device has three dedicated parallel pins (STBY, CTRL1 and CTRL2) for controlling the power down modes.

DETAILS OF SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and SDOUT (serial interface data output) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 13; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 08h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

Serial Register Write

The internal register of the ADS42LB49/ADS42LB69 can be programmed following these steps:

1. Drive SEN pin low
2. Set the R/W bit to ‘0’ (bit A7 of the 8 bit address)
3. Set bit A6 in the address field to ‘0’
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content has to be written
5. Write 8 bit data which is latched in on the rising edge of SCLK.

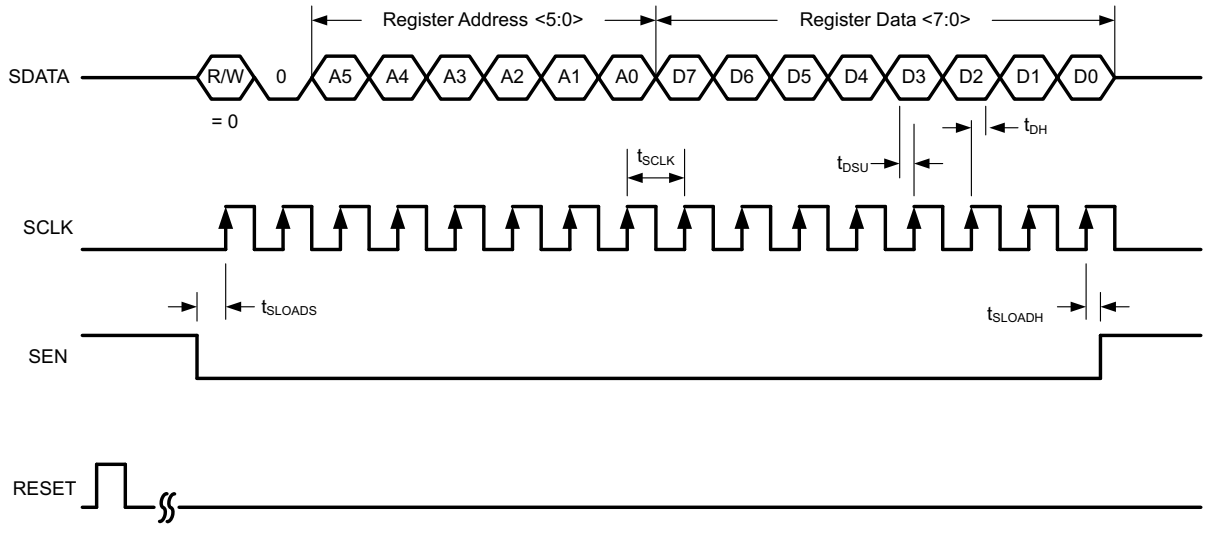


Figure 13. Serial Register Write Timing Diagram

Table 1. Reset Timing (only when Serial Interface is Used)(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to $1/t_{SCLK}$)	>DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: TMIN = –40°C to TMAX = +85°C, AVDD3V = 3.3V, AVDD, DRVDD = 1.9V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SEN pin low
2. Set the R/W bit (A7) to '1'. This setting disables any further writes to the registers
3. Set bit A6 in the address field to 0.
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content has to be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK falling edge.
7. To enable register writes, reset the R/W register bit to '0'.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.

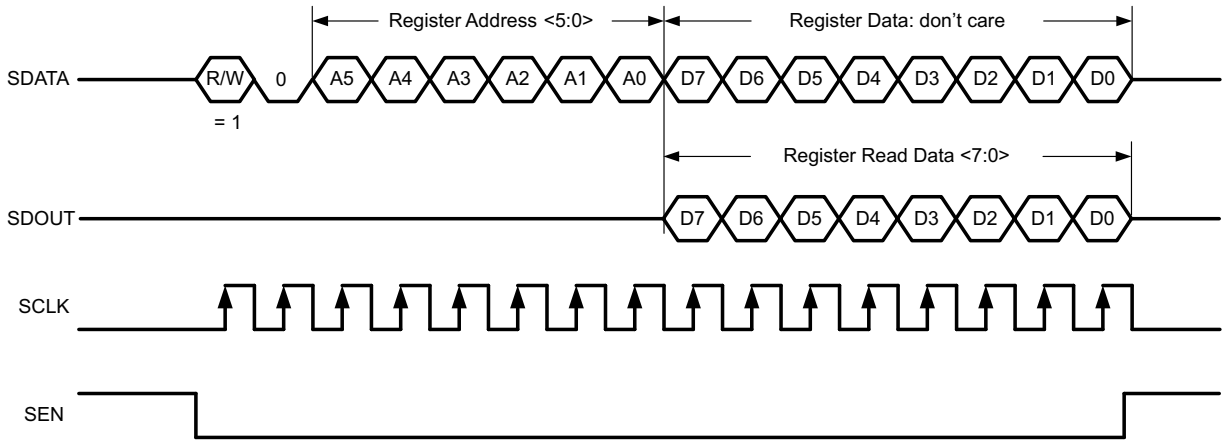


Figure 14. Serial Register Readout Timing Diagram

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SUMMARY OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
4	0	LVDS LOW			LVDS LOW EN	LVDS HIGH		
5	LVDS HIGH EN	0	0	0	0	0	0	0
6	0	0	0	0	0	0	CLK DIV	
7	0	0	0	0	0	SYNCIN DELAY		
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	1	0	0	RESET
B	CHA GAIN					CHA GAIN EN	FLIP DATA	0
C	CHBGAIN					CHB GAIN EN	OVR ON LSB	FAST OVR ON LSB
D	0	0	0	0	0	0	0	FAST OVR ON PIN
F	CHA TEST PATTERNS				CHB TEST PATTERNS			
10	CUSTOM PATTERN 1 (15:8)							
11	CUSTOM PATTERN 1 (7:0)							
12	CUSTOM PATTERN 2 (15:8)							
13	CUSTOM PATTERN 2 (7:0)							
14	0	0	0	0	LVDS CLK STRENGTH	LVDS DATA STRENGTH	DISABLE OUTPUT CHA	DISABLE OUTPUT CHB
15	0	0	0	0	0	0	0	DDR - QDR
16	LOW FREQ DDR	LOW FREQ QDR	DDR OUTPUT TIMING					0
17	CLKOUT DELAY EN	0	QDR TIMING CHA					INV CLK OUT CHA
18	0	0	QDR TIMING CHB					INV CLK OUT CHB
1F	FAST OVR THRESHOLD							
30	0	0	SYNCINEN	0	0	0	0	0

PRODUCT PREVIEW

DESCRIPTION OF SERIAL INTERFACE REGISTERS

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
4	0	LVDS LOW			LVDS LOW EN	LVDS HIGH		

Default: 00h

D6-D4, D2-D0 **LVDS LOW** and **LVDS HIGH** Controls the LVDS output swing

D6-D4 (LVDS Low)	D2-D0 (LVDS High)	Output Voltage (mW)
011	101	475
001	110	435
000	000	350
100	001	310
100	010	280
101	011	240
110	111	130

D3 **LVDS LOW EN** Enables change of default low level LVDS output voltage to value in <D6–D4>

0 Normal operation

1 LVDS low level change enabled

Sets the high level LVDS output voltage

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
5	LVDS HIGH EN	0	0	0	0	0	0	0

Default: 00h

D7 **LVDS HIGH EN** enables change of default high level LVDS output voltage to value in x04h <D6 – D4>

0 Normal operation

1 LVDS low level change enabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
6	0	0	0	0	0	0	CLK DIV	

Default: 00h

D1-D0 **CLK DIV** Internal clock divider for input sample clock

00 /1 (clock divider bypassed)

01 /2

10 /1

11 /4

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
7	0	0	0	0	0	SYNCIN DELAY		

Default: 00h

D2-D0	**SYNCIN DELAY**	Controls the delay of the SYNC input with respect to input clock in 60ps steps	
000	0 ps delay	100	240 ps delay
001	60 ps delay	101	300 ps delay
010	120 ps delay	110	360 ps delay
011	180 ps delay	111	420 ps delay

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	1	0	0	RESET

Default: 00h

D7	**PDN CHA**	Power down channel A
0	normal operation	
1	power down	
D6	**PDN CHB**	Power down channel B
0	normal operation	
1	power down	
D5	**STBY**	Dual ADC is placed into standby mode
0	normal operation	
1	power down	
D4	**DATA FORMAT**	Digital output data format
0	2s complement	
1	offset binary	
D3	**Must be set to 1**	
D0	**RESET**	Software reset applied

This bit resets all internal registers to the default values and self-clears to ‘0’

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
B	CHA GAIN					CHA GAIN EN	FLIP DATA	0

Default: 00h

D7-D3 **CHA GAIN** Digital Gain for channel A (must set CHA GAIN EN bit first (D2))

Register Value	Digital Gain	Max Input Voltage		Register Value	Digital Gain	Max Input Voltage (Vpp)
00000	0 dB	**2.0 Vpp**		01010	1.5 dB	1.7 Vpp
00001	–2.7 dB	2.7 Vpp		01011	2 dB	1.6 Vpp
00010	–2.3 dB	2.6 Vpp		01100	2.5 dB	1.5 Vpp
00011	–2.0 dB	**2.5 Vpp**		01101	3 dB	1.4 Vpp
00100	–1.5 dB	2.4 Vpp		01110	3.5 dB	1.3 Vpp
00101	–1.0 dB	2.2 Vpp		01111	4 dB	1.25 Vpp
00110	–0.5 dB	2.1 Vpp		10000	4.5 dB	1.2 Vpp
00111	0 dB	**2.0 Vpp**		10001	5 dB	1.1 Vpp
01000	0.5 dB	1.9 Vpp		10010	5.5 dB	1.05 Vpp
01001	1 dB	1.8 Vpp		10011	6 dB	1.0 Vpp

D2 **CHA GAIN EN** Digital Gain enable bit for Channel A

0 Digital gain disabled

1 Digital gain enabled

D1 **FLIP DATA** Flips bit order on LVDS output bus (LSB vs MSB)

0 normal operation

1 output bus flipped

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
C	CHB GAIN					CHB GAIN EN	OVR ON LSB	FAST OVR ON LSB

Default: 00h

D7-D3 **CHB GAIN** Digital Gain for channel B (must set CHA GAIN EN bit first (D2))

Register Value	Digital Gain	Max Input Voltage		Register Value	Digital Gain	Max Input Voltage (Vpp)
00000	0 dB	**2.0 Vpp**		01010	1.5 dB	1.7 Vpp
00001	–2.7 dB	2.7 Vpp		01011	2 dB	1.6 Vpp
00010	–2.3 dB	2.6 Vpp		01100	2.5 dB	1.5 Vpp
00011	–2.0 dB	**2.5 Vpp**		01101	3 dB	1.4 Vpp
00100	–1.5 dB	2.4 Vpp		01110	3.5 dB	1.3 Vpp
00101	–1.0 dB	2.2 Vpp		01111	4 dB	1.25 Vpp
00110	–0.5 dB	2.1 Vpp		10000	4.5 dB	1.2 Vpp
00111	0 dB	**2.0 Vpp**		10001	5 dB	1.1 Vpp
01000	0.5 dB	1.9 Vpp		10010	5.5 dB	1.05 Vpp
01001	1 dB	1.8 Vpp		10011	6 dB	1.0 Vpp

D2 **CHB GAIN EN** Digital Gain enable bit for Channel B
0 Digital gain disabled
1 Digital gain disabled

D1 **OVR ON LSB** replaces LSB data (D1,D0) with normal OVR indicator
0 normal operation
1 OVR on LSB enabled

D0 **FAST OVR ON LSB** replaces LSB data (D1,D0) with fast OVR indicator
0 normal operation
1 fast OVR on LSB enabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
D	0	0	0	0	0	0	0	FAST OVR ON PIN

D0 **FAST OVR ON PIN** Selects if normal OVR or fast OVR signal gets presented on OVR pins. This feature is only available in QDR MODE
0 normal OVR on OVR pins
1 fast OVR on OVR pins

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
F	CHA TEST PATTERNS				CHB TEST PATTERNS			

Default: 00h

D7-D4	**CHA TEST PATTERNS**	ChA test pattern programmability
0000	Normal Operation	
0001	Outputs all 0s	
0010	Outputs all 1s	
0011	Outputs toggle pattern:	Output data are an alternating sequence of *1010101010101010* and *0101010101010101*
0100	Output digital ramp:	output data increments by one LSB every clock cycle from code 0 to 65535
0101	Increment pattern:	pattern gets incremented by step size set in custom pattern 1 (0x10 and 0x11, 16bit)
0110	Single pattern:	output data is custom pattern 1 (0x10 and 0x11)
0111	Double pattern:	output data alternates between custom pattern 1 and custom pattern 2
1000	Deskew pattern:	output data is 0xAAAA
1001	SYNC pattern:	output data is 0xFFFF
1010	PRBS pattern:	output data is PRBS
1011	8P sine:	output data is a 8 point sine wave
D3-D0	**CHB TEST PATTERNS**	ChB test pattern programmablility
0000	Normal Operation	
0001	Outputs all 0s	
0010	Outputs all 1s	
0011	Outputs toggle pattern:	Output data are an alternating sequence of *1010101010101010* and *0101010101010101*
0100	Output digital ramp:	output data increments by one LSB every clock cycle from code 0 to 65535
0101	Increment pattern:	pattern gets incremented by step size set in custom pattern 1 (0x10 and 0x11, 16bit)
0110	Single pattern:	output data is custom pattern 1 (0x10 and 0x11)
0111	Double pattern:	output data alternates between custom pattern 1 and custom pattern 2
1000	Deskew pattern:	output data is 0xAAAA
1001	SYNC pattern:	output data is 0xFFFF
1010	PRBS pattern:	output data is PRBS
1011	8P sine:	output data is a 8 point sine wave

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
10	CUSTOM PATTERN 1 (15:8)							

Default: 00h

D7-D0 **CUSTOM PATTERN 1 (15:8)** Set the custom pattern 1 (15:8) using these bits for both channels

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
11	CUSTOM PATTERN 1 (7:0)							

Default: 00h

D7-D0 **CUSTOM PATTERN 1 (7:0)** Set the custom pattern 1 (7:0) using these bits for both channels

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
12	CUSTOM PATTERN 2 (15:8)							

Default: 00h

D7-D0 **CUSTOM PATTERN 2 (15:8)** Set the custom pattern 2 (15:8) using these bits for both channels

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
13	CUSTOM PATTERN 2 (7:0)							

Default: 00h

D7-D0 **CUSTOM PATTERN 2 (7:0)** Set the custom pattern 2 (7:0) using these bits for both channels

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
14	0	0	0	0	LVDS CLK STRENGTH	LVDS DATA STRENGTH	DISABLE OUTPUT CHA	DISABLE OUTPUT CHB

Default: 00h

D3 **LVDS CLK STRENGTH** increases the LVDS drive strength

0 normal operation

1 increases LVDS clock output strength by

D2 **LVDS DATA STRENGTH** increases the LVDS drive strength

0 normal operation

1 doubles the LVDS output swing

D1 **DISABLE OUTPUT CHA** disables LVDS output bus chA

0 normal operation

1 chA output bus disabled

D0 **DISABLE OUTPUT CHB** disables LVDS output bus chB

0 normal operation

1 chB output bus disabled

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
15	0	0	0	0	0	0	0	DDR - QDR

Default: 00h

D0 **DDR – QDR** selects output interface between DDR and QDR LVDS mode

0 QDR LVDS mode

1 DDR LVDS mode

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
16	LOW FREQ DDR	LOW FREQ QDR	DDR OUTPUT TIMING					0

Default: 00h

D7 **LOW FREQ DDR** improves output timing for sampling rates below 140Msps in DDR LVDS mode

0 normal operation

1 improved output timing

D6 **LOW FREQ QDR** improves output timing for sampling rates below 140Msps in QDR LVDS mode

0 normal operation

1 improved output timing

D5-D1 **DDR OUTPUT TIMING** adjusts position of output data clock with respect to output data. CLKOUT DELAY EN bit in address 0x17 bit D7 needs to be enabled first.
Relative clock position can be calculated independent of sampling rate: P[ns] = T/R – 1 where T is sampling clock period and R is divider ratio.

	R	Example for 250Msps		R	Example for 250Msps
00101	5	–200 ps	01110	3.31	209 ps
00111	4.53	–117 ps	01011	3.07	303 ps
00000	4	0 ps (default)	10100	2.88	391 ps
01101	3.61	180 ps	10000	2.67	500 ps

PRODUCT PREVIEW

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
17	CLKOUT DELAY EN	0	QDR OUTPUT TIMING CHA					INVCLK OUT CHA

Default: 00h

D7 **CLKOUT DELAY EN** enables timing adjustment of output data clock

0 normal operation

1 output clock delay enabled

D5-D1 **QDR OUTPUT TIMING CHA** adjusts position of output data clock on chA with respect to output data. CLKOUT DELAY EN bit in address 0x17 bit D7 needs to be enabled first. Relative clock position can be calculated independent of sampling rate: P[ns] = 0.5 x (T/R – 1) where T is sampling clock period and R is divider ratio.

	R	Example for 250Msps		R	Example for 250Msps
00101	5	–100 ps	01110	3.31	104 ps delay
00111	4.53	–59 ps	01011	3.07	151 ps delay
00000	4	0 ps (default)	10100	2.88	195 ps delay
01101	3.61	54 ps	10000	2.67	250 ps delay

D0 **INV CLK OUT CHA** inverts polarity of the output clock for chA (QDR mode only)

0 normal operation

1 chA output clock inverted

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
18	0	0	QDR OUTPUT TIMING CHB					INVCLK OUT CHB

Default: 00h

D7 **INV CLK OUT CHB** inverts polarity of the output clock for chB (QDR mode only)

0 normal operation

1 chB output clock inverted

D5-D1 **QDR OUTPUT TIMING CHB** adjusts position of output data clock on chB with respect to output data. CLKOUT DELAY EN bit in address 0x17 bit D7 needs to be enabled first. Relative clock position can be calculated independent of sampling rate: P[ns] = 0.5 x (T/R – 1) where T is sampling clock period and R is divider ratio.

	R	Example for 250Msps		R	Example for 250Msps
00101	5	–100 ps	01110	3.31	104 ps delay
00111	4.53	–59 ps	01011	3.07	151 ps delay
00000	4	0 ps (default)	10100	2.88	195 ps delay
01101	3.61	54 ps	10000	2.67	250 ps delay

Register Address	Register Data							
A7-A0 IN HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1F	FAST OVR THRESHOLD							

Default: FFh

D7-D0 **FAST OVR THRESHOLD**

The ADS42LB49/69 has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered 9 clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 255). After reset, when FAST OVR EN is set, the default value of the FAST OVR THRESHOLD bits is 255 (decimal).

Register Address	Register Data							
A7-A0 IN HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
30	0	0	SYNCIN EN	0	0	0	0	0

Default: 00h

D5 **SYNCIN EN** Enable bit for SYNCIN input.

0 SYNC disabled

1 SYNC enabled

PRODUCT PREVIEW

FEATURES

ANALOG INPUTS

The ADS42LB49/69 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50Ω matching for RF applications.

The buffer also helps to isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to 1.85V using 5kΩ resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5V) and (VCM – 0.5V), resulting in a 2Vpp (default) differential input swing. The input sampling circuit has a 3dB bandwidth that extends up to 650MHz. Figure 15 shows an equivalent circuit for the analog input.

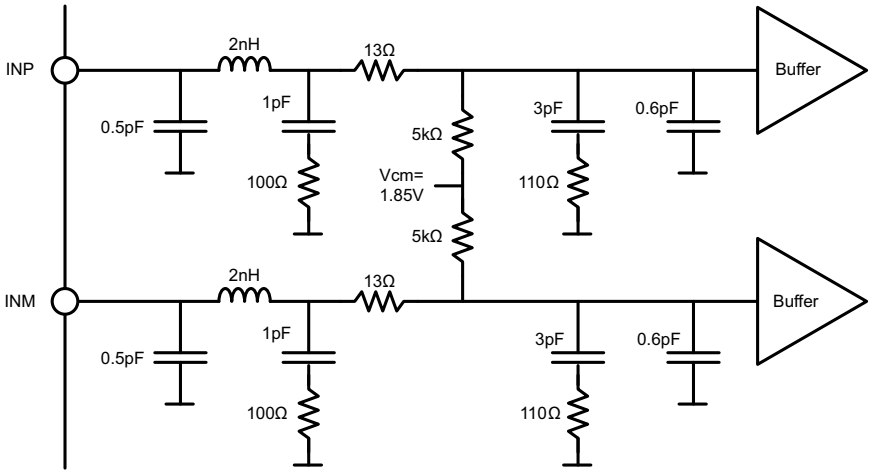


Figure 15. Analog Inputs

DIGITAL GAIN

The input full-scale amplitude can be selected between 1Vpp to 2.7Vpp (default is 2Vpp) by choosing the appropriate digital gain setting via SPI register write. This provides an option to trade off SNR for SFDR performance. A larger input full-scale increases SNR performance (2.5Vpp recommended for maximum SNR) while reduced input swing typically results in better SFDR performance.

DIGITAL GAIN	MAX INPUT VOLTAGE
-2 dB	2.5 Vpp
-1 dB	2.2 Vpp
0 dB (default)	2.0 Vpp
1 dB	1.8 Vpp
2 dB	1.6 Vpp
3 dB	1.4 Vpp
4 dB	1.25 Vpp
5 dB	1.1 Vpp
6 dB	1.0 Vpp

OVER-RANGE INDICATION

The ADS42LB49/69 provides two different overrange indications. The normal OVR (default) is triggered if the final 16 bit data output exceeds the maximum code value. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 9 clock cycles enabling a quicker reaction to an overrange event.

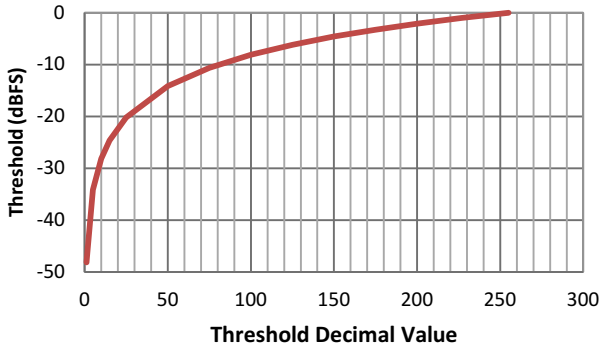
By default the normal overrange indication is output only on the OVRA and OVRB pins. Using the SPI register map, the normal OVR indication can also be embedded in the serialized output data stream replacing the 2 LSBs of the ADC output data. Furthermore the fast OVR indication can be presented instead

OVR on LSB (0xC, D1)	FOVR EN (0xD, D0)	FOVR on LSB (0xC, D1)	DESCRIPTION
0	0	0	Normal OVR on OVRA/B pins (default)
1	0	0	Normal OVR on OVRA/B pins and on LSBs
0	1	0	Fast OVR on OVRA/B pins
0	1	1	Fast OVR on OVRA/B pins and on LSBs

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered 9 output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] / 255). After reset, when FAST OVR EN is set, the default value of the FAST OVR THRESHOLD bits is 255 (decimal).

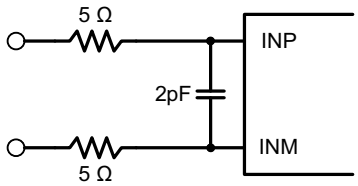
The full-scale is including digital gain – for example with +1dB digital gain the full-scale value is reduced from 2Vpp to 1.8Vpp.

In terms of full scale input, the fast OVR threshold can be calculated as: 20*log(<FOVR Threshold>/255).



ANALOG INPUT DRIVING CIRCUIT

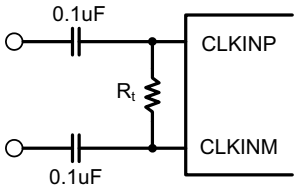
For maximum SFDR performance it is recommended to place a 5Ω resistor in series with the inputs and a 2pF shunt capacitor at the analog inputs. This circuit helps absorb some of the residual sampling glitches and improves HD2 and HD3 performance over a very wide input frequency range.



PRODUCT PREVIEW

CLOCK INPUTS

The ADS42LB49/69 clock input can be driven differentially with a sine wave, LVPECL or LVDS source with little or no difference in performance. The common mode voltage of the clock input is set to 1.4V using internal 5kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close as possible to the clock inputs in order to minimize signal reflections and jitter degradation.



CLOCK INPUTS

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 96dB for a 16bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantization\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{ThermalNoise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation due to sample clock jitter can be calculated as following:

$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{in} \times T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has three components – the internal aperture jitter (85fs for ADS42JB49/69) which is set by the noise of the clock input buffer, the external clock jitter and the jitter from the analog input signal. It can be calculated as following:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2 + (T_{Jitter,Analog\_input})^2} \quad (3)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter.

The ADS42LB49/69 has a thermal noise of 74.1dBFS and internal aperture jitter of 85fs. The SNR depending on amount of external jitter for different input frequencies is shown in Figure 16.

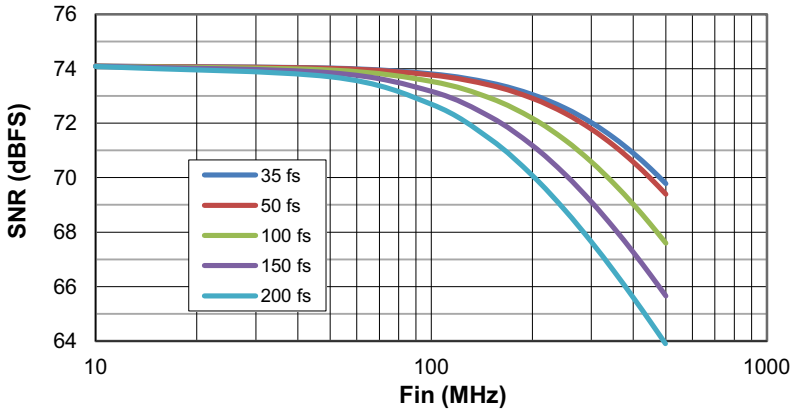


Figure 16. SNR vs Input Frequency and External Clock Jitter

INPUT CLOCK DIVIDER

The ADS42LB49/69 is equipped with an internal divider on the clock input. This allows operation with a faster input clock simplifying the system clock distribution design. The clock divider can be bypassed (/1) for operation with a 250MHz clock while /2 option supports a maximum input clock of 500MHz and the /4 option a maximum input clock frequency of 1GHz.

POWER DOWN CONTROL

The power down functions of the ADS42LB49/69 can be controlled either through the parallel control pins (CTRL1&2) or through a SPI register setting.

Table 2. Power Down Control

CTRL1	CTRL2	DESCRIPTION
Low	Low	Normal operation
High	Low	ChA powered down
Low	High	ChB powered down
High	High	Global power don

PACKAGING INFORMATION

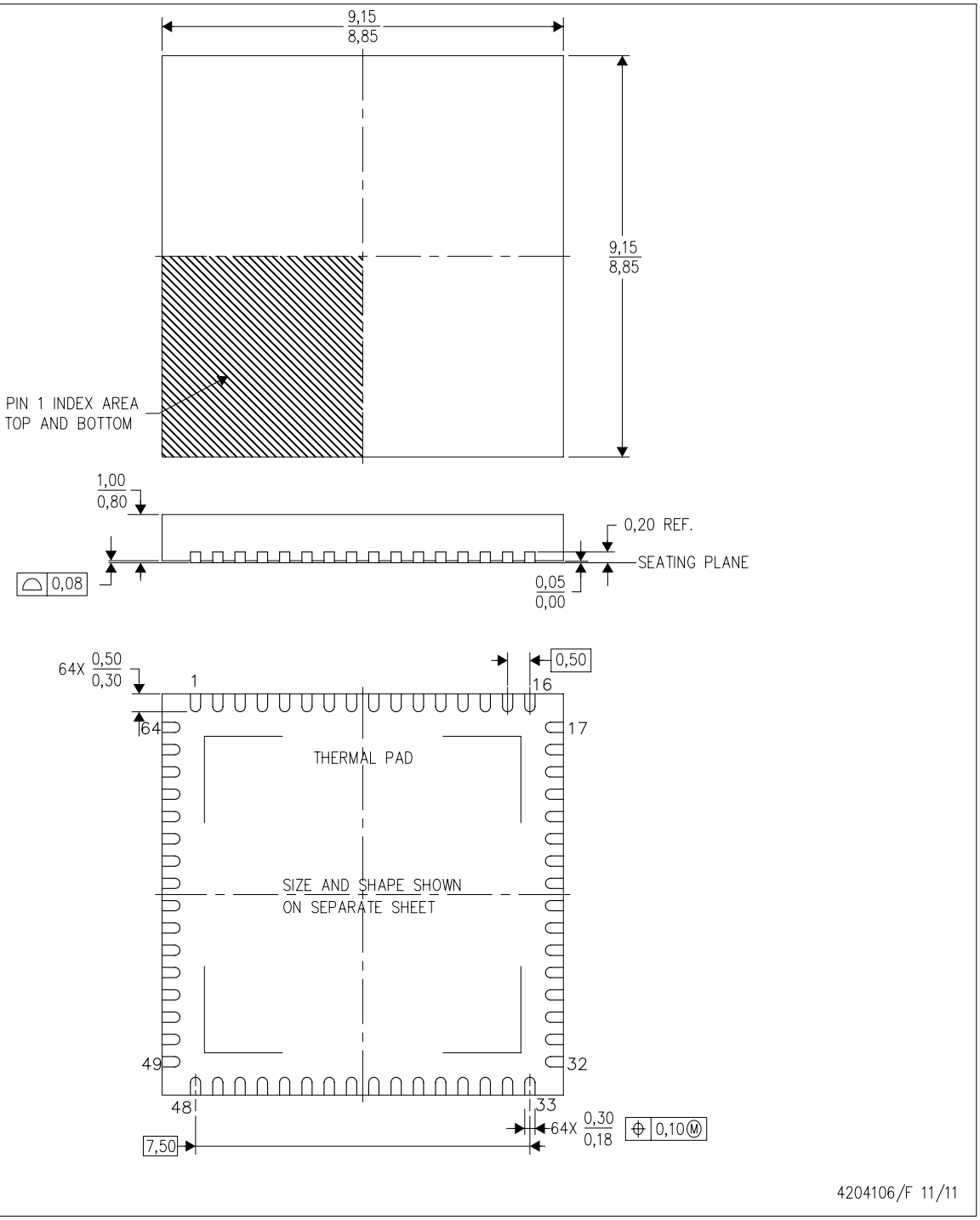
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS42LB49IRGCR	PREVIEW	VQFN	RGC	64		TBD	Call TI	Call TI	
ADS42LB49IRGCT	PREVIEW	VQFN	RGC	64		TBD	Call TI	Call TI	
ADS42LB69IRGCR	PREVIEW	VQFN	RGC	64		TBD	Call TI	Call TI	
ADS42LB69IRGCT	PREVIEW	VQFN	RGC	64		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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