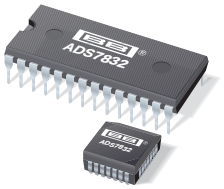
BURR - BROWN®



ADS7832

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

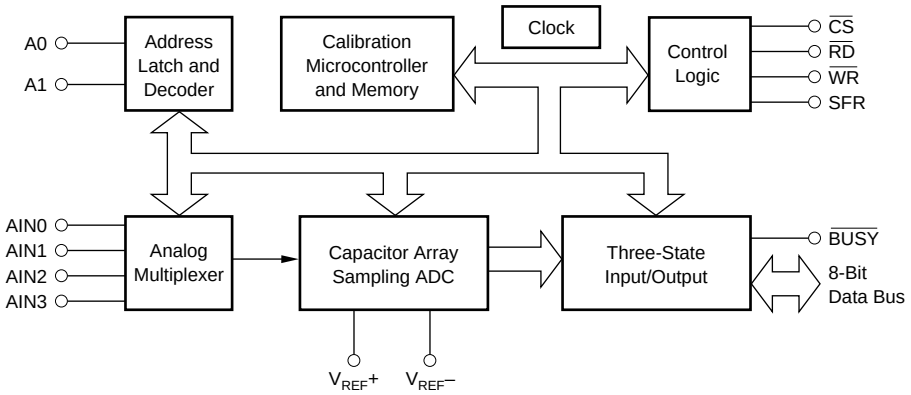
FEATURES

- **PIN COMPATIBLE TO ADC7802 AND ADS7803**
- **SINGLE SUPPLY: +5V OR +3.3V**
- **LOW POWER: 14mW plus Power Down**
- **SIGNAL-TO-(NOISE + DISTORTION) RATIO OVER TEMPERATURE:**
  69dB min with f_{IN} = 1kHz
  66dB min with f_{IN} = 50kHz
- **FAST CONVERSION TIME: 8.5µs Including Acquisition (117kHz Sampling Rate)**
- **FOUR-CHANNEL INPUT MULTIPLEXER**
- **AUTOCAL: No offset or Gain Adjust Required**

DESCRIPTION

The ADS7832 is a monolithic CMOS 12-bit analog-to-digital converter with internal sample/hold and four-channel multiplexer. It is designed and tested for full dynamic performance with input signals to 50kHz. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADS7832 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



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PDS-1332B
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SBAS051

SPECIFICATIONS

ADS7832 Electrical Specifications with 3.3V Supply

$V_A = V_D = V_{REF}+ = 3.3V \pm 10\%$; $V_{REF}– = AGND = DGND = 0V$; CLK = 1MHz external, $T_A = –40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7832BP/ADS7832BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT	$V_A = V_D = V_{REF+} = 3.0V$				
Voltage Input Range		0		V_{REF+}	V
Input Capacitance			40		pF
On State Bias Current				100	nA
Off State Bias Current	$T_A = +25°C$			10	nA
	$T_A = –40°C$ to $+85°C$			100	nA
On Resistance Multiplexer			400		Ω
Off Resistance Multiplexer			10		MΩ
Channel Separation	$F_{IN} = 1kHz$, $V_{REF}+ = 3.0V$		0.5		LSB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$			V_A		V
$V_{REF}–$			0		V
For Derated Performance[2]: $V_{REF}+$	$(V_{REF}+) – (V_{REF}–) \geq 2.5V$	2.5		V_A	V
$V_{REF}–$		0		0.5	V
Input Reference Current			100	200	µA
THROUGHPUT SPEED					
Conversion Time With External Clock (Including Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz			17	µs
	CLK = 500kHz			34	µs
With Internal Clock Using Recommended Clock Components	$T_A = +25°C$		30		µs
	$T_A = –40°C$ to $+85°C$		30		µs
Slew Rate			2		V/µs
Multiplexer Settling Time to 1/2 LSB			0.5		µs
Multiplexer Access Time			20		ns
SAMPLING DYNAMICS					
Full Power Bandwidth	–3dB		2		MHz
Aperture Jitter					ps
Aperture Delay	SRF D2 LOW[3]		5		µs
	SFR D2 HIGH		5		ns
DC ACCURACY					
Integral Nonlinearity, All Channels	SFR D2 LOW			±0.75	LSB[4]
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±0.5		LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±0.6		LSB
Differential Nonlinearity				±0.75	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±0.5	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels				
	SFR D2 LOW			±0.75	LSB
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±1		LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±4		LSB
Offset Error Drift	Between Calibration Cycles				
	SFR D2 LOW		±0.2		ppm/°C
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±0.5		ppm/°C
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±1		ppm/°C
Channel-to-Channel Mismatch	SFR D2 LOW		±0.25		LSB
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±0.5		LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±1		LSB
Power Supply Sensitivity	$V_D = V_A = +3.3V \pm 10\%$ (without recalibration)		±0.125		LSB
AC ACCURACY					
Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 1kHz$	69	71		dB[1]
	$f_{IN} = 50kHz$	66	69		dB
Total Harmonic Distortion	$f_{IN} = 50kHz$		–75		dB
Signal-to-Noise Ratio	$f_{IN} = 50kHz$		70		dB
Spurious Free Dynamic Range	$f_{IN} = 1kHz$		85		dB
	$f_{IN} = 50kHz$		82		dB

SPECIFICATIONS (CONT)

ADS7832 Electrical Specifications with 3.3V Supply

$V_A = V_D = V_{REF}+ = 3.3V \pm 10\%$; $V_{REF}- = AGND = DGND = 0V$; CLK = 1MHz external, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7832BP/ADS7832BN MIN	TYP	MAX	UNITS
DIGITAL INPUTS					
Voltage Levels: V_{IL}		–0.3		+0.8	V
V_{IH}		0.7 • V_D		V_D +0.3V	V
Current Levels: I_{IL}	CAL (Internal Pull-Up)		10		µA
I_{IL}	All Other Inputs			±10	µA
I_{IH}	SFR (Internal Pull-Down)		90		µA
I_{IH}	CLK			1.5	mA
I_{IH}	All Other Inputs			±10	µA
I_{IH}	Power Down Mode (SFR D3 HIGH)			±100	nA
DIGITAL OUTPUTS					
Data Format			Parallel 12 Bits in Two Bytes		
Data Coding			Straight Binary		
V_{OL}	I_{SINK} = 1.6mA			0.2 • V_D	V
V_{OH}	I_{SOURCE} = 200µA	0.8 • V_D			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_D			±1	µA
Output Capacitance	High-Z State		4		pF
CALIBRATION TIMING					
Calibration Cycle	Power On or Power Failure			37393	Clock Cycles
Calibration Cycle	During Normal Operation			4625	Clock Cycles
DIGITAL TIMING					
Bus Access Time				83	ns
Bus Relinquish Time				83	ns
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A	Tested at 3.0V	3	3.3		V
V_D	Tested at 3.0V	3	3.3		V
Supply Current: I_A			2.5	3	mA
I_D			300	500	µA
Power Dissipation	Power Up Mode or During Conversion		7.5		mW
	Power Down Mode, No Clock Running		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

* These specifications need to be added based on performance of final silicon.

NOTES: (1) All specifications in dB are referred to a full-scale input range. (2) Over this range, total error will typically not exceed ±1LSB. (3) In this mode, the ADS7832 acquires the input signal for five clock cycles after a start command, before the input is held and conversion begins. (4) LSB means Least Significant Bit. For a 0V to 5V input range, one LSB is 1.22mV. For a 0V to 2.5V input range, one LSB is 610µV.

SPECIFICATIONS

ADS7832 Electrical Specifications with 5V Supply

V_A = V_D = 5V ±10%; V_{REF}+ = 5.0V; V_{REF}– = AGND = DGND = 0V; CLK = 1MHz external 50% ±2% Duty Cycle, T_A = –40°C to +85°C, after calibration at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7832BP/ADS7832BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	V_D = V_A = V_{REF}+ = 5V	0		5	V
Input Capacitance			40		pF
On State Bias Current				100	nA
Off State Bias Current	T_A = +25°C			10	nA
	T_A = –40°C to +85°C			100	nA
On Resistance Multiplexer			400		Ω
Off Resistance Multiplexer			10		MΩ
Channel Separation	F_{IN} = 1kHz, V_D = V_A = V_{REF}+ = 5V		0.5		LSB
REFERENCE INPUT					
For Specified Performance:	V_{REF} = V_A = 5V				
V_{REF}+			V_A		V
V_{REF}–			0		V
For Derated Performance[2]:	(V_{REF}+) – (V_{REF}–) ≥ 2.5V				
V_{REF}+		2.5		V_A	V
V_{REF}–		0		1	V
Input Reference Current			100	200	µA
THROUGHPUT SPEED					
Conversion Time With External Clock (Including	CLK = 2MHz			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz			17	µs
	CLK = 500kHz			34	µs
With Internal Clock Using Recommended	T_A = +25°C		30		µs
Clock Components	T_A = –40°C to +85°C		30		µs
Slew Rate		2			mV/µs
Multiplexer Settling Time to 1/2 LSB			0.5		µs
Multiplexer Access Time			20		ns
SAMPLING DYNAMICS					
Full Power Bandwidth	–3dB		4		MHz
Aperture Jitter			10		ps
Aperture Delay	SRF D2 LOW[3]		2.5		µs
	SFR D2 HIGH		5		ns
DC ACCURACY					
Integral Nonlinearity, All Channels	SFR D2 LOW			±0.75	LSB[4]
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±0.5		LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±0.6		LSB
Differential Nonlinearity				±0.75	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±0.50	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels				
	SFR D2 LOW			±0.75	LSB
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±1		LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±4		LSB
Offset Error Drift	Between Calibration Cycles				
	SFR D2 LOW		±0.2		ppm/°C
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±0.5		ppm/°C
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±1		ppm/°C
Channel-to-Channel Mismatch	SFR D2 LOW		±0.25		LSB
	SFR D2 HIGH, Internal Clock or Sampling Command Synchronous to External Clock		±0.5		LSB
	SFR D2 HIGH, Sampling Command Asynchronous to External Clock		±1.0		LSB
Power Supply Sensitivity	V_D = V_A = +5V ±10% (without recalibration)		±0.125		LSB

SPECIFICATIONS (CONT)

ADS7832 Electrical Specifications with 5V Supply

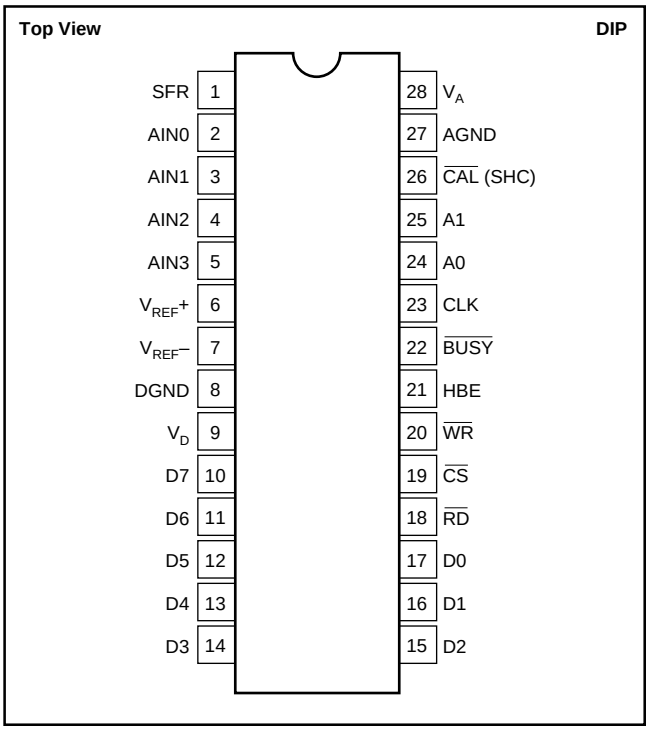
$V_A = V_D = 5V \pm 10\%$; $V_{REF}+ = 5V$; $V_{REF}- = AGND = DGND = 0V$; CLK = 1MHz external 50% ±2% Duty Cycle, $T_A = -40°C$ to $+85°C$, after calibration at any temperature, unless otherwise specified.

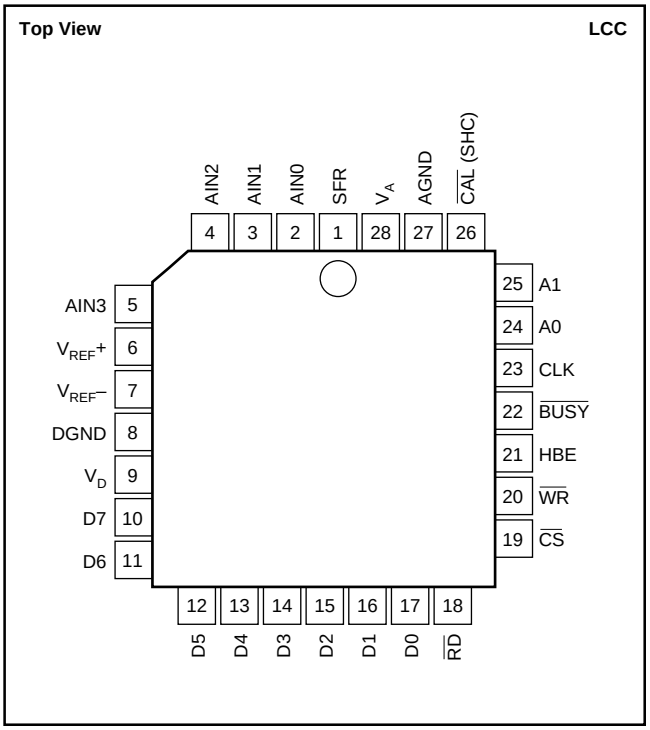
PARAMETER	CONDITIONS	ADS7832BP/ADS7832BN MIN	TYP	MAX	UNITS
AC ACCURACY					
Signal-to-(Noise + Distortion) Ratio	f_{IN} = 1kHz	69	71		dB(1)
	f_{IN} = 50kHz	66	69		dB
Total Harmonic Distortion	f_{IN} = 50kHz		–75		dB
Signal-to-Noise Ratio	f_{IN} = 50kHz		70		dB
Spurious Free Dynamic Range	f_{IN} = 1kHz		85		dB
	f_{IN} = 50kHz		82		dB
DIGITAL INPUTS					
Voltage Levels: V_{IL}	CLK	–0.3		0.8	V
V_{IH}	CLK	3.5		V_D +0.3V	V
V_{IL}	All Others	–0.3		0.8	V
V_{IH}	All Others	2.4		V_D +0.3V	V
Current Levels: I_{IL}	CAL (Internal Pull-Up)		10		µA
I_{IL}	All Other Inputs			±10	µA
I_{IH}	SFR (Internal Pull-Down)		90		µA
I_{IH}	CLK			1.5	mA
I_{IH}	All Other Inputs			±10	µA
I_{IH}	Power Down Mode (SFR D3 HIGH)			±100	nA
DIGITAL OUTPUTS					
Data Format	Parallel 12 Bits in Two Bytes				
Data Coding	Straight Binary				
V_{OL}	I_{SINK} = 1.6mA			0.4	V
V_{OH}	I_{SOURCE} = 200µA	4			V
Leakage Current	High-Z State			±1	µA
Output Capacitance	High-Z State		4		pF
CALIBRATION TIMING					
Calibration Cycle	Power On or Power Failure			37393	Clock Cycles
Calibration Cycle	During Normal Operation			4625	Clock Cycles
DIGITAL TIMING					
Bus Access Time				83	ns
Bus Relinquish Time				83	ns
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A	Tested at 5.5V		5	5.5	V
V_D	Tested at 5.5V		5	5.5	V
Supply Current: I_A	Tested at 5.5V		2.5	5.5	mA
I_D	Tested at 5.5V		300	500	µA
Power Dissipation	Power Up Mode or During Conversion		14		mW
	Power Down Mode, No Clock Running		50		µW
TEMPERATURE RANGE					
Specification		–40		85	°C
Storage		–65		150	°C

*These specifications need to be added based on performance of final silicon.

NOTES: (1) All specifications in dB are referred to a full-scale input range. (2) Over this range, total error will typically not exceed ±1LSB. (3) In this mode, the ADS7832 acquires the input signal for five clock cycles after a start command, before the input is held and conversion begins. (4) LSB means Least Significant Bit. For a 0V to 5V input range, one LSB is 1.22mV. For a 0V to 2.5V input range, one LSB is 610µV.

PIN CONFIGURATIONS





PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO, dB	INTEGRAL NONLINEARITY MAXIMUM LSB	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7832BN	69	±3/4	–40°C to +85°C	28-Pin LCC	251
ADS7832BP	69	±3/4	–40°C to +85°C	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground 7V
V_D to Digital Ground 7V
V_A to V_D ..... ±0.3V
Analog Ground to Digital Ground ..... ±0.3V
Control Inputs to Digital Ground ..... –0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground ..... –0.3V to V_A + 0.3V
Maximum Junction Temperature ..... 150°C
Internal Power Dissipation 875mW
Lead Temperature (soldering, 10s) ..... +260°C
(soldering, 3s) ..... +360°C
Thermal Resistance, θ_{JA} ..... 75°C/W
Maximum Input Current to Any Pin ..... ±50mA
ESD: Human Body Model 1kV

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	V_{REF}+	Positive voltage reference input. Must be ≤ (V_A + 0.3V).
7	V_{REF}–	Negative voltage reference input.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. Must be ≤ (V_A + 0.3V) and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$).
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal or external clock operation. For external clock operation, connect to a 74HC-compatible clock source. For internal clock operation, connect per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 A0 Selected Channel LOW LOW AIN0 LOW HIGH AIN1 HIGH LOW AIN2 HIGH HIGH AIN3
26	$\overline{CAL}$ (SHC)	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. If D2 of the SFR is programmed HIGH, pin 26 will be an input to control the sample-to-hold timing. A rising edge on pin 26 will switch from sample-mode to hold-mode and initiate a conversion. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. Must be ≥ (V_D – 0.3V) and ((V_{REF} +) – 0.3V)

THEORY OF OPERATION

ADS7832 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by an on-chip microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADS7832 to most micro-controllers, microprocessors or digital storage systems.

The on-chip sampling provides excellent dynamic performance for input signals to 50kHz, and has a full-power –3dB bandwidth of 4MHz. Full control over sample-to-hold timing is available for applications where this is critical.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW, with a 50µW power down option.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADS7832 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles. The successive

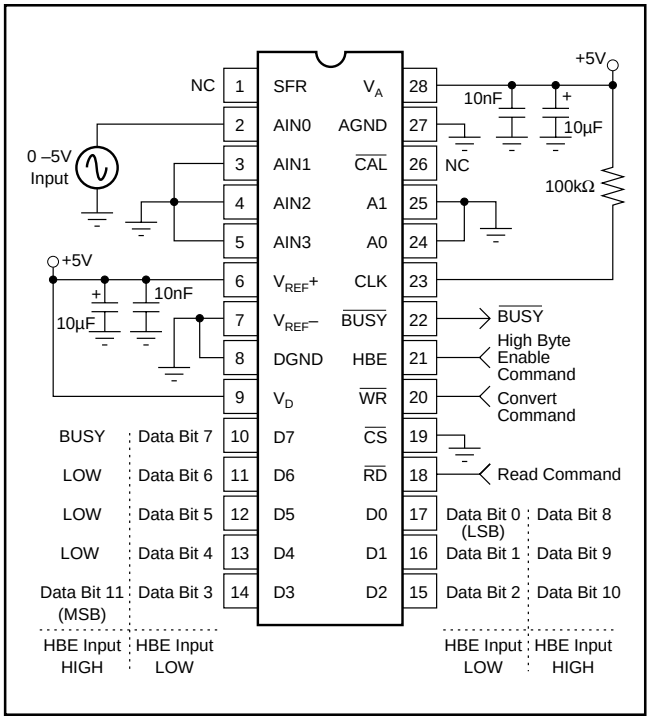


FIGURE 1. Basic Operation.

approximation conversion takes place during clock cycles 6 through 17.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

A conversion can also be initiated by a rising edge on pin 26, if a HIGH has been written to D2 of the Special Function Register, as discussed below.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 4608 clock cycles, and a normal conversion (17 clock cycles) is added automatically. Thus, at the end of a calibration cycle, there is valid conversion data in the output registers. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages have settled and are stable, an internal timer provides a waiting period of 37,393 clock cycles between power-up/power-failure and the start of the calibration cycle.

READING DATA

Data from the ADS7832 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in

straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

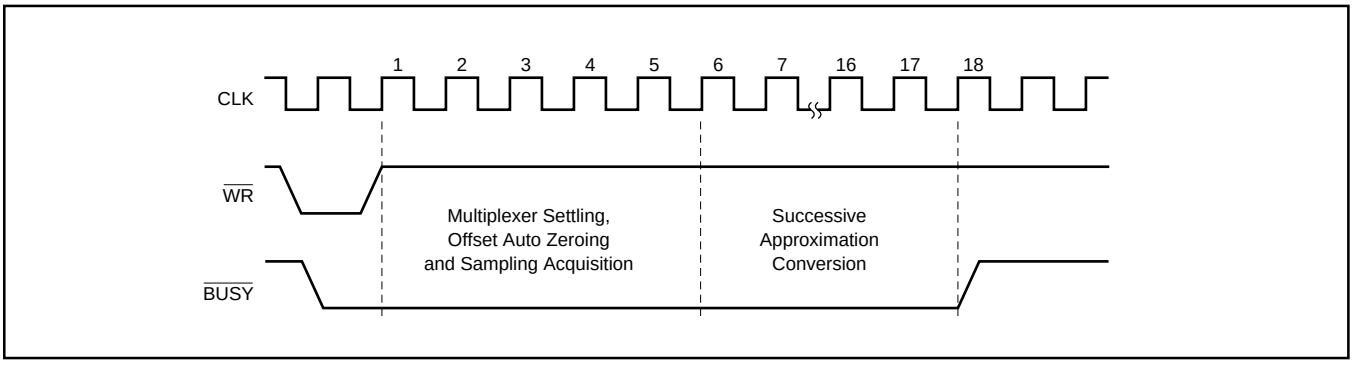


FIGURE 2. Converter Timing.

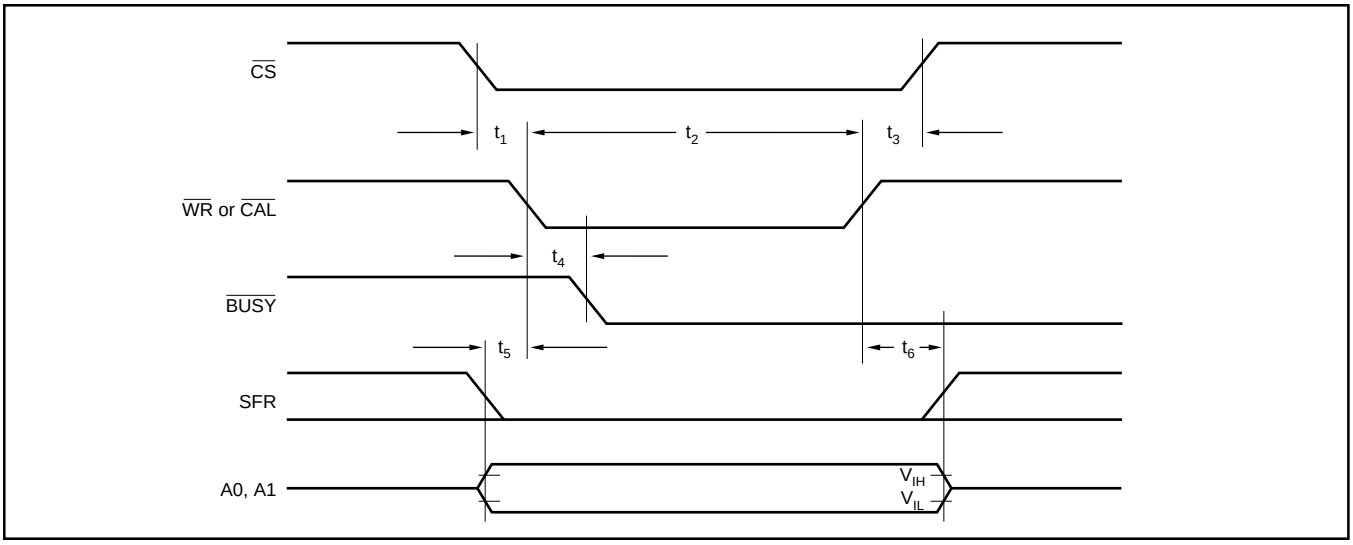


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

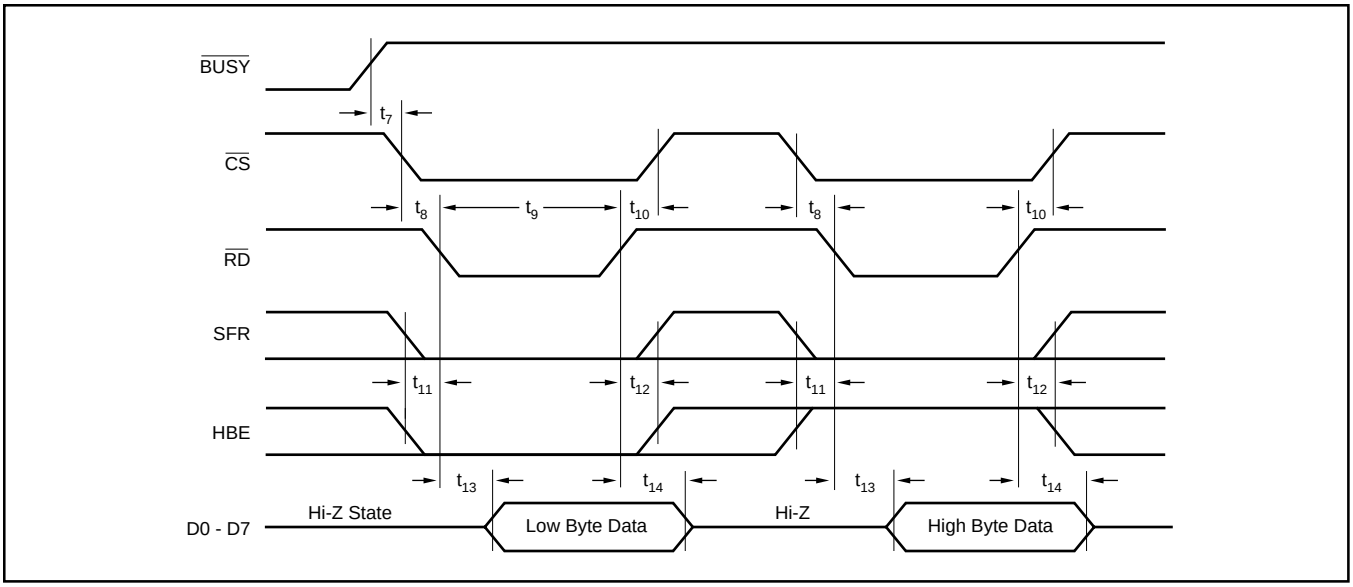


FIGURE 4. Read Cycle Timing.

ADS7832 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

TRANSPARENT MODE

This is the default mode for ADS7832. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after BUSY has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 9 show the digital timing of ADS7832 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADS7832, or to write additional instructions to the converter.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH.) The Power Fail flag in the SFR is set when the power supply falls below about 2.7V. The flag also means that a new calibration has been started,

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, latched Output Mode enabled.
D1	$\overline{CAL}$ Flag	If HIGH, calibration cycle in progress.
D2	Pin 26 Status	If LOW, pin 26 used as input to initiate calibration cycle. If HIGH, pin 26 used as input to control sample-to-hold timing.
D3	Power Down Status	If HIGH, in Power Down Mode (Power Down Mode is the default condition).
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred (supply fell below 2.7V). Always write as LOW.
D6	$\overline{CAL}$ ERROR Flag	If HIGH, an overflow occurred during calibration.
D7	$\overline{BUSY}$ Flag	If HIGH, conversion or calibration in progress.

NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.

TABLE II. Reading the Special Function Register.

SYMBOL	PARAMETER[1]	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time[2]	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time[2]	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time[2]	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time[2]	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time)[3]		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time)[3]		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR[3]	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns
t_{18}	Acquisition Time. Pin 26 LOW with D2 in SFR HIGH	2.5			µs
t_{19}	Sample-to-Hold Aperture Delay. (D2 in SFR HIGH)		5		ns
t_{20}	Delay from rising edge on pin 26 to start of conversion. (D2 in SFR HIGH)			1.5	CLK cycles

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 8 and 9 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 2MHz external, T_A = –40°C to +85°C).

and any data written to the SFR has been lost. Thus, the ADS7832 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) Note that writing to the SFR also initiates a new conversion.

POWER DOWN MODE

Writing a HIGH to D3 in the SFR puts the ADS7832 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. The internal clock and analog circuitry are turned off, although the output registers and SFR can still be accessed normally. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. Note that if the power supply falls below 3V and then recovers, a calibration is automatically initiated, and the SFR will be reset. D3 will be HIGH, and the ADS7832 will be in the Power Down Mode.

During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7832 will revert to power down. Also, writing to D1 and D3 in the SFR will initiate a calibration, do a single conversion and revert to the Power Down Mode, in 4,625 clock cycles. Accurate conversion results will be available in the output registers.

The activation delay from power down to normal operation is included in the sampling time. No extra time is required, either when coming out of the Power Down Mode or when making a single conversion in the Power Down Mode.

SAMPLE/HOLD CONTROL MODE

With D2 in the SFR HIGH, a rising edge input on pin 26 will switch the ADS7832 from sample-mode to hold-mode with a 5ns aperture delay. This also initiates a conversion, which will start within 1.5 CLK cycles.

This mode allows full control over the sample-to-hold timing, which is especially useful where external events trigger sampling timing.

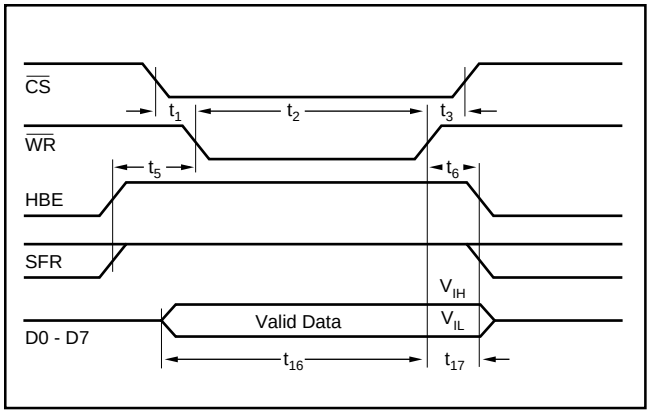


FIGURE 5. Writing to the SFR.

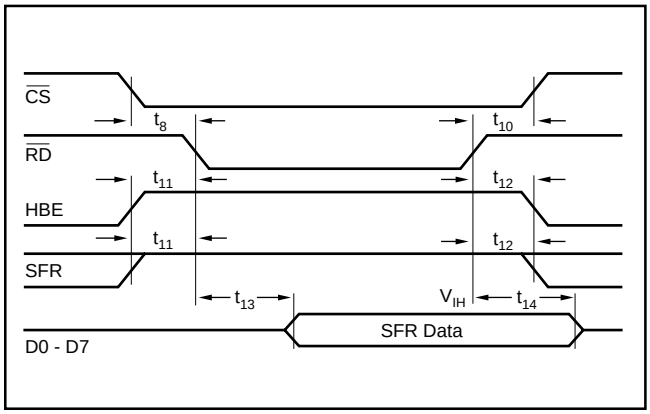


FIGURE 6. Reading the FSR.

In the Sample/Hold Control Mode, pin 26 must be held LOW a minimum of 2.5µs between conversions to allow accurate acquisition of input signals. Also, offset error will increase in this mode, since auto-zeroing of the comparator is not synchronized to the sampling. Minimum offset is achieved by synchronizing the sampling signal to CLK, whether internal or external. Ideally, the sampling signal rising edge should be delayed 20ns from the falling edge of CLK. This will keep offset error to about 1LSB.

In the Sample/Hold Control Mode, a LOW pulse on $\overline{WR}$ (with $\overline{CS}$ LOW) will not initiate a conversion, but the rising edge will latch the multiplexer channel according to the inputs on A0 and A1. When changing channels, this must be done at least 2.5µs before pin 26 goes HIGH (to start a conversion.)

OPERATION	$\overline{CS}$/$\overline{WR}$	SFR/HBE	D0	D1	D2	D3	D5	D4/D6/D7
Enables Transparent Mode for Data Latches	LOW	HIGH	LOW	X	X	X	X	LOW
Enables Latched Output Mode for Data Latches	LOW	HIGH	HIGH(1)	X	X	X	X	LOW
Initiates Calibration Cycle	LOW	HIGH	X	HIGH	X	X	X	LOW
Activates Sample/Hold Control Mode	LOW	HIGH	X	X	HIGH(1)	X	X	LOW
Activates Power Down Mode(2)	LOW	HIGH	X	X	X	HIGH(1)	X	LOW
Resets Power Fail Flag	LOW	HIGH	X	X	X	X	LOW	LOW

NOTES: (1) Writing a LOW here reactivates the standard mode of operation. (2) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADS7832 will revert to power down. (3) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.

TABLE III. Writing to the Special Function Register.

CONTROL LINES

Table IV shows the functions of the various control lines on the ADS7832. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

INSTALLATION

INPUT IMPEDANCE

ADS7832 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

In many applications, a simple passive low-pass filter as shown in Figure 10a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 10a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 10b should be used.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADS7832, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}-$ to insure low source impedance. These capacitors should be located as close as possible to the ADS7832 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+$ = 5V and $V_{REF}-$ = 0V, the converter can function with $V_{REF}+$ as low as 4.5V and $V_{REF}-$ as high as 1V.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle. (See SFR section for alternate use as Sample/Hold Control Mode input.)
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

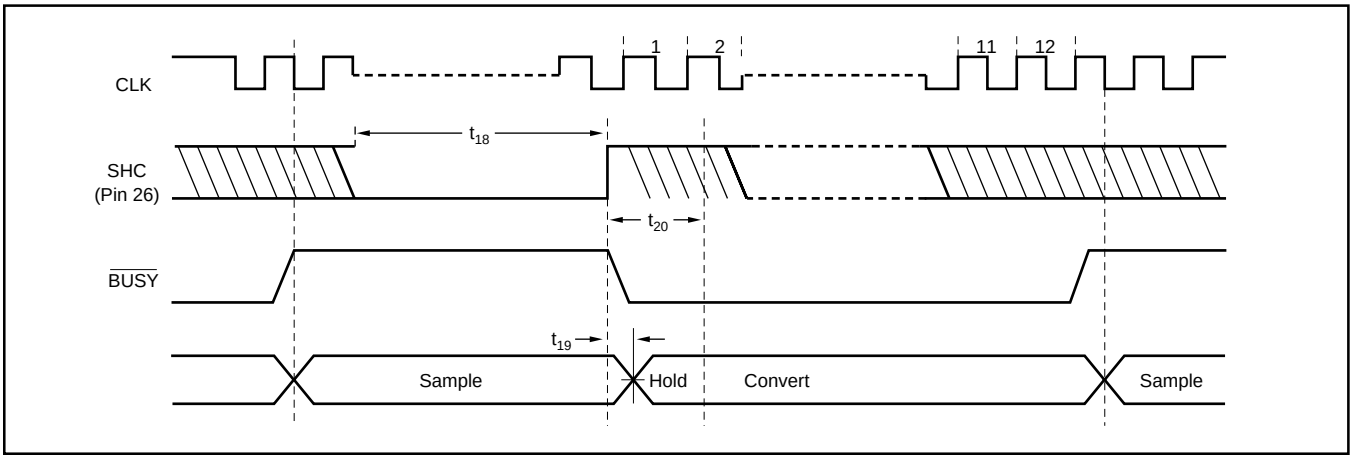


FIGURE 7. Timing for Initiating Conversion in Sample/Hold Control Mode (D2 in SFR HIGH).

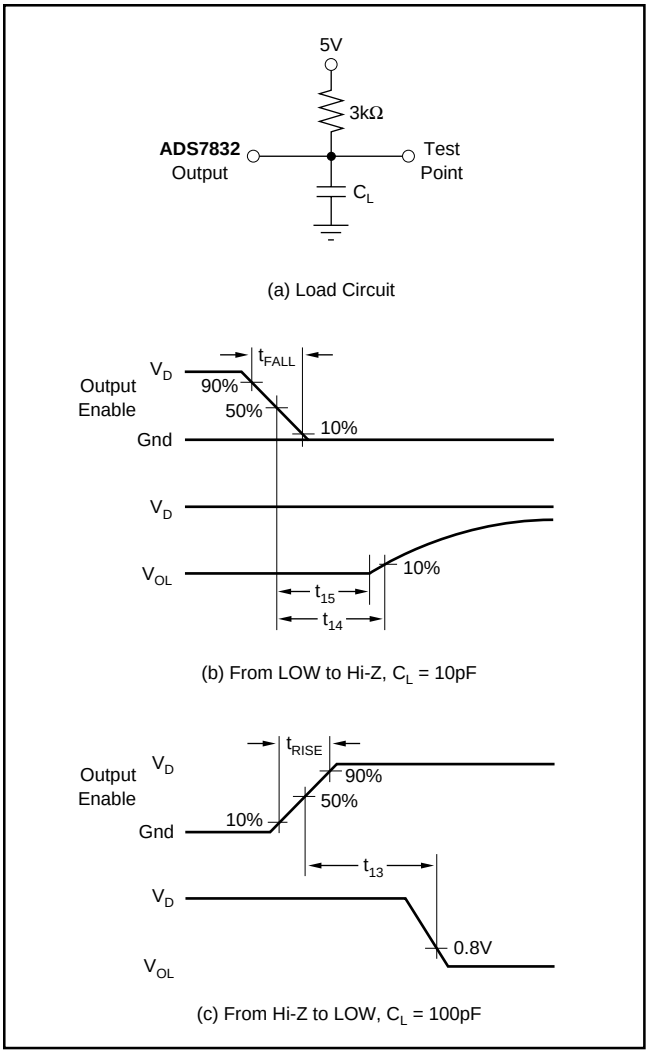


FIGURE 8. Measuring Active LOW to/from Hi-Z State.

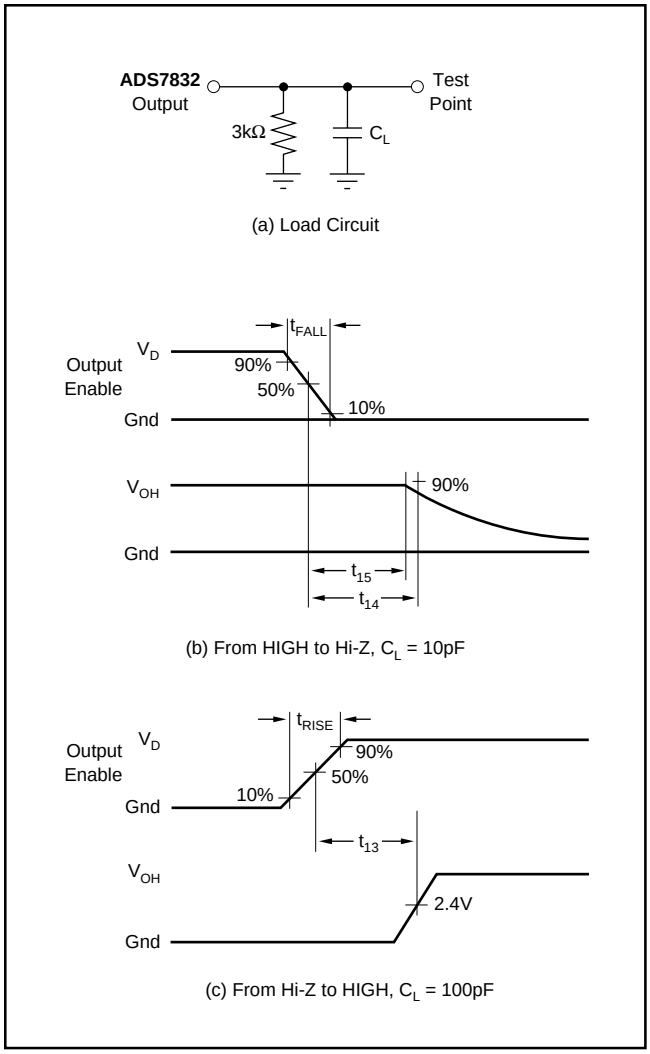


FIGURE 9. Measuring Active HIGH to/from Hi-Z State.

As long as there is at least a 4.5V difference between V_{REF}+ and V_{REF}–, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB

The power supply to the reference source needs to be considered during system design to prevent V_{REF}+ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 33,056 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADS7832 should be bypassed with 10µF tantalum capacitors as close to the part as possible. Although ADS7832 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 11 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADS7832 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADS7832, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The V_{REF}– pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADS7832 clock from an external source is shown in Figure 12a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The duty cycle of the external clock can vary as long as the LOW time and HIGH time are each at least 200ns wide. Synchronizing the conversion clock to an external system clock is

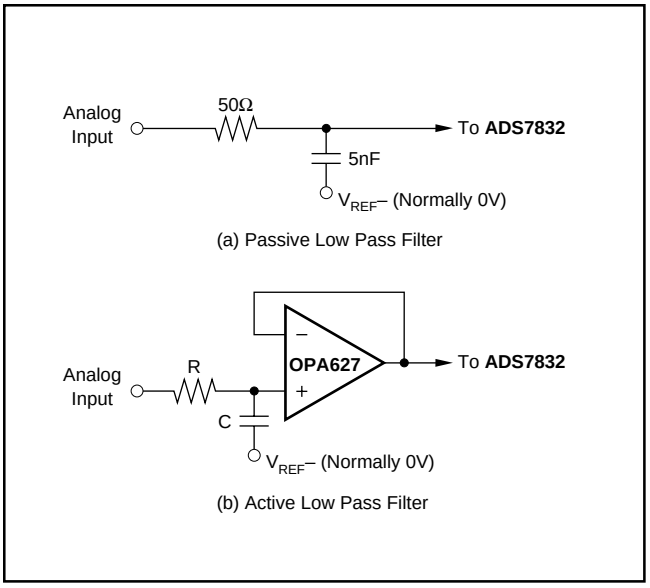


FIGURE 10. Input Signal Conditioning.

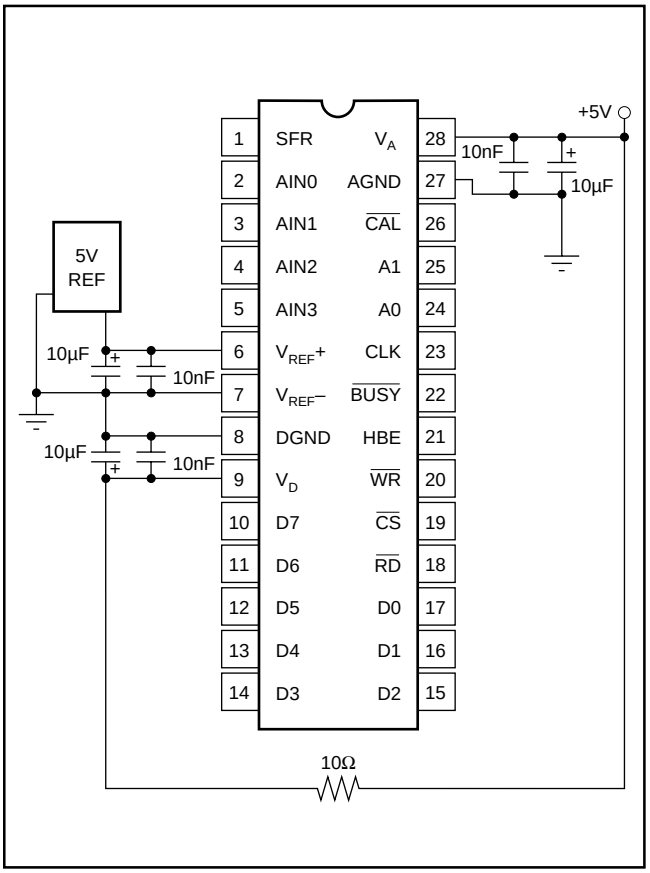


FIGURE 11. Power Supply and Reference Decoupling.

recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.4MHz.

INTERNAL CLOCK OPERATION

Figure 12b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

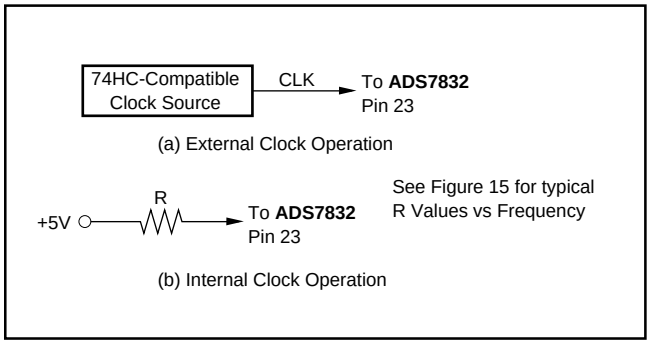


FIGURE 12. Internal Clock Operation.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 13 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADS7832, using a precision, low-cost complete difference amplifier, INA105.

Figure 14 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADS7832. The precision of this circuit will depend on the matching and tracking of the three resistors used.

To trim this circuit for full 12-bit precision, R_2 and R_3 need to be adjustable over appropriate ranges. To trim, first have the ADS7832 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R_3 until the ADS7832 output toggles between the codes FFE hex and FFF hex. This makes R_3 extremely close to R_1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R_2 until the ADS7832 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADS7832, to match the performance of the self-calibration provided by the converter.

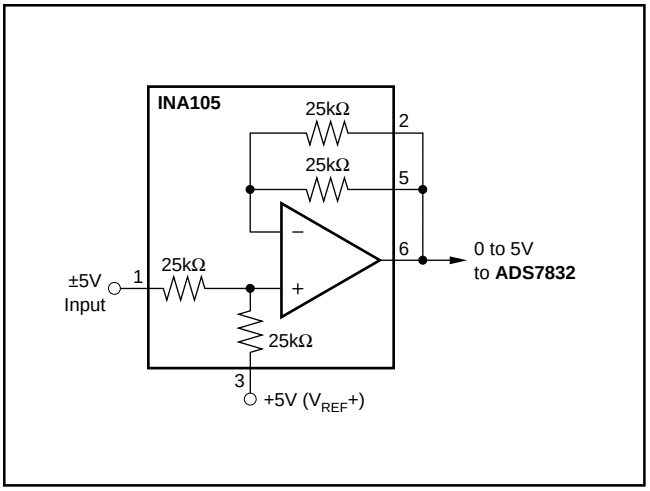


FIGURE 13. ±5V Input Range.

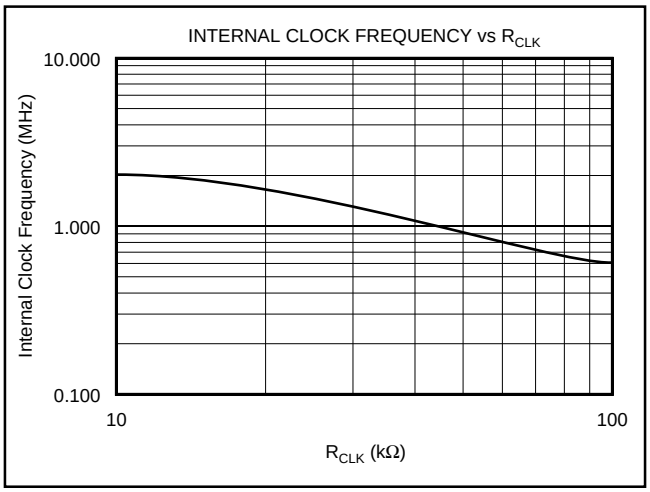


FIGURE 15. Internal Clock Frequency vs R_{CLK} Resistor Value.

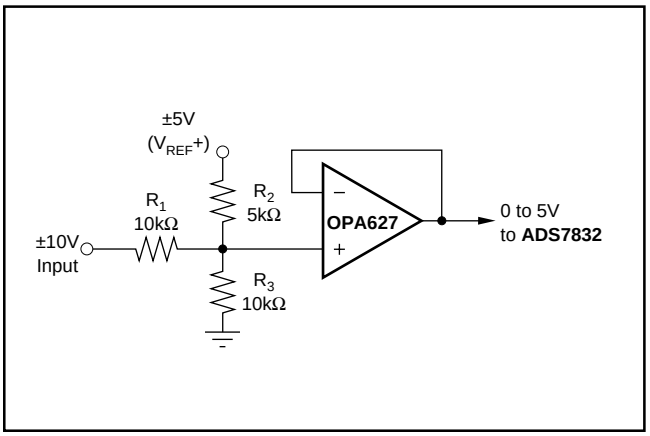


FIGURE 14. ±10V Input Range.

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