15-BIT 250-KSPS SERIAL CMOS SAMPLING ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS8509-HT

FEATURES

- **250-kHz Sampling Rate**
- **4-V, 5-V, 10-V, ±3.33-V, ±5-V, and ±10-V Input Ranges**
- **±4.5 LSB Max INL (at 175°C)**
- **±2.2 LSB Max DNL (at 175°C), 15-Bit No Missing Codes**
- **SPI Compatible Serial Output with Daisy-Chain (TAG) Feature**
- **Single 5-V Supply**
- **Pin-Compatible with ADS7809 (Low Speed) and 12-Bit ADS8508/7808**
- **Uses Internal or External Reference**
- **87-mW Typ Power Dissipation at 250 KSPS to 5 V, While the Innovative Design Allows Operation**
- **28-Pin SSOP Package**
- **Simple DSP Interface**

APPLICATIONS

- **Down-hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extreme (–40°C to 175°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

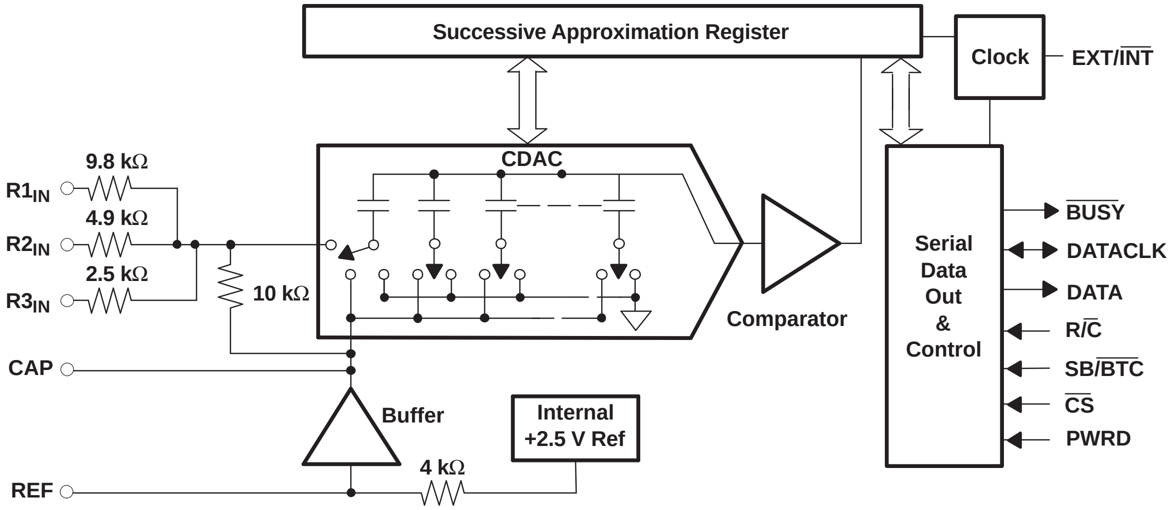
(1) Custom temperature ranges available

DESCRIPTION

The ADS8509 is a complete 15-bit sampling analog-to-digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 15-bit, capacitor-based, successive approximation register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be output using the internal clock or can be synchronized to an external data clock. The ADS8509 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS8509 is specified at a 250-kHz sampling rate over the full temperature range. Precision resistors provide various input ranges including ±10 V and 0 V to 5 V, while the innovative design allows operation from a single 5-V supply with power dissipation under 110 mW.

The ADS8509 is available in a 28-pin SSOP package and is fully specified for operation from -40°C to 175°C.


Successive Approximation Register
Clock
EXT/$\overline{INT}$
CDAC
9.8 kΩ
4.9 kΩ
2.5 kΩ
10 kΩ
$R1_{IN}$
$R2_{IN}$
$R3_{IN}$
CAP
REF
Buffer
Internal +2.5 V Ref
4 kΩ
Comparator
Serial Data Out & Control
$\overline{BUSY}$
DATACLK
DATA
R/$\overline{C}$
SB/$\overline{BTC}$
$\overline{CS}$
PWRD

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8509HDB	–40°C to 175°C	SSOP-28	DB	ADS8509HDB	Tube, 50

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Analog inputs	$R1_{IN}$	±25 V
	$R2_{IN}$	±25 V
	$R3_{IN}$	±25 V
	REF	$+V_{ANA}$ + 0.3 V to AGND2 – 0.3 V
	CAP	Indefinite short to AGND2, momentary short to V_{ANA}
Ground voltage differences	DGND, AGND2	±0.3 V
	V_{ANA}	6 V
	V_{DIG} to V_{ANA}	0.3 V
	V_{DIG}	6 V
Digital inputs		–0.3 V to $+V_{DIG}$ + 0.3 V
Maximum junction temperature		190°C
Storage temperature range		–65°C to 175°C
Internal power dissipation		700 mW
Lead temperature (soldering, 1.6 mm from case 10 seconds)		260°C

(1) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC[1]		ADS8509 DB 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	69.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	27.4	
θ_{JB}	Junction-to-board thermal resistance[4]	30.7	
ψ_{JT}	Junction-to-top characterization parameter[5]	2.7	
ψ_{JB}	Junction-to-board characterization parameter[6]	30.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

At f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference and 0.1%, 0.25-W fixed resistors (see Figure 30 and Figure 31) (unless otherwise specified)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution					16	Bits
ANALOG INPUT							
	Voltage range[(1)]						
	Impedance[(1)]						
	Capacitance				50		pF
THROUGHPUT SPEED							
	Conversion cycle		Acquire and convert			4	μs
	Throughput rate			250			kHz
DC ACCURACY							
INL	Integral linearity error			–4.5		4.5	LSB[(2)]
DNL	Differential linearity error			–2.2		2.2	LSB
	No missing codes			15			Bits
	Transition noise[(3)]				1		LSB
	Full-scale error[(4) (5)]	±10-V Range	Int. ref. with 0.1% external fixed resistors	–1.75		1.75	%FSR
		All other ranges		–1.75		1.75	
	Full-scale error drift		Int. ref.		±7		ppm/°C
	Full-scale error[(4) (5)]	±10-V Range	Ext. ref. with 0.1% external fixed resistors	-1.25		1.25	%FSR
		All other ranges			±0.75		
	Full-scale error drift		Ext. ref.		±2		ppm/°C
	Bipolar zero error[(4)]			–17		17	mV
	Bipolar zero error drift				±0.4		ppm/°C
	Unipolar zero error[(4)]	10-V Range		–11		11	mV
		4-V and 5-V Range		–5.5		5.5	
	Unipolar zero error drift				±2		ppm/°C
	Recovery to rated accuracy after power down		1-μF Capacitor to CAP		1		ms
	Power supply sensitivity (V_{DIG} = V_{ANA} = V_D)		+4.75 V < V_D < +5.25 V	–12		12	LSB
AC ACCURACY							
SFDR	Spurious-free dynamic range		f_I = 20 kHz	85	95		dB[(6)]
THD	Total harmonic distortion		f_I = 20 kHz		–92	–85	dB
SINAD	Signal-to-(noise+distortion)		f_I = 20 kHz	81	85		dB
			–60-dB Input		30		dB
SNR	Signal-to-noise ratio		f_I = 20 kHz	81	86		dB
	Full-power bandwidth[(7)]				500		kHz
SAMPLING DYNAMICS							
	Aperture delay				5		ns
	Transient response		FS Step			2	μs
	Overvoltage recovery[(8)]				150		ns
REFERENCE							
	Internal reference voltage		No load	2.455	2.5	2.545	V

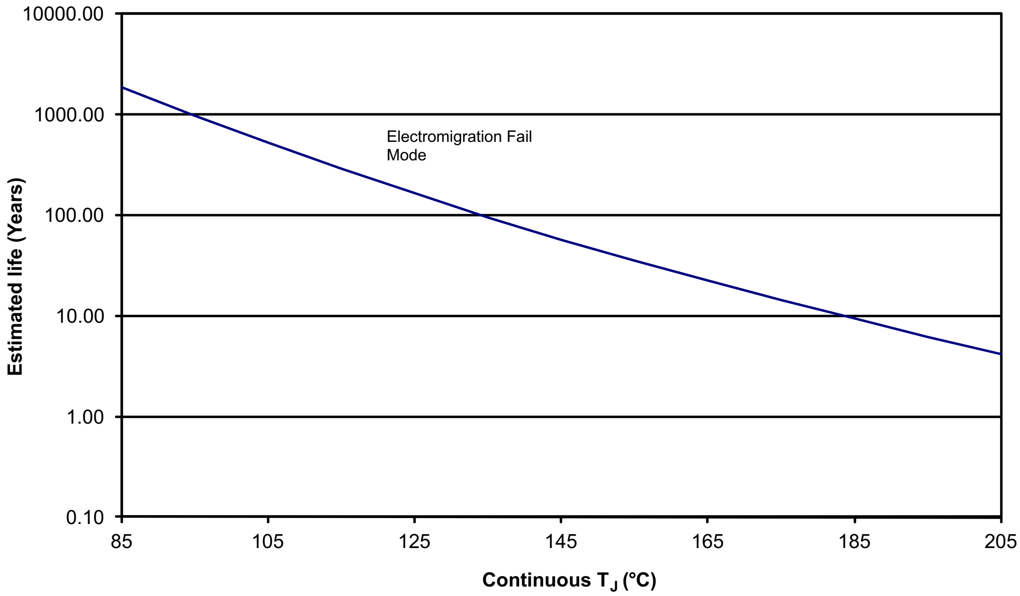
(1) ±10 V, 0 V to 5 V, etc. (see Table 2). For normal operation, the analog input should not exceed configured range ±20%.
(2) LSB means least significant bit. For the ±10-V input range, one LSB is 305 μV.
(3) Typical rms noise at worst case transitions and temperatures.
(4) As measured with fixed resistors shown in Figure 30 and Figure 31. Adjustable to zero with external potentiometer. Factory calibrated with 0.1%, 0.25-W resistors.
(5) For bipolar input ranges, full-scale error is the worst case of –full-scale or +full-scale uncalibrated deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.
(6) All specifications in dB are referred to a full-scale ±10-V input.
(7) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

At f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference and 0.1%, 0.25-W fixed resistors (see Figure 30 and Figure 31) (unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal reference source current (must use external buffer)			1		µA
	Internal reference drift			8		ppm/°C
	External reference voltage range for specified linearity		2.2	2.5	2.75	V
	External reference current drain	Ext. 2.5-V ref.			100	µA
DIGITAL INPUTS						
	Logic levels					
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{IH}	High-level input voltage		2		V_{DIG} +0.3 V	V
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{IH}	High-level input current	V_{IH} = 5 V			±10	µA
DIGITAL OUTPUTS						
	Data format (serial 16-bits)					
	Data coding (binary 2's complement or straight binary)					
	Pipeline delay (conversion results only available after completed conversion)					
	Data clock (selectable for internal or external data clock)					
	Internal clock (output only when transmitting data)	EXT/$\overline{INT}$ Low		9		MHz
	External clock (can run continually but not recommended for optimum performance)	EXT/$\overline{INT}$ High	0.1		26	MHz
V_{OL}	Low-level output voltage	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	4			V
	Leakage current	Hi-Z State, V_{OUT} = 0 V to V_{DIG}			±5	µA
	Output capacitance	Hi-Z State			15	pF
POWER SUPPLIES						
V_{DIG}	Digital input voltage	Must be ≤ V_{ANA}	4.75	5	5.25	V
V_{ANA}	Analog input voltage		4.75	5	5.25	V
I_{DIG}	Digital input current			4		mA
I_{ANA}	Analog input current			10		mA
POWER DISSIPATION						
	PWRD Low	f_S = 250 kHz		87	110	mW
	PWRD High			50		µW
TEMPERATURE RANGE						
	Specified Junction Temperature Range[9]		–40		175	°C
	Storage		–65		175	°C

(9) The internal reference may not be started correctly beyond the industrial temperature range (–40°C to 85°C), therefore use of an external reference is recommended.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

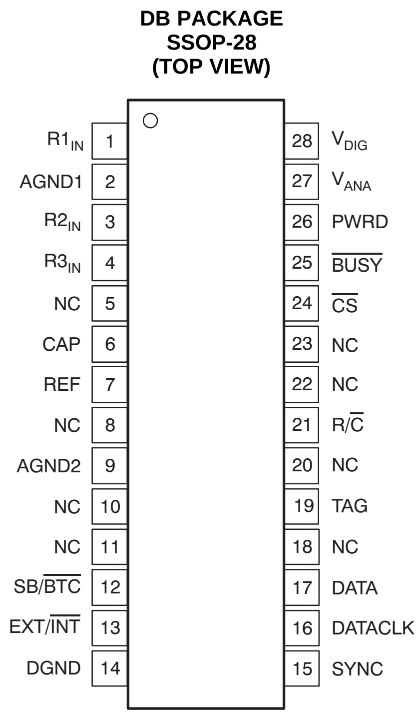
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

(4) This device is qualified for 1000 hours of continuous operation at maximum rated temperature.

Figure 1. ADS8509-HT Operating Life Derating Chart

PIN CONFIGURATIONS



Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
AGND1	2	–	Analog ground. Used internally as ground reference point. Minimal current flow.
AGND2	9	–	Analog ground
BUSY	25	O	Busy output. Falls when a conversion is started and remains low until the conversion is completed and the data is latched into the output shift register.
CAP	6	–	Reference buffer capacitor. 2.2-µF Tantalum to ground.
$\overline{CS}$	24	–	Chip select. Internally ORed with R/$\overline{C}$.
DATA	17	O	Serial data output. Data is synchronized to DATACLK with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16 bits of data, the ADS8509 outputs the level input on TAG as long as $\overline{CS}$ is low and R/$\overline{C}$ is high (see Figure 9 and Figure 10). If EXT/$\overline{INT}$ is low, data is valid on both the rising and falling edges of DATACLK, and between conversions DATA stays at the level of the TAG input when the conversion was started.
DATACLK	16	I/O	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data is synchronized to this clock. If EXT/$\overline{INT}$ is low, DATACLK transmits 16 pulses after each conversion and then remains low between conversions.
DGND	14	–	Digital ground
EXT/$\overline{INT}$	13	–	Selects external or internal clock for transmitting data. If high, data is output synchronized to the clock input on DATACLK. If low, a convert command initiates the transmission of the data from the previous conversion, along with 16-clock pulses output on DATACLK.
NC	5, 8, 10, 11, 18, 20, 22, 23	–	No connect
PWRD	26	I	Power down input. If high, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
R/$\overline{C}$	21	I	Read/convert input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is low, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is high, a rising edge on R/$\overline{C}$ with $\overline{CS}$ low or a falling edge on $\overline{CS}$ with R/$\overline{C}$ high transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
REF	7	I/O	Reference input/output. Outputs internal 2.5-V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2-µF tantalum capacitor.
$R1_{IN}$	1	I	Analog input. See Table 2 for input range connections.
$R2_{IN}$	3	I	Analog input. See Table 2 for input range connections.
$R3_{IN}$	4	I	Analog input. See Table 2 for input range connections.
SB/$\overline{BTC}$	12	I	Select straight binary or binary 2's complement data output format. If high, data is output in a straight binary format. If low, data is output in a binary 2's complement format.
SYNC	15	O	Sync output. This pin is used to supply a data synchronization pulse when the EXT level is high and at least one external clock pulse has occurred when not in the read mode. See the external clock modes desciptions.
TAG	19	I	Tag input for use in the external clock mode. If EXT is high, digital data input from TAG is output on DATA with a delay that is dependent on the external clock mode. See Figure 9 and Figure 10.
V_{ANA}	27	I	Analog supply input. Nominally +5 V. Connect directly to pin 20 and decouple to ground with 0.1-µF ceramic and 10-µF tantalum capacitors.
V_{DIG}	28	I	Digital supply input. Nominally +5 V. Connect directly to pin 19. Must be ≤ V_{ANA}.

TIMING REQUIREMENTS, T_A = –40°C to 175°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{w1}	Pulse duration, convert	40			ns
t_{d1}	Delay time, $\overline{\text{BUSY}}$ from R/$\overline{\text{C}}$ low		6	20	ns
t_{w2}	Pulse duration, $\overline{\text{BUSY}}$ low			2.2	µs
t_{d2}	Delay time, $\overline{\text{BUSY}}$, after end of conversion		5		ns
t_{d3}	Delay time, aperture		5		ns
t_{conv}	Conversion time			2.2	µs
t_{acq}	Acquisition time	1.8			µs
t_{conv} + t_{acq}	Cycle time			4	µs
t_{d4}	Delay time, R/$\overline{\text{C}}$ low to internal DATACLK output		270		ns
t_{c1}	Cycle time, internal DATACLK		110		ns
t_{d5}	Delay time, data valid to internal DATACLK high	15	35		ns
t_{d6}	Delay time, data valid after internal DATACLK low	20	35		ns
t_{c2}	Cycle time, external DATACLK	35			ns
t_{w3}	Pulse duration, external DATACLK high	15			ns
t_{w4}	Pulse duration, external DATACLK low	15			ns
t_{su1}	Setup time, R/$\overline{\text{C}}$ rise/fall to external DATACLK high	15			ns
t_{su2}	Setup time, R/$\overline{\text{C}}$ transition to $\overline{\text{CS}}$ transition	10			ns
t_{d7}	Delay time, SYNC, after external DATACLK high	3		35	ns
t_{d8}	Delay time, data valid	2		20	ns
t_{d9}	Delay time, $\overline{\text{CS}}$ to rising edge	10			ns
t_{d10}	Delay time, previous data available after $\overline{\text{CS}}$, R/$\overline{\text{C}}$ low	2			µs
t_{su3}	Setup time, $\overline{\text{BUSY}}$ transition to first external DATACLK	5			ns
t_{d11}	Delay time, final external DATACLK to $\overline{\text{BUSY}}$ falling edge			1	µs
t_{su3}	Setup time, TAG valid	0			ns
t_{h1}	Hold time, TAG valid	2			ns

PARAMETER MEASUREMENT INFORMATION

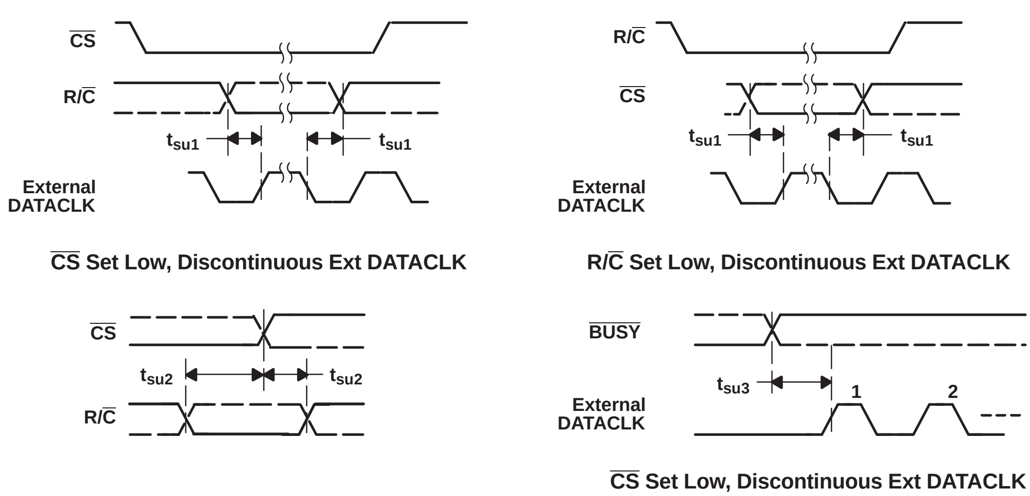


Figure 2. Critical Timing

PARAMETER MEASUREMENT INFORMATION (continued)

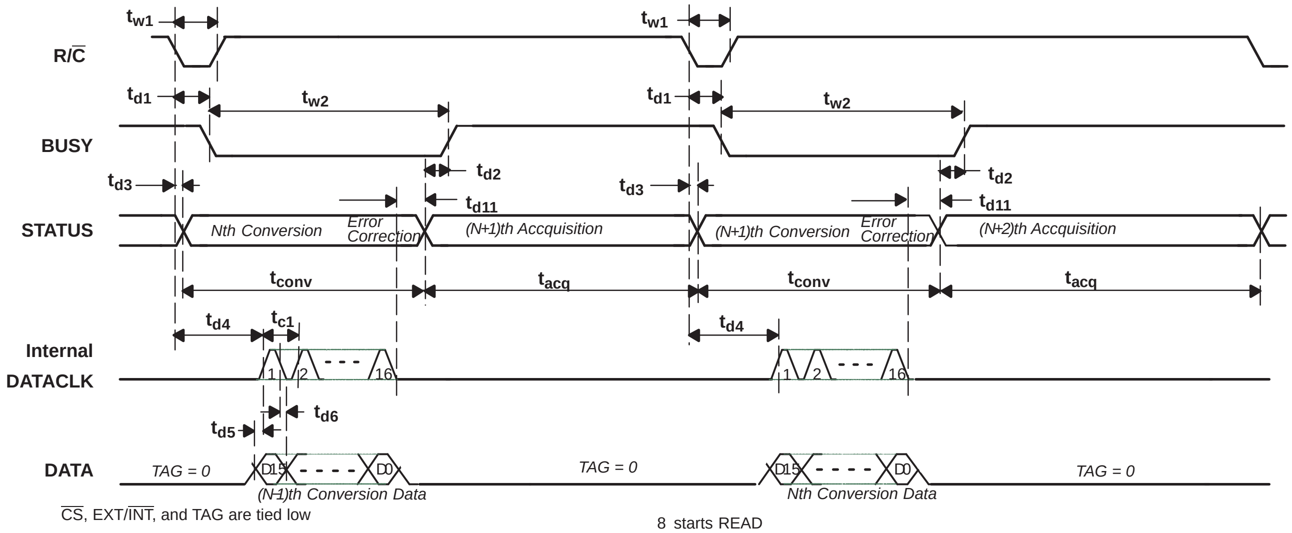


Figure 3. Basic Conversion Timing (Internal DATACLK - Read Previous Data During Conversion)

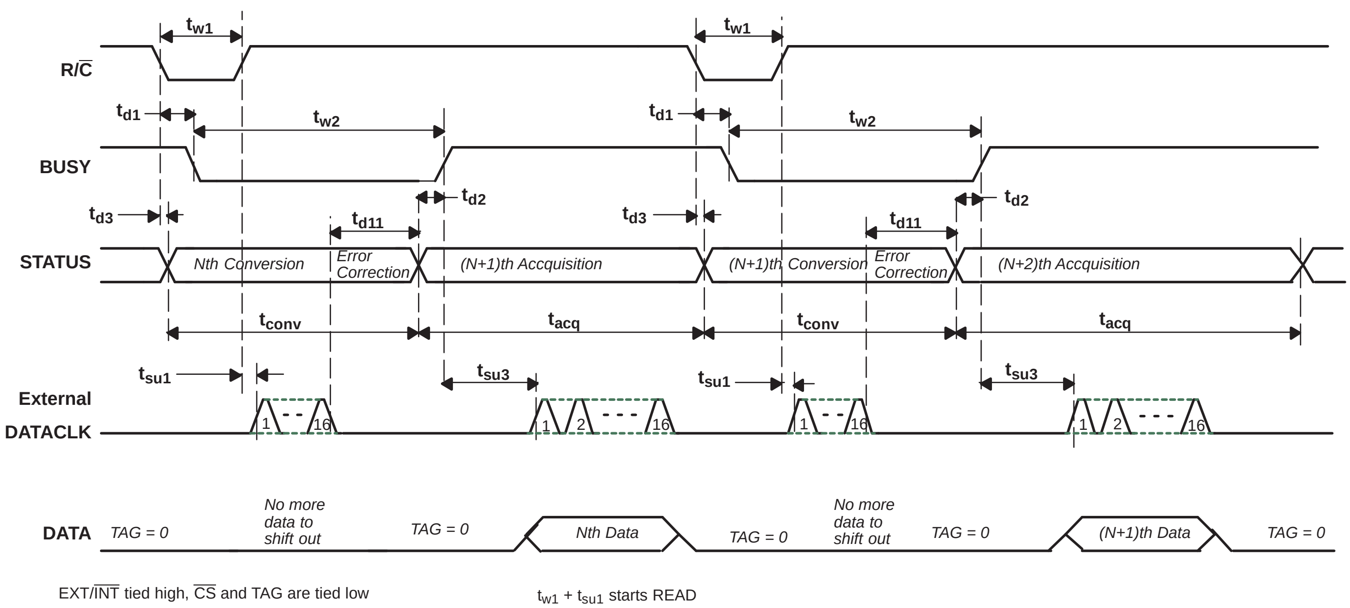


Figure 4. Basic Conversion Timing (External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

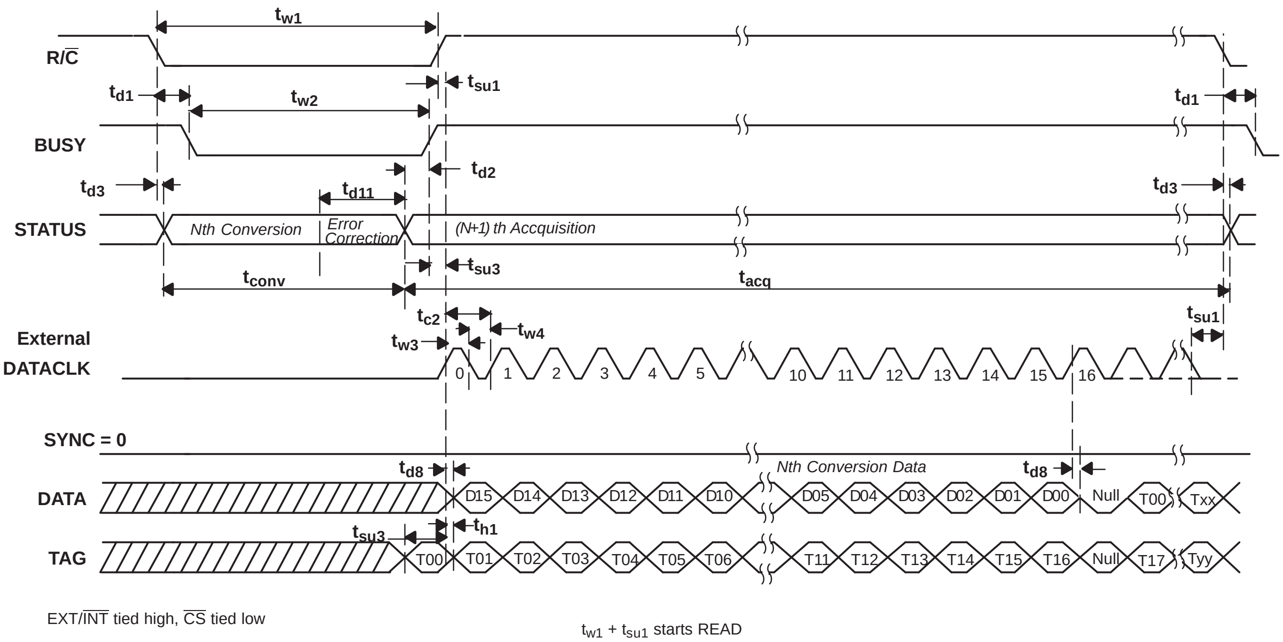


Figure 5. Read After Conversion (Discontinuous External DATACLK)

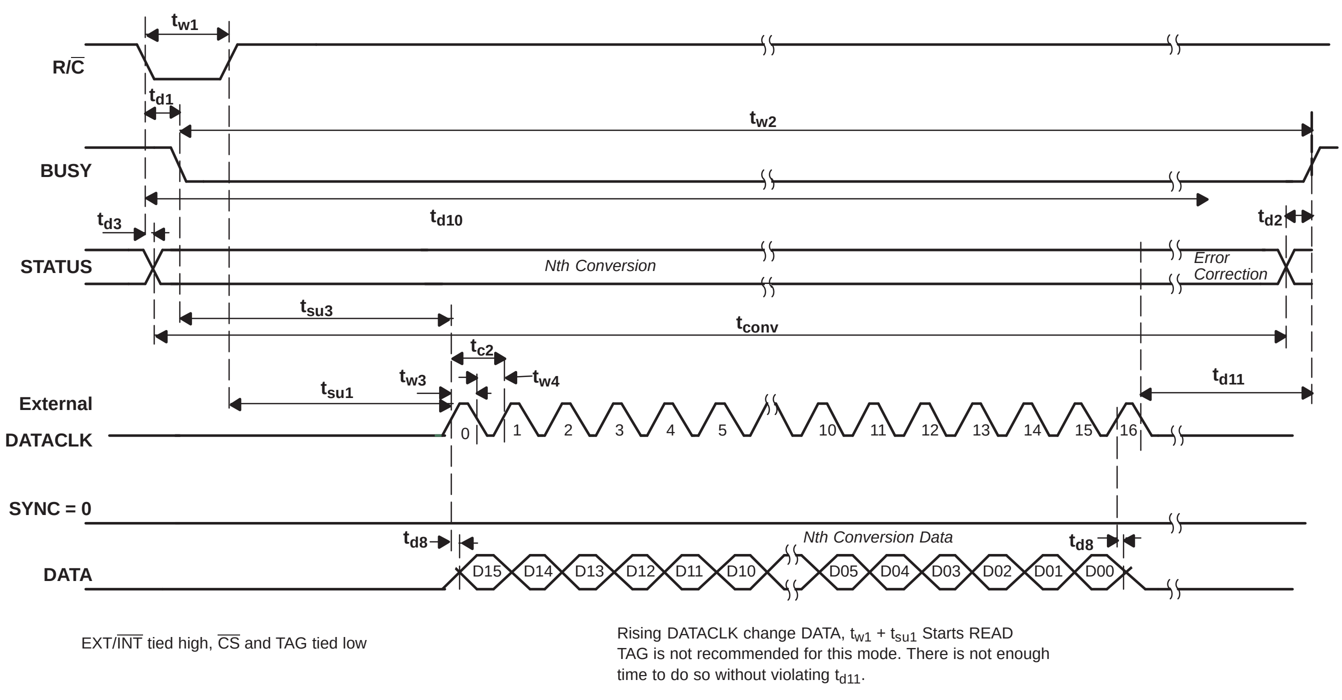


Figure 6. Read During Conversion (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

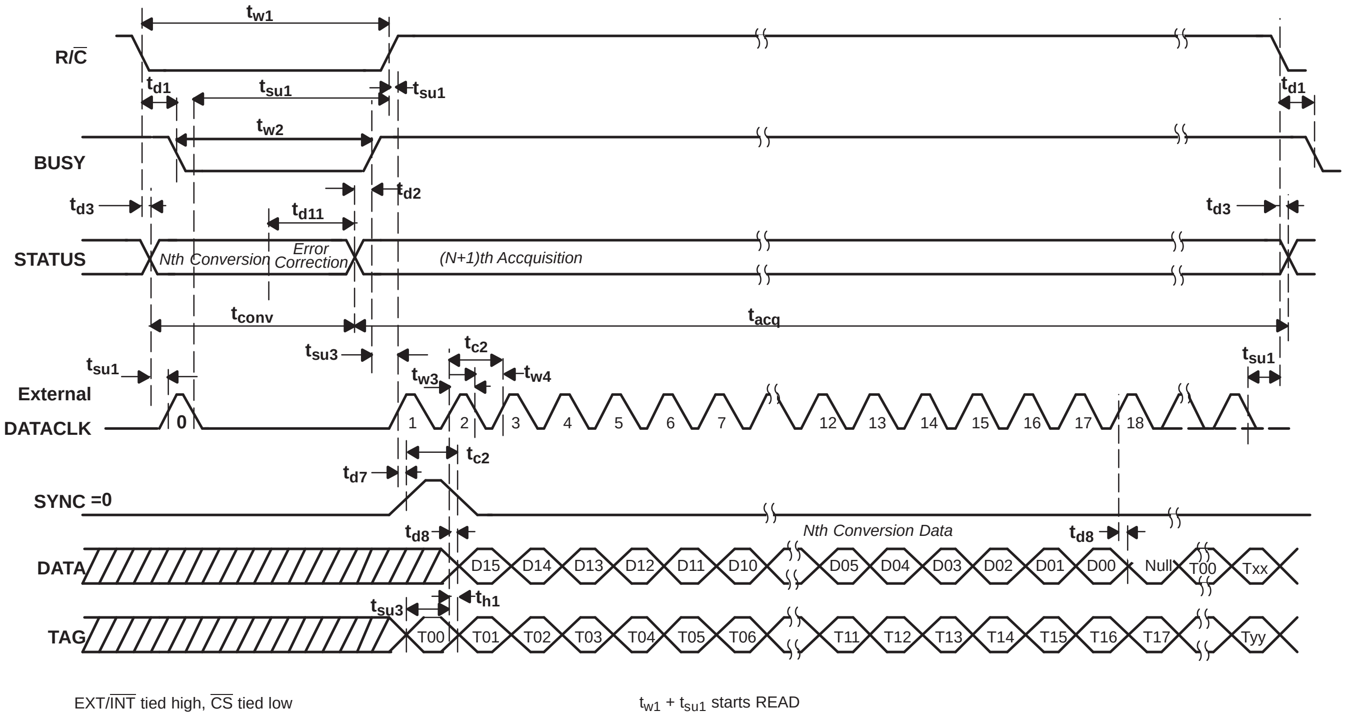


Figure 7. Read After Conversion With SYNC (Discontinuous External DATACLK)

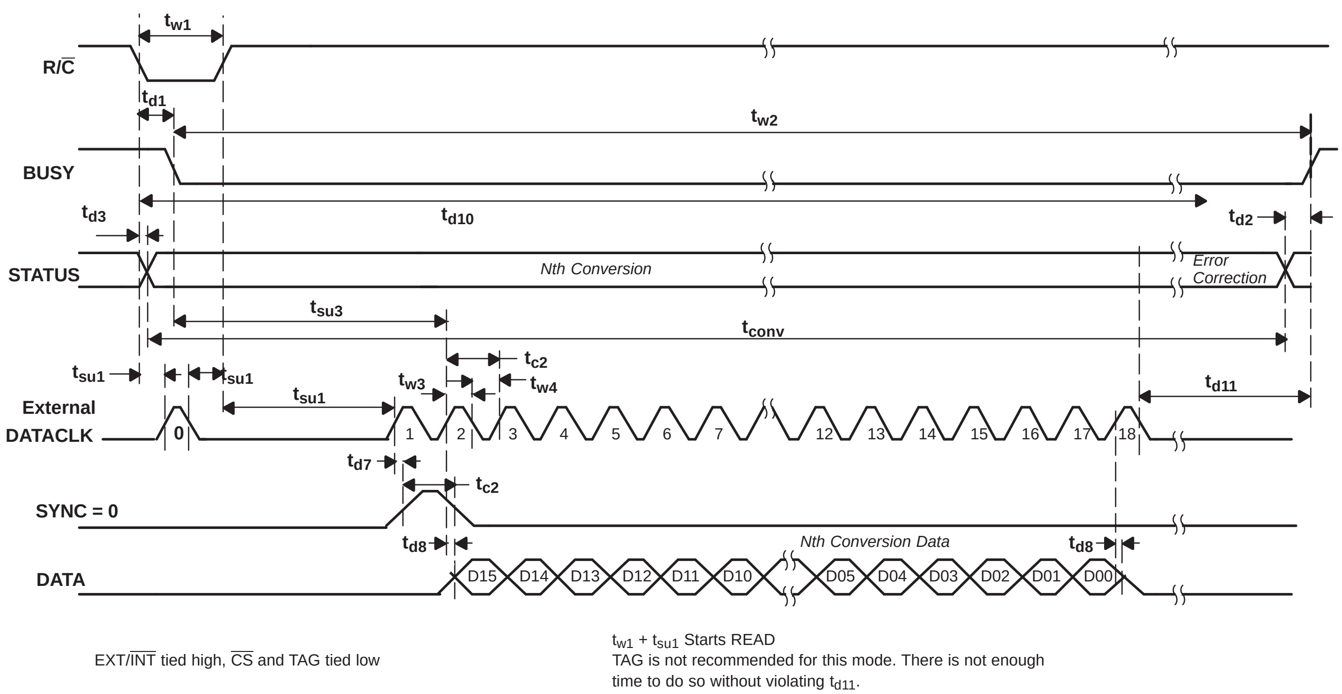


Figure 8. Read During Conversion With SYNC (Discontinuous External DATACLK)

PARAMETER MEASUREMENT INFORMATION (continued)

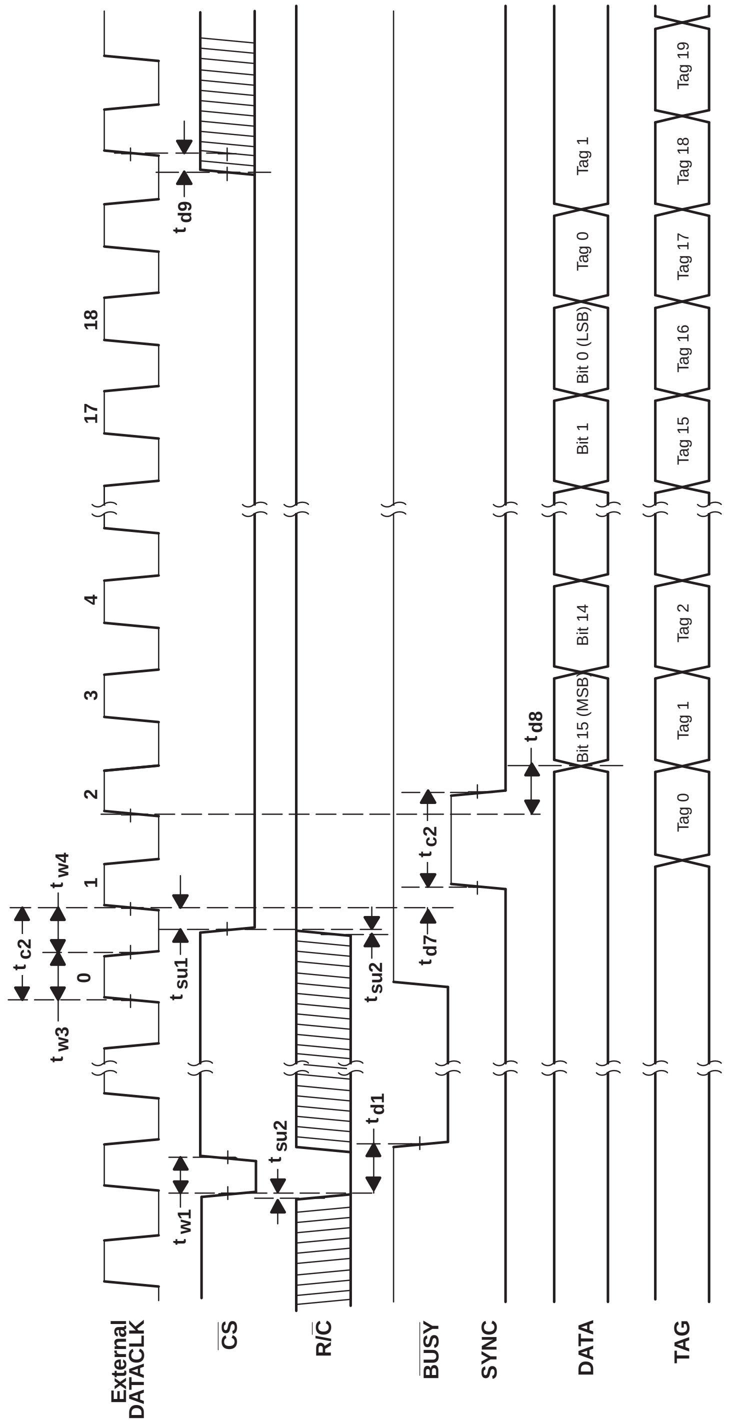


Figure 9. Conversion and Read Timing with Continuous External DATACLK (EXT/$\overline{\text{INT}}$ Tied High) Read After Conversions (Not Recommended)

PARAMETER MEASUREMENT INFORMATION (continued)

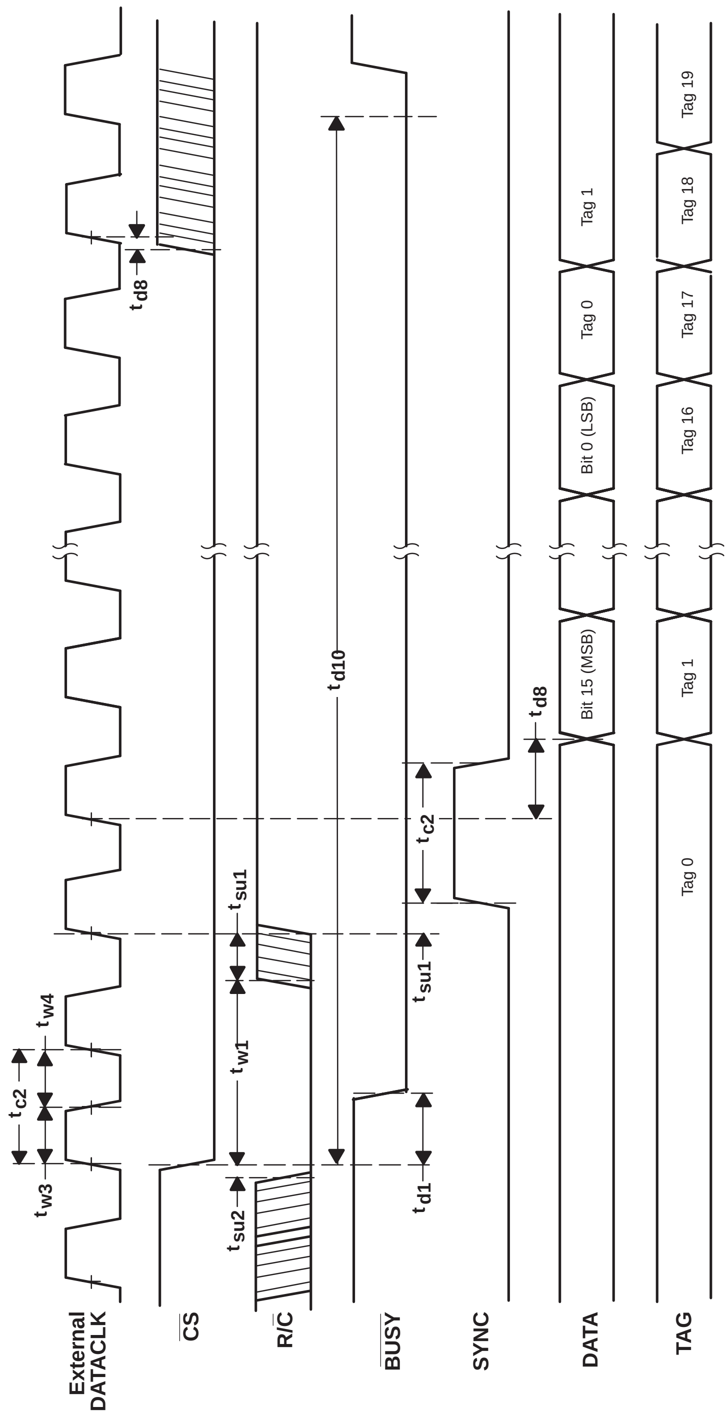


Figure 10. Conversion and Read Timing with Continous External DATACLK (EXT/$\overline{\text{INT}}$ Tied High) Read Previous Conversion Results During Conversion (Not Recommended)

TYPICAL CHARACTERISTICS

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

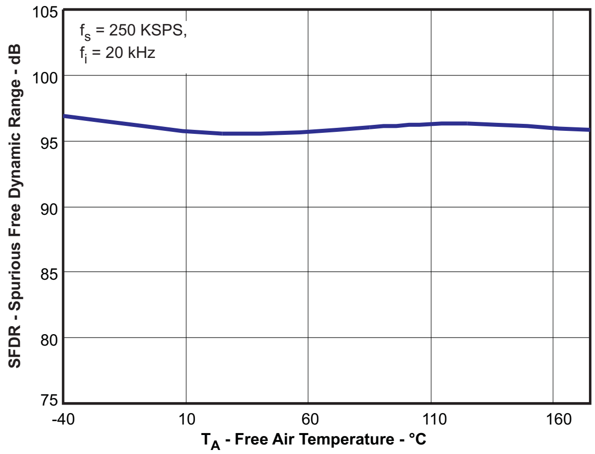


Figure 11.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

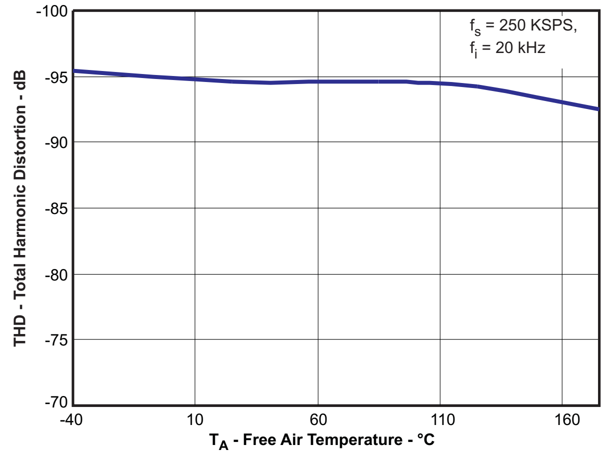


Figure 12.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

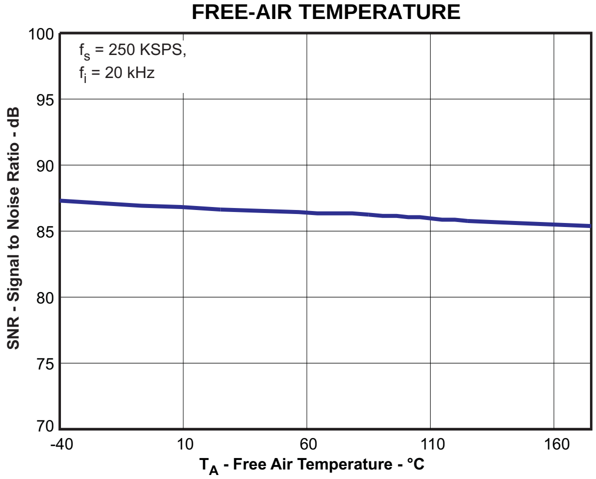


Figure 13.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

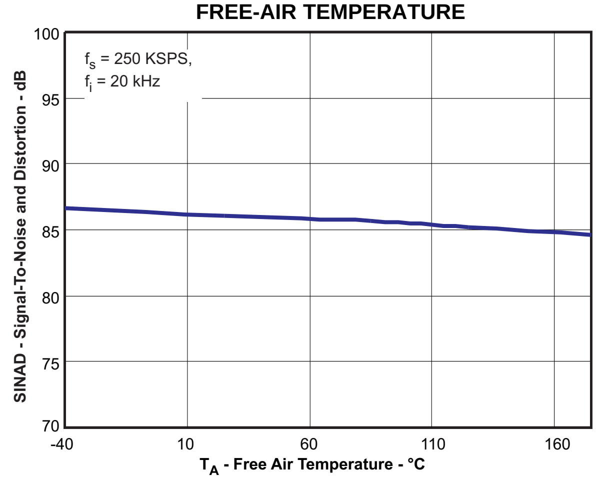


Figure 14.

TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

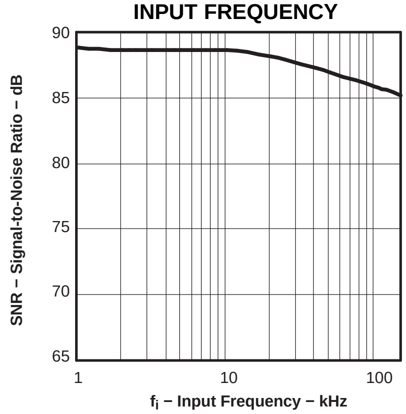


Figure 15.

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

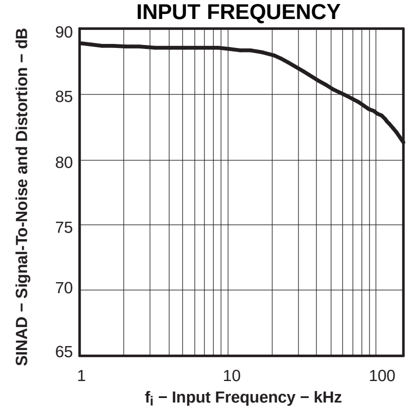


Figure 16.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

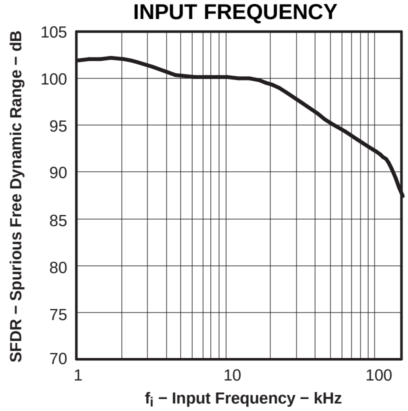


Figure 17.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

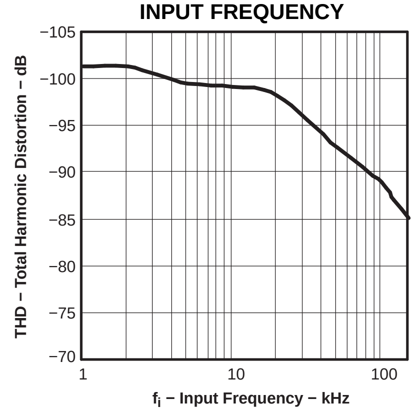


Figure 18.

INTERNAL REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

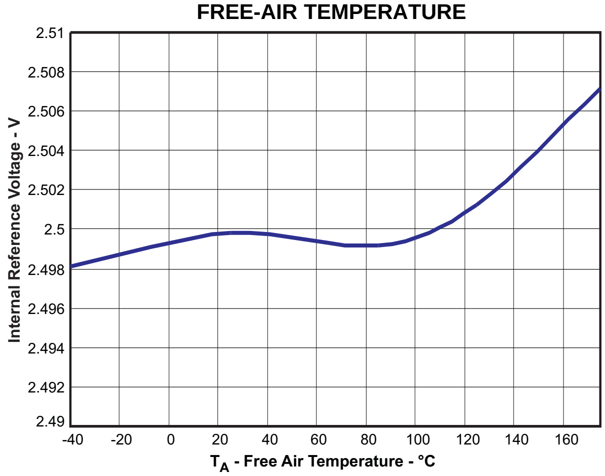


Figure 19.

BIPOLAR ZERO SCALE ERROR vs FREE-AIR TEMPERATURE

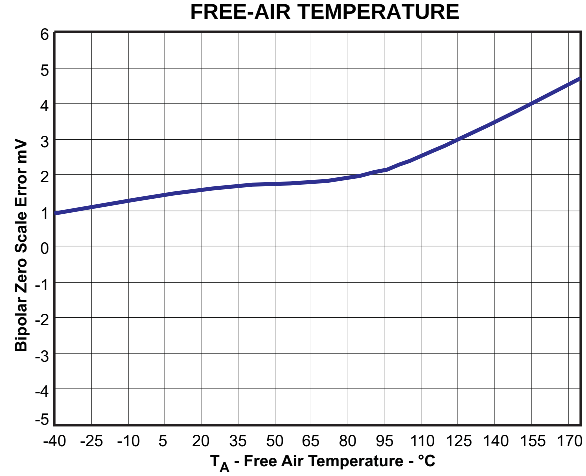


Figure 20.

TYPICAL CHARACTERISTICS (continued)

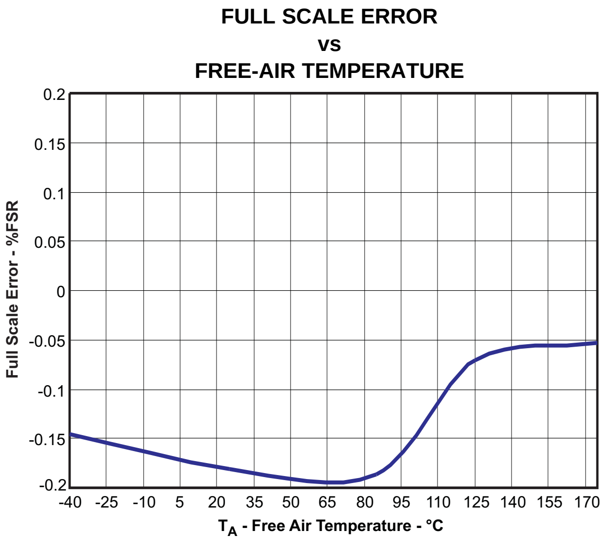


Figure 21.

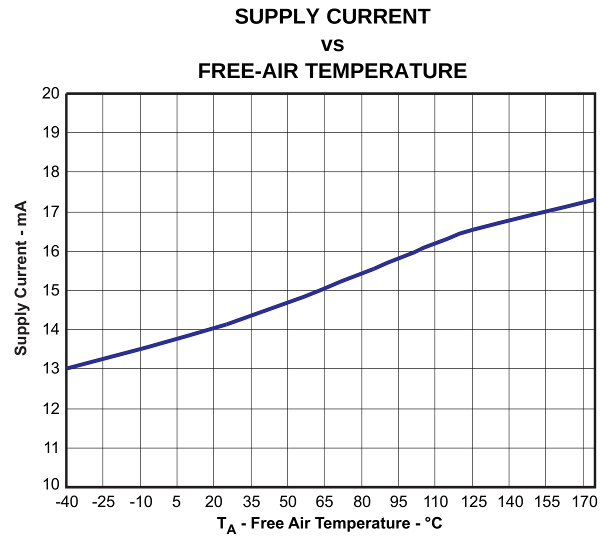


Figure 22.

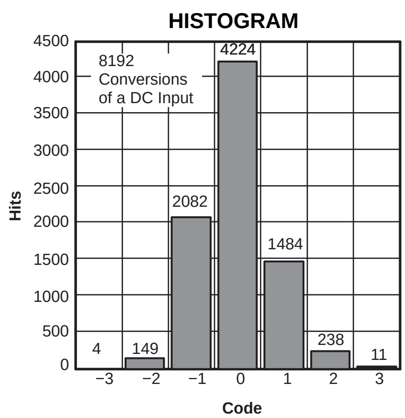


Figure 23.

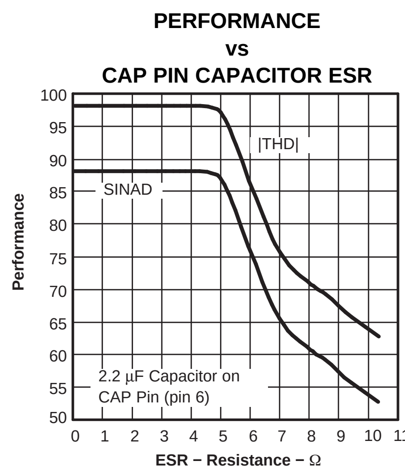


Figure 24.

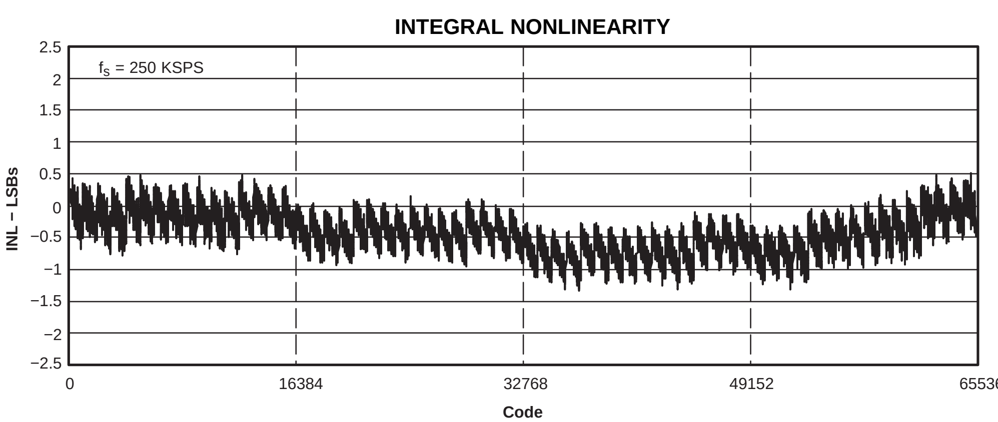


Figure 25.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL NONLINEARITY

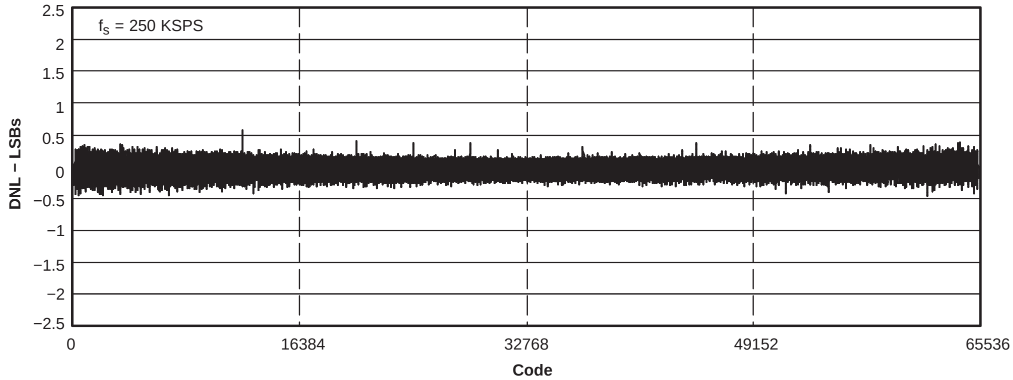


Figure 26.

FFT (20-kHz Input)

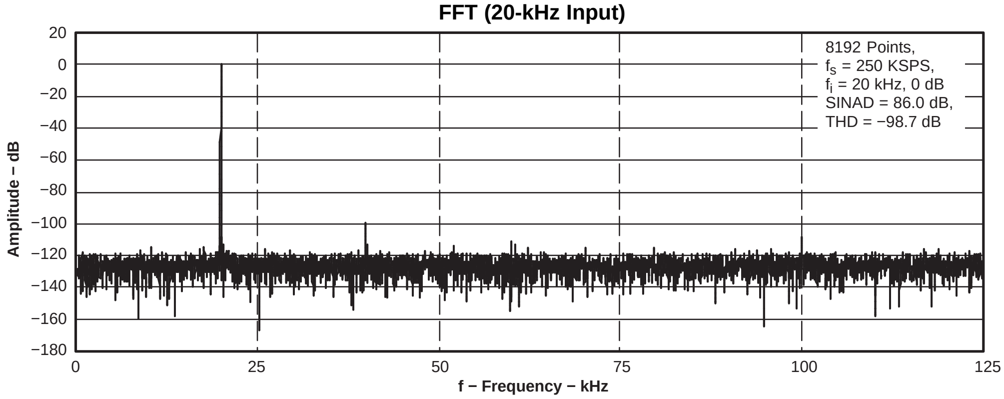


Figure 27.

BASIC OPERATION

Two signals control conversion in the ADS8509: $\overline{CS}$ and R/$\overline{C}$. These two signals are internally ORed together. To start a conversion the chip must be selected, $\overline{CS}$ low, and the conversion signal must be active, R/$\overline{C}$ low. Either signal can be brought low first. Conversion starts on the falling edge of the second signal. $\overline{BUSY}$ goes low when conversion starts and returns high after the data from that conversion is shifted into the internal storage register. Sampling begins when $\overline{BUSY}$ goes high.

To reduce the number of control pins $\overline{CS}$ can be tied low permanently. The R/$\overline{C}$ pin now controls conversion and data reading exclusively. In the external clock mode this means that the ADS8509 clocks out data whenever R/$\overline{C}$ is brought high and the external clock is active. In the internal clock mode data is clocked out every convert cycle regardless of the states of $\overline{CS}$ and R/$\overline{C}$. The ADS8509 provides a TAG input for cascading multiple converters together.

READING DATA

The conversion result is available as soon as BUSY returns to high, therefore data always represents the conversion previously completed even when it is read during a conversion. The ADS8509 outputs serial data in either straight binary or binary two's compliment format. The SB/$\overline{BTC}$ pin controls the format. Data is shifted out MSB first. The first conversion immediately following a power-up does not produce a valid conversion result.

Data can be clocked out with either the internally generated clock or with an external clock. The EXT/$\overline{INT}$ pin controls this function. If an external clock is used, the TAG input can be used to daisy-chain multiple ADS8509 data pins together.

INTERNAL DATACLK

In internal clock mode data for the previous conversion is clocked out during each conversion period. The internal data clock is synchronized to the internal conversion clock so that is does not interfere with the conversion process.

The DATACLK pin becomes an output when EXT/$\overline{\text{INT}}$ is low. 16 Clock pulses are generated at the beginning of each conversion after timing t_8 is satisfied, i.e. only the previous conversion result can be read during conversion. DATACLK returns to low when it is inactive. The 16 bits of serial data are shifted out the DATA pin synchronous to this clock with each bit available on a rising and then a falling edge. The DATA pin returns to the state of the TAG pin input sensed at the start of transmission.

EXTERNAL DATACLK

The external clock mode offers several ways to retrieve conversion results. However, since the external clock cannot be synchronized to the internal conversion clock care must be taken to avoid corrupting the data.

When EXT/$\overline{\text{INT}}$ is set high, the R/$\overline{\text{C}}$ and $\overline{\text{CS}}$ signals control the read state. When the read state is initiated, the result from the previously completed conversion is shifted out the DATA pin synchronous to the external clock that is connected to the DATACLK pin. Each bit is available on a falling and then a rising edge. The maximum external clock speed of 28.5 MHz allows data to be shifted out quickly either at the beginning of conversion or the beginning of sampling.

There are several modes of operation available when using an external clock. It is recommended that the external clock run only while reading data. This is discontinuous clock mode. Since the external clock is not synchronized to the internal clock that controls conversion slight changes in the external clock can cause conflicts that can corrupt the conversion process. Specifications with a continuously running external clock cannot be ensured. It is especially important that the external clock does not run during the second half of the conversion cycle (approximately the time period specified by t_{d11}, see the TIMING REQUIREMENTS table).

In discontinuous clock mode data can be read during conversion or during sampling, with or without a SYNC pulse. Data read during conversion must meet the t_{d11} timing specification. Data read during sampling must be complete before starting a conversion.

Whether reading during sampling or during conversion a SYNC pulse is generated whenever at least one rising edge of the external clock occurs while the part is not in the read state. In the *discontinuous external clock with SYNC* mode a SYNC pulse follows the first rising edge after the read command. The data is shifted out after the SYNC pulse. The first rising clock edge after the read command generates a SYNC pulse. The SYNC pulse can be detected on the next falling edge and then the next rising edge. Successively, each bit can be read first on the falling edge and then on the next rising edge. Thus 17 clock pulses after the read command are required to read on the falling edge. 18 Clock pulses are necessary to read on the rising edge.

Table 1. DATACLK Pulses

DESCRIPTION	DATACLK PULSES REQUIRED	
	WITH SYNC	WITHOUT SYNC
Read on falling edge of DATACLK	17	16
Read on rising edge of DATACLK	18	17

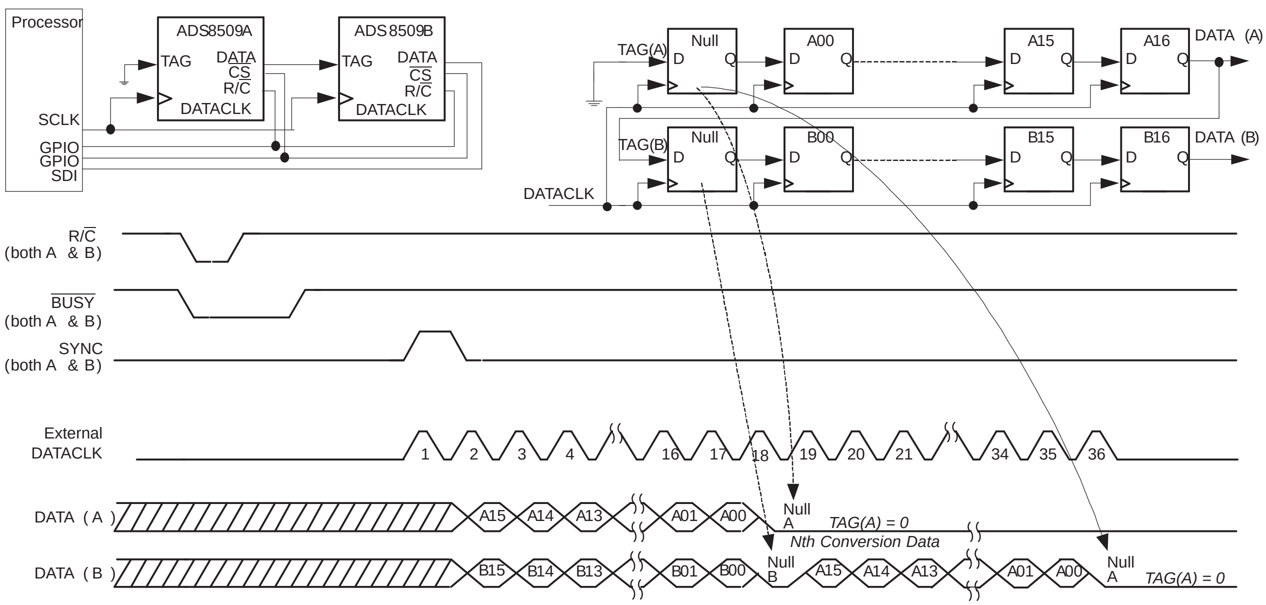
If the clock is entirely inactive when not in the read state a SYNC pulse is not generated. In this case the first rising clock edge shifts out the MSB. The MSB can be read on the first falling edge or on the next rising edge. In this *discontinuous external clock mode with no SYNC*, 16 clocks are necessary to read the data on the falling edge and 17 clocks for reading on the rising edge. Data always represents the conversion already completed.

TAG FEATURE

The TAG feature allows the data from multiple ADS8509 converters to be read on a single serial line. The converters are cascaded together using the DATA pins as outputs and the TAG pins as inputs as illustrated in Figure 28. The DATA pin of the last converter drives the processor's serial data input. Data is then shifted through each converter, synchronous to the externally supplied data clock, onto the serial data line. The internal clock cannot be used for this configuration.

The preferred timing uses the discontinuous external data clock during the sampling period. Data must be read during the sampling period because there is not sufficient time to read data from multiple converters during a conversion period without violating the t_{d11} constraint (see the EXTERNAL DATACLOCK section). The sampling period must be sufficiently long to allow all data words to be read before starting a new conversion.

Note, in Figure 28, that a NULL bit separates the data word from each converter. The state of the DATA pin at the end of a READ cycle reflects the state of the TAG pin at the start of the cycle. This is true in all READ modes, including the internal clock mode. For example, when a single converter is used in internal clock mode, the state of the TAG pin determines the state of the DATA pin after all 16 bits have shifted out. When multiple converters are cascaded together, this state forms the NULL bit that separates the words. Thus, with the TAG pin of the first converter grounded as shown in Figure 28 the NULL bit becomes a zero between each data word.



EXT/$\overline{INT}$ tied high, $\overline{CS}$ of both converter A and B, TAG input of converter A are tied low.

Figure 28. Timing of TAG Feature With Single Conversion (Using External DATACLK)

ANALOG INPUTS

The ADS8509 has six analog input ranges as shown in Table 2. The offset and gain specifications are factory calibrated with 0.1%, 0.25-W, external resistors as shown in Figure 30 and Figure 31. The external resistors can be omitted if larger gain and offset errors are acceptable or if using software calibration. The hardware trim circuitry shown in Figure 30 and Figure 31 can reduce the errors to zero.

The analog input pins $R1_{IN}$, $R2_{IN}$, and $R3_{IN}$ have ±25-V overvoltage protection. The input signal must be referenced to AGND1. This minimizes the ground loop problem typical to analog designs. The analog input should be driven by a low impedance source. A typical driving circuit using OPA627 or OPA132 is shown in Figure 29.

The ADS8509 can operate with its internal 2.5-V reference or an external reference. An external reference connected to pin 6 (REF) bypasses the internal reference. The external reference must drive the 4-kΩ resistor that separates pin 6 from the internal reference (see the illustration on page 1). The load varies with the difference between the internal and external reference voltages. The external reference voltage can vary from 2.3 V to 2.7 V. The internal reference is approximately 2.5 V. The reference, whether internal or external, is buffered internally with a buffer with its output on pin 5 (CAP).

The ADS8509 is factory tested with 2.2-μF capacitors connected to pins 5 and 6 (CAP and REF). Each capacitor should be placed as close as possible to its pin. The capacitor on pin 6 band limits the internal reference noise. A smaller capacitor can be used but it may degrade SNR and SINAD. The capacitor on pin 5 stabilizes the reference buffer and provides switching charge to the CDAC during conversion. Capacitors smaller than 1 μF can cause the buffer to become unstable and may not hold sufficient charge for the CDAC. The parts are tested to specifications with 2.2 μF so larger capacitors are not necessary. The equivalent series resistor (ESR) of these compensation capacitors is also critical. The total ESR must be kept under 3 Ω. See the TYPICAL CHARACTERISTICS section concerning how ESR affects performance.

Neither the internal reference nor the buffer should be used to drive an external load. Such loading can degrade performance. Any load on the internal reference causes a voltage drop across the 4-kΩ resistor and affects gain. The internal buffer is capable of driving ±2-mA loads but any load can cause perturbations of the reference at the CDAC, degrading performance. It should be pointed out that, unlike other competitor's parts with similar input structure, the ADS8509 does not require a second high-speed amplifier used as a buffer to isolate the CAP pin from the signal dependent current in the $R3_{IN}$ pin but can tolerate it if one does exist.

The external reference voltage can vary from 2.3 V to 2.7 V. The reference voltage determines the size of the least significant bit (LSB). The larger reference voltages produce a larger LSB, which can improve SNR. Smaller reference voltages can degrade SNR.

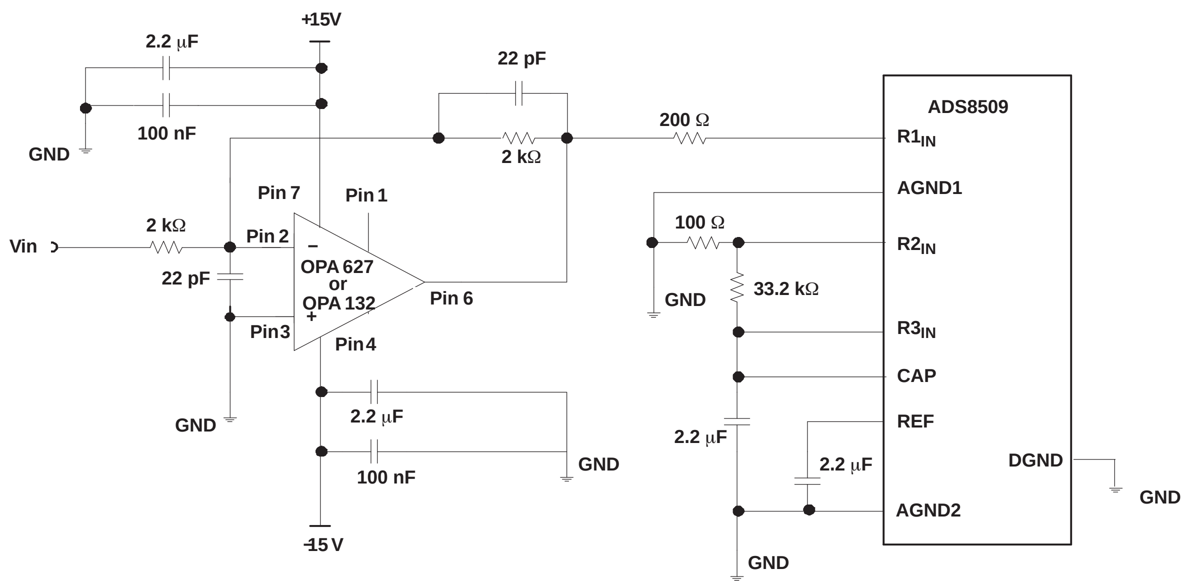


Figure 29. Typical Driving Circuitry (±10 V, No Trim)

Table 2. Input Range Connections (See Figure 30 and Figure 31 for Complete Information)

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200 Ω TO	CONNECT $R2_{IN}$ VIA 100 Ω TO	CONNECT R3 TO	IMPEDANCE
±10 V	V_{IN}	AGND	CAP	11.5 kΩ
±5 V	AGND	V_{IN}	CAP	6.7 kΩ
±3.33 V	V_{IN}	V_{IN}	CAP	5.4 kΩ
0 V to 10 V	AGND	V_{IN}	AGND	6.7 kΩ
0 V to 5 V	AGND	AGND	V_{IN}	5.0 kΩ
0 V to 4 V	V_{IN}	AGND	V_{IN}	5.4 kΩ

Table 3. Control Truth Table

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate conversion and output data using internal clock	1 > 0	0	1	0	Output	0	x	Initiates conversion *n*. Data from conversion *n - 1* clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	
Initiate conversion and output data using external clock	1 > 0	0	1	1	Input	0	x	Initiates conversion *n*.
	0	1 > 0	1	1	Input	0	x	Initiates conversion *n*.
	1 > 0	1	1	1	Input	x	x	Outputs data with or without SYNC pulse. See section READING DATA.
	1 > 0	1	0	1	Input	0	x	Outputs data with or without SYNC pulse. See section READING DATA.
	0	0 > 1	0	1	Input	0	x	
No actions	0	0	0 > 1	x	x	0	x	This is an acceptable condition.
Power down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed..
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Select output format	x	x	x	x	x	x	0	Serial data is output in binary 2's complement format.
	x	x	x	x	x	x	1	Serial data is output in straight binary format.

Table 4. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY 2'S COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-scale range	±10	±5	±3.33 V	0 V to 10 V	0 V to 5 V	0 V to 4 V				
Least significant bit (LSB)	305 μV	153 μV	102 μV	153 μV	76 μV	61 μV				
Full scale (FS - 1LSB)	9.999695 V	4.999847 V	3.333231 V	9.999847 V	4.999924 V	3.999939 V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0 V	0 V	0 V	5 V	2.5 V	2 V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB below midscale	–305 μV	153 μV	±102 μV	4.999847 V	2.499924 V	1.999939 V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full scale	–10 V	–5 V	–3.333333 V	0 V	0 V	0 V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

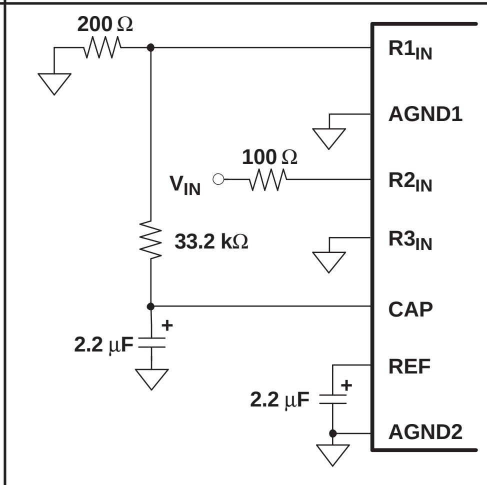
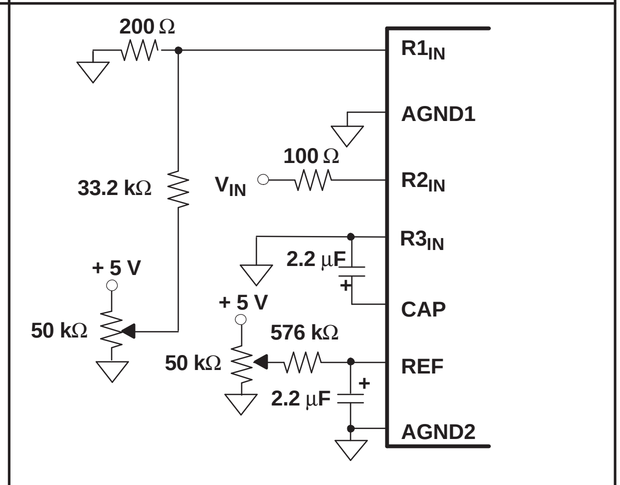
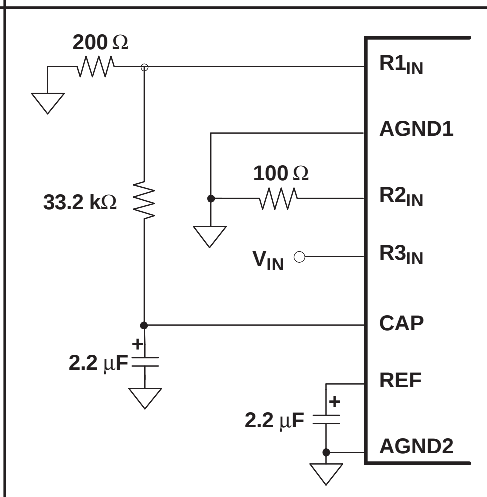
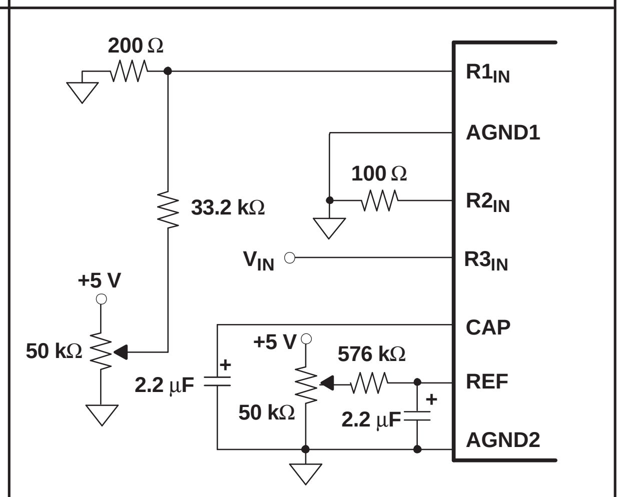
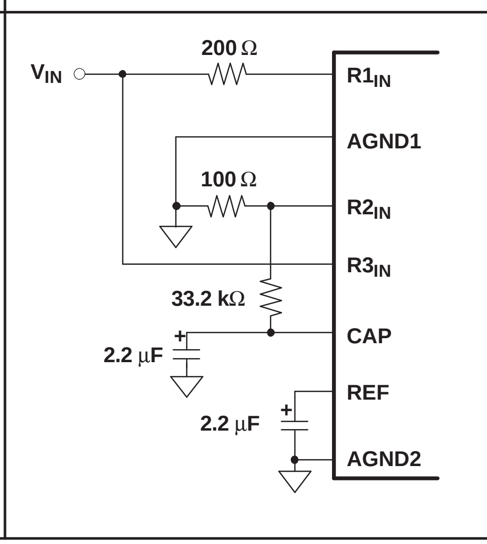
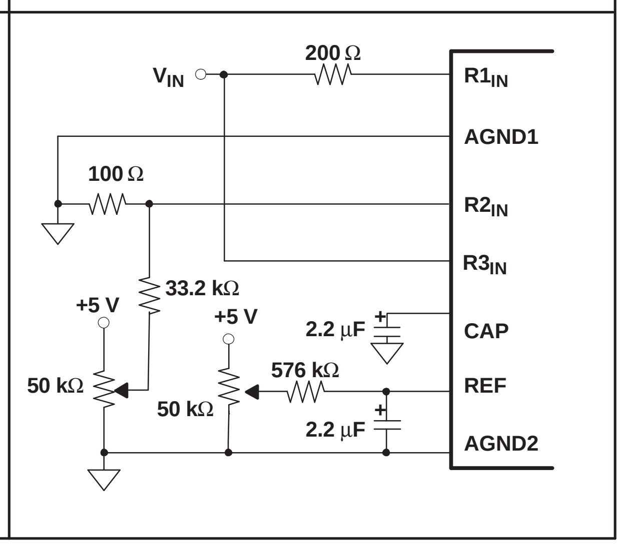
Input Range	Without Trim	With Trim (Adjust Offset First at 0 V, Then Adjust Gain)
0 V – 10 V		
0 V – 5 V		
0 V – 4 V		

Figure 30. Offset/Gain Circuits for Unipolar Input Ranges

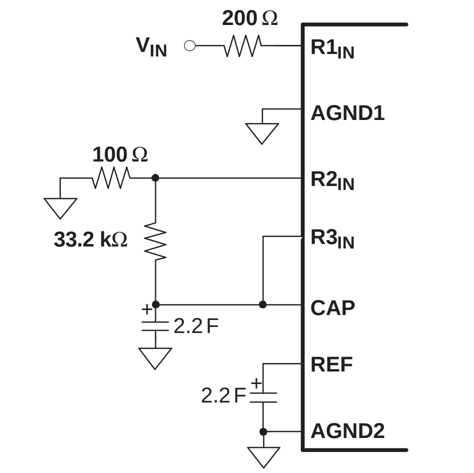
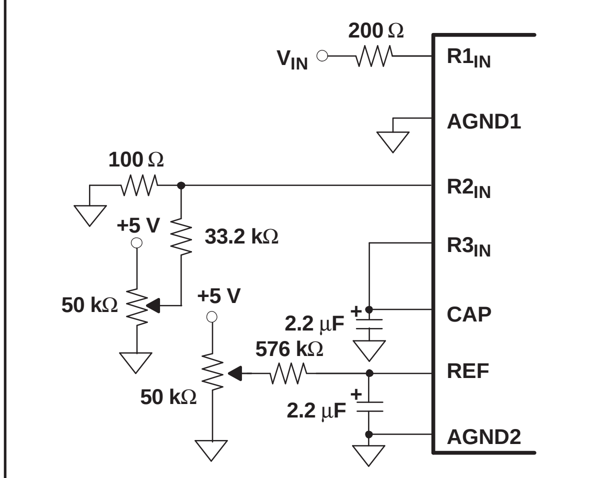
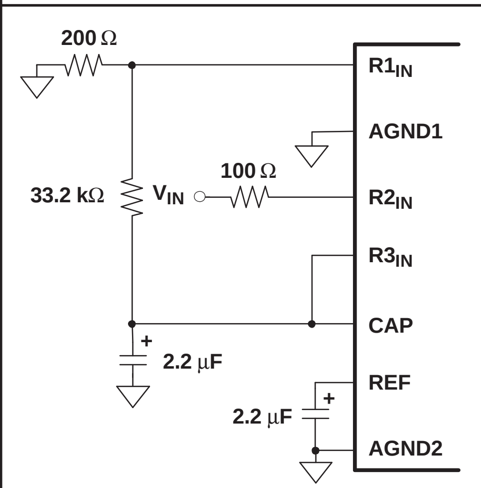
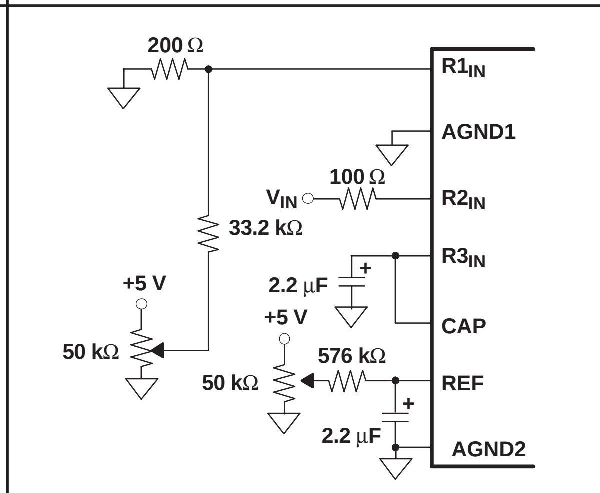
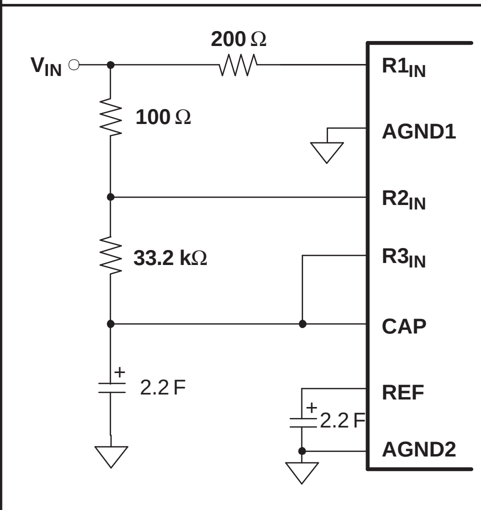
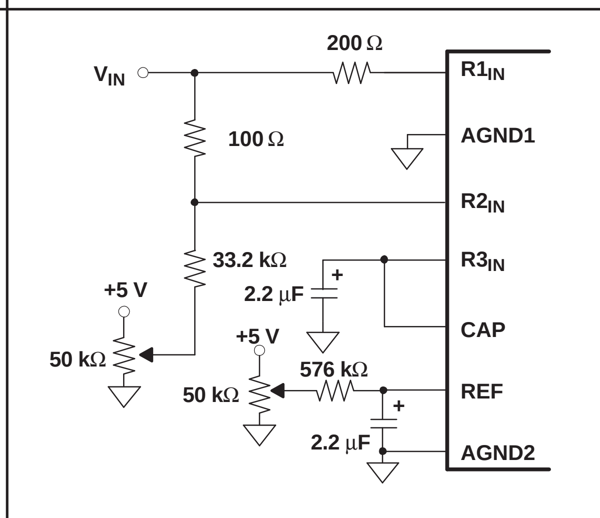
Input Range	Without Trim	With Trim (Adjust Offset First at 0 V, Then Adjust Gain)
±10 V		
± 5 V		
±3.3 V		

Figure 31. Offset/Gain Circuits for Bipolar Input Ranges

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS8509HDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF ADS8509-HT :

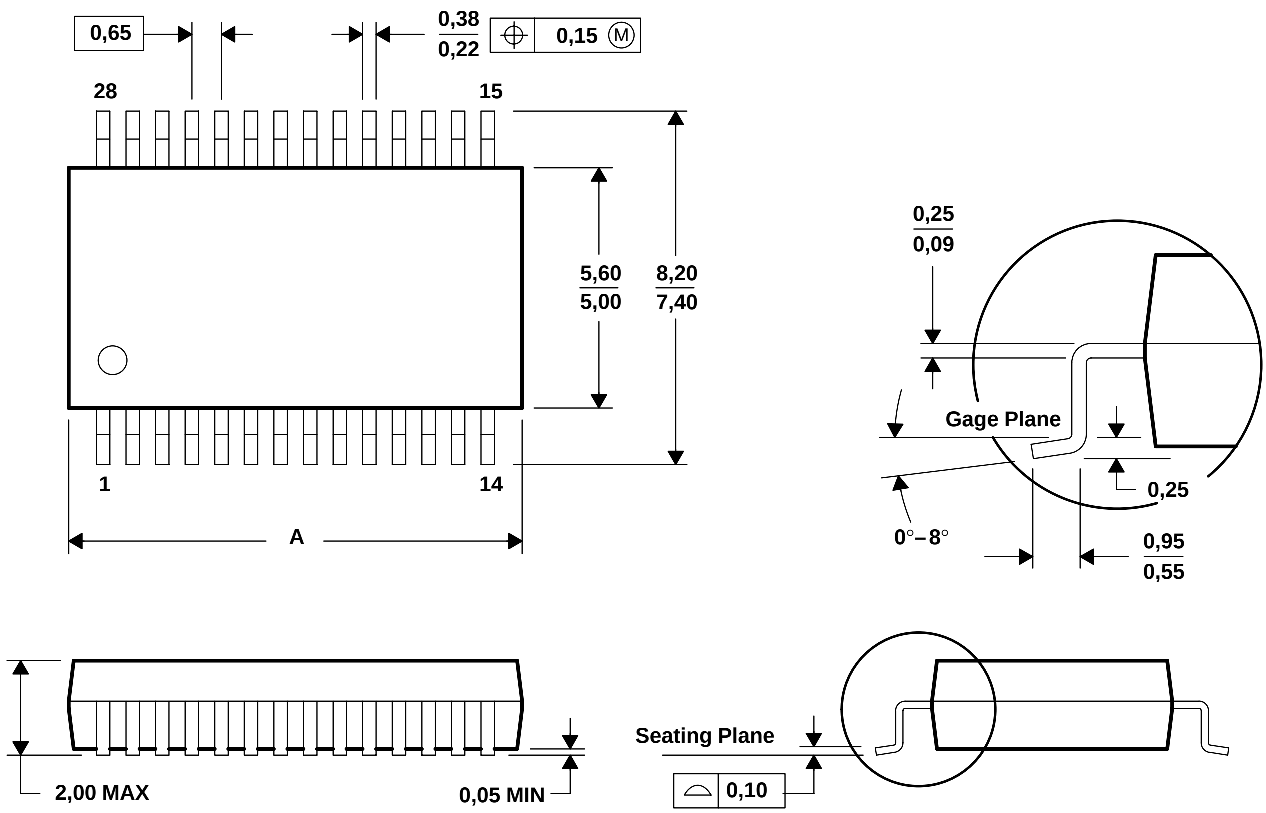
- Catalog: ADS8509

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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