Burr-Brown Products from Texas Instruments

ADS901

SBAS054A – MAY 2001

SpeedPLUS™ 10-Bit, 20MHz, +3V Supply ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW POWER: 48mW at +3V
- SUPPLY RANGE: +2.7V to +3.7V
- ADJUSTABLE FULL SCALE RANGE WITH EXTERNAL REFERENCES
- NO MISSING CODES
- WIDEBAND TRACK/HOLD: 350MHz
- POWER DOWN: 15mW
- SSOP-28 PACKAGE

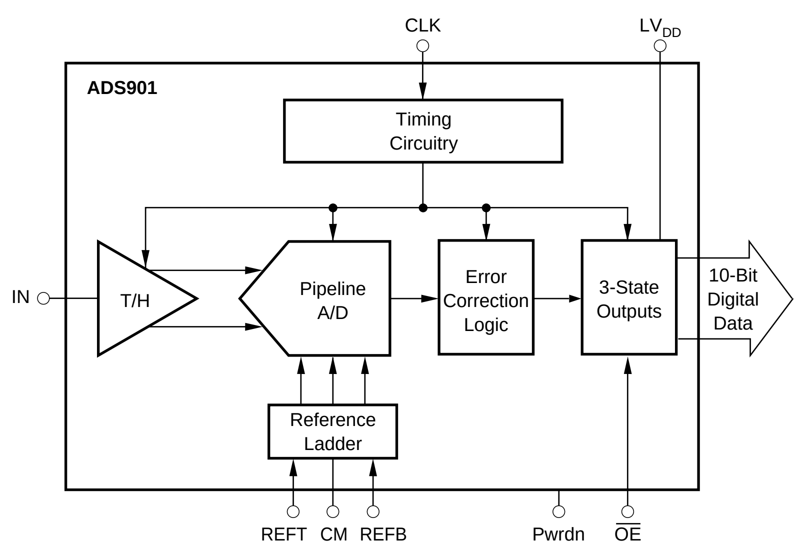
APPLICATIONS

- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- DIGITAL CAMERAS
- COMPUTER SCANNERS
- COMMUNICATIONS

DESCRIPTION

The ADS901 is a high-speed pipelined analog-to-digital converter that operates from a +3V power supply. This complete converter includes a wide bandwidth track/hold and a 10-bit quantizer. The full scale input range is set by external references.

The ADS901 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. The ADS901 is available in an SSOP-28 package.



TEXAS INSTRUMENTS
www.ti.com

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Logic V_{DD}	+6V
Analog Input	$+V_S$ +0.3V
Logic Input	$+V_S$ +0.3V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS901E	SSOP-28	324	–40°C to +85°C	ADS901E	ADS901E	Rail
ADS901E	SSOP-28	324	–40°C to +85°C	ADS901E	ADS901E/1K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “ADS901E/1K” will get a single 1000-piece Tape and Reel.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = LV_{DD} = +3V, REFB = 1V, REFT = 2V, Specified Input Range = 1V to 2V, Sampling Rate = 20MHz, unless otherwise specified.

			ADS901E			
PARAMETER	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution				10		Bits
Specified Temperature Range	Ambient Air		–40		+85	°C
ANALOG INPUT						
Specified Full Scale Input Range(1)				1Vp-p		V
Common-Mode Voltage (Midscale)				1.5		V
Analog Input Bias Current				1		µA
Input Impedance				1.25 || 5		MΩ || pF
DIGITAL INPUT						
Logic Family				CMOS Compatible		
Convert Command (Start Conversion)	Start Conversion			Rising Edge of Convert Clock		
CONVERSION CHARACTERISTICS						
Sample Rate		Full	10k		20M	Samples/s
Data Latency				5		Clk Cyc

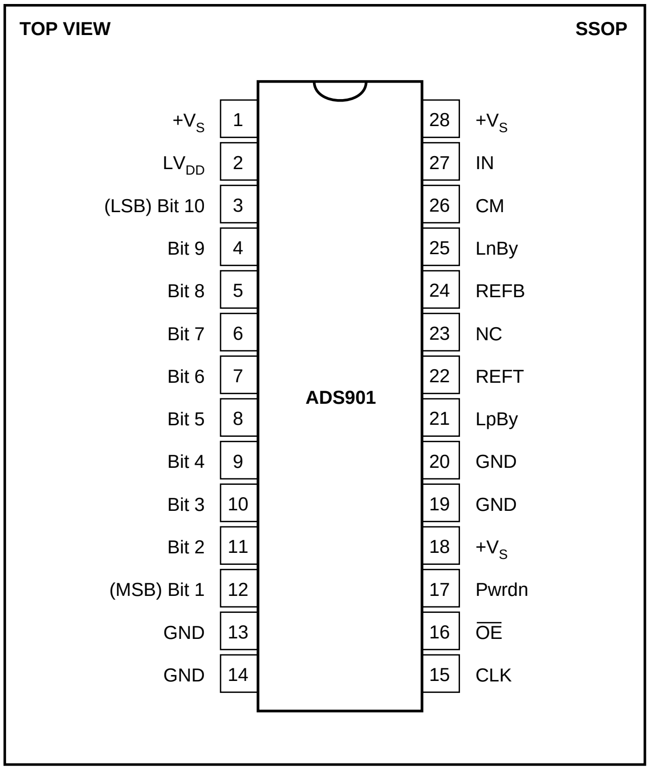
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = LV_{DD} = +3V, REFB = 1V, REFT = 2V, Specified Input Range = 1V to 2V, Sampling Rate = 20MHz, unless otherwise specified.

			ADS901E			
PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Differential Linearity Error (Largest Code Error)						
f = 500kHz		Full		±0.8		LSB
f = 9MHz		Full		±0.9	±1.0	LSB
No Missing Codes		Full		Guaranteed		
Integral Nonlinearity Error, f = 500kHz		Full		±3.5		LSB
Spurious Free Dynamic Range(2)						
f = 500kHz (–1dBFS(3) input)		Full		50		dBFS(3)
f = 9MHz (–1dBFS input)		Full	45	49		dBFS
Signal-to-Noise Ratio (SNR)	Referred to Sinewave Input Signal					
f = 500kHz (–1dBFS input)		Full		53		dB
f = 9MHz (–1dBFS input)		Full	48	53		dB
Maximum SNR	Referred to DC Full Scale Input Signal					
f = 9MHz (–1dBFS input)				62		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		Full		50		dB
f = 3.58MHz (–1dBFS input)		Full		50		dB
f = 9MHz (–1dBFS input)		Full	45	49		dB
Effective Number of Bits(4)	f_{IN} = 3.58MHz			8.0		Bits
Differential Gain Error	NTSC, PAL			2.3		%
Differential Phase Error	NTSC, PAL			1.0		degrees
Output Noise	Input Grounded			0.2		LSB rms
Aperture Delay Time				3		ns
Aperture Jitter				7		ps rms
Analog Input Bandwidth						
Small Signal	–20dBFS Input			350		MHz
Full Power	0dBFS Input			100		MHz
Overvoltage Recovery Time(5)				2		ns
DIGITAL OUTPUTS	C_L = 15pF					
Logic Family				CMOS Compatible		
Logic Coding				Straight Offset Binary		
High Output Voltage, V_{OH}			+2.4		LV_{DD}	V
Low Output Voltage, V_{OL}					+0.4	V
3-State Enable Time	$\overline{OE}$ = L			20	40	ns
3-State Disable Time	$\overline{OE}$ = H			18	10	ns
Internal Pull-Down to Gnd				50		kΩ
Power-Down Enable Time	Pwrdn = L			133		ns
Power-Down Disable Time	Pwrdn = H			18		ns
Internal Pull-Down to Gnd				50		kΩ
ACCURACY	f_S = 2.5MHz					
Gain Error		Full		2.5		%FS
Input Offset(6)		Full		0.4		%FS
Power Supply Rejection (Gain)	Δ V_S = +10%	Full		56		dB
Power Supply Rejection (Offset)		Full		68		dB
External REFT Voltage Range		Full	REFB +0.5	2	V_S–0.8	V
External REFB Voltage Range		Full	0.8	1	REFT –0.5	V
Reference Input Resistance				4		kΩ
POWER SUPPLY REQUIREMENTS						
Supply Voltage: +V_S	Operating	Full	+2.7	+3.0	+3.7	V
Supply Current: +I_S	Operating	Full		16		mA
Power Dissipation	Operating	Full		49	60	mW
Power Dissipation (Power Down)	Operating	Full		15		mW
Thermal Resistance, θ_{JA}						
28-Lead SSOP				89		°C/W

NOTES: (1) The single-ended input range is set by REFB and REFT values. (2) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS is dB relative to full scale. (4) Based on (SINAD - 1.76)/6.02. (5) No "Rollover" of bits. (6) Offset Deviation from Ideal Negative Full Scale.

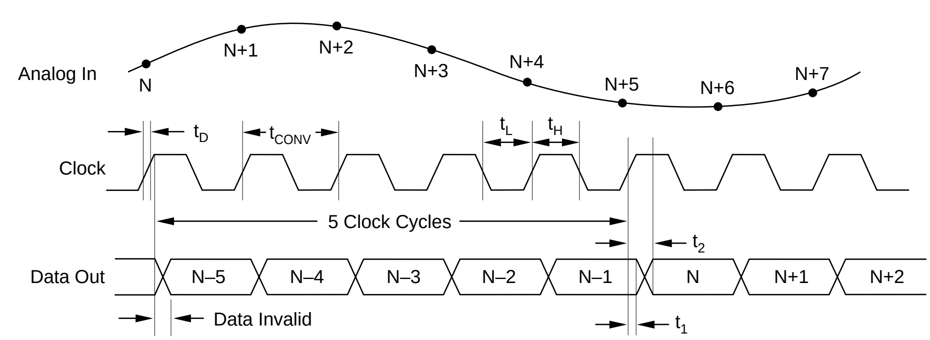
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	$+V_S$	Analog Supply
2	LV_{DD}	Output Logic Driver Supply Voltage
3	Bit 10	Data Bit 10 (D0) (LSB)
4	Bit 9	Data Bit 9 (D1)
5	Bit 8	Data Bit 8 (D2)
6	Bit 7	Data Bit 7 (D3)
7	Bit 6	Data Bit 6 (D4)
8	Bit 5	Data Bit 5 (D5)
9	Bit 4	Data Bit 4 (D6)
10	Bit 3	Data Bit 3 (D7)
11	Bit 2	Data Bit 2 (D8)
12	Bit 1	Data Bit 1 (D9) (MSB)
13	GND	Analog Ground
14	GND	Analog Ground
15	CLK	Convert Clock Input
16	$\overline{OE}$	Output Enable, Active Low
17	Pwrdn	Power Down Pin
18	$+V_S$	Analog Supply
19	GND	Analog Ground
20	GND	Analog Ground
21	LpBy	Positive Ladder Bypass
22	REFT	Top Reference Input
23	NC	No Connection
24	REFB	Bottom Reference Input
25	LnBy	Negative Ladder Bypass
26	CM	Common-Mode Voltage Output
27	IN	Analog Input
28	$+V_S$	Analog Supply

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	50		100µs	ns
t_L	Clock Pulse Low	24	25		ns
t_H	Clock Pulse High	24	25		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, $C_L = 0pF$	3.9			ns
t_2	New Data Delay Time, $C_L = 15pF$ max			12	ns

TYPICAL CHARACTERISTICS

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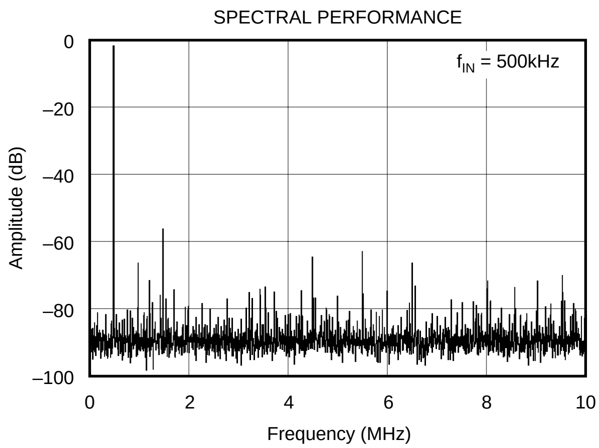
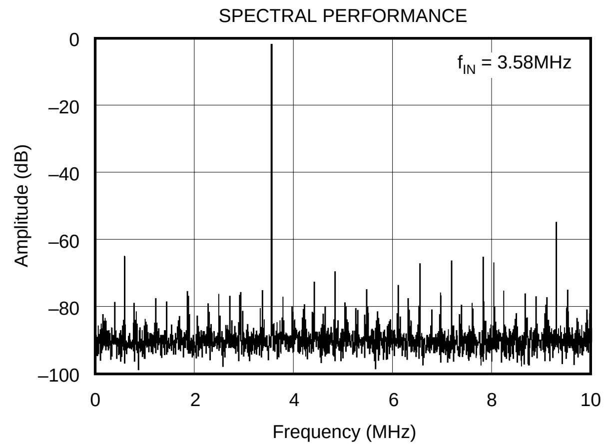
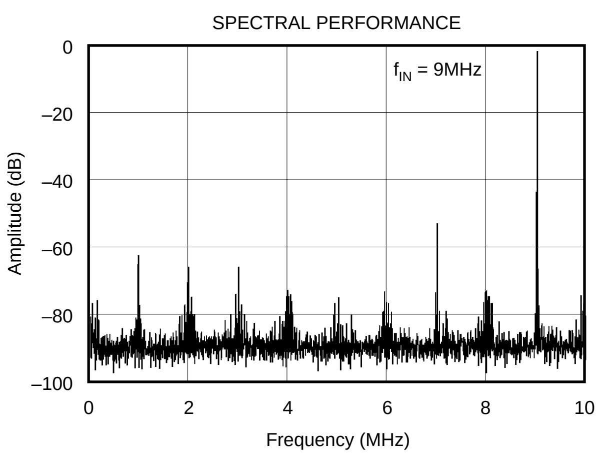
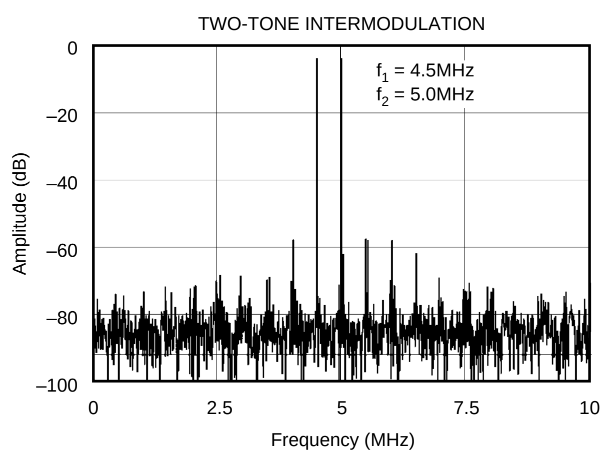
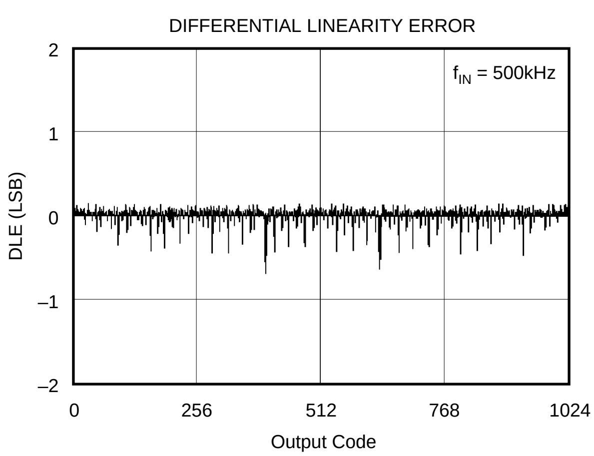
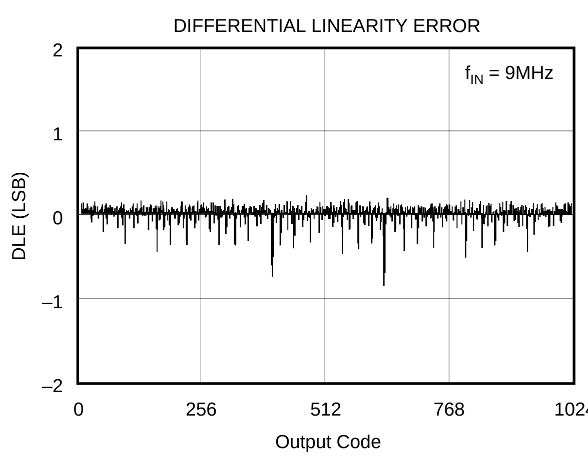








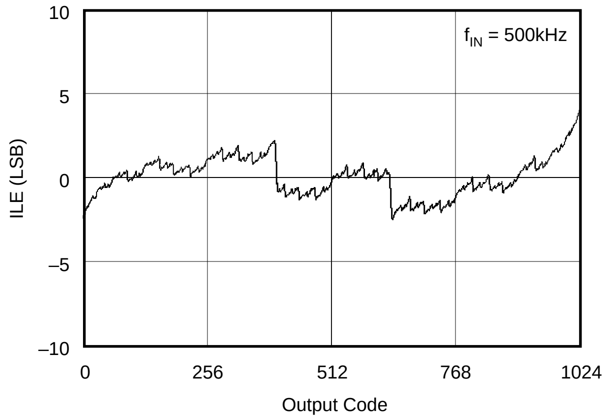




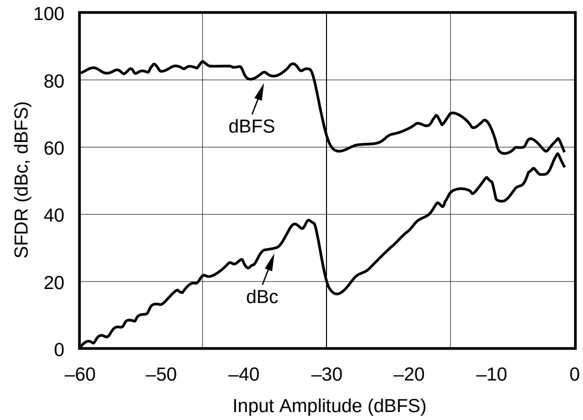
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = Logic V_{DD} = +3V, REFB = 1V, REFT = 2V, Specified Input Range = 1V to 2V, Sampling Rate = 20MHz, unless otherwise specified.

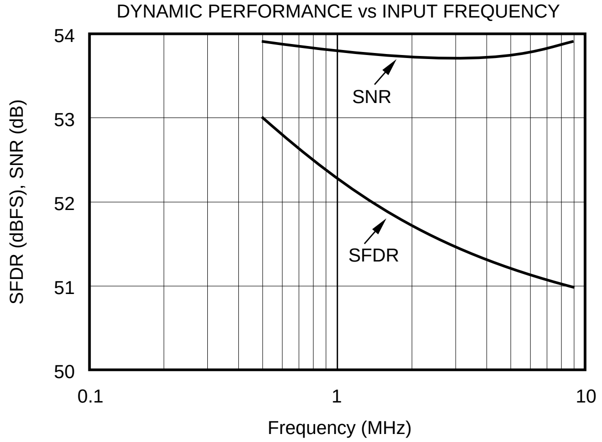
INTEGRAL LINEARITY ERROR



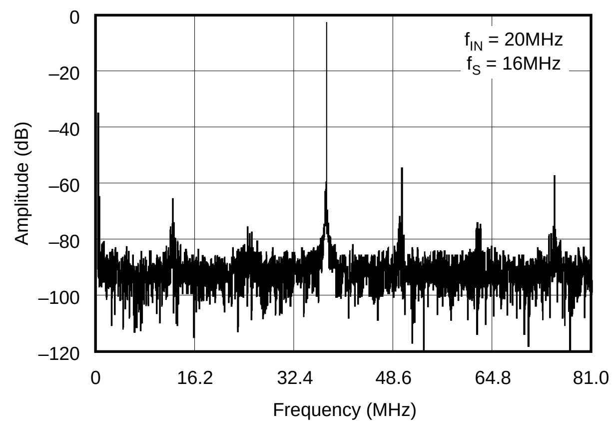
SWEPT POWER SFDR



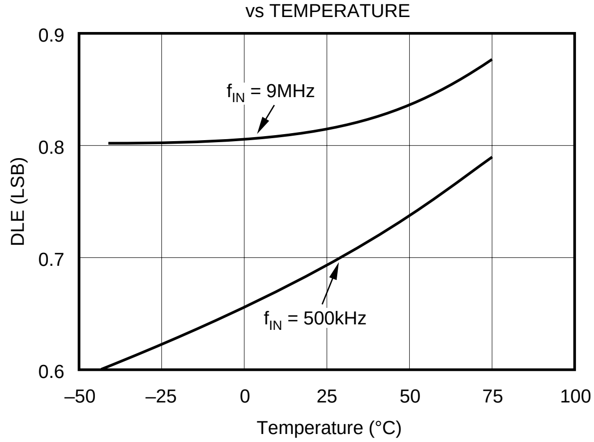
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



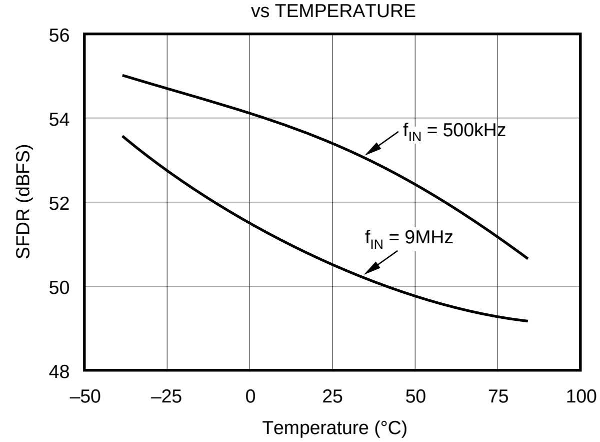
UNDERSAMPLING



DIFFERENTIAL LINEARITY ERROR
vs TEMPERATURE



SPURIOUS FREE DYNAMIC RANGE (SFDR)
vs TEMPERATURE



TYPICAL CHARACTERISTICS (Cont.)

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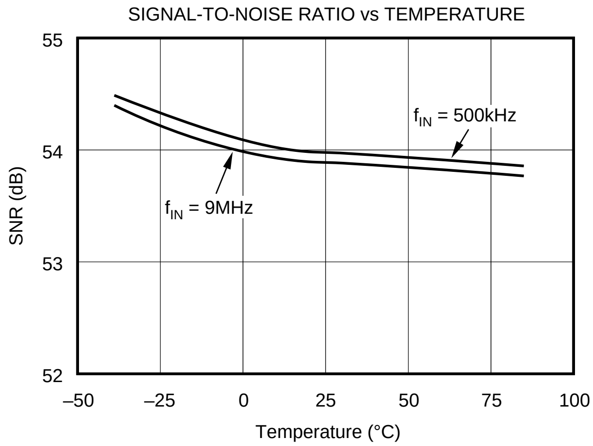

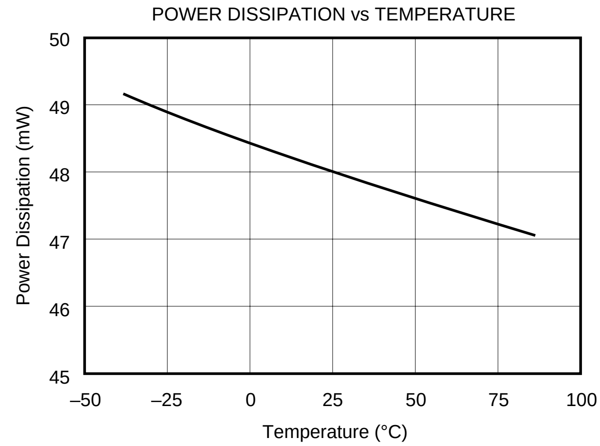

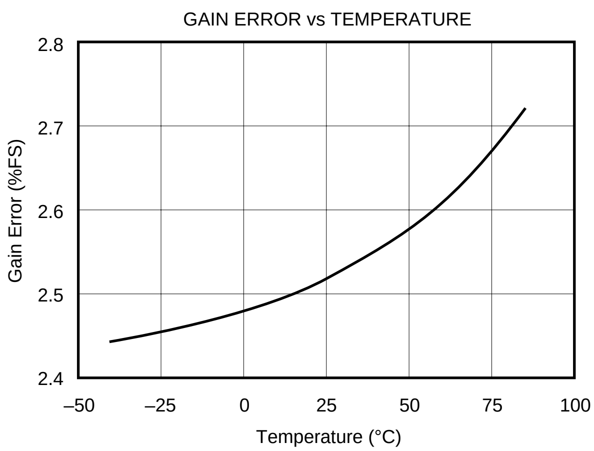

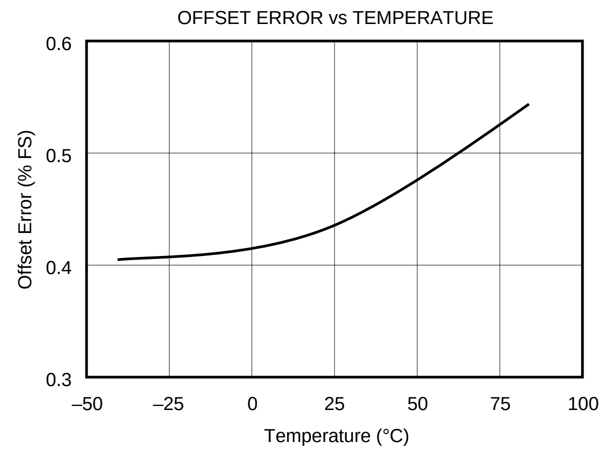

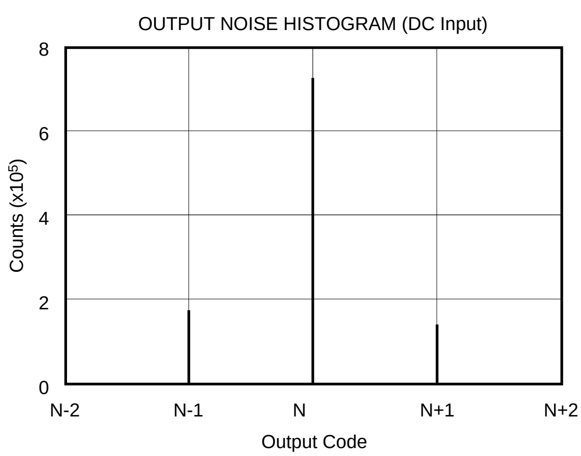

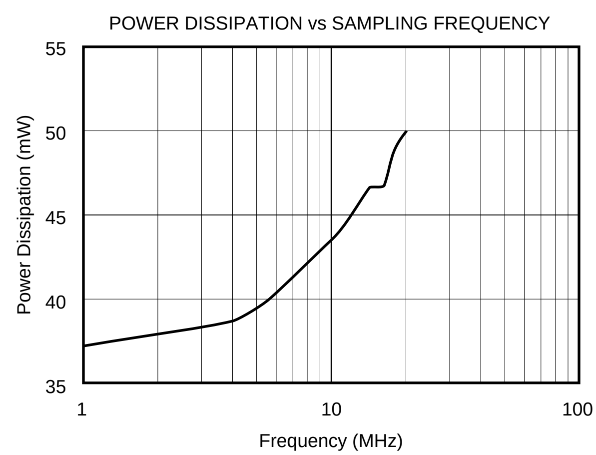

THEORY OF OPERATION

The ADS901 is a high speed sampling analog-to-digital converter that utilizes a pipeline architecture. The fully differential topology and digital error correction guarantee 10-bit resolution. The differential track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi1$ and $\phi2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi1$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track/hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer. Consequently, the input signal-to-noise performance. Other parameters such as small-signal and full-power bandwidth, and wideband noise are also defined in this stage.

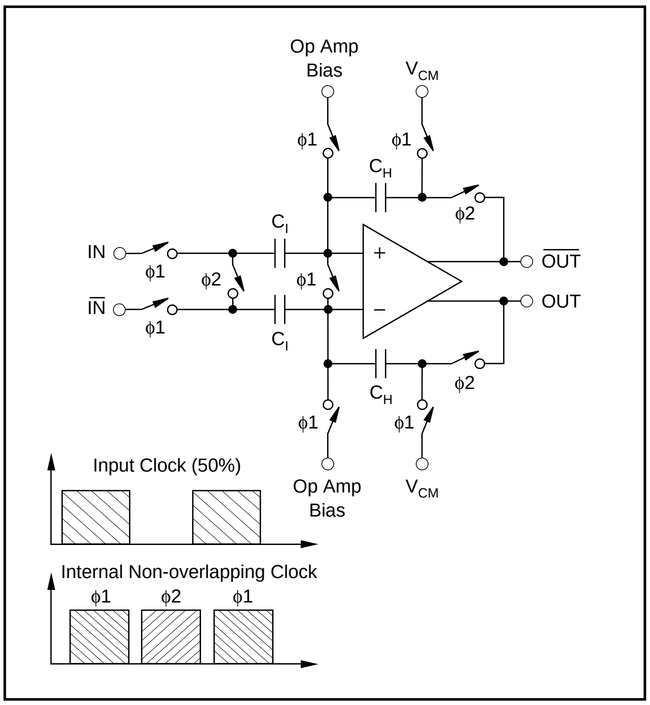

FIGURE 1. Input Track/Hold Configuration with Timing Signals.

The pipelined quantizer architecture has 9 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is the same frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique provides the ADS901 with excellent differential linearity and guarantees no missing codes at the 10-bit level.

To accommodate a bipolar signal swing, the ADS901 operates with a common-mode voltage (V_{CM}) which is derived from the external references. Due to the symmetric resistor ladder inside the ADS901, the V_{CM} is situated between the top and bottom reference voltage. Equation (1) can be used for calculating the common-mode voltage level.

$$V_{CM} = (REFT + REFB)/2 \qquad (1)$$

There is a 5.0 clock cycle data latency from the start convert signal to the valid output data. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. The digital outputs of the ADS901 can be set to a high impedance state by driving the three-state (pin 16) with a logic "HI". Normal operation is achieved with pin 16 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes but is not recommended to be used dynamically.

APPLICATIONS

SIGNAL SWING AND COMMON-MODE CONSIDERATIONS

The ADS901 is designed to operate on a +3V single supply voltage. The nominal input signal swing is 1Vp-p, situated between +1V and +2V. This means that the signal swings ±0.5V around a common-mode voltage of +1.5V, which is half the supply voltage ($V_{CM} = V_S/2$). In some applications it might be advantageous to increase the input signal swing. This will improve the achievable signal-to-noise performance. However, considerations should be made to keep the signal swing within the linear range of operation of the driving circuitry to avoid any excessive distortion. In extreme situations the performance of the converter will start to degrade due to variations of the input's switch on-resistance over the input voltage. Therefore, the signal swing should remain approximately 0.5V away from each rail during normal operation.

DRIVING THE ANALOG INPUTS

AC-COUPLED DRIVER

Figure 2 shows an example of an ac-coupled, single-ended interface circuit using a high-speed op amp that operates on

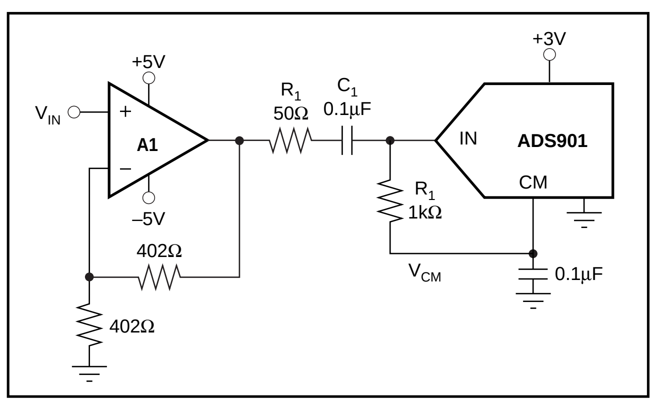

FIGURE 2. AC-Coupled, Single-Ended Interface Circuit.

dual supplies (OPA650, OPA658). The mid-point reference voltage, V_{CM}, biases the bipolar, ground-referenced input signal. The capacitor C_1 and resistor R_1 form a high-pass filter with the –3dB frequency set at

$$f_{-3dB} = 1/(2 \pi R_1 C_1) \quad (2)$$

The values for C_1 and R_1 are not critical in most applications and can be set freely. The values shown correspond to a frequency of 1.6kHz.

Figure 3 depicts a circuit that can be used in single-supply applications. The mid-reference voltage biases the op amp up to the appropriate common-mode voltage, for example V_{CM} = +1.5V. With the use of capacitor C_G the DC gain for the non-inverting op amp input is set to +1V/V. As a result the transfer function is modified to

$$V_{OUT} = V_{IN} \{(1 + R_F/R_G) + V_{CM}\} \quad (3)$$

Again, the input coupling capacitor C_1 and resistor R_1 form a high-pass filter. At the same time the input impedance is defined by R_1. Resistor R_S isolates the op amp's output from the capacitive load to avoid gain peaking or even oscillation. It can also be used to establish a defined bandwidth to reduce the wideband noise. The recommended value is usually between 10Ω and 100Ω.

DC-COUPLED INTERFACE CIRCUIT

Many systems are now requiring +3V single supply capability of both the A/D converter and its driver. Figure 4 shows an example for DC-coupled configuration operating solely on a +3V supply voltage. The OPA632 provides excellent performance in this demanding application. Its wide input and output voltage ranges, an low distortion, supports the ADS901 well. The OPA632 is configured for a gain of +2. The 374Ω and 2.26kΩ resistors at the input level-shift V_{IN} so that V_{OUT} is within the allowed output voltage range when V_{IN} = 0. The input impedance of the driver circuit is set to match to a 50Ω source impedance. The input level-shifting was designed that V_{IN} can be between 0V and 5V, while delivering an output voltage of 1V to 2V into the ADS901. Both the OPA632 and ADS901 have a power-down function pin with the same polarity for those systems the need to conserve power.

EXTERNAL REFERENCE

The ADS901 requires external references on pin 22 (REFT) and 24 (REFB). Internally those pins are connected through a resistor ladder, which has a nominal resistance of 4kΩ (±15%). In order to establish a correct voltage drop across the ladder the external reference circuit must be able to typically supply 250µA of current. With this current the full-scale input range of the ADS901 is set between +1V and +2V, or 1Vp-p. In general, the voltage drop across REFT and REFB determines the input full-scale range (FSR) of the ADS901. Equation (4) can be used to calculate the span.

$$FSR = REFT - REFB \quad (4)$$

Depending on the application, several options are possible to supply the external reference voltages to the ADS901 without degrading the typical performance.

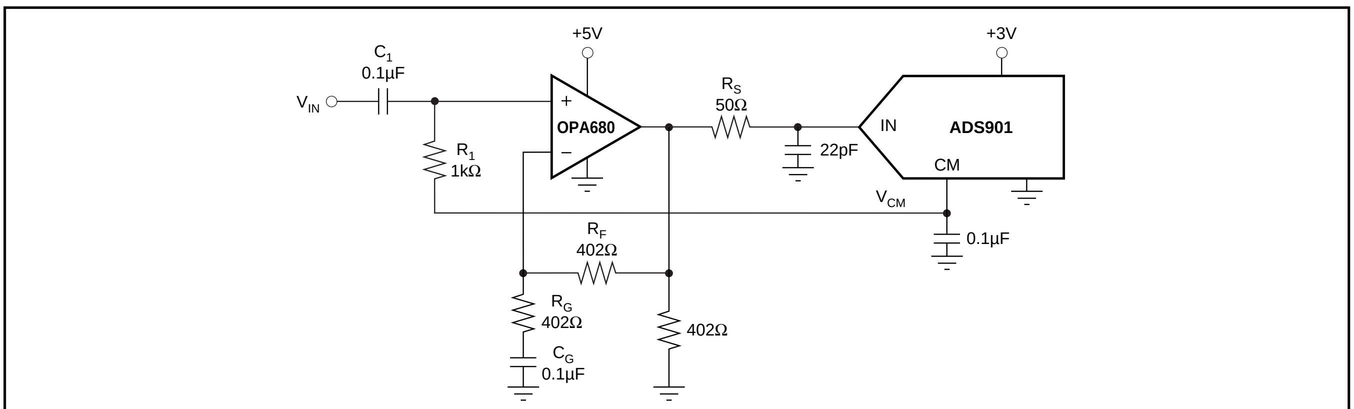

FIGURE 3. Interface Circuit. Example using the voltage feedback amplifier OPA680.

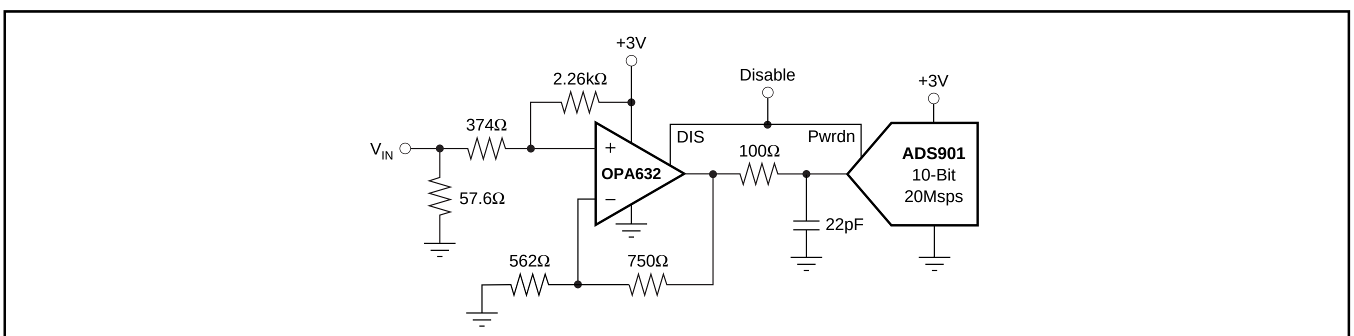

FIGURE 4. DC-Coupled Interface Circuit for +3V Single-Supply Operation.

LOW-COST REFERENCE SOLUTION

The easiest way to achieve the required reference voltages is to place the reference ladder of the ADS901 between the supply rails, as shown in Figure 5. Two additional resistors (R_T, R_B) are necessary to set the correct current through the ladder. However depending on the desired full-scale swing and supply voltage different resistor values might be selected.

The trade-offs, when selecting this reference circuit, are variations in the reference voltages due to component tolerances and power supply variations. In any case, it is recommended to bypass the reference ladder with at least 0.1µF ceramic capacitors, as shown in Figure 5. The capacitors serve a dual purpose. They will bypass most of the high frequency transient noise which results from feedthrough of the clock and switching noise from the T/H stages. Secondly, they serve as a charge reservoir to supply instantaneous current to internal nodes.

SINGLE-ENDED INPUT	STRAIGHT OFFSET BINARY (SOB) PIN 12 FLOATING or LO
+FS (IN = +2V)	1111111111
+FS –1LSB	1111111111
+FS –2LSB	1111111110
+3/4 Full Scale	1110000000
+1/2 Full Scale	1100000000
+1/4 Full Scale	1010000000
+1LSB	1000000001
Bipolar Zero (IN +1.5V)	1000000000
–1LSB	0111111111
–1/4 Full Scale	0110000000
–1/2 Full Scale	0100000000
–3/4 Full Scale	0010000000
–FS +1LSB	0000000001
–FS (IN = +1V)	0000000000

TABLE I. Coding Table for the ADS901.

PRECISE REFERENCE SOLUTION

For those applications requiring a higher level of dc accuracy and drift, a reference circuit with a precision reference element might be used (see Figure 6). A stable +1.2V reference voltage is established by a two terminal bandgap reference diode, the REF1004-1.2. Using a general-purpose single-supply dual operational amplifier (A1), like an OPA2237, OPA2234 or OPA2343, the two required reference voltages for the ADS901 can be generated by setting each op amp to the appropriate gain; for example: set REFT to +2V and REFB to +1V.

CLOCK INPUT

The clock input of the ADS901 is designed to accommodate either +5V or +3V CMOS logic levels. To drive the clock input with a minimum amount of duty cycle variation and support maximum sampling rates (20Msps), high speed or advanced CMOS logic should be used (HC/HCT, AC/ACT). When digitizing at high sampling rates, a 50% duty cycle clock with fast rise and fall times (2ns or less) are recommended to meet the rated performance specifications. However, the ADS901 performance is tolerant to duty cycle variations of as much as ±10% without degradation. For applications operating with input frequencies up to Nyquist or undersampling applications, special consideration must be made to provide a clock with very low jitter. Clock jitter leads to aperture jitter (t_A) which can be the ultimate limitation to achieving good SNR performance. Equation (5) shows the relationship between aperture jitter, input frequency and the signal-to-noise ratio:

$$SNR = 20\log_{10} [1/(2 \pi f_{IN} t_A)] \quad (5)$$

For example, with a 10MHz full-scale input signal and an aperture jitter of t_A = 20ps, the SNR is clock jitter limited to 58dB.

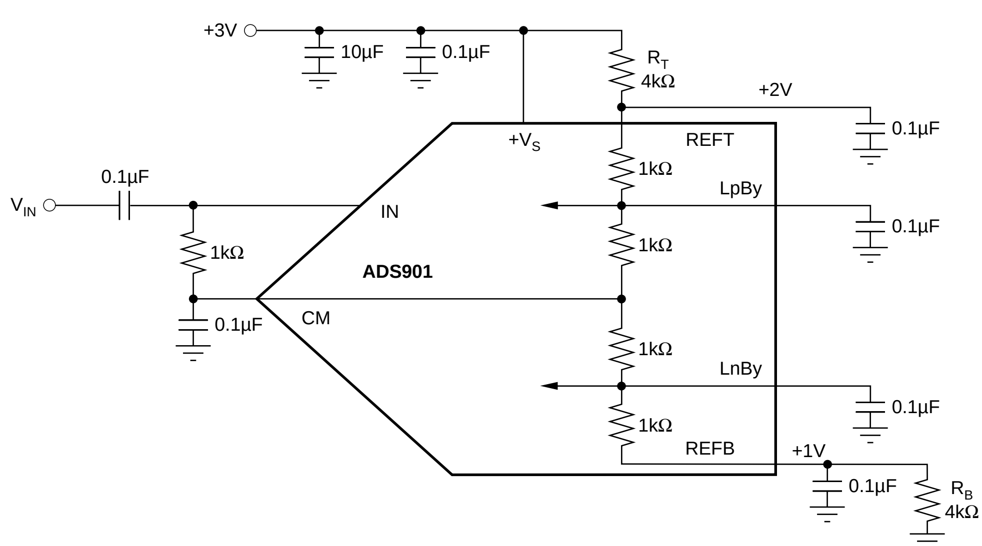

FIGURE 5. Low Cost Solution to Supply External Reference Voltages and Recommended Reference Bypassing.

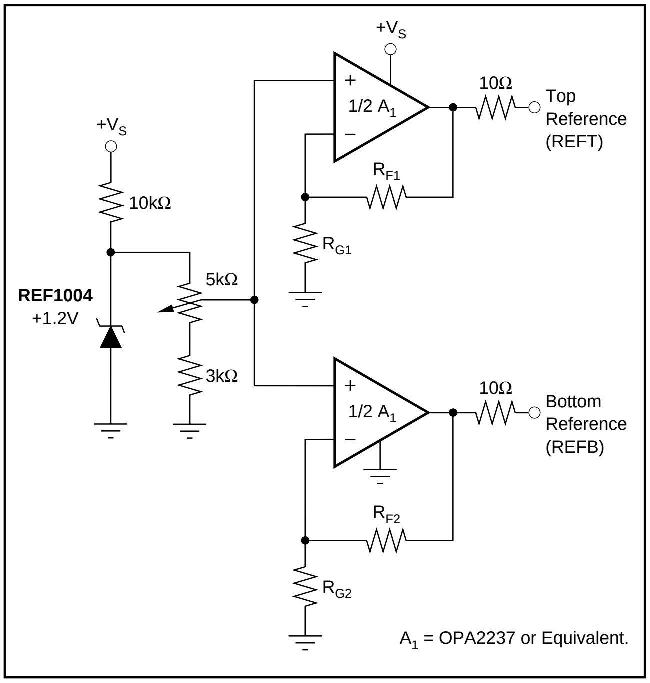

FIGURE 6. Precise Solution to Supply External Reference Voltages.

DIGITAL OUTPUTS

There is a 5.0 clock cycle data latency from the start convert signal to the valid output data. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. The digital outputs of the ADS901 can be set to a high impedance state by driving the three-state (pin 16) with a logic "HI". Normal operation is achieved with pin 16 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes but is not recommended to be used dynamically.

The digital outputs of the ADS901 are standard CMOS stages and designed to be compatible to both high speed TTL and CMOS logic families. The logic thresholds are for low-voltage CMOS: V_{OL} = 0.4V, V_{OH} = 2.4V, which allows the ADS901 to directly interface to 3V-logic. The digital outputs of the ADS901 use a dedicated digital supply pin (pin 2, LV_{DD}). By adjusting the voltage on LV_{DD}, the digital output levels will vary respectively. In any case, it is recommended to limit the fan-out to one, to keep the capacitive loading on the data lines below the specified 15pF. If necessary, external buffers or latches may be used to provide the added benefit of isolating the A/D converter from any digital activities on the bus coupling back high frequency noise and degrading the performance.

POWER-DOWN MODE

The ADS901's low power consumption can be further reduced by initiating a power down mode. For this, the Pwrdn-Pin (Pin 17) must be tied to a logic "High" reducing the current drawn from the supply by approximately 70%. In normal operation the power-down mode is disabled by an internal pull-down resistor (50kΩ).

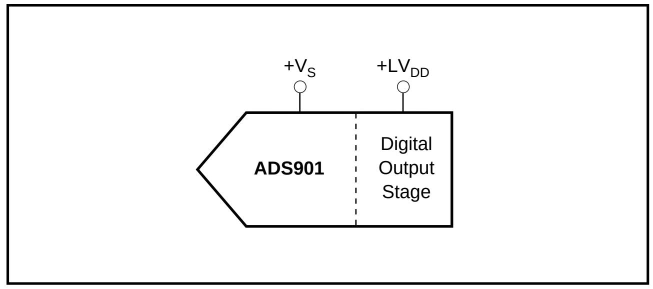

FIGURE 7. Independent Supply Connection for Output Stage.

During power-down the digital outputs are set in 3-state. With the clock applied, the converter does not accurately process the sampled signal. After removing the power-down condition the output data from the following 5 clock cycles is invalid (data latency).

DECOUPLING AND GROUNDING CONSIDERATIONS

The ADS901 converter have several supply pins, one of which is dedicated to supply only the output driver. The remaining supply pins are not, as is often the case, divided into analog and digital supply pins since they are internally connected on the chip. For this reason it is recommended to treat the converter as an analog component and to power it from the analog supply only. Digital supply lines often carry high levels of noise which can couple back into the converter and limit the achievable performance.

Because of the pipeline architecture, the converter also generates high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 8 shows the recommended decoupling scheme for the analog supplies. In most cases 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore they should be located as close to the supply pins as possible.

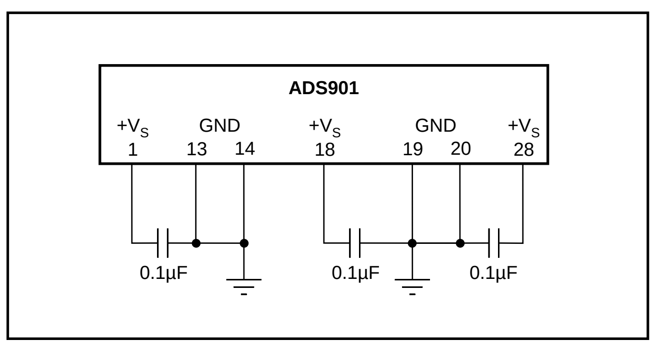

FIGURE 8. Recommended Bypassing for Analog Supply Pins.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS901E	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS901EG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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