Triple-Channel Digital Isolators

Preliminary Technical Data ADuM1300/ADuM1301*

FEATURES

Low Power Operation
- **5V Operation:**
  - **1.0 mA per Channel Max. @ 0–2 Mbps**
  - **3.5 mA per Channel Max. @ 10 Mbps**
- **3V Operation:**
  - **0.7 mA per Channel Max. @ 0–2 Mbps**
  - **2.1 mA per Channel Max. @ 10 Mbps**

Bi-Directional Communication

3/5V Level Translation

High Temperature Operation: 100 °C

High Data Rate: DC – 100 Mbps (NRZ)

Precise Timing Characteristics:
- **2 ns max. Pulse Width Distortion**
- **2 ns max. Channel-Channel Matching**

High Common Mode Transient Immunity: >25 kV/μs

Output Enable Function

Wide Body SOIC 16-Lead Package

Safety and Regulatory Approvals (Pending)
- **UL Recognition**
  - **2500 Vrms for 1 min. per UL 1577**
- **CSA Component Acceptance Notice #5A**
- **VDE Certificate of Conformity**
  - **DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01**
  - **DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000**
  - **V_{IORM} = 560V_{PEAK}**

APPLICATIONS

SPI Interface/Data Converter Isolation

Data Converter Isolation

RS-232/422/485 Transceiver Isolation

Digital Fieldbus Isolation

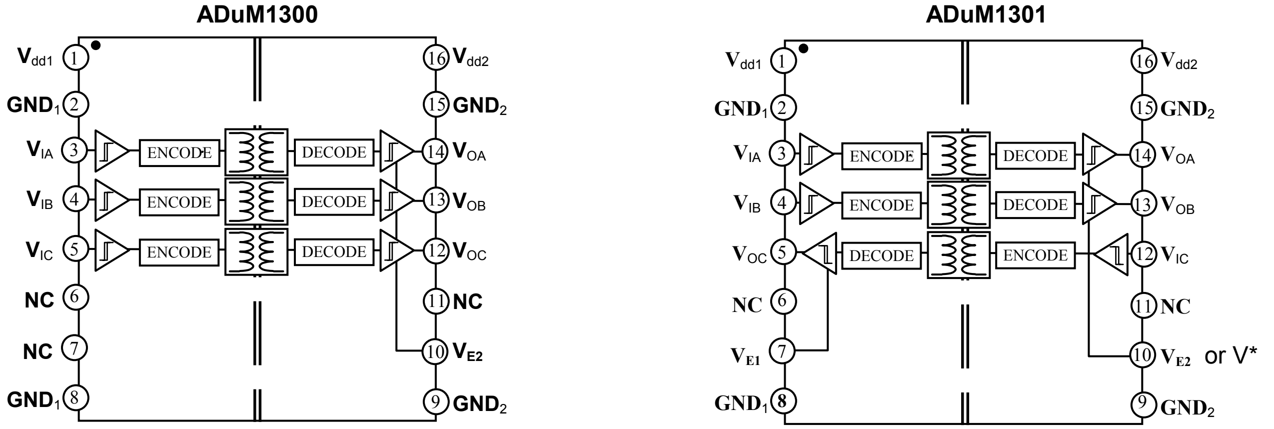
DESCRIPTION

The ADuM130x are three-channel digital isolators based on Analog Devices' *i*Coupler® technology. Combining high-speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, non-linear transfer functions, and temperature and lifetime effects are eliminated with the simple, *i*Coupler digital interfaces and stable performance characteristics. Furthermore, *i*Coupler devices run at one-tenth to one-sixth the power consumption of optocouplers at comparable signal data rates.

The ADuM130x isolators provide three independent isolation channels in a variety of channel configurations and data rates (see Ordering Guide). Both ADuM130x models operate with the supply voltage of either side ranging from 2.7V to 5.5V providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM130x provides low pulse width distortion (<2 ns for CRW grade), and tight channel-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM130x isolators have a patented refresh feature that ensures DC-correctness in the absence of input logic transitions and during power-up/down conditions.

FUNCTIONAL BLOCK DIAGRAMS



Note
For Principles of Operation, See Application Note "Method of Operation, DC Correctness, and Magnetic Field Immunity" in this data sheet.

*Protected by U.S. patent 5,952,849 and 6,525,566. Additional patents are pending.
*i*Coupler is a registered trademark of Analog Devices, Inc.

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ADuM1300/ADuM1301 ELECTRICAL CHARACTERISTICS, 5V OPERATION[1]

4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V. All Min/Max specifications apply over the entire recommended operation range unless otherwise noted. All typical specifications are at T_A = 25 °C, V_{DD1} = V_{DD2} = 5V.

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, quiescent	$I_{DDI(Q)}$		0.50	0.53	mA	
Output Supply Current, per Channel, quiescent	$I_{DDO(Q)}$		0.19	0.21	mA	
ADuM1300, Total Supply Current, Three Channels[2]:						
DC–2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.6	2.1	mA	DC–1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.7	0.8	mA	DC–1 MHz logic signal freq.
10 Mbps (BRW and CRW grades only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		6.5	8.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.9	2.2	mA	5 MHz logic signal freq.
100 Mbps (CRW grade only)						
V_{DD1} Supply Current	$I_{DD1(100)}$		57	77	mA	50 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(100)}$		16	17	mA	50 MHz logic signal freq.
ADuM1301, Total Supply Current, Three Channels[2]:						
DC–2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.3	1.7	mA	DC–1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		1.0	1.3	mA	DC–1 MHz logic signal freq.
10 Mbps (BRW and CRW grades only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		5.0	6.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		3.4	4.2	mA	5 MHz logic signal freq.
100 Mbps (CRW grade only)						
V_{DD1} Supply Current	$I_{DD1(100)}$		43	57	mA	50 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(100)}$		29	37	mA	50 MHz logic signal freq.
For All Models:						
Input Currents	$I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}$	-10	0.01	10	µA	$0 \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or V_{DD2} $0 \leq V_{E1}, V_{E2} \leq V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}			2.0	V	
Logic Low Input Threshold	V_{IL}, V_{EL}	0.8				
Logic High Output Voltages	$V_{OAH}, V_{OBH}, V_{OCH}$	$V_{DD1,2}$ - 0.1	5.0		V	I_{Ox} = -20 µA, $V_{Ix} = V_{IxH}$
		$V_{DD1,2}$ - 0.4	4.8		V	I_{Ox} = -4 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	$V_{OAL}, V_{OBL}, V_{OCL}$		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	I_{Ox} = 400 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$

ELECTRICAL CHARACTERISTICS, 5V OPERATION[1] (continued)

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
ADuM130xARW:						
Minimum Pulse Width[3]	PW			1000	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50		100	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[5]	PWD			40	ns	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L= 15pF,CMOS signal levels
ADuM130xBRW:						
Minimum Pulse Width[3]	PW			100	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20		50	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[5]	PWD			3	ns	C_L= 15pF,CMOS signal levels
Change Versus Temperature			5		ps/ºC	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			15	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			3	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			15	ns	C_L= 15pF,CMOS signal levels
ADuM130xCRW:						
Minimum Pulse Width[3]	PW		6.7	10	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		100	150		Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	18	25	32	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L= 15pF,CMOS signal levels
Change Versus Temperature			3		ps/ºC	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			10	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			2	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			10	ns	C_L= 15pF,CMOS signal levels
For All Models:						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		3	5	ns	C_L= 15pF,CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		3	5	ns	C_L= 15pF,CMOS signal levels
Output Rise/Fall Time (10-90%)	t_R/t_f		2.5		ns	C_L= 15pF,CMOS signal levels
Common Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µS	$V_{Ix}=V_{DD1/DD2}$, V_{CM} = 1000V, transient magnitude = 800V
Common Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µS	V_{Ix} = 0, V_{CM} = 1000V, transient magnitude = 800V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDO(D)}$		0.05		mA/Mbps	

ADuM1300/ADuM1301 ELECTRICAL CHARACTERISTICS, 3V OPERATION[1]

2.7V ≤ V_{DD1} ≤ 3.6V, 2.7V ≤ V_{DD2} ≤ 3.6V. All Min/Max specifications apply over the entire recommended operation range unless otherwise noted. All typical specifications are at T_A = 25 °C, V_{DD1} = V_{DD2} = 3.0V.

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, quiescent	$I_{DDI(Q)}$		0.26	0.31	mA	
Output Supply Current, per Channel, quiescent	$I_{DDO(Q)}$		0.11	0.14	mA	
ADuM1300, Total Supply Current, Three Channels[2]:						
DC–2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.9	1.4	mA	DC–1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.4	0.5	mA	DC–1 MHz logic signal freq.
10 Mbps (BRW and CRW grades only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		3.4	4.9	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.1	1.3	mA	5 MHz logic signal freq.
100 Mbps (CRW grade only)						
V_{DD1} Supply Current	$I_{DD1(100)}$		31	49	mA	50 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(100)}$		8	11	mA	50 MHz logic signal freq.
ADuM1301, Total Supply Current, Three Channels[2]:						
DC–2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.7	1.1	mA	DC–1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.6	0.8	mA	DC–1 MHz logic signal freq.
10 Mbps (BRW and CRW grades only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		2.6	3.7	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		1.8	2.5	mA	5 MHz logic signal freq.
100 Mbps (CRW grade only)						
V_{DD1} Supply Current	$I_{DD1(100)}$		24	36	mA	50 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(100)}$		16	23	mA	50 MHz logic signal freq.
For All Models:						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}	-10	0.01	10	µA	$0 \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or V_{DD2} $0 \leq V_{E1}, V_{E2} \leq V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}			1.6	V	
Logic Low Input Threshold	V_{IL}, V_{EL}	0.4				
Logic High Output Voltages	V_{OAH}, V_{OBH},	$V_{DD1,2}$-0.1	3.0		V	I_{Ox} = -20 µA, $V_{Ix} = V_{IxH}$
	V_{OCH}	$V_{DD1,2}$-0.4	2.8		V	I_{Ox} = -4 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL},		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
	V_{OCL}		0.04	0.1	V	I_{Ox} = 400 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$

ELECTRICAL CHARACTERISTICS, 3V OPERATION[1] (continued)

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
ADuM130xARW:						
Minimum Pulse Width[3]	PW			1000	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50		100	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[5]	PWD			40	ns	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L= 15pF,CMOS signal levels
ADuM130xBRW:						
Minimum Pulse Width[3]	PW			100	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20		50	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[5]	PWD			3	ns	C_L= 15pF,CMOS signal levels
Change Versus Temperature			5		ps/ºC	C_L= 15pF,CMOS signal levels
Propagation Delay Skew (Equal Temperature)[6]	t_{PSK}			22	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			3	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			22	ns	C_L= 15pF,CMOS signal levels
ADuM130xCRW:						
Minimum Pulse Width[3]	PW		6.7	10	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		100	150		Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	34	45	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\|t_{PLH}-t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L= 15pF,CMOS signal levels
Change Versus Temperature			3		ps/ºC	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			16	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			2	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			16	ns	C_L= 15pF,CMOS signal levels
For All Models:						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		3	5	ns	C_L= 15pF,CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		3	5	ns	C_L= 15pF,CMOS signal levels
Output Rise/Fall Time (10-90%)	t_R/t_f		3		ns	C_L= 15pF,CMOS signal levels
Common Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µS	$V_{Ix}=V_{DD1/DD2}$, V_{CM} = 1000V, transient magnitude = 800V
Common Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µS	V_{Ix} = 0, V_{CM} = 1000V, transient magnitude = 800V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDO(D)}$		0.03		mA/Mbps	

ADuM1300/ADuM1301 ELECTRICAL CHARACTERISTICS, Mixed 5/3V or 3/5V OPERATION[1]

5/3V operation: 4.5V ≤ V_{DD1} ≤ 5.5V, 2.7V ≤ V_{DD2} ≤ 3.6V. 3/5V operation: 2.7V≤ V_{DD1} ≤ 3.6V, 4.5V ≤ V_{DD2} ≤ 5.5V. All Min/Max specifications apply over the entire recommended operation range unless otherwise noted.
All typical specifications are at T_A=25°C, V_{DD1} = 3.0V, V_{DD2} = 5V or V_{DD1} = 5V, V_{DD2} = 3.0V.

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, quiescent	$I_{DDI(Q)}$				mA	
5/3V Operation			0.50	0.53	mA	
3/5V Operation			0.26	0.31	mA	
Output Supply Current, per Channel, quiescent	$I_{DDO(Q)}$				mA	
5/3V Operation			0.11	0.14	mA	
3/5V Operation			0.19	0.21	mA	
ADuM1300, Total Supply Current, Three Channels[2]:						
DC–2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5/3V Operation			1.6	2.1	mA	DC–1 MHz logic signal freq.
3/5V Operation			0.9	1.4	mA	DC–1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5/3V Operation			0.4	0.5	mA	DC–1 MHz logic signal freq.
3/5V Operation			0.7	0.8	mA	DC–1 MHz logic signal freq.
10 Mbps (BRW and CRW grades only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5/3V Operation			6.5	8.2	mA	5 MHz logic signal freq.
3/5V Operation			3.4	4.9	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5/3V Operation			1.1	1.3	mA	5 MHz logic signal freq.
3/5V Operation			1.9	2.2	mA	5 MHz logic signal freq.
100 Mbps (CRW grade only)						
V_{DD1} Supply Current	$I_{DD1(100)}$					
5/3V Operation			57	77	mA	50 MHz logic signal freq.
3/5V Operation			31	49	mA	50 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(100)}$					
5/3V Operation			8	11	mA	50 MHz logic signal freq.
3/5V Operation			16	17	mA	50 MHz logic signal freq.
ADuM1301, Total Supply Current, Three Channels[2]:						
DC–2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5/3V Operation			1.3	1.7	mA	DC–1 MHz logic signal freq.
3/5V Operation			0.7	1.1	mA	DC–1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5/3V Operation			0.6	0.8	mA	DC–1 MHz logic signal freq.
3/5V Operation			1.0	1.3	mA	DC–1 MHz logic signal freq.
10 Mbps (BRW and CRW grades only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5/3V Operation			5.0	6.2	mA	5 MHz logic signal freq.
3/5V Operation			2.6	3.7	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5/3V Operation			1.8	2.5	mA	5 MHz logic signal freq.
3/5V Operation			3.4	4.2	mA	5 MHz logic signal freq.
100 Mbps (CRW grade only)						
V_{DD1} Supply Current	$I_{DD1(100)}$					
5/3V Operation			43	57	mA	50 MHz logic signal freq.
3/5V Operation			24	36	mA	50 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(100)}$					
5/3V Operation			16	23	mA	50 MHz logic signal freq.
3/5V Operation			29	37	mA	50 MHz logic signal freq.

ELECTRICAL CHARACTERISTICS, Mixed 5/3V or 3/5V OPERATION[1] (continued)

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
For All Models:						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{E1}, I_{E2}	-10	0.01	10	µA	$0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID} \le V_{DD1}$ or V_{DD2} $0 \le V_{E1}, V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}					
5/3V Operation				2.0	V	
3/5V Operation				1.6	V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5/3V Operation		0.8			V	
3/5V Operation		0.4			V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}	$V_{DD1/2}$-0.1	$V_{DD1/2}$		V	I_{Ox} = -20 µA, $V_{Ix} = V_{IxH}$
		$V_{DD1/2}$-0.4	$V_{DD1/2}$-0.2		V	I_{Ox} = -4 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	I_{Ox} = 400 µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM130xARW:						
Minimum Pulse Width[3]	PW			1000	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50		100	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH}-t_{PHL} \rvert$[5]	PWD			40	ns	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L= 15pF,CMOS signal levels
ADuM130xBRW:						
Minimum Pulse Width[3]	PW			100	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	15		50	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH}-t_{PHL} \rvert$[5]	PWD			3	ns	C_L= 15pF,CMOS signal levels
Change Versus Temperature			5		ps/°C	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			22	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			3	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			22	ns	C_L= 15pF,CMOS signal levels
ADuM130xCRW:						
Minimum Pulse Width[3]	PW		6.7	10	ns	C_L= 15pF,CMOS signal levels
Maximum Data Rate[4]		100	150		Mbps	C_L= 15pF,CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	29	40	ns	C_L= 15pF,CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH}-t_{PHL} \rvert$[5]	PWD		0.5	2	ns	C_L= 15pF,CMOS signal levels
Change Versus Temperature			3		ps/°C	C_L= 15pF,CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			14	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Co-Directional Channels[7]	t_{PSKCD}			2	ns	C_L= 15pF,CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			14	ns	C_L= 15pF,CMOS signal levels
For All Models:						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		3	5	ns	C_L= 15pF,CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		3	5	ns	C_L= 15pF,CMOS signal levels
Output Rise/Fall Time (10-90%)	t_R/t_f					C_L= 15pF,CMOS signal levels
5/3V Operation			3.0		ns	
3/5V Operation			2.5		ns	
Common Mode Transient Immunity at Logic High Output[8]	$\lvert CM_H \rvert$	25	35		kV/µS	$V_{Ix}=V_{DD1/DD2}$, V_{CM} = 1000V, transient magnitude = 800V
Common Mode Transient Immunity at Logic Low Output[8]	$\lvert CM_L \rvert$	25	35		kV/µS	V_{Ix} = 0, V_{CM} = 1000V, transient magnitude = 800V
Refresh Rate	f_r					
5/3V Operation			1.2		Mbps	
3/5V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$					
5/3V Operation			0.19		mA/Mbps	
3/5V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$					
5/3V Operation			0.03		mA/Mbps	
3/5V Operation			0.05		mA/Mbps	

ADuM1300/ADuM1301—ELECTRICAL CHARACTERISTICS

NOTES:

[1] All voltages are relative to their respective ground.

[2] Supply current values are for all three Channels combined running at identical data rates. Output supply current values are are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in "Power Consumption" application note in this data sheet. See TPCs 1-3 for information on per-channel supply current as a function of data rate for unloaded and loaded. See TPCs 4-7 for total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM1300/1301 channel configurations.

[3] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[4] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[5] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[6] t_{PSK} is the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[7] Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[8] CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8V_{DD2}$. CM_L is the maximum common mode voltage slew rate than can be sustained while maintaining $V_O < 0.8V$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[9] Dynamic Supply Current is the incremental amount of supply current required for a 1 Mbps increased in signal data rate.
See TPCs 1-3 for information on per-channel supply current for unloaded and loaded conditions. See "Power Consumption" application note in this data sheet for guidance on calculating per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	$R_{I\text{-}O}$		10^{12}		Ω	
Capacitance (Input-Output)[1]	$C_{I\text{-}O}$		1.7		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		33		°C/W	Thermocouple
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		28		°C/W	located at center of package underside

NOTES:

[1] Device considered a two-terminal device: pins 1, 2, 3,4,5,6,7, and 8 shorted together and pins 9,10,11,12,13,14,15, and 16 shorted together.

REGULATORY INFORMATION

The ADuM130x will be approved by the following organizations upon product release:

UL[1]	CSA	VDE[2]
To be recognized under 1577 component recognition program	To be approved under CSA Component Acceptance Notice #5A	To be approved according to: DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01 DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000

NOTES:

[1] In accordance with UL1577, each ADuM130x is proof tested by applying an insulation test voltage ≥3000 Vrms for 1 second (current leakage detection limit = 5 µA)

[2] In accordance with DIN EN 60747-5-2, each ADuM130x is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V_{RMS}	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.40 min.	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.51 min.	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Gap (Internal Clearance)		0.02 min.	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110,1/89,Table 1)

DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS (PENDING)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110			
for rated mains voltage <= 150Vrms		I - IV	
for rated mains voltage <= 300Vrms		I - III	
for rated mains voltage <= 400Vrms		I - II	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	Vpeak
Input to Output Test Voltage, Method b1 V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1sec, Partial Discharge < 5pC	V_{PR}	1050	Vpeak
Input to Output Test Voltage, Method a	V_{PR}		
After Environmental Tests Subgroup 1) V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5pC		896	Vpeak
After Input and/or Safety Test Subgroup 2/3) V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5pC		672	Vpeak
Highest Allowable Over-Voltage (Transient Over-voltage, t_{TR} =10 sec)	V_{TR}	4000	Vpeak
Safety-limiting values (Maximum value allowed in the event of a failure, also see Thermal Derating Curve, Figure 1)			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	265	mA
Output Current	$I_{S,OUTPUT}$	335	mA
Insulation Resistance at Ts, V_{IO} = 500V	Rs	$>10^9$	Ω

This isolator is suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety date shall be ensured by means of protective circuits.
"*" marking on packages denotes DIN EN 60747-5-2 approval for 560 V_{PEAK} working voltage.

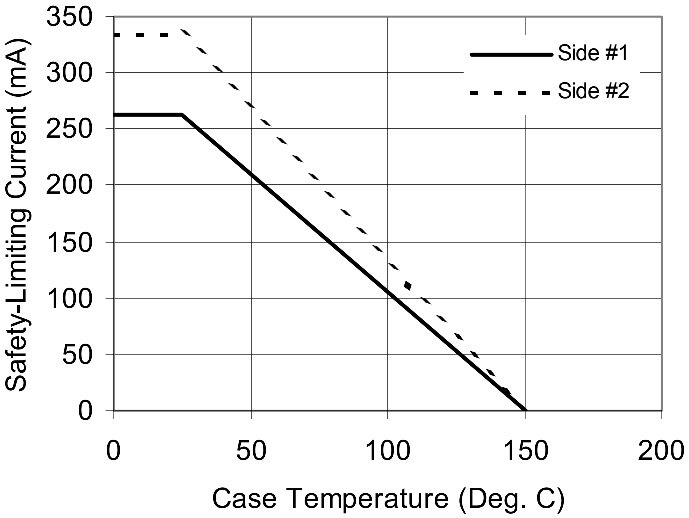


Figure 1. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units
Operating Temperature	T_A	-40	100	°C
Supply Voltages[1]	$V_{DD1,2}$	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

NOTES:

[1] All voltages are relative to their respective ground.

See application note "Method of Operation, DC Correctness, and Magnetic Field Immunity" for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_{ST}	-65	150	°C
Ambient Operating Temperature	T_A	-40	100	°C
Supply Voltages[2]	V_{DD1}, V_{DD2}	-0.5	6.5	V
Input Voltage[2,3]	V_{IA}, V_{IB}, V_{IC}, V_{E1}, V_{E2}	-0.5	V_{DDI}+ 0.5	V
Output Voltage[2,3]	V_{OA}, V_{OB}, V_O	-0.5	V_{DDO}+ 0.5	V
Average Output Current, Per Pin[4]				
Side 1	I_{O1}	-23	23	mA
Side 2	I_{O2}	-30	30	mA
ESD (Human Body Model)		-2.0	2.0	KV
Lead Solder Temperature (Hand Soldering)	Heating at Lead Tip 275°C ±10° for 20 Seconds			
Solder Reflow Temperature Profile	JEDEC Standard 20A			

NOTES:

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Ambient temperature = 25 °C unless otherwise noted.

[2] All voltages are relative to their respective ground.

[3] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.

[4] See Figure 1 for maximum rated current values for various temperatures.

Table I. Truth Table (Positive Logic)

V_{IX} Input[1]	V_{EX} Input	V_{DDI} State[1]	V_{DDO} State[1]	V_{OX} Output[1]	Note
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs returns to input state within 1 µsec of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs returns to input state within 1 µsec of V_{DDO} power restoration if V_{EX} state is H or NC. Outputs returns to high impedance state within 5 ns of V_{DDO} power restoration if V_{EX} state is L.

NOTE:

[1] V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, or C). V_{EX} refers to the output enable signal on the same sie as the V_{OX} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

ORDERING GUIDE

Model	No. Inputs, V_{DD1} Side	No. Inputs, V_{DD2} Side	Max. Data Rate (Mbps)	Max. Propagation Delay, 5V (ns)	Max. Pulse Width Distortion (ns)	Channel-to-Channel Matching, Co-Directional Channels (ns)	Package Description
ADuM1300ARW	3	0	1	100	40	40	16-Lead Wide Body SOIC
ADuM1300BRW	3	0	10	50	3	3	16-Lead Wide Body SOIC
ADuM1300CRW	3	0	100	30	2	2	16-Lead Wide Body SOIC
ADuM1301ARW	2	1	1	100	40	40	16-Lead Wide Body SOIC
ADuM1301BRW	2	1	10	50	3	3	16-Lead Wide Body SOIC
ADuM1301CRW	2	1	100	30	2	2	16-Lead Wide Body SOIC

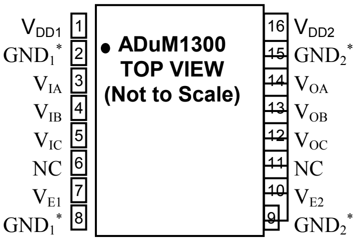
NOTE:

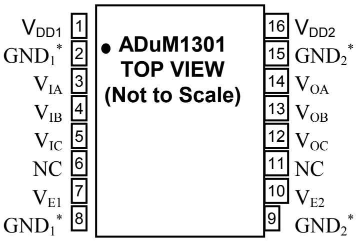
The addition of an "-RL" suffix to any model designates a 13" (1000 units) tape and reel option.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuM130x features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS





NOTE:
* Pins 2 and 8 are internally connected. Connecting both to GND_1 is recommended. Pins 9 and 15 are internally connected. Connecting both to GND_2 is recommended. Output enable pin 7 on ADuM1300 may be left disconnected if outputs are to be always enabled. Output enable pins 7 and 10 on ADuM130 may be left disconnected if outputs are to be always enabled.

Package branding is as follows:

ADuM1300

AD1300xRW

YYWW *
XXXXXX.X

ADUM1301

AD1301xRW

YYWW *
XXXXXX.X

Where:
x = Performance Grade (may be “A”, “B”, or “C” – see Ordering Guide)
RW = Package Designator (RW denotes wide body SOIC)
* = DIN EN 60747-5-2 mark
YYWW = Date Code
XXXXXX.X = Lot Code

PIN FUNCTION DESCRIPTION

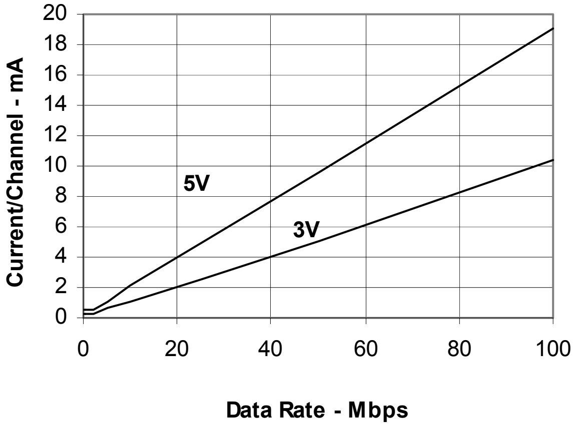
ADUM1300

Pin No.	Mnemonic	Function
1	V_{DD1}	Supply voltage for isolator Side 1, 2.7 – 5.5V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic input A.
4	V_{IB}	Logic input B.
5	V_{IC}	Logic input C.
6	NC	No Connect
7	NC	No Connect
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output enable 2. Active high logic input. V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low.
11	NC	No Connect
12	V_{OC}	Logic output C.
13	V_{OB}	Logic output B.
14	V_{OA}	Logic output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply voltage for isolator Side 1, 2.7 – 5.5V.

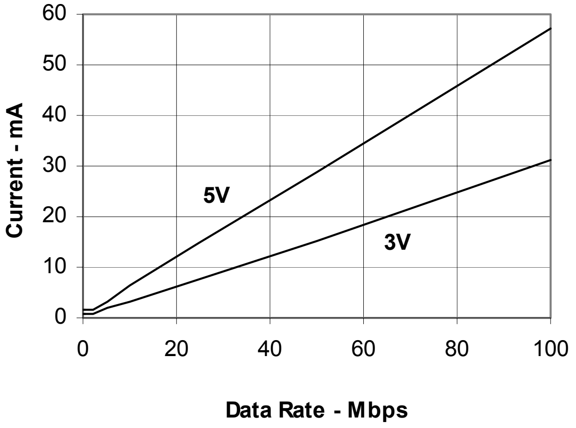
ADUM1301

Pin No.	Mnemonic	Function
1	V_{DD1}	Supply voltage for isolator Side 1, 2.7 – 5.5V.
2	GND_1	Ground 1. Ground reference for isolator Side 1.
3	V_{IA}	Logic input A.
4	V_{IB}	Logic input B.
5	V_{OC}	Logic output C.
6	NC	No Connect
7	V_{E1}	Output enable 1. Active high logic input. V_{OC} output is enabled when V_{E1} is high or disconnected. V_{OC} is disabled when V_{E1} is low.
8	GND_1	Ground 1. Ground reference for isolator Side 1.
9	GND_2	Ground 2. Ground reference for isolator Side 2.
10	V_{E2}	Output enable 2. Active high logic input. V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. V_{OA} and V_{OB} outputs are disabled when V_{E2} is low.
11	NC	No Connect
12	V_{IC}	Logic input C.
13	V_{OB}	Logic output B.
14	V_{OA}	Logic output A.
15	GND_2	Ground 2. Ground reference for isolator Side 2.
16	V_{DD2}	Supply voltage for isolator Side 1, 2.7 – 5.5V.

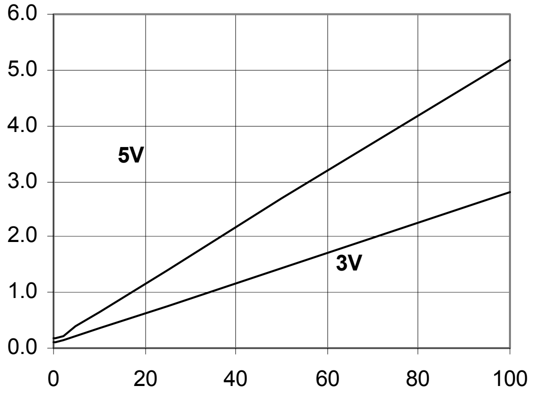
TYPICAL PERFORMANCE CHARACTERISTICS



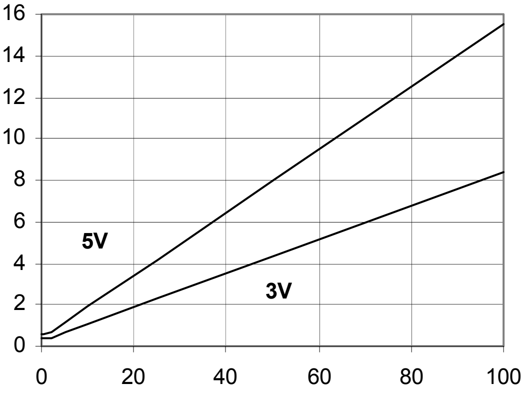
TPC 1. Typical Input Supply Current per Channel vs. Data Rate for 5V and 3V Operation.



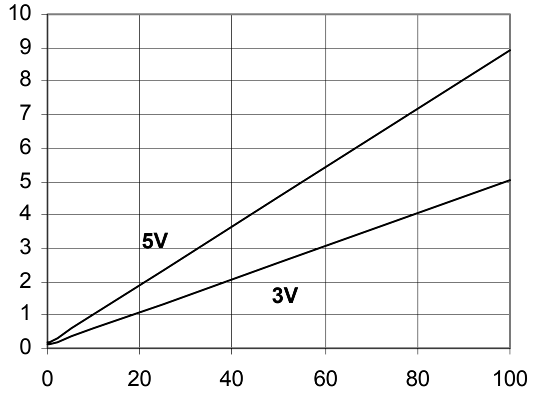
TPC 4. Typical ADuM1300 V_{DD1} Supply Current vs. Data Rate for 5V and 3V Operation.



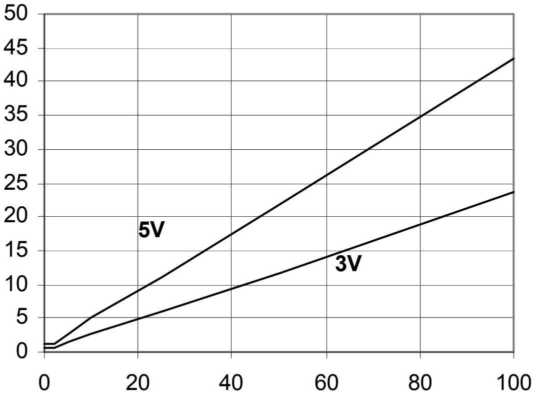
TPC 2. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (No Output Load).



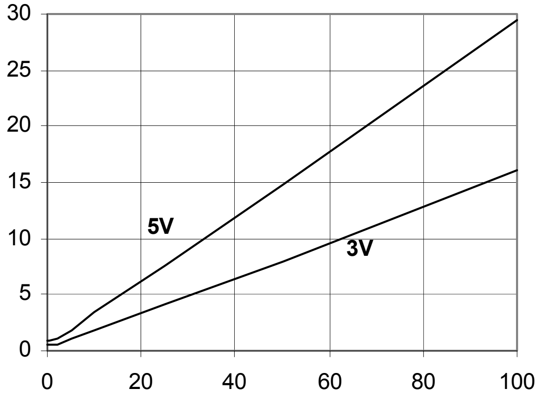
TPC 5. Typical ADuM1300 V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation.



TPC 3. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (15 pF Output Load).



TPC 6. Typical ADuM1301 V_{DD1} Supply Current vs. Data Rate for 5V and 3V Operation.



TPC 7. Typical ADuM1301 V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation.

Application Information:

PC Board Layout

The ADuM130x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (Figure 2). Bypass capacitors are most conveniently connected between Pins 1 and 2 for V_{DD1} and between Pins 15 and 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pins 1 and 8 and between Pins 9 and 16 should also be considered unless the ground pair on each package side are connected close to the package.

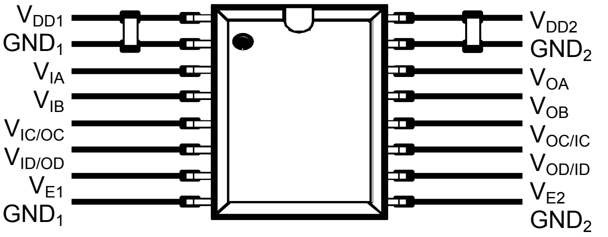


Figure 2. Recommended Printed Circuit Board Layout.

Propagation Delay-Related Parameters

Propagation Delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The propagation delay to a logic Low output may differ from the propagation delay to a logic High.

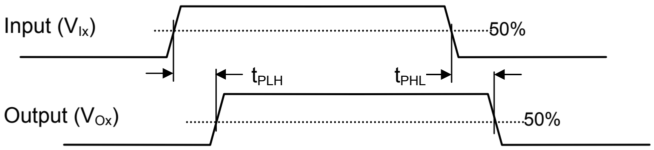


Figure 3. Propagation Delay Parameters.

Pulse Width Distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved. Channel-to-Channel Matching refers to the maximum amount the Propagation Delay differs among channels within a single ADuM130x component. Propagation Delay Skew refers to the maximum amount the Propagation Delay differs among multiple ADuM130x components operated under the same conditions.

DC Correctness and Magnetic Field Immunity

Positive and negative logic transitions at the isolator input cause narrow (~1ns) pulses to be sent via the transformer to the Decoder. The Decoder is bistable and is therefore either Set or Reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than 2 µs, a periodic set of "refresh" pulses indicative of the correct input state are sent to ensure "DC correctness" at the output. If the Decoder receives no pulses for more than about 5 µs, then the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table I) by the Watchdog timer circuit.

The limitation on the ADuM130x's magnetic field immunity is set by the condition in which induced voltage in the transformer's "receiving" coil is sufficiently large to either falsely set or reset the Decoder. The analysis below defines the conditions under which this may occur. The ADuM130x's 3V operating condition is examined as it represents the most susceptible mode of operation: The pulses at the transformer output have an amplitude greater than 1.0V. The Decoder has a sensing thresholds at about 0.5V therefore establishing a 0.5V margin in which induced voltages can be tolerated. The induced voltage induced across the "receiving" coil is given by:

$$V = (-d\beta/dt)\Sigma\pi r_n^2;\ n = 1,2,\ldots,N$$

where:

β = magnetic flux density (Gauss)

N = number of turns in receiving coil

r_n = radius of nth turn in receiving coil (cm)

Given the geometry of the receiving coil in the ADuM130x and an imposed requirement that the induced voltage be at most 50% of the 0.5V margin at the Decoder, a maximum allowable magnetic field is calculated as shown in figure below.

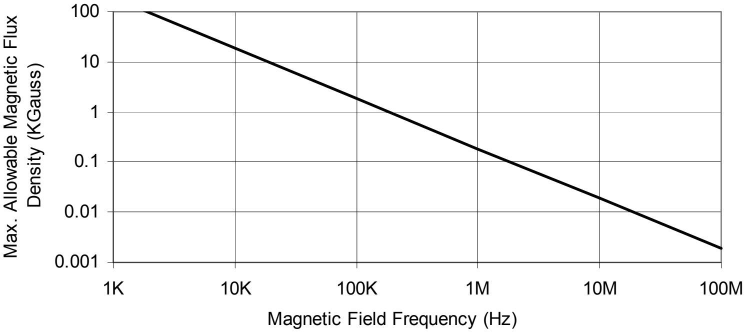


Figure 4. Max. Allowable External Magnetic Flux Density.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 KGauss induces a voltage of 0.25V at the receiving coil. This is about 50% of the sensing threshold and will not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst case polarity) it would reduce the received pulse from > 1.0V to 0.75V – still well above the 0.5V sensing threshold of the Decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM130x transformers. Figure 5 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM130x is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, one would have to place a current of 0.5 kA 5 mm away from the ADuM130x to affect the component's operation.

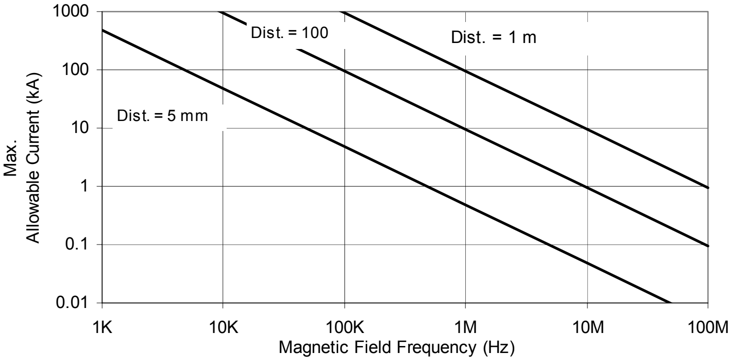


Figure 5. Maximum Allowable Current for Various Current-to-ADuM130x Spacings.

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

Power Consumption

The supply current at a given channel of the ADuM140x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by:

$I_{DDI} = I_{DDI(Q)} \qquad f \leq 0.5f_r$

$I_{DDI} = I_{DDI(D)}*(2f - f_r)+I_{DDI(Q)} \qquad f > 0.5f_r$

For each output channel, the supply current is given by:

$I_{DDO} = I_{DDO(Q)} \qquad f \leq 0.5f_r$

$I_{DDO} = (I_{DDO(D)}+ C_L V_{DDO})*(2f-f_r)+I_{DDO(Q)} \qquad f > 0.5f_r$

where:

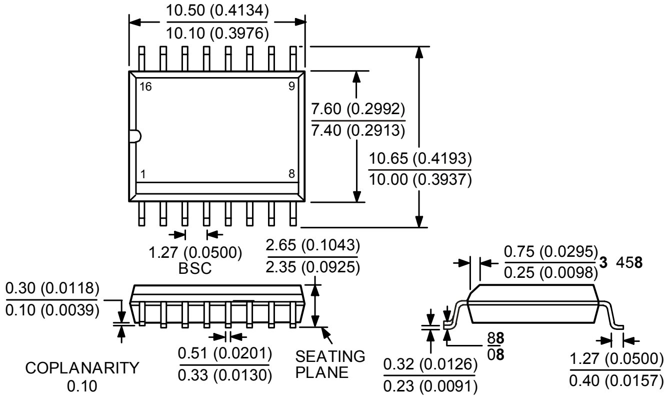
$I_{DDI(D)}$, $I_{DDO(D)}$:	input and output dynamic supply current per channel (mA/Mbps)
C_L:	output load capacitance (pF)
V_{DDO}:	output supply voltage (V)
f:	input logic signal frequency (Hz, half of the input data rate, NRZ signaling)
f_r:	input stage refresh rate (bps)
$I_{DDI(Q)}$, $I_{DDO(Q)}$:	specified input and output quiescent supply current

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. TPCs 1 and 2 provide per-channel supply currents as a function of data rate for an unloaded output condition. TPC 3 provides per-channel supply current as a function of data rate for a 15 pF output condition. TPCs 4-7 provide total I_{DD1} and I_{DD2} supply current as a function of data rate for ADuM1300/1 channel configurations.

Package Outline Drawing:

16-Lead Small Outline, Wide Body
(RW-16)

Dimensions are in mm and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN