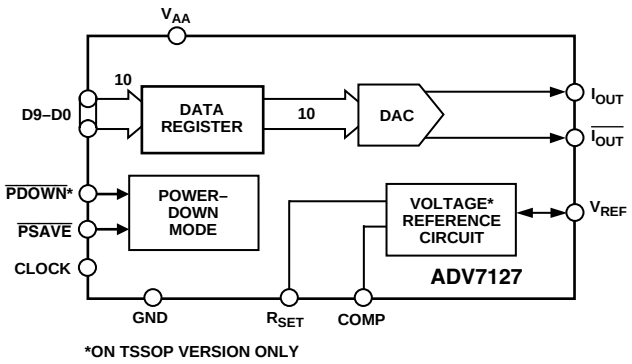
CMOS, 240 MHz 10-Bit High Speed Video DAC

ADV7127

FEATURES
240 MSPS Throughput Rate
10-Bit D/A Converters
SFDR
–70 dB typ: f_{CLK} = 50 MHz; f_{OUT} = 1 MHz
–53 dB typ: f_{CLK} = 140 MHz; f_{OUT} = 40 MHz
RS-343A/RS-170 Compatible Output
Complementary Outputs
DAC Output Current Range: 2 mA to 26 mA
TTL Compatible Inputs
Internal Voltage Reference (1.23 V) on TSSOP Package
Single Supply +5 V/+3.3 V Operation
28-Lead SOIC Package and 24-Lead TSSOP Package
Low Power Dissipation (30 mW min @ 3 V)
Low Power Standby Mode (10 mW min @ 3 V)
Power-Down Mode (60 mW min @ 3 V)
Power-Down Mode Available on TSSOP Package
Industrial Temperature Range (–40°C to +85°C)

APPLICATIONS
Digital Video Systems (1600 × 1200 @ 100 Hz)
High Resolution Color Graphics
Digital Radio Modulation
Image Processing
Instrumentation
Video Signal Reconstruction
Direct Digital Synthesis (DDS)
Wireless LAN

FUNCTIONAL BLOCK DIAGRAM



*ON TSSOP VERSION ONLY

GENERAL DESCRIPTION

The ADV7127 (ADV®) is a high speed, digital-to-analog convertor on a single monolithic chip. It consists of a 10-bit, video D/A converter with on-board voltage reference, complementary outputs, a standard TTL input interface and high impedance analog output current sources.

The ADV7127 has a 10-bit wide input port. A single +5 V/ +3.3 V power supply and clock are all that are required to make the part functional.

The ADV7127 is fabricated in a CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7127 is available in a small outline 28-lead SOIC or 24-lead TSSOP package.

The ADV7127 TSSOP package also has a power-down mode. Both ADV7127 packages have a power standby mode.

The ADV7127 TSSOP package has an on-board voltage reference circuit. The ADV7127 SOIC package requires an external reference.

PRODUCT HIGHLIGHTS

1. 240 MSPS Throughput.
2. Guaranteed monotonic to 10 bits.
3. Compatible with a wide variety of high resolution color graphics systems including RS-343A and RS-170A.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADV7127–SPECIFICATIONS

5 V SOIC SPECIFICATIONS (V_{AA} = +5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)	10			Bits	
Integral Nonlinearity (BSL)	–1	0.4	+1	LSB	
Differential Nonlinearity	–1	0.25	+1	LSB	Guaranteed Monotonic
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current, I_{IN}	–1		+1	μA	V_{IN} = 0.0 V or V_{AA}
PSAVE Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		18.5	mA	
Output Compliance Range, V_{OC}	0		+1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		10		pF	I_{OUT} = 0 mA
Offset Error	–0.025		+0.025	% FSR	Tested with DAC Output = 0 V
Gain Error[2]	–5.0		+5.0	% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE (Ext.)					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
POWER DISSIPATION					
Digital Supply Current[3]		3.4	9	mA	f_{CLK} = 50 MHz
Digital Supply Current[3]		10.5	15	mA	f_{CLK} = 140 MHz
Digital Supply Current[3]		18	25	mA	f_{CLK} = 240 MHz
Analog Supply Current		33	37	mA	R_{SET} = 560 Ω
Analog Supply Current		5		mA	R_{SET} = 4933 Ω
Standby Supply Current[4]		2.1	5.0	mA	PSAVE = Low, Digital and Control Inputs at V_{AA}
Power Supply Rejection Ratio		0.1	0.5	%/%	

NOTES

[1]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.

[2]Gain error = ((Measured (FSC)/Ideal (FSC) –1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times (3FFH)$ and K = 7.9896.

[3]Digital supply is measured with continuous clock with data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

[4]These max/min specifications are guaranteed by characterization to be over 4.75 V to 5.25 V range.

Specifications subject to change without notice.

5 V TSSOP SPECIFICATIONS

(V_{AA} = +5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)	10			Bits	
Integral Nonlinearity (BSL)	–1	0.4	+1	LSB	
Differential Nonlinearity	–1	0.25	+1	LSB	Guaranteed Monotonic
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
PDOWN Input High Voltage[2]		3		V	
PDOWN Input Low Voltage[2]		1		V	
Input Current, I_{IN}	–1		+1	μA	V_{IN} = 0.0 V or V_{AA}
PSAVE Pull-Up Current		20		μA	
PDOWN Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		18.5	mA	
Output Compliance Range, V_{OC}	0		+1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		10		pF	I_{OUT} = 0 mA
Offset Error	–0.025		+0.025	% FSR	Tested with DAC Output = 0 V
Gain Error[3]	–5.0		+5.0	% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE (Ext. and Int.)[4]					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
POWER DISSIPATION					
Digital Supply Current[5]		1.5	3	mA	f_{CLK} = 50 MHz
Digital Supply Current[5]		4	6	mA	f_{CLK} = 140 MHz
Digital Supply Current[5]		6.5	10	mA	f_{CLK} = 240 MHz
Analog Supply Current		23	27	mA	R_{SET} = 560 Ω
Analog Supply Current		5		mA	R_{SET} = 4933 Ω
Standby Supply Current[6]		3.8	6	mA	PSAVE = Low, Digital and Control Inputs at V_{AA}
PDOWN Supply Current[2]		1		mA	
Power Supply Rejection Ratio		0.1	0.5	%/%	

NOTES

[1]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.

[2]This power-down feature is only available on the ADV7127 in the TSSOP package.

[3]Gain error = ((Measured (FSC)/Ideal (FSC) –1) × 100), where Ideal = V_{REF} /R_{SET} × K × (3FFH) and K = 7.9896.

[4]Internal voltage reference is available only on the ADV7127 TSSOP package.

[5]Digital supply is measured with continuous clock with data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

[6]These max/min specifications are guaranteed by characterization to be over 4.75 V to 5.25 V range.

Specifications subject to change without notice.

ADV7127–SPECIFICATIONS

3.3 V SOIC SPECIFICATIONS[1] (V_{AA} = +3.0 V–3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)			10	Bits	R_{SET} = 680 Ω
Integral Nonlinearity (BSL)	–1	0.5	+1	LSB	R_{SET} = 680 Ω
Differential Nonlinearity	–1	0.25	+1	LSB	R_{SET} = 680 Ω
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}		0.8		V	
Input Current, I_{IN}	–1		+1	μA	V_{IN} = 0.0 V or V_{DD}
PSAVE Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		18.5	mA	
Output Compliance Range, V_{OC}	0		+1.4	V	
Output Impedance, R_{OUT}		70		kΩ	
Output Capacitance, C_{OUT}		10		pF	
Offset Error		0	0	% FSR	Tested with DAC Output = 0 V
Gain Error[3]		0		% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE (Ext.)					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
POWER DISSIPATION					
Digital Supply Current[4]		2.2	5.0	mA	f_{CLK} = 50 MHz
Digital Supply Current[4]		6.5	12.0	mA	f_{CLK} = 140 MHz
Digital Supply Current[4]		11	15	mA	f_{CLK} = 240 MHz
Analog Supply Current		32	35	mA	R_{SET} = 560 Ω
Analog Supply Current		5		mA	R_{SET} = 4933 Ω
Standby Supply Current		2.4	5.0	mA	PSAVE = Low, Digital and Control Inputs at V_{DD}
Power Supply Rejection Ratio		0.1	0.5	%/%	

NOTES

[1]These max/min specifications are guaranteed by characterization to be over 3.0 V to 3.6 V range.

[2]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.

[3]Gain error = ((Measured (FSC)/Ideal (FSC) –1) × 100) , where Ideal = $V_{REF}/R_{SET} \times K \times$ (3FFH) and K = 7.9896.

[4]Digital supply is measured with continuous clock with data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

Specifications subject to change without notice.

3.3 V TSSOP SPECIFICATIONS[1] (V_{AA} = +3.0 V–3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)			10	Bits	R_{SET} = 680 Ω
Integral Nonlinearity (BSL)	–1	0.5	+1	LSB	R_{SET} = 680 Ω
Differential Nonlinearity	–1	0.25	+1	LSB	R_{SET} = 680 Ω
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}		0.8		V	
PDOWN Input High Voltage[3]		2.1		V	
PDOWN Input Low Voltage[3]		0.6		V	
Input Current, I_{IN}	–1		+1	μA	V_{IN} = 0.0 V or V_{DD}
PSAVE Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		18.5	mA	
Output Compliance Range, V_{OC}	0		+1.4	V	
Output Impedance, R_{OUT}		70		kΩ	
Output Capacitance, C_{OUT}		10		pF	
Offset Error		0	0	% FSR	Tested with DAC Output = 0 V
Gain Error[4]		0		% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE (Ext.)					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
VOLTAGE REFERENCE (Int.)[5]					
Reference Range, V_{REF}		1.235		V	
POWER DISSIPATION					
Digital Supply Current[6]		1	2	mA	f_{CLK} = 50 MHz
Digital Supply Current[6]		2.5	4.5	mA	f_{CLK} = 140 MHz
Digital Supply Current[6]		4	6	mA	f_{CLK} = 240 MHz
Analog Supply Current		22	25	mA	R_{SET} = 560 Ω
Analog Supply Current		5		mA	R_{SET} = 4933 Ω
Standby Supply Current		2.6	3	mA	PSAVE = Low, Digital and Control Inputs at V_{DD}
PDOWN Supply Current		20		μA	
Power Supply Rejection Ratio		0.1	0.5	%/%	

NOTES

[1]These max/min specifications are guaranteed by characterization to be over 3.0 V to 3.6 V range.

[2]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.

[3]This power-down feature is only available on the ADV7127 in the TSSOP package.

[4]Gain error = ((Measured (FSC)/Ideal (FSC) –1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times$ (3FFH) and K = 7.9896.

[5]Internal voltage reference is available only on the ADV7127 TSSOP package.

[6]Digital supply is measured with continuous clock with data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

Specifications subject to change without notice.

ADV7127–SPECIFICATIONS

5 V/3.3 V DYNAMIC SPECIFICATIONS

(V_{AA} = (3 V–5.25 V)[1], V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications are for T_A = +25°C unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units
DAC PERFORMANCE				
Glitch Impulse[2, 3]		10		pVs
Data Feedthrough[2, 3]		22		dB
Clock Feedthrough[2, 3]		33		dB

NOTES
[1]These max/min specifications are guaranteed by characterization.
[2]TTL input values are for 0 V and 3 V with input rise/fall times ≤3 ns, measured at the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.

Specifications subject to change without notice.

5 V TIMING SPECIFICATIONS[1]

(V_{AA} = +5 V ± 5%[2], V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units	Condition
ANALOG OUTPUTS					
Analog Output Delay, t_6		5.5		ns	
Analog Output Rise/Fall Time, t_7[4]		1.0		ns	
Analog Output Transition Time, t_8[5]		15		ns	
Analog Output Skew, t_9[6]		1	2	ns	
CLOCK CONTROL					
f_{CLK}[7]	0.5		50	MHz	50 MHz Grade
f_{CLK}[7]	0.5		140	MHz	140 MHz Grade
f_{CLK}[7]	0.5		240	MHz	240 MHz Grade
Data and Control Setup, t_1	1.5			ns	
Data and Control Hold, t_2	2.5			ns	
Clock Pulsewidth High, t_4	1.875	1.1		ns	f_{MAX} = 240 MHz
Clock Pulsewidth Low t_5	1.875	1.25		ns	f_{MAX} = 240 MHz
Clock Pulsewidth High t_4	2.85			ns	f_{MAX} = 140 MHz
Clock Pulsewidth Low t_5	2.85			ns	f_{MAX} = 140 MHz
Clock Pulsewidth High t_4	8.0			ns	f_{MAX} = 50 MHz
Clock Pulsewidth Low t_5	8.0			ns	f_{MAX} = 50 MHz
Pipeline Delay, t_{PD}[6]	1.0	1.0	1.0	Clock Cycles	
PSAVE Up Time, t_{10}[6]		2	10	ns	
PDOWN Up Time, t_{11}[8]		320		ns	

NOTES
[1]Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) 0 for both 5 V and 3.3 V supplies.
[2]These maximum and minimum specifications are guaranteed over this range.
[3]Temperature range: T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.
[4]Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5]Measured from 50% point of full-scale transition to 2% of final value.
[6]Guaranteed by characterization.
[7]f_{CLK} max specification production tested at 125 MHz and 5 V. Limits specified here are guaranteed by characterization.
[8]This power-down feature is only available on the ADV7127 in the TSSOP package.

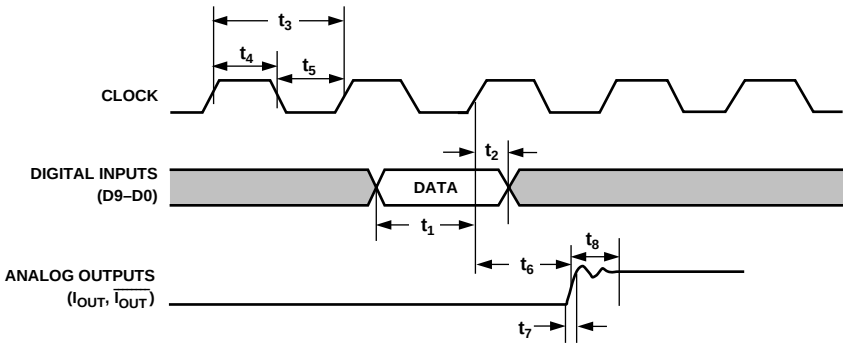
Specifications subject to change without notice.

3.3 V TIMING SPECIFICATIONS[1] (V_{AA} = +3.0 V–3.6 V[2], V_{REF} = 1.235 V, R_{SET} = 560 Ω. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted, $T_{J\ MAX}$ = 110°C)

Parameter	Min	Typ	Max	Units	Condition
ANALOG OUTPUTS					
Analog Output Delay, t_6		7.5		ns	
Analog Output Rise/Fall Time, t_7[4]		1.0		ns	
Analog Output Transition Time, t_8[5]		15		ns	
Analog Output Skew, t_9[6]		1	2	ns	
CLOCK CONTROL					
f_{CLK}[7]			50	MHz	50 MHz Grade
f_{CLK}[7]			140	MHz	140 MHz Grade
f_{CLK}[7]			240	MHz	240 MHz Grade
Data and Control Setup, t_2[6]	1.5			ns	
Data and Control Hold, t_2[6]	2.5			ns	
Clock Pulsewidth High, t_4		1.1		ns	f_{MAX} = 240 MHz
Clock Pulsewidth Low t_5[6]		1.4		ns	f_{MAX} = 240 MHz
Clock Pulsewidth High t_4[6]	2.85			ns	f_{MAX} = 140 MHz
Clock Pulsewidth Low t_5[6]	2.85			ns	f_{MAX} = 140 MHz
Clock Pulsewidth High t_4[6]	8.0			ns	f_{MAX} = 50 MHz
Clock Pulsewidth Low t_5[6]	8.0			ns	f_{MAX} = 50 MHz
Pipeline Delay, t_{PD}[6]	1.0	1.0	1.0	Clock Cycles	
PSAVE Up Time, t_{10}[6]		4	10	ns	
PDOWN Up Time, t_{11}[8]		320		ns	

NOTES
[1]Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) 0 for both 5 V and 3.3 V supplies.
[2]These maximum and minimum specifications are guaranteed over this range.
[3]Temperature range: T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.
[4]Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5]Measured from 50% point of full-scale transition to 2% of final value.
[6]Guaranteed by characterization.
[7]f_{CLK} max specification production tested at 125 MHz and 5 V limits specified here are guaranteed by characterization.
[8]This power-down feature is only available on the ADV7127 in the TSSOP package.

Specifications subject to change without notice.



NOTES:
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.
3. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.

Figure 1. Timing Diagram

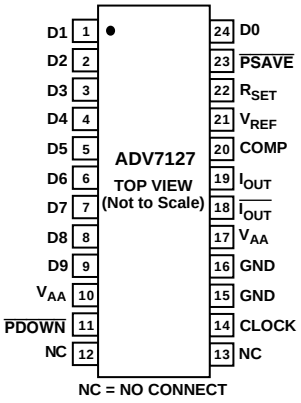
ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . +7 V
Voltage on any Digital Pin . . . . . GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . –40°C to +85°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapor Phase Soldering (1 Minute) . . . . . 220°C
I_{OUT} to GND[2] . . . . . 0 V to V_{AA}

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

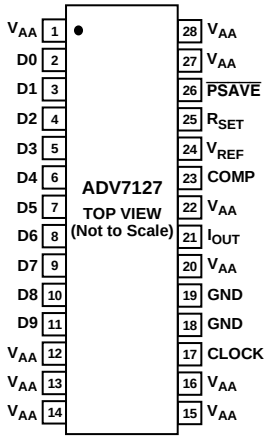
PIN CONFIGURATIONS

24-Lead TSSOP



NC = NO CONNECT

28-Lead SOIC



ORDERING GUIDE[1]

	Speed Options		
Package	**50 MHz**	**140 MHz**	**240 MHz**
R-28[2]	ADV7127KR50	ADV7127KR140	ADV7127JR240
RU-24[3]	ADV7127KRU50	ADV7127KRU140	ADV7127JRU240

NOTES
[1]50 MHz and 140 MHz devices are specified for –40°C to +85°C operation; 240 MHz devices are specified for 0°C to +70°C.
[2]SOIC Package.
[3]TSSOP Package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7127 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Mnemonic	Function
CLOCK	Clock Input (TTL Compatible). The rising edge of CLOCK latches the R0–R9, G0–G9, B0–B9, $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
D0–D9	Data Inputs (TTL Compatible). Data is latched on the rising edge of CLOCK. D0 is the least significant data bit. Unused data inputs should be connected to either the regular PCB power or ground plane.
I_{OUT}	Current Output. This high impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable.
R_{SET}	Full-Scale Adjust Control. A resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on I_{OUT} is given by: $I_{OUT}\,(mA) = 7968 \times V_{REF}(V)/R_{SET}(\Omega)$
COMP	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage Reference Input. An external 1.23 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog Power Supply (5 V ± 5%). All V_{AA} pins on the ADV7127 must be connected.
GND	Ground. All GND pins must be connected.
$\overline{I_{OUT}}$	Differential Current Output. Capable of directly driving a doubly terminated 75 Ω load. If not required, this output should be tied to ground.
$\overline{\text{PSAVE}}$	Power Save Control Pin. The part is put into standby mode when $\overline{\text{PSAVE}}$ is low. The internal voltage reference circuit is still active on the TSSOP in this case.
$\overline{\text{PDOWN}}$	Power-Down Control Pin (24-Lead TSSOP Only). The ADV7127 completely powers down, including the voltage reference circuit, when $\overline{\text{PDOWN}}$ is low.

TERMINOLOGY

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. A 10-bit DAC contains 1024 different levels, while an 8-bit DAC contains 256.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion that may be visually observed.

5 V–Typical Performance Characteristics

(V_{AA} = +5 V, V_{REF} = 1.235 V, I_{OUT} = 17.62 μA, 50 Ω Doubly Terminated Load, Differential Output Loading, T_A = +25°C)

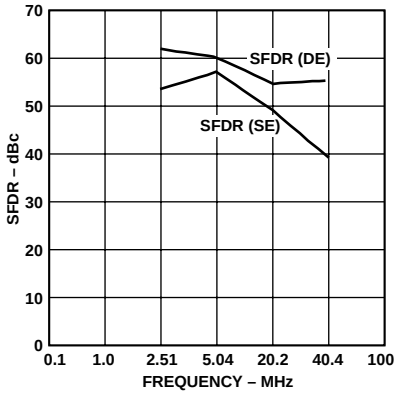


Figure 2. SFDR vs. f_{OUT} @ f_{CLOCK} = 140 MHz (Single-Ended and Differential)

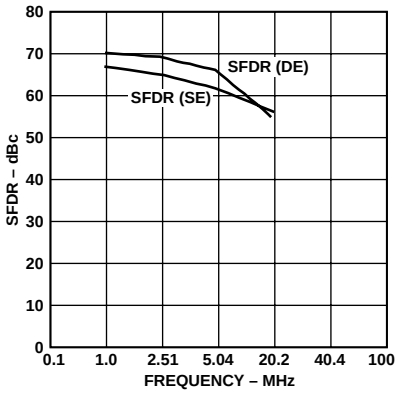


Figure 3. SFDR vs. f_{OUT} @ f_{CLOCK} = 50 MHz (Single-Ended and Differential)

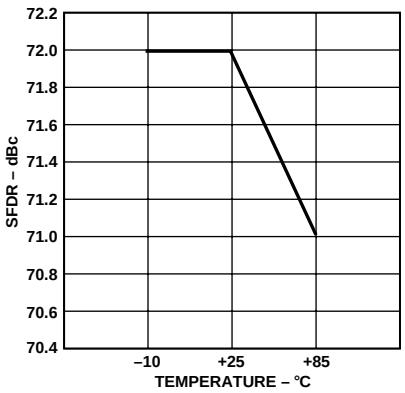


Figure 4. SFDR vs. Temperature @ f_{CLOCK} = 50 MHz (f_{OUT} = 1 MHz)

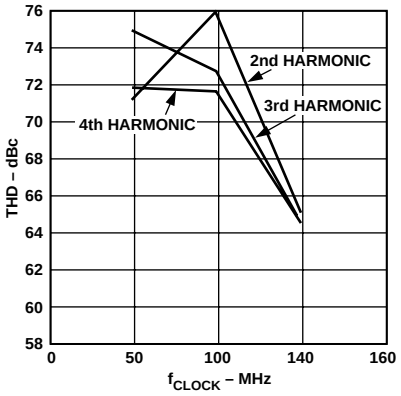


Figure 5. THD vs. f_{CLOCK} @ f_{OUT} = 2 MHz (2nd, 3rd and 4th Harmonics)

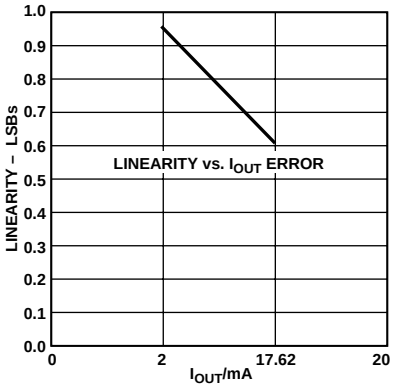


Figure 6. Linearity vs. I_{OUT}

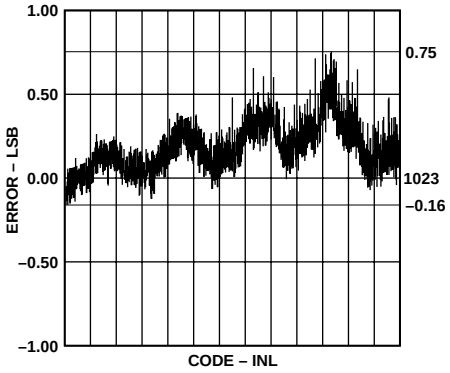


Figure 7. Typical Linearity

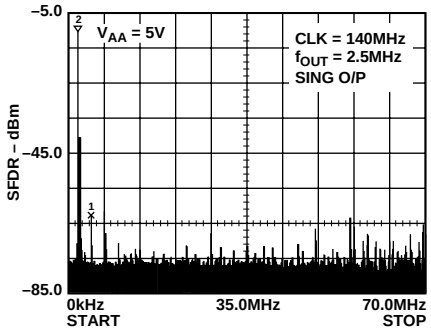


Figure 8. SFDR (Single-Tone) @ f_{CLOCK} = 140 MHz (f_{OUT1} = 2 MHz)

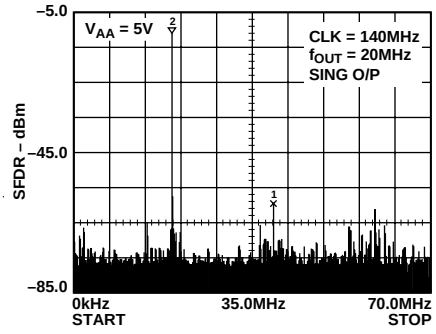


Figure 9. Single-Tone SFDR @ f_{CLOCK} = 140 MHz (f_{OUT1} = 20 MHz)

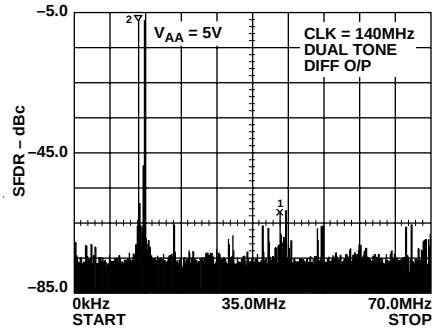


Figure 10. Dual-Tone SFDR @ f_{CLOCK} = 140 MHz (f_{OUT1} = 13.5 MHz, f_{OUT2} = 14.5 MHz)

3 V–Typical Performance Characteristics

(V_{AA} = +3 V, V_{REF} = 1.235 V, I_{OUT} =17.62 μA, 50 Ω Doubly Terminated Load, Differential Output Loading, T_A = +25°C)

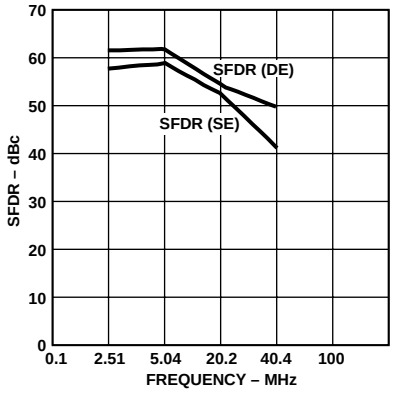


Figure 11. SFDR vs. f_{OUT} @ f_{CLOCK} = 140 MHz (Single-Ended and Differential)

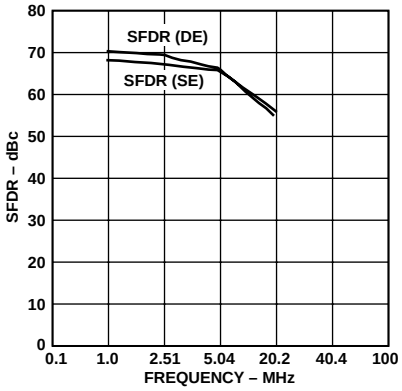


Figure 12. SFDR vs. f_{OUT} @ f_{CLOCK} = 50 MHz (Single-Ended and Differential)

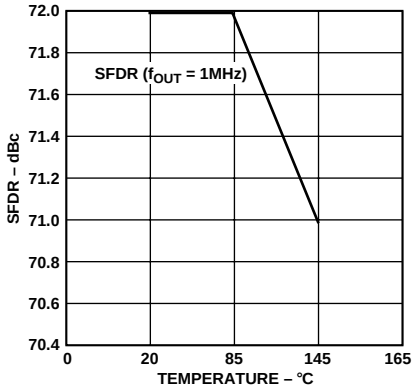


Figure 13. SFDR vs. Temperature @ f_{CLOCK} = 50 MHz, (f_{OUT} = 1 MHz)

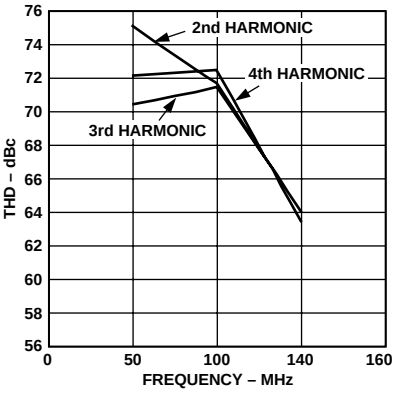


Figure 14. THD vs. f_{CLOCK} @ f_{OUT} = 2 MHz (2nd, 3rd and 4th Harmonics)

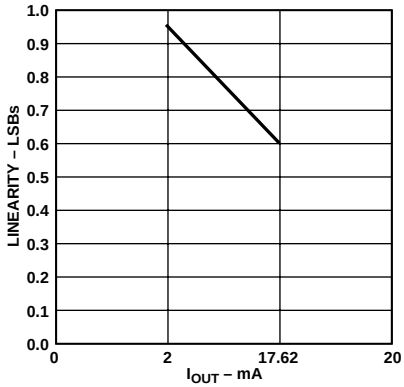


Figure 15. Linearity vs. I_{OUT}

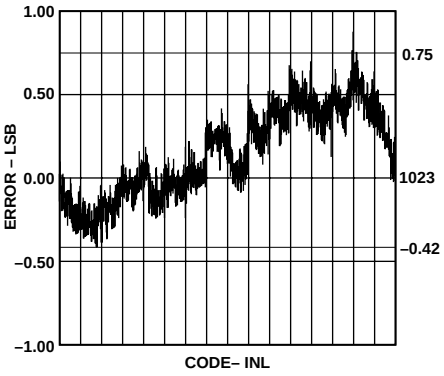


Figure 16. Typical Linearity

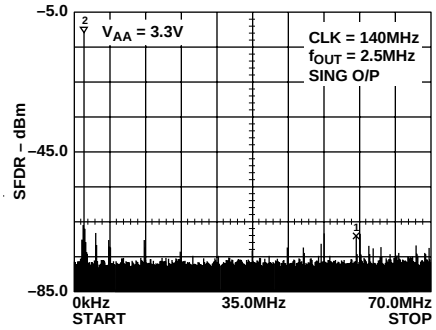


Figure 17. Single-Tone SFDR @ f_{CLOCK} = 140 MHz (f_{OUT1} = 2 MHz)

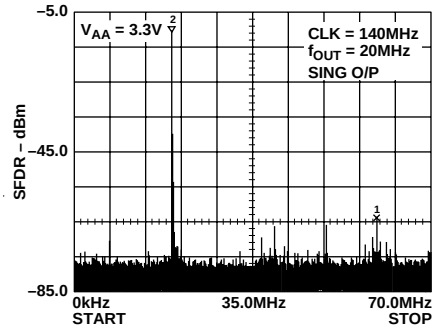


Figure 18. Single-Tone SFDR @ f_{CLOCK} = 140 MHz (f_{OUT1} = 20 MHz)

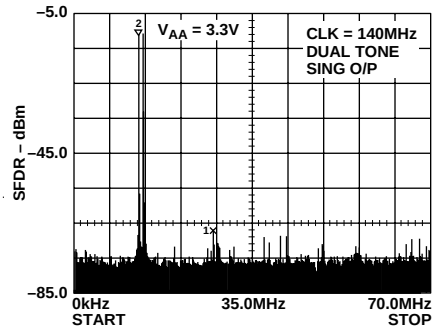


Figure 19. Dual-Tone SFDR @ f_{CLOCK} = 140 MHz (f_{OUT1} = 13.5 MHz, f_{OUT2} = 14.5 MHz)

CIRCUIT DESCRIPTION AND OPERATION

The ADV7127 contains one 10-bit D/A converter, with one input channel containing a 10-bit register. A reference amplifier is also integrated on board the part.

Digital Inputs

Ten bits of data (color information) D0–D9 are latched into the device on the rising edge of each clock cycle. This data is presented to the 10-bit DAC and is then converted to an analog output waveform. See Figure 20.

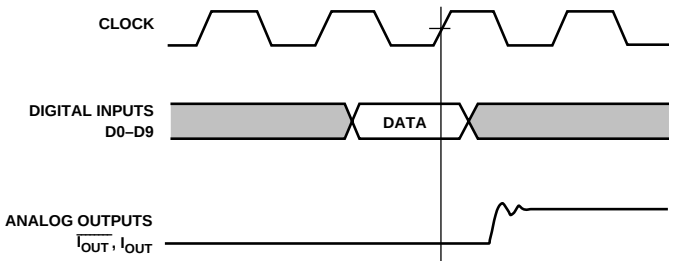


Figure 20. Video Data Input/Output

All these digital inputs are specified to accept TTL logic levels.

Clock Input

The CLOCK input of the ADV7127 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and hence the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

Dot Rate = (*Horiz Res*) × (*Vert Res*) × (*Refresh Rate*)/(*Retrace Factor*)

Horiz Res = Number of Pixels/Line.

Vert Res = Number of Lines/Frame.

Refresh Rate = Horizontal Scan Rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.

Retrace Factor = Total Blank Time Factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

Therefore, if we have a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate and a retrace factor of 0.8, then:

Dot Rate = 1024 × 1024 × 60/0.8
= 78.6 MHz

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the ADV7127 on the rising edge of CLOCK, as previously described in the Digital Inputs section. It is recommended that the CLOCK input to the ADV7127 be driven by a TTL buffer (e.g., 74F244).

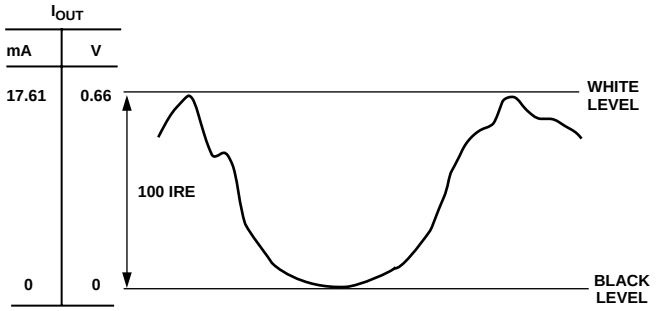


Figure 21. I_{OUT} Video Output Waveform

Table I. Video Output Truth Table (RSET = 560 Ω, R_{LOAD} = 37.5 Ω)

Description Data	I_{OUT}	$\overline{I_{OUT}}$	DAC Input
WHITE LEVEL	17.62	0	3FF
VIDEO	Video	17.62 – Video	Data
BLACK LEVEL	0	17.62	000H

Power Management

The $\overline{PSAVE}$ input of the ADV7127 puts the part into standby mode. It is used to reduce power consumption. When $\overline{PSAVE}$ is low, the power may be reduced to approximately 10 mW at 3 V. The ADV7127 in TSSOP package also has a power-down feature where the entire part, including the voltage reference circuit, is powered down. In this case, power on the ADV7127 can be reduced to 60 µW at 3 V.

Table II. Power Management

Mode	ADV7127 TSSOP	ADV7127 SOIC
Power-Save	10 mW Typically at 3 V	10 mW Typically at 3 V
Power-Down	Power 60 µW at 3 V	Not Available

Reference Input

The ADV7127 has an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor. Alternatively, the part could, if required, be overdriven by an external 1.23 V reference (AD1580).

A resistance R_{SET} connected between the R_{SET} pin and GND determines the amplitude of the output video level according to the following equation:

$$I_{OUT}\ (mA) = 7{,}968 \times V_{REF}(V)/R_{SET}(\Omega) \quad (1)$$

Using a variable value of R_{SET}, as shown in Figure 22, allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels as quoted in the specification page. These values typically correspond to the RS-343A video waveform values as shown in Figure 21.

D/A Converter

The ADV7127 contains a 10-bit D/A converter. The DAC is designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = "1") or GND (bit = "0") by a sophisticated decoding scheme. The use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Output

The analog output of the ADV7127 is a high impedance current source. The current output is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 22 shows the required configuration for the output connected into a doubly terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor.

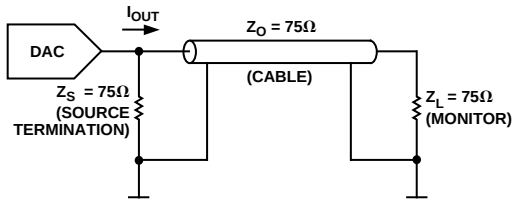


Figure 22. Analog Output Termination for RS-343A

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 23. The output current level of the DAC remains unchanged, but the source termination resistance, Z_S, on the DAC is increased from 75 Ω to 150 Ω.

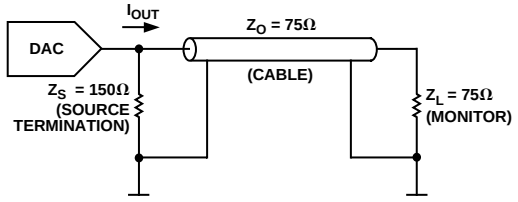


Figure 23. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an Application Note entitled "Video Formats & Required Load Terminations" available from Analog Devices, publication no. E1228-15-1/89.

Figure 21 shows the video waveforms associated with the current output driving the doubly terminated 75 Ω load of Figure 22.

Gray Scale Operation

The ADV7127 can be used for stand-alone, gray scale (monochrome) or composite video applications (i.e., only one channel used for video information).

Video Output Buffer

The ADV7127 is specified to drive transmission line loads, which is what most monitors are rated as. The analog output configurations to drive such loads are described in the Analog Interface section and illustrated in Figure 23. However, in some applications it may be required to drive long "transmission line" cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between two and four will be required. These buffers will also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84x series of monolithic op amps. In very high frequency applications (80 MHz), the AD9617 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

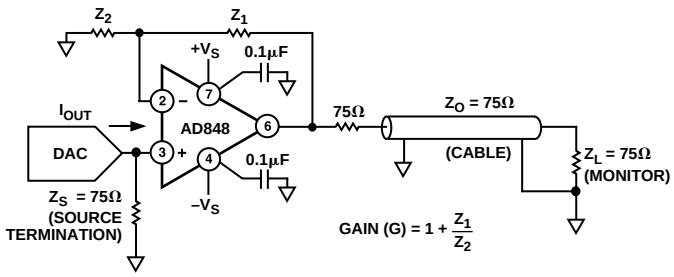


Figure 24. AD848 As an Output Buffer

PC Board Layout Considerations

The ADV7127 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7127 it is imperative that great care be given to the PC board layout. Figure 25 shows a recommended connection diagram for the ADV7127.

The layout should be optimized for lowest noise on the ADV7127 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should be minimized to inductive ringing.

Ground Planes

The ADV7127 and associated analog circuitry, should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 25. This bead should be located as close as possible (within 3 inches) to the ADV7127.

The analog ground plane should encompass all ADV7127 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the ADV7127.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7127 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 25. This bead should be located within three inches of the ADV7127.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7127 power pins, voltage reference circuitry and any output amplifiers.

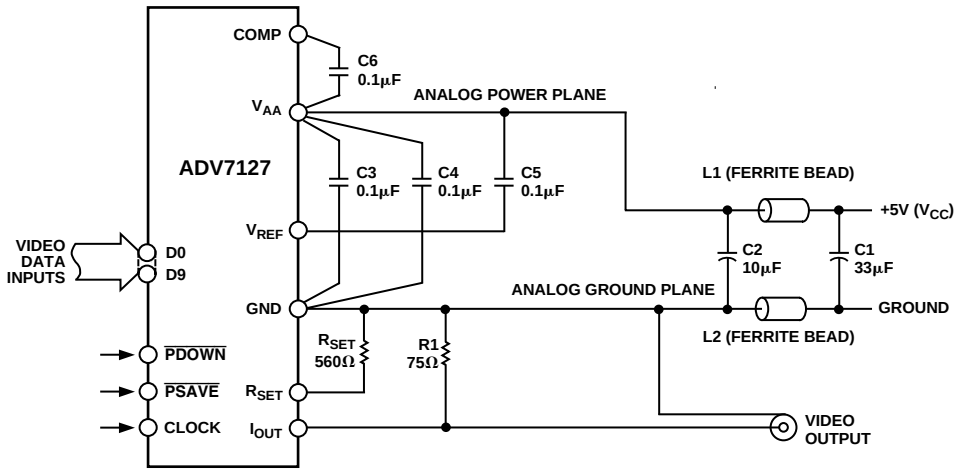
The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors (see Figure 25).

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV7127 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1	33μF TANTALUM CAPACITOR	
C2	10μF TANTALUM	
C3, C4, C5, C6	0.1μF CERAMIC CAPACITOR	
L1, L2	FERRITE BEAD	FAIR-RITE 274300111 OR MURATA BL01/02/03
R1	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	560Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 25. Typical Connection Diagram and Component List

Digital Signal Interconnect

The digital signal lines to the ADV7127 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7127 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7127 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

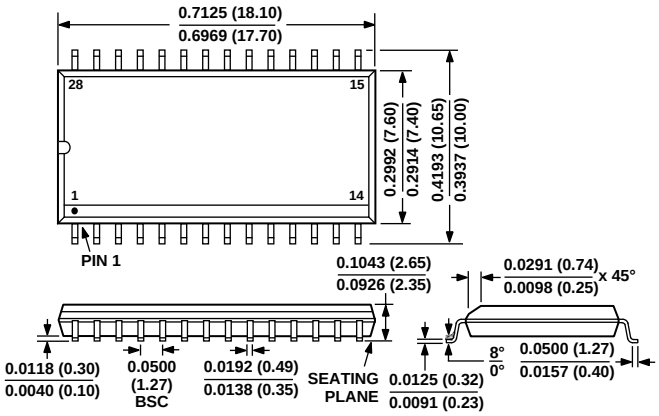
For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7127 so as to minimize reflections.

Additional information on PCB design is available in an application note entitled "Design and Layout of a Video Graphics System for Reduced EMI." This application note is available from Analog Devices, publication number E1309-15-10/89.

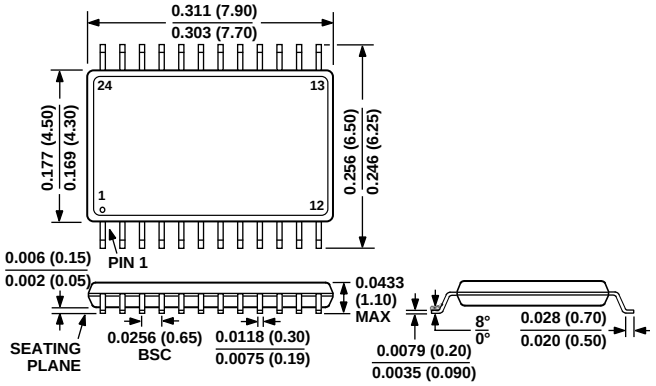
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead SOIC
(R-28)



24-Lead TSSOP
(RU-24)



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