Integrated Digital CCIR-601 YCrCb to PAL/NTSC Video Encoder

ADV7174

FEATURES

CCIR-601 YCrCb to PAL/NTSC Video Encoder
Single 27MHz Clock required (x 2 Oversampling)
Pixel Port supports:
CCIR-656 4:2:2 8-Bit Parallel Input Format
4:2:2 16-Bit Parallel Input Format
SMPTE 170M NTSC Compatible Composite Video Output
CCIR624/CCIR601 PAL Compatible Composite Video Output
SCART/PERITV Support
YUV Output Mode
Simultaneous Composite and S-VHS Y/C or RGB/YUV Video Outputs.
Programmable Luma Filters (Low-Pass/Notch)
Square Pixel Support (Slave Mode)
10-Bit DAC resolution for Encoded Video Channels
8-Bit DAC resolution for RGB Output
YUV Interpolation for Accurate Subcarrier Construction
Programmable Sub-Carrier Frequency and Phase.
Programmable LUMA Delay
Color Signal Control/Burst Signal Control
Interlaced/Non Interlaced Operation
Complete on-chip Video Timing Generator
Master/Slave Operation Supported with Programmability
Close Captioning support.
8 Color On-Screen Display
On Board Color Bar Generation
On Board Voltage Reference
Low Power Mode
2 Wire Serial MPU Interface (I^2C Compatible)
+5 V CMOS Monolithic Construction
44-Pin PQFP Thermally Enhanced Package

APPLICATIONS

MPEG-1 and MPEG-2 Video
DVD
Digital Satellite/Cable Systems (Set Top Boxes/IRDs)
Digital TVs
CD Video/Karaoke
Professional Studio Quality
PC Video/Mulimedia

GENERAL DESCRIPTION

The ADV7174 is an integrated Digital Video Encoder that converts Digital CCIR-601 4:2:2 8 or 16-bit Component Video Data into a standard analog baseband television signal compatible with world wide standards NTSC, PAL B/D/G/H/I, PAL M or
PAL N. This 4:2:2 data-stream is interpolated into 4:4:4 Component Video (YUV). The YUV Video is interpolated to two times the pixel rate. The Color-Difference Components (UV) are quadrature modulated using a Sub-Carrier frequency generated by an on-chip synthesiser (also running at two times the pixel rate). The two times Pixel Rate sampling allows more accurate generation of the Sub-Carrier because Frequency and Phase Errors are reduced by the higher Sampling Rate. The luminance and chrominance components are then digitally combined and the resulting Composite signal is output via a 10-Bit DAC. In addition to the Composite output signal, there is the facility to output S-VHS Y/C Video (10-Bits), RGB or YUV Video (8-Bits). The Y/C, RGB or YUV format is simultaneously available at the Analog Outputs with the Composite Video Signal. Each Analog Output generates a standard Video-Level signal into a Doubly Terminated 75Ω load.

The ADV7174 also supports both a PAL and NTSC square pixel mode in slave mode.

The Output Video Frames are synchronised with the incoming data Timing Reference Codes. Optionally the Encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ & FIELD Timing Signals. These timing signals can be adjusted to change pulse width and position while the part is in the master mode. The Encoder requires a single two times pixel rate (27 MHz) Clock for standard operation. Alternatively the Encoder requires a 24.54 MHz Clock for NTSC or 29.5MHz Clock for PAL square pixel mode operation. All internal clocks are generated on-chip.

Other features of the ADV7174 include an internal color bar generator, lower power mode and the ability to switch the DACs off individually. The ADV7174 also provides an 8 color look up table for overlay on the video output.

The ADV7174 modes are set up over a two wire serial bi-directional port (I^2C Compatible) with 2 slave addresses.

The ADV7174 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7174 is packaged in a 44-Pin thermally enhanced PQFP package (Patent pending).

The ADV7174 is protected by US patents numbers 5,343,196 and 5,442,355 and other intellectual property rights.

AUG 96 REV. 0

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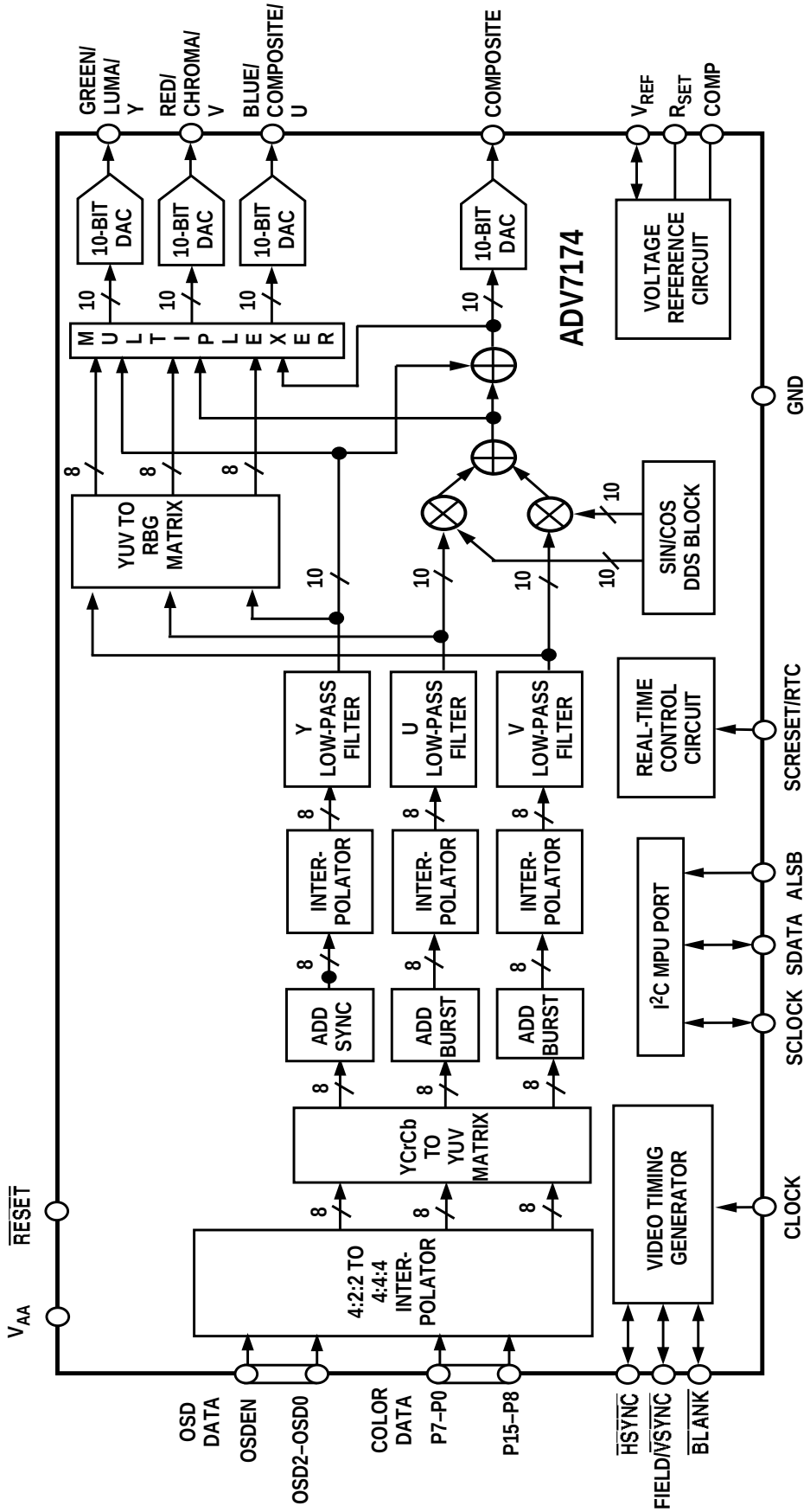
FUNCTIONAL BLOCK DIAGRAM



ADV7174–SPECIFICATIONS

(V_{AA} = + 5V[1], V_{REF} = 1.235 V R_{SET} = 150 Ω.
All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Model		ADV7174			
Parameter	**Conditions[1]**	**Min**	**Typ**	**Max**	**Units**
STATIC PERFORMANCE					
Resolution (each DAC)				9	Bits
Accuracy (each DAC)					
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Floating-State Leakage Current				10	μA
Floating-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current[3]		32	34.7	37	mA
Output Current[4]			8		mA
DAC to DAC Matching			2	5	%
Output Compliance, V_{OC}		0		+1.4	V
Output Impedance, R_{OUT}			15		KΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0mA			30	pF
VOLTAGE REFERENCE					
Voltage Reference Range, V_{REF}	$I_{VREFOUT}$= 20μA	1.112	1.235	1.359	V
POWER REQUIREMENTS[5]					
V_{AA}			5		V
I_{DAC}[6]			140	155	mA
I_{CCT}[7]			110	150	mA
Power Supply Rejection Ratio	COMP = 0.1μF		0.02	0.5	% / %
DYNAMIC PERFORMANCE[8]					
Luma Bandwidth[9] (Low Pass Filter)	NTSC Mode				
Stop Band Cutoff	>50dB Attenuation			7.5	MHz
Pass Band Cutoff	< 0.06dB Attenuation			2.3	MHz
Chroma Bandwidth	NTSC Mode				
Stop Band Cutoff	>40dB Attentuation			3.6	MHz
Pass Band Cutoff	<.1dB Attenuation			1.0	MHz
Luma Bandwidth[9] (Low Pass Filter)	PAL MODE				
Stop Band Cutoff	>50dB Attenuation			8.0	MHz
Pass Band Cutoff	< 0.06dB Attenuation			3.4	MHz
Chroma Bandwidth	PAL MODE				
Stop Band Cutoff	>40dB Attentuation			4.0	MHz
Pass Band Cutoff	<.1dB Attenuation			1.3	MHz
Differential Gain			0.8		%
Differential Phase			0.8		°
Differential Gain	Lower Power Mode		7		%
Differential Phase	Lower Power Mode		2		°
SNR	RMS		60		dB rms
SNR	Peak Periodic		56		dB p-p
Hue Accuracy			1.0		°
Color Saturation Accuracy			1.0		%

NOTES
[1]±5% for all versions.
[2]Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Full drive into 37.5Ohm load.
[4]Minimum drive with buffered/scaled output load.
[5]Power measurements are taken with Clock Frequency = 27MHz. Max T_J = 110°C.
[6]I_{DAC} is the total current to drive all 4 DACs. Turning off one DAC reduces I_{DAC} correspondingly.
[7]I_{CCT} (Circuit Current) is the continuous current required to drive the device.
[8] Guaranteed by characterisation.
[9] These specifications are for the low pass filter only. For the other internal filters please see Figure 3.
Specifications subject to change without notice.

AC CHARACTERISTICS[1]

Parameter	Min	Typ	Max	Units	Condition
Chroma Nonlinear Gain		0.6		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		1		±°	NTSC
Chroma Nonlinear Phase		1.7		±°	PAL
Chroma/Luma Intermod		0.2		±%	Referenced to 714 mV (NTSC)
Chroma/Luma Intermod		0.4		±%	Referenced to 700 mV (PAL)
Chroma/Luma Gain Ineq		0.6		±%	
Chroma/Luma Delay Ineq		1		ns	
Luminance Nonlinearity		0.8		±%	
Chroma AM Noise		60		dB	
Chroma PM Noise		59		dB	

TIMING–SPECIFICATIONS[2]

(V_{AA} = + 5V[3], V_{REF} = 1.235 V R_{SET} = 150 Ω.
All specifications T_{MIN} to T_{MAX}[4] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Condition
MPU PORT[1]					
SCLOCK Frequency	0		100	KHz	
SCLOCK High Pulse Width, t_1	4.0			µs	
SCLOCK Low Pulse Width, t_2	4.7			µs	
Hold Time (Start Condition), t_3	4.0			µs	After this period the first clock pulse is generated
Setup Time (Start Condition), t_4	4.7			µs	Relevent for repeated Start Condition
Data Setup Time, t_5	250			ns	
SDATA, SCLOCK Rise Time, t_6			1	µs	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	4.7			µs	
ANALOG OUTPUTS[1,5]					
Analog Output Delay		5		ns	
DAC Analog Output Skew		0		ns	
CLOCK CONTROL AND PIXEL PORT[6]					
F_{CLOCK}	24.52	27	29.5	MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}	3.5			ns	
Data Hold Time t_{12}	1			ns	
Control Setup Time t_{11}	4			ns	
Control Hold Time t_{12}	2			ns	
Digital Output Access Time t_{13}			24	ns	
Digital Output Hold Time t_{14}		6		ns	
Pipeline Delay t_{15}		37		Clock cycles	

NOTES ON TIMING CHARACTERISTICS

[1] Guaranteed by characterisation .

[2] TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points.
Timing reference points at 50% for inputs and outputs.
Analog output load ≤ 10 pF.

[3] ±5% for all versions

[4] Temperature Range (T_{min} to T_{max}) ; 0 to + 70 °C

NOTES ON ANALOG OUTPUTS

[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

NOTES ON PIXEL PORT

[6] Pixel Port consists of the following inputs:

Pixel Inputs:	P15-P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock Input:	CLOCK

Specifications subject to change without notice.

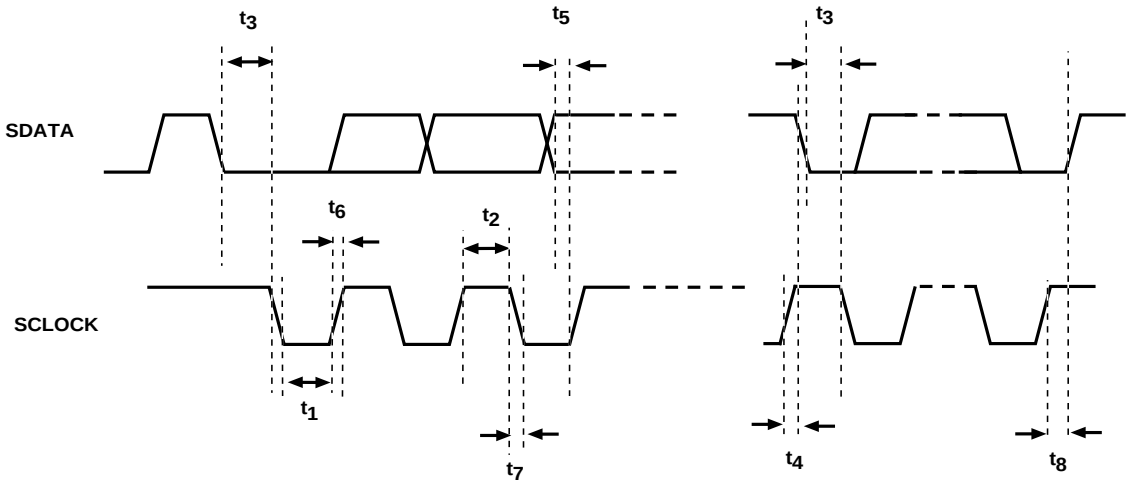


Figure 1. MPU Port Timing Diagram

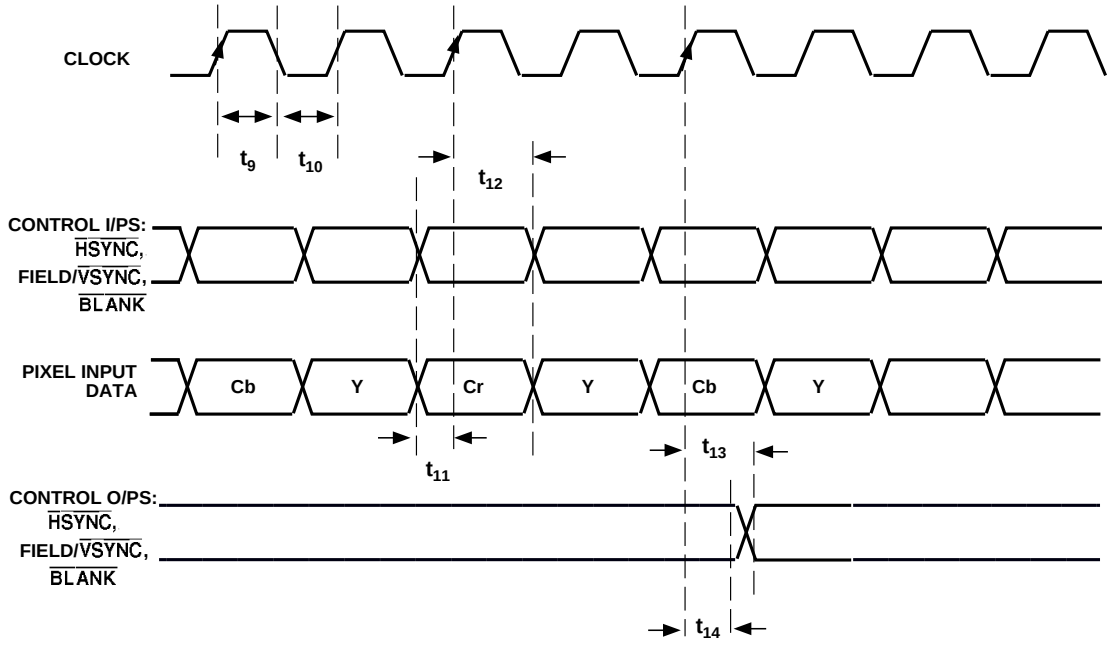


Figure 2. Pixel and Control Data Timing Diagram

ABSOLUTE MAXIMUM RATINGS *

V_{AA} to GND.....7V
Voltage on any Digital Input Pin.....GND-0.5V to V_{AA}+0.5V
Storage Temperature (T_S).....-65°C to +150°C
Junction Temperature(T_J).....+150°C
Lead Temperature (Soldering, 10 secs).....+260°C
Analog Outputs to GND[1].....GND -0.5 to V_{AA}

NOTES

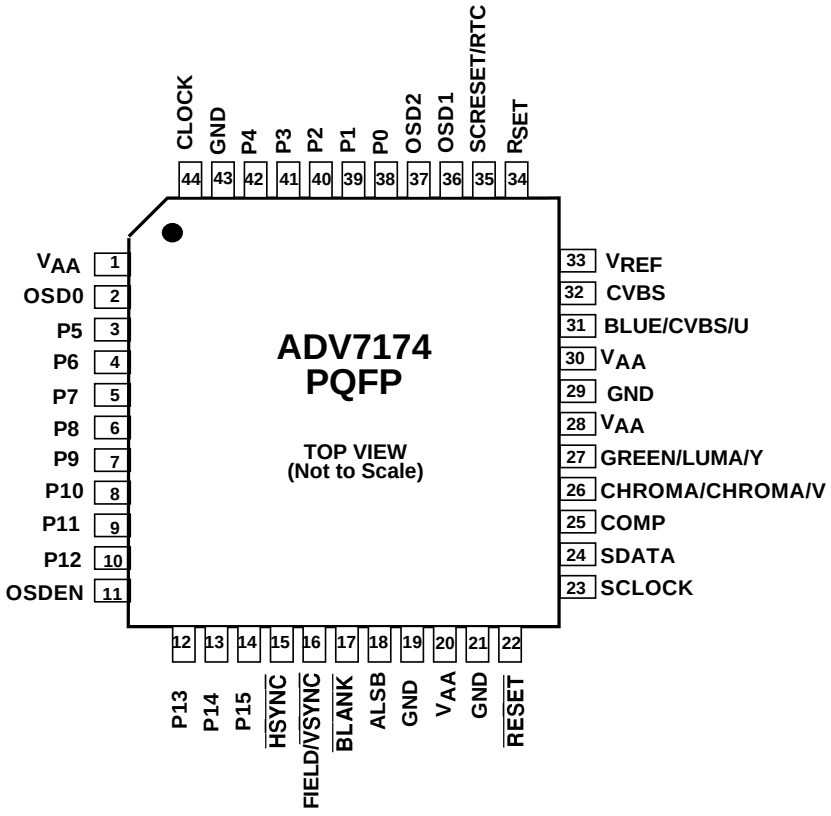
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

Model Option	Temperature Range	Package
ADV7174KS	0°C to 70°C	S-44

ADV7174 PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7174 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.