National Semiconductor

AH0014/AH0014C* DPDT, AH0015/AH0015C Quad SPST, AH0019/AH0019C* Dual DPST-TTL/DTL Compatible MOS Analog Switches

General Description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in hermetic dual-in-line package.

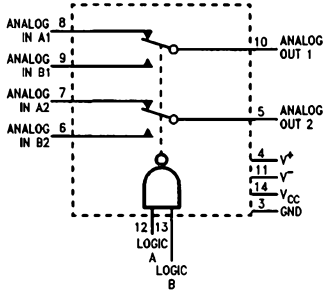
These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

Features

- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Analog signals in excess of 25 MHz
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

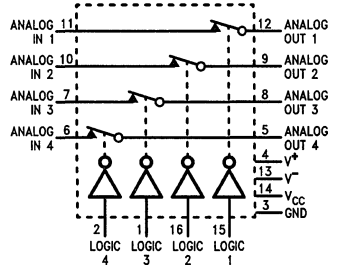
Block and Connection Diagrams



Note: All logic inputs shown at logic "1". TL/K/10125–1

Order Number AH0014D or AH0014CD
See NS Package Number D14D

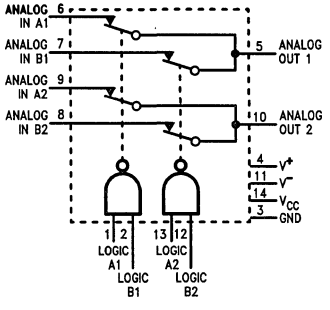
Quad SPST



Note: All logic inputs shown at logic "1". TL/K/10125–2

Order Number AH0015D or AH0015CD
See NS Package Number D16C

Dual DPST



Note: All logic inputs shown at logic "1".

TL/K/10125–3

Order Number AH0019D or AH0019CD
See NS Package Number D14D

*Previously called NH0014/NH0014C and NH0019/NH0019C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			1	μA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input—Each Gate (Note 3)	V_{CC} = 5.5V, V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input—Each Gate (Note 3)	V_{CC} = 5.5V, V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance—Each Gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current—Each Input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current—Each Output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time—t_{OFF}	See Test Circuit; T_A = 25°C		600	750	ns
Analog Turn-ON Time—t_{ON}	See Test Circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

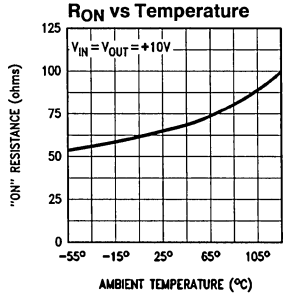
Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. $V^- = -20V$. $V^+ = +10V$ and an analog test current of 1 mA unless otherwise specified.

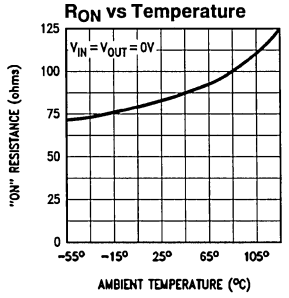
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. $V^+ = +10V$, $V^- = -22V$.

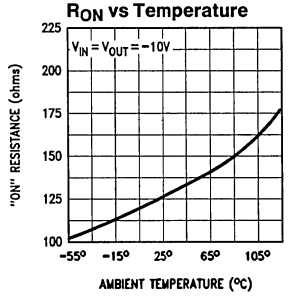
Note 3: Current measured is drawn from V_{CC} supply.

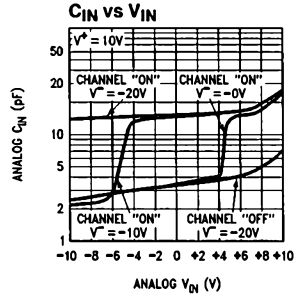
Note 4: All analog switch pins except measurement pin are tied to V^+.

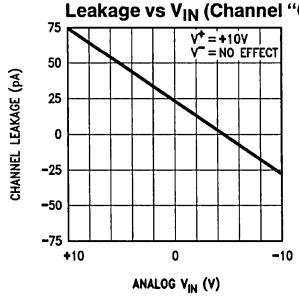
Analog Switch Characteristics (Note 2)

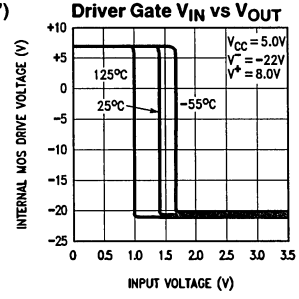






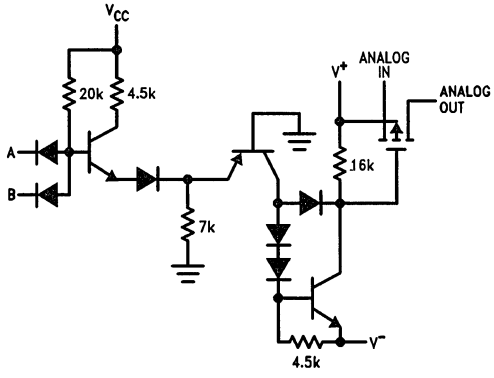






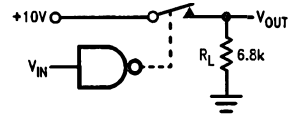
TL/K/10125-6

Schematic (Single Driver Gate and MOS Switch Shown)

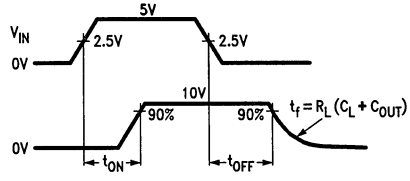


TL/K/10125-7

Analog Switching Time Test Circuit



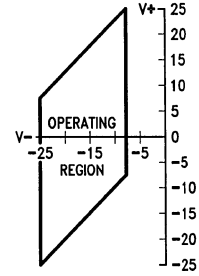
TL/K/10125-8



TL/K/10125-9

Selecting Power Supply Voltage

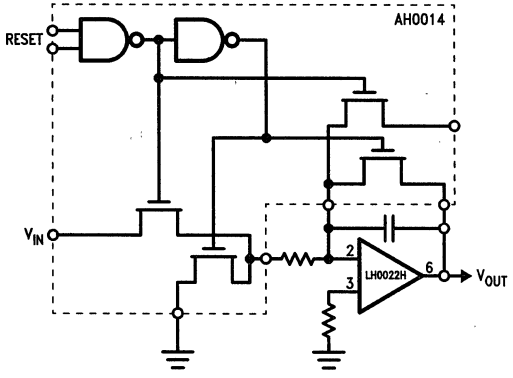
The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between $-25V$ and $-8V$. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



TL/K/10125-10

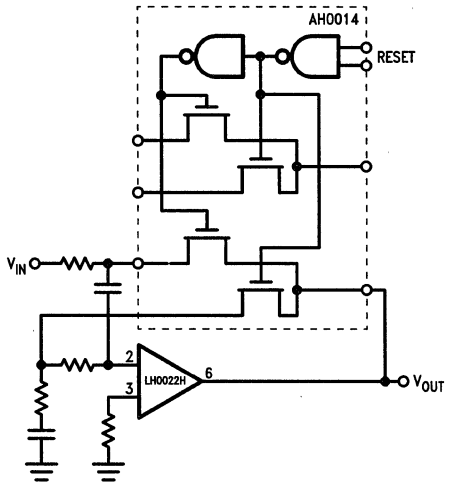
Typical Applications

Integrator



TL/K/10125–4

Reset Stabilized Amplifier



TL/K/10125–5

National Semiconductor

AH5009/AH5010/AH5011/AH5012 Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches economically fulfills a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

Applications

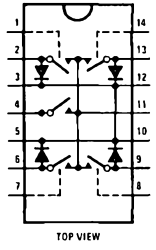
- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

■ Interfaces with standard TTL and CMOS	
■ "ON" resistance match	2Ω
■ Low "ON" resistance	100Ω
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

Connection and Schematic Diagrams (All switches shown are for logical "1" input)

Dual-In-Line Package

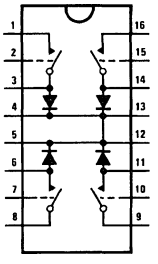


TOP VIEW

AH5009C and AH5010C MUX Switches
(4-Channel Version Shown)
Order Number AH5009CM,
AH5009CN, AH5010CM or AH5010CN
See NS Package Number M14A or N14A

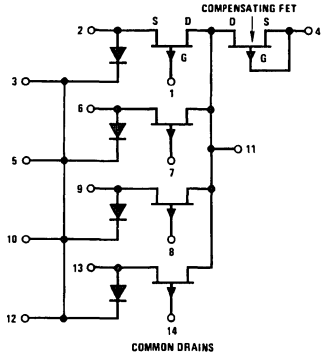
LOGIC DRIVE	4 CHANNEL MUX	4 SPST SWITCHES
5V LOGIC	AH5010C	AH5012C
15V LOGIC	AH5009C	AH5011C

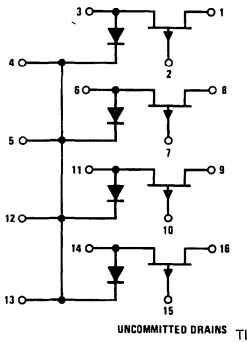
Dual-In-Line Package



TOP VIEW

AH5011C and AH5012C SPST Switches
(Quad Version Shown)
Order Number AH5011CM,
AH5011CN, AH5012CM or AH5012CN
See NS Package Number M16A or N16A





Note: All diode cathodes are internally connected to the substrate.

TL/H/5659–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
AH5009/AH5010/AH5011/AH5012	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Soldering Information:	
N Package 10 sec	300°C
SO Package Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics AH5010 and AH5012 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$4.5V \le V_{GD} \le 11V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 3.8V$ $T_A = 85°C$	0.02	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.08	1 200	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$	0.13	5 10	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$	0.1	10 20	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 0.35V$, $I_S = 2$ mA $T_A = +85°C$	90	150 240	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0V$, $I_D = 1$ mA	4	20	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit	120		dB

Electrical Characteristics AH5009 and AH5011 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$11V \le V_{GD} \le 15V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 10.3V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.04	0.5 100	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$		2 1	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$		5 2	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 1.5V$, $I_S = 2$ mA $T_A = 85°C$	60	100 160	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0V$, $I_D = 1$ mA	2	10	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	50	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit. f = 100 Hz.	120		dB

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

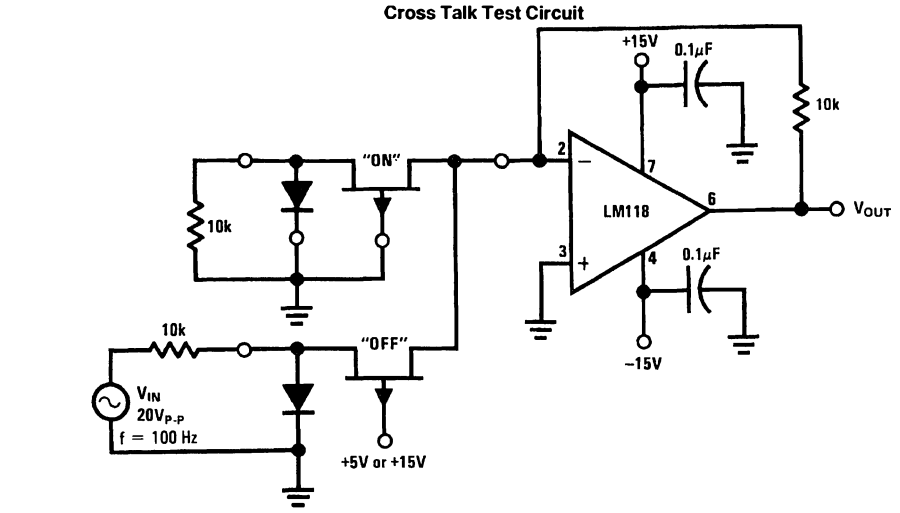
Note 2: Test conditions 25°C unless otherwise noted.

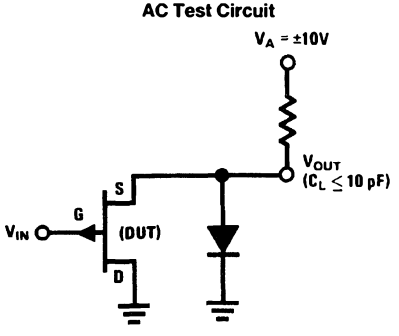
Note 3: "OFF" and "ON" notation refers to the conduction state of the FET switch.

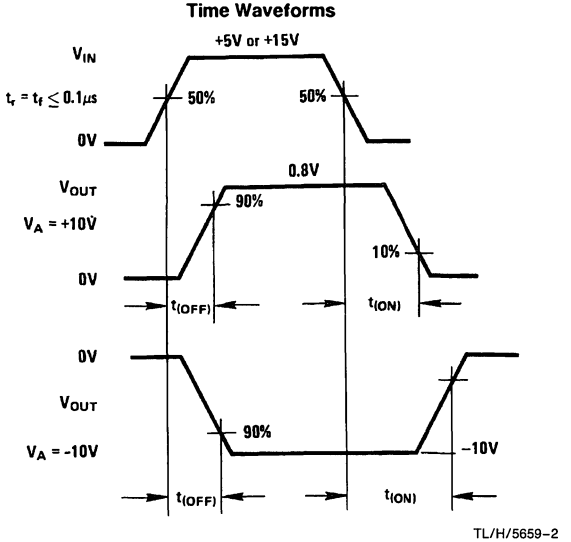
Note 4: Thermal Resistance:

	θ_{JA}
N14A, N16A	92°C/W
M14A, M16A	115°C/W

Test Circuits and Switching Time Waveforms



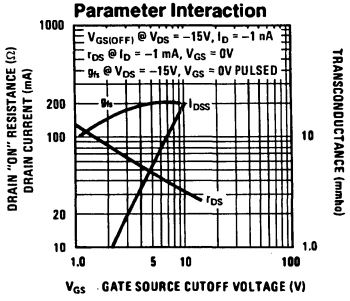




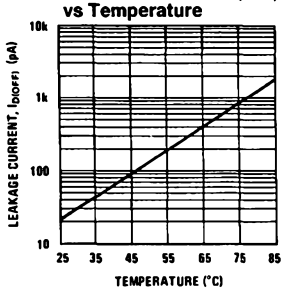
TL/H/5659–2

Typical Performance Characteristics

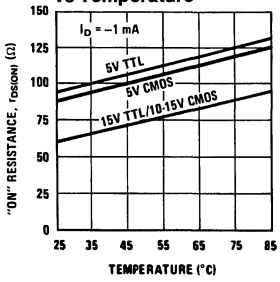
Parameter Interaction



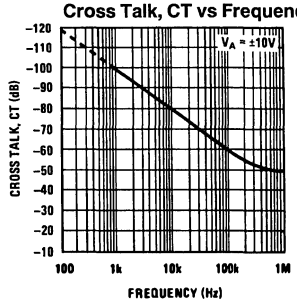
Leakage Current, $I_{D(OFF)}$ vs Temperature



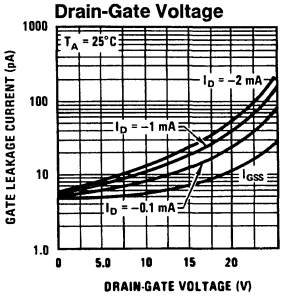
"ON" Resistance, $r_{DS(ON)}$ vs Temperature



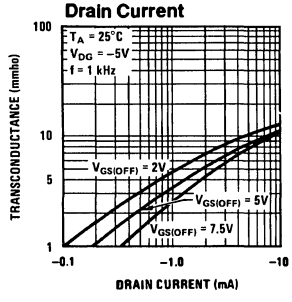
Cross Talk, CT vs Frequency



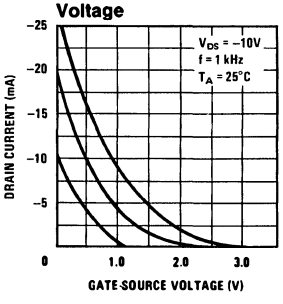
Leakage Current vs Drain-Gate Voltage



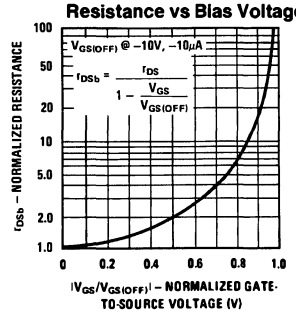
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



TL/H/5659–3

Applications Information

Theory of Operation

The AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AH5010), 5V-10V CMOS (AH5010), open collector 15V TTL/CMOS (AH5009).

Two basic switch configurations are available: 4 independent switches (SPST) and 4 pole switches used for multiplexing (4 PST-MUX). The MUX versions such as the AH5009 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V input will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AH series of analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{min} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \quad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \quad (2b)$$

whichever is larger.

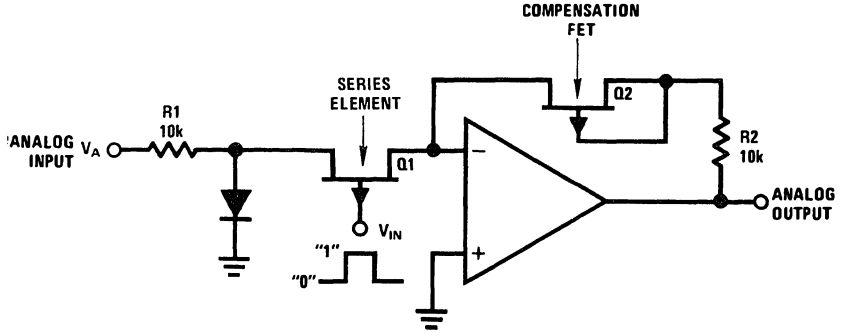


FIGURE 1. Use of Compensation FET

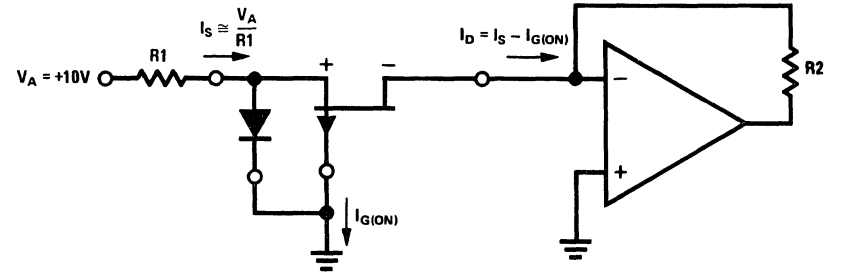


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FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch $\cong 20$ mA

In a typical application, V_A might $= \pm 10V$, $A_D = 0.1\%$, $0°C \leq T_A \leq 85°C$. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{(10V)}{\left(\frac{20\ mA}{10}\right)} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong 10V/5k$ or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AH5010. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\, A_D}{(N)\, I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value of the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if $N = 10$, $A_D = 0.1\%$, and $I_{D(OFF)} \leq 10$ nA at 85°C for the AH5009. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

TTL Compatibility

The AH series can be driven with two different logic voltage swings: the even numbered part types are specified to be driven from standard 5V TTL logic and the odd numbered types from 15V open collector TTL.

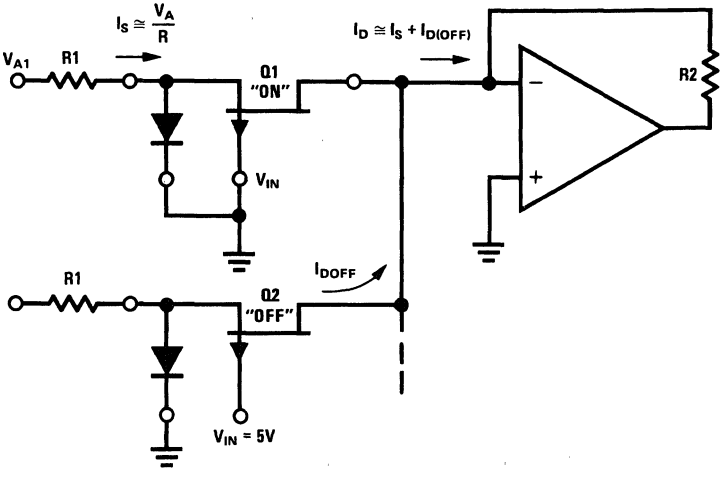

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FIGURE 3

Applications Information (Continued)

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5*. In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} at the expense of power dissipation in the low state.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6*.

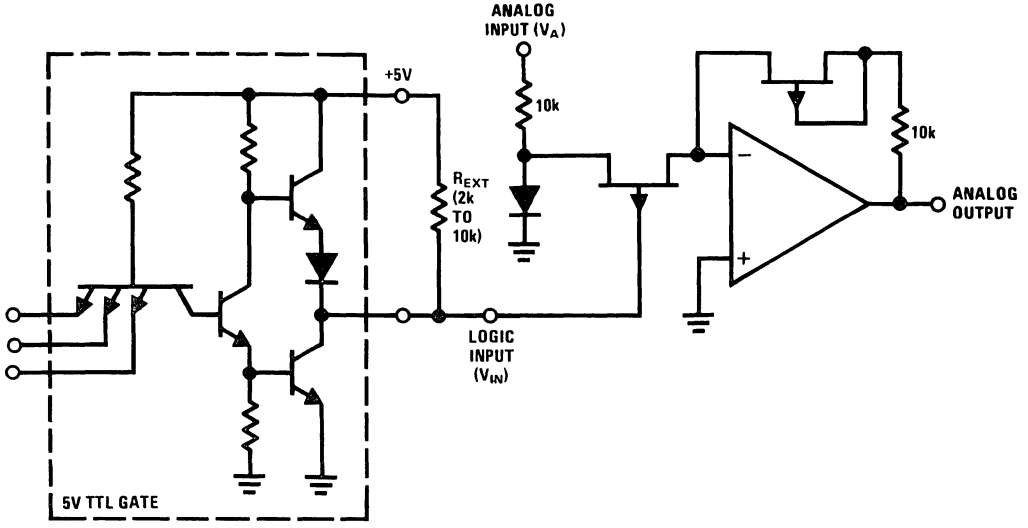

FIGURE 4. Interfacing with +5V TTL

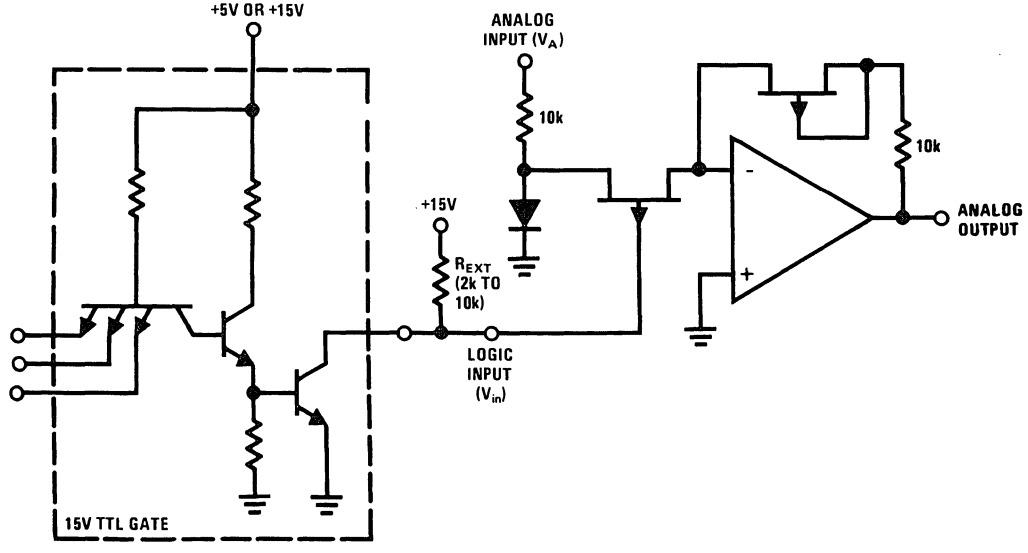

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FIGURE 5. Interfacing with +15V Open Collector TTL

Applications Information (Continued)

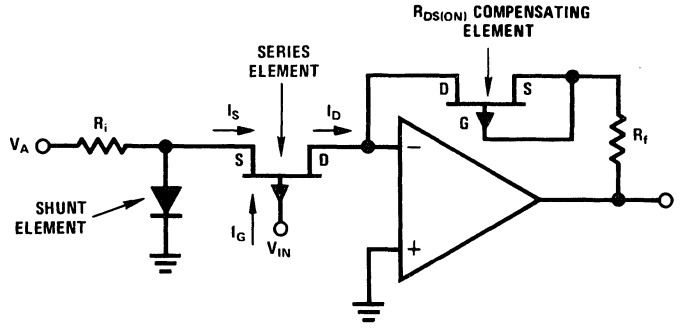
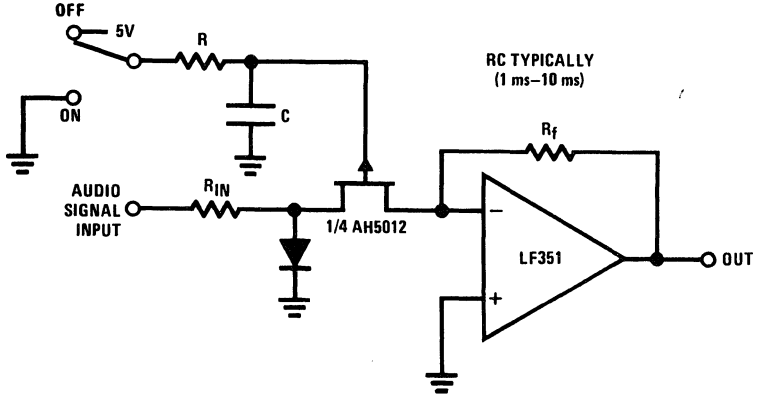


FIGURE 6. Definition of Terms

Typical Applications

De-Glitched Switch for Noiseless Audio Switching



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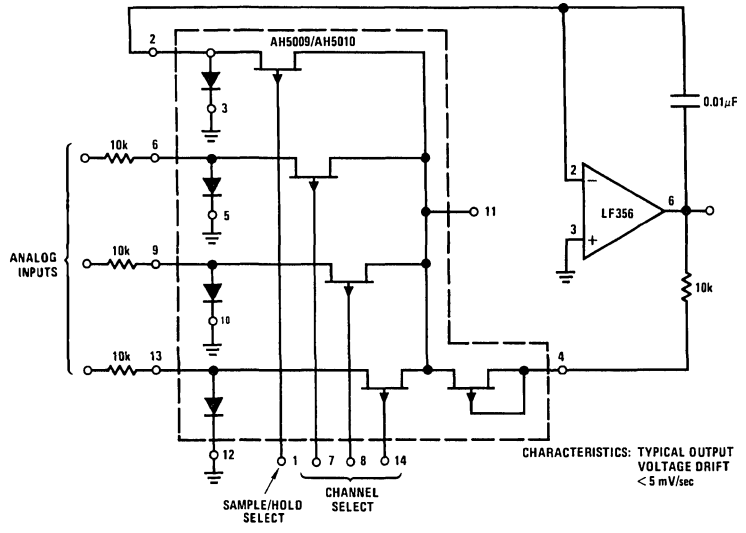
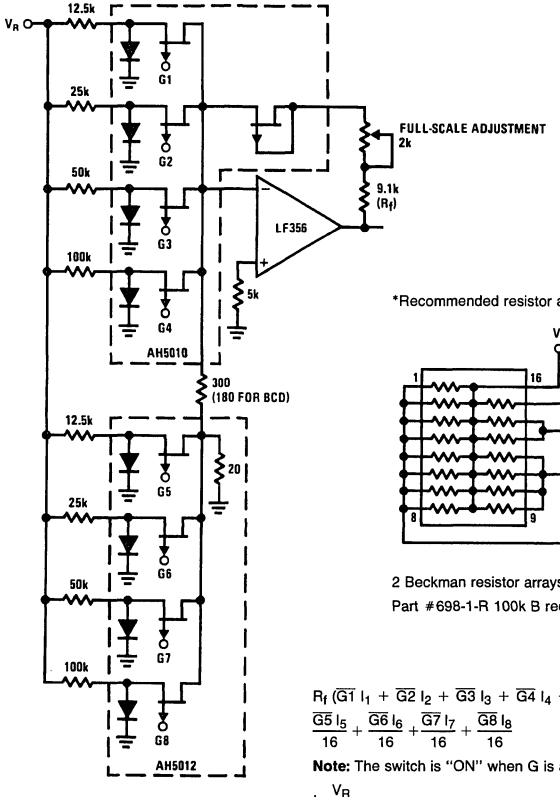
Typical Applications (Continued)

3-Channel Multiplexer with Sample and Hold



8-Bit Binary (BCD) Multiplying D/A Converter*



*Recommended resistor array connection for D/A application

2 Beckman resistor arrays
Part #698-1-R 100k B recommended

$$R_f\left(\frac{\overline{G1}\,I_1}{16}+\frac{\overline{G2}\,I_2}{16}+\frac{\overline{G3}\,I_3}{16}+\frac{\overline{G4}\,I_4}{16}+\frac{\overline{G5}\,I_5}{16}+\frac{\overline{G6}\,I_6}{16}+\frac{\overline{G7}\,I_7}{16}+\frac{\overline{G8}\,I_8}{16}\right)$$

Note: The switch is "ON" when G is at 0V (Logic "0")

$$I=\frac{V_R}{R}$$

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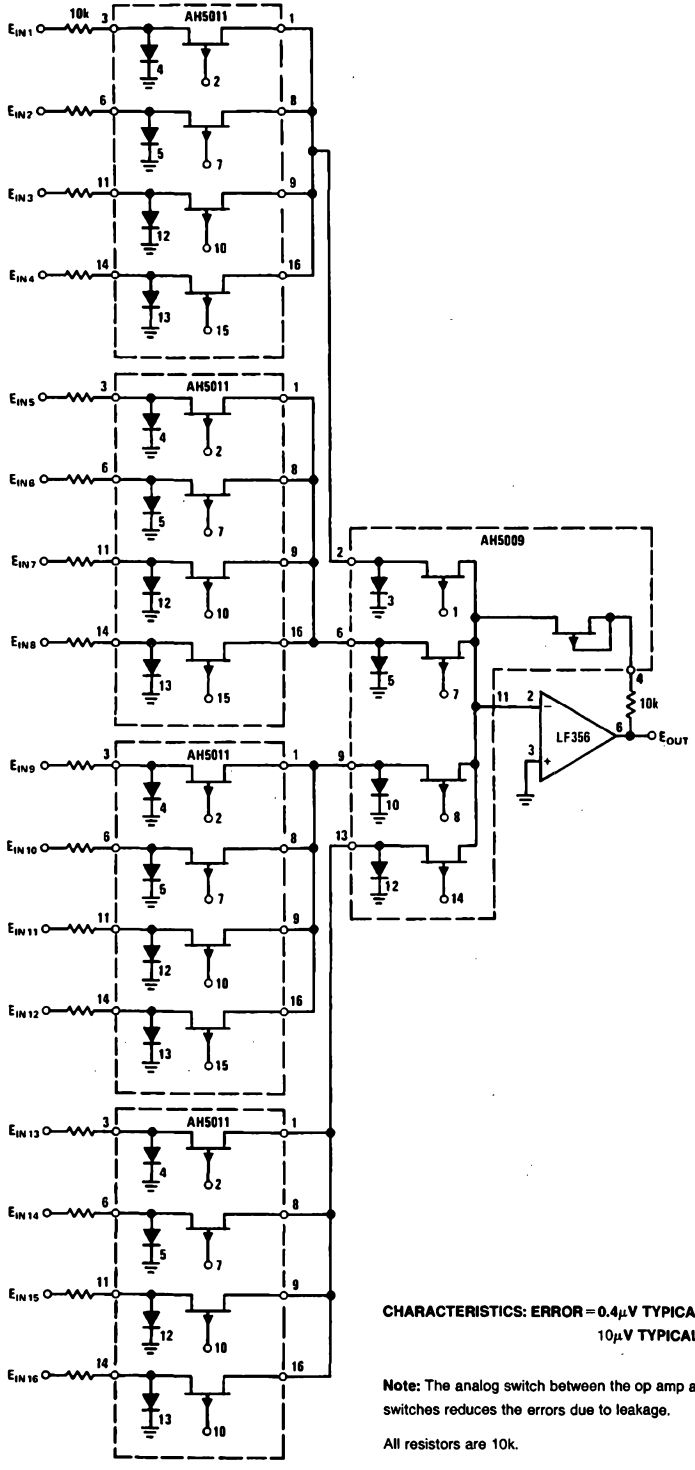
Typical Applications (Continued)

16-Channel Multiplexer



CHARACTERISTICS: ERROR = 0.4μV TYPICAL @ 25°C
10μV TYPICAL @ 70°C

Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k.

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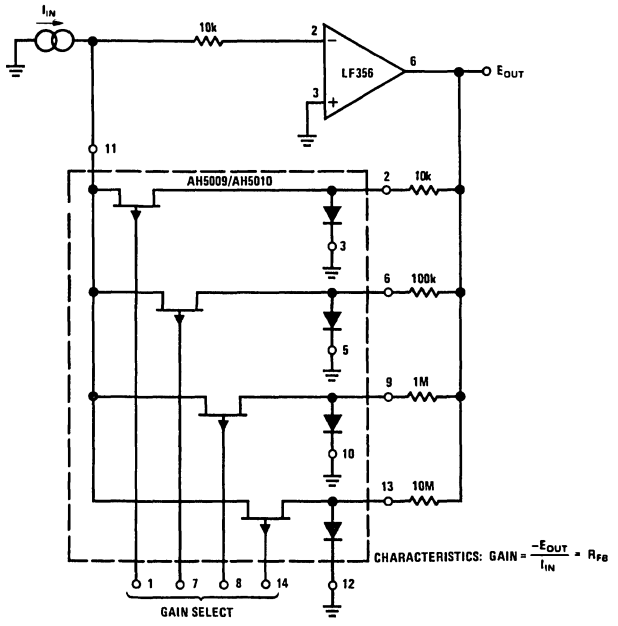
Typical Applications (Continued)

Gain Programmable Amplifier



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