Am2502/3/4 Family

Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- Can be used as serial-to-parallel converter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

3

FUNCTIONAL DESCRIPTION

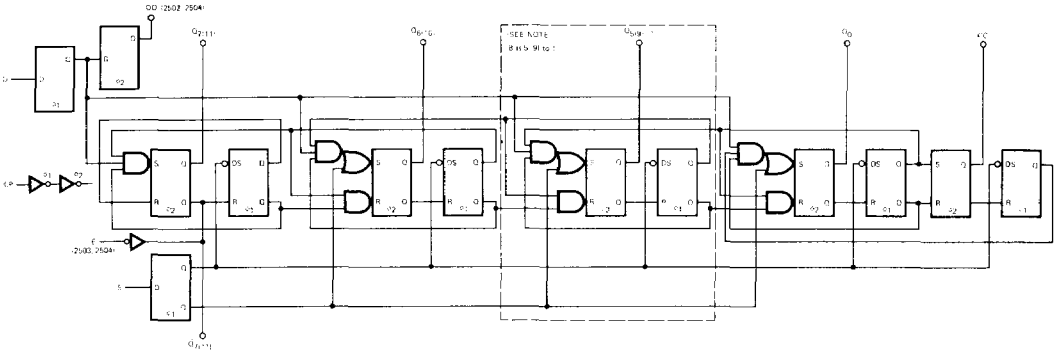
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the *clock LOW-to-HIGH transition in order to guarantee correct resetting.* After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

LOGIC DIAGRAMS



Notes: 1. Cell logic is repeated for register stages. Q_5 to Q_1 Am2502/3, Q_9 to Q_1 Am2504.
2. Numbers in parentheses are for Am2504.

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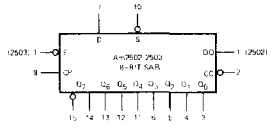
LOGIC SYMBOLS



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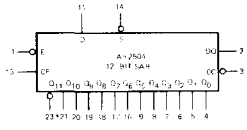
V_{CC} = Pin 16
GND = Pin 8



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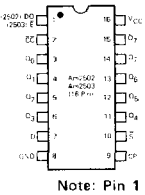
V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 15 22

CONNECTION DIAGRAMS – Top Views

D-16, P-16



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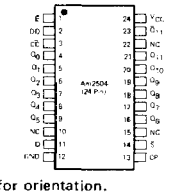
D-24, P-24



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Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS over operating temperature and voltage ranges

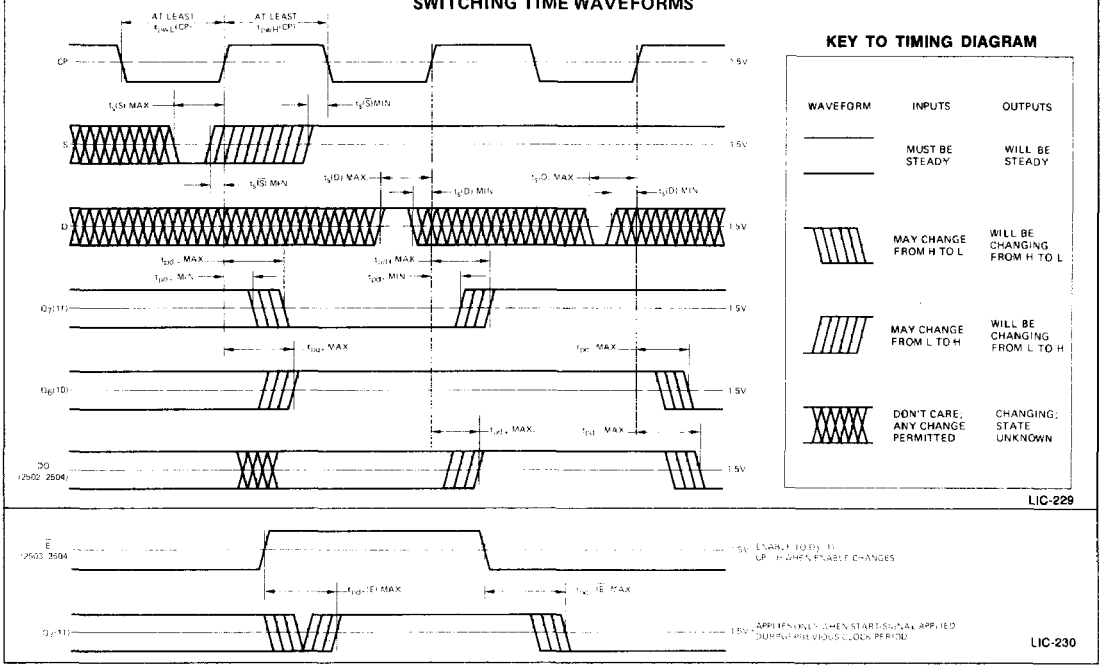
Parameters	Description	Test Conditions			Am2502/3/4 Min	Am2502/3/4 Typ (Note 1)	Am2502/3/4 Max	Am25L02/L03/L04 Min	Am25L02/L03/L04 Typ (Note 1)	Am25L02/L03/L04 Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		2.4	3.6		V
V_{OL}	Output LOW Voltage (Note 2)	V_{CC} = MIN, I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	0.15	0.3		V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8			0.7	V
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		CP, D, $\overline{S}$		−1.0	−1.6		−0.25	−0.4	mA
				$\overline{E}$		−1.5	−2.4		−0.4	−0.6	
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V		CP, D		6.0	40		2.0	20	μA
				E, $\overline{S}$		12.0	80		4.0	40	
	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−10	−25	−45	−4.0	−15	−35	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	Am25(L)02	XM		65	85		25	33	mA
				XC		65	95		25	35	
			Am25(L)03	XM		60	80		22	31	
				XC		60	90		22	33	
			Am25(L)04	XM		90	110		30	42	
				XC		90	124		30	45	

Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. V_{OL}(MAX) = 0.4V with total device fanout of less than 50 TTL Unit Loads (80mA). Otherwise, V_{OL}(MAX) = 0.45V.

SWITCHING CHARACTERISTICS T_A = 25°C, V_{CC} = +5.0V, C_L = 15pF

Parameters	Description		Am2502/3/4 Min	Am2502/3/4 Typ	Am2502/3/4 Max	Am25L02/3/4 Min	Am25L02/3/4 Typ	Am25L02/3/4 Max	Units
t_{pd+}	Turn Off Delay CP to Output HIGH (except Q_{11}, $\overline{Q}_{11}$)		10	29	45	20	75	110	ns
	Turn Off Delay CP to Q_{11} or $\overline{Q}_{11}$ HIGH		10	35	50	30	100	140	
t_{pd-}	Turn On Delay CP to Output LOW		10	27	40	20	75	100	ns
t_s(D)	Setup Time Data Input		−10	4.0	10	−15	8.0	20	ns
t_s(S)	Setup Time Start Input		0	9.0	16	0	20	25	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	Am2503/Am2504) C_P = H, $\overline{S}$ = L		15	23		50	75	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			20	30		60	75	
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46		100	150	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20		70	100	ns
f_{max}	Maximum Clock Frequency		15	25		3.5	5.0		MHz

SWITCHING TIME WAVEFORMS



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2 L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the register.

$\overline{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$\overline{Q}_7(11)$ The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{E})$ The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\overline{E})$ The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

t_s(D) Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

$t_s(\overline{S})$ Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

t_{pw}(CP) The minimum clock pulse width (LOW or HIGH) required for proper register operation.

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

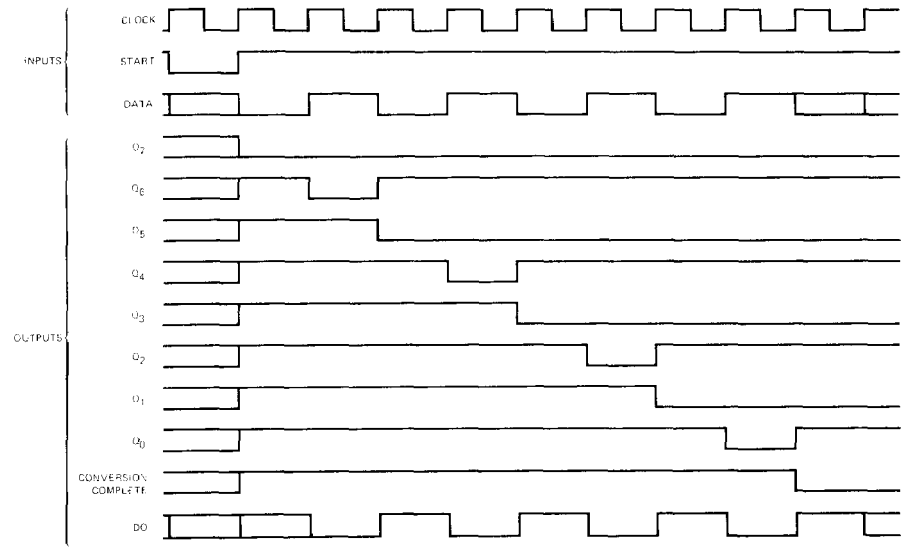
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: *Truth Table for Am2504 is extended to include 12 outputs.*

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital *output from the register is active LOW. That is, a logic* "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion. Additional data input gating should be used to eliminate the possibility of false BCD codes.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (Q_{11}) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

Am25(L)02/3 TIMING CHART



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Am2502/3 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ (2503)	1	1.5	2	–	–
DO (2502)	1	–	–	12	6
$\overline{CC}$	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	1	1	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
$\overline{S}$	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
Q_7	14	–	–	12	6
$\overline{Q}_7$	15	–	–	12	6
V_{CC}	16	–	–	–	–

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am2504 LOADING RULES (IN UNIT LOADS)

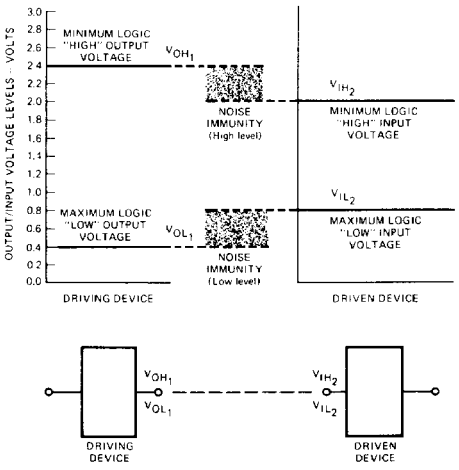
Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$	1	1.5	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	1	1	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
Q_{11}	21	–	–	12	6
NC	22	–	–	–	–
$\overline{Q}_{11}$	23	–	–	12	6
V_{CC}	24	–	–	–	–

A Standard TTL Unit Load is defined as 40μA measured at 2.4V HIGH and –1.6mA measured at 0.4V LOW.

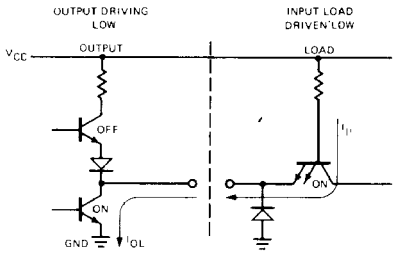
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

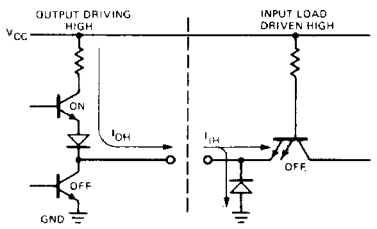
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW



Current Interface Conditions – HIGH



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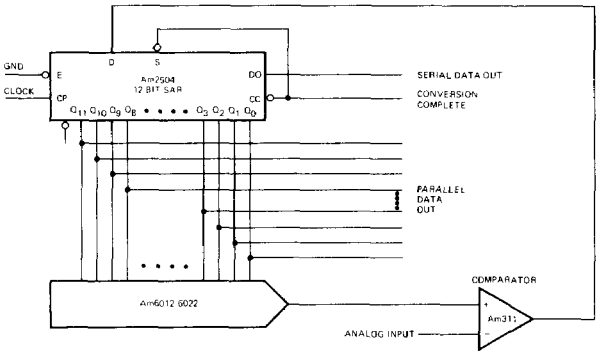
Am2502/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter



This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second.

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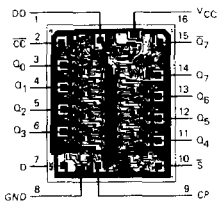
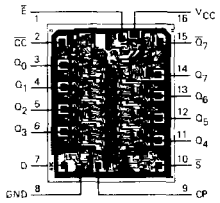
Metallization and Pad Layouts

Am2502



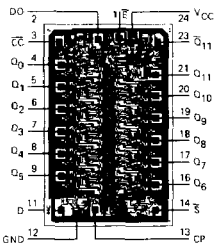
DIE SIZE 0.087" X 0.105"

Am2503



DIE SIZE 0.087" X 0.105"

Am2504



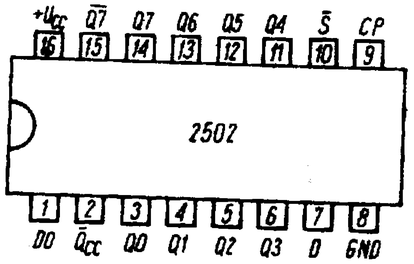
DIE SIZE 0.087" X 0.135"

ORDERING INFORMATION*

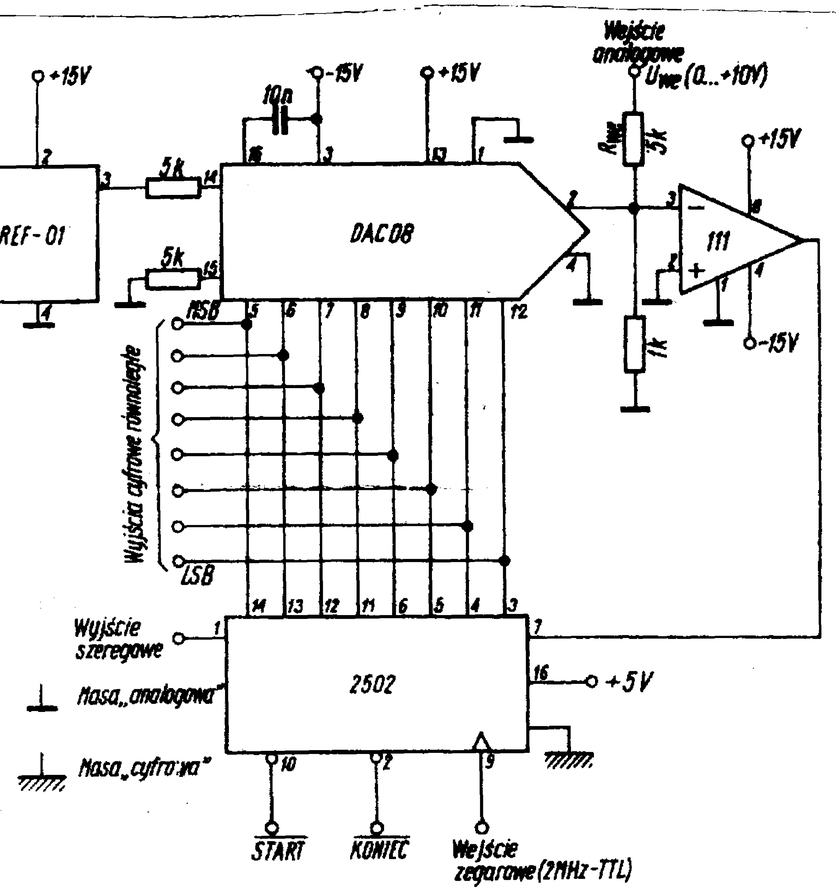
Order Number	Order Number	Package Type	Temperature Range	Bits
Am2502DM	Am25L02DM	Hermetic DIP	−55 to +125°C	8
Am2503DM	Am25L03DM	Hermetic DIP	−55 to +125°C	8
Am2504DM	Am25L04DM	Hermetic DIP	−55 to +125°C	12
Am2502FM	Am25L02FM	Flat Package	−55 to +125°C	8
Am2503FM	Am25L03FM	Flat Package	−55 to +125°C	8
Am2504FM	AM25L04FM	Flat Package	−55 to +125°C	12
Am2502XM	Am25L02XM	Dice	−55 to +125°C	8
Am2503XM	Am25L03XM	Dice	−55 to +125°C	8
Am2504XM	Am25L04XM	Dice	−55 to +125°C	8
Am2502DC	Am25L02DC	Hermetic DIP	0 to +70°C	8
Am2503DC	Am25L03DC	Hermetic DIP	0 to +70°C	8
Am2504DC	Am25L04DC	Hermetic DIP	0 to +70°C	12
Am2502PC	Am25L02PC	Plastic	0 to +70°C	8
Am2503PC	Am25L03PC	Plastic	0 to +70°C	8
Am2504PC	Am25L04PC	Plastic	0 to +70°C	12
Am2502XC	Am25L02XC	Dice	0 to +70°C	8
Am2503XC	Am25L03XC	Dice	0 to +70°C	8
Am2504XC	Am25L04XC	Dice	0 to +70°C	12

*Also available with burn-in processing. To order add suffix B to part number.

DVS AM 2502



Rys. 8. Rozkład wyprowadzeń rejestru aproksymacyjnego 2502



Rys. 9. Schemat 8-bitowego kompensacyjnego przetwornika a c

Tablica 3. **Opis działania aproksymacyjnego 2502**

Numer zbocza zegarowego	Wejścia		Wyjścia									
	D	S	D0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{Qcc}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	X	L	H	H	H	H	H	H	H	H
2	D6	H	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0	L