ADVANCE INFORMATION

Am29240™, Am29245™, and Am29243™

High-Performance RISC Microcontrollers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

All three microcontrollers in the Am29240™ microcontroller series have the following characteristics:

- **Completely integrated system for embedded applications**
- **Full 32-bit architecture**
- **4-Kbyte, two-way set-associative instruction cache**
- **4-Gbyte virtual address space, 304-Mbyte physical space implemented**
- **Glueless system interfaces with on-chip wait state control**
- **36 VAX million instructions per second (MIPS) sustained at 25 MHz**
- **Four banks of ROM, each separately programmable for 8-, 16-, or 32-bit interface**
- **Four banks of DRAM, each separately programmable for 16- or 32-bit interface**
- **Single-cycle ROM burst-mode and DRAM page-mode access**
- **6-port peripheral interface adapter**
- **16-line programmable I/O port**
- **Bidirectional parallel port controller**
- **Interrupt controller**
- **Fully pipelined integer unit**
- **Three-address instruction architecture**
- **192 general purpose registers**
- **Traceable Cache™ technology instruction and data cache tracing**
- **IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port and Boundary Scan Architecture**
- **Binary compatibility with all 29K™ family microprocessors and microcontrollers**
- **Fully static system-clock capabilities**
- **CMOS technology/TTL compatible**
- **196-pin Plastic Quad Flat Pack (PQFP) package***
- **5-V power supply***

Note: ** The new Am29240EH, Am29245EH, and Am29243EH microcontrollers are packaged as 208-pin PQFPs and use a 3.3-V power supply with 5-V-tolerant I/O. Before beginning a new design, check with your field representative for schedule and availability of the Am29240EH microcontroller series, described in Amendment 1 (order #17787/1).*

Am29240 Microcontroller

The Am29240 microcontroller has the following additional features:

- **2-Kbyte, two-way set-associative data cache**
- **Single-cycle 32-bit multiplier for faster integer math; two-cycle Multiply Accumulate (MAC) function**
- **16-entry on-chip Memory Management Unit (MMU) with one Translation Look-Aside Buffer**
- **4-channel double-buffered DMA controller with queued reload**
- **Two serial ports (UARTs)**
- **Bidirectional bit serializer/deserializer**
- **20- and 25-MHz operating frequencies**
- **Scalable Clocking™ feature with full- and double-speed internal clock**

Am29245 Microcontroller

The low-cost Am29245™ microcontroller is similar to the Am29240 microcontroller, without the data cache and 32-bit multiplier. It includes the following features:

- **16-entry on-chip MMU with one TLB**
- **Bidirectional bit serializer/deserializer**
- **Two-channel DMA controller**
- **One serial port (UART)**
- **16-MHz operating frequency**

Am29243 Microcontroller

The Am29243™ data microcontroller is similar to the Am29240 microcontroller, without the video interface. It includes the following features:

- **2-Kbyte, two-way set-associative data cache**
- **Single-cycle 32-bit multiplier for faster integer math; two-cycle MAC**
- **32-entry on-chip MMU with dual TLBs**
- **4-channel, double-buffered DMA controller with queued reload**
- **Two serial ports (UARTs)**
- **20- and 25-MHz operating frequencies**
- **Scalable Clocking feature with full- and double-speed internal clock**
- **DRAM parity**

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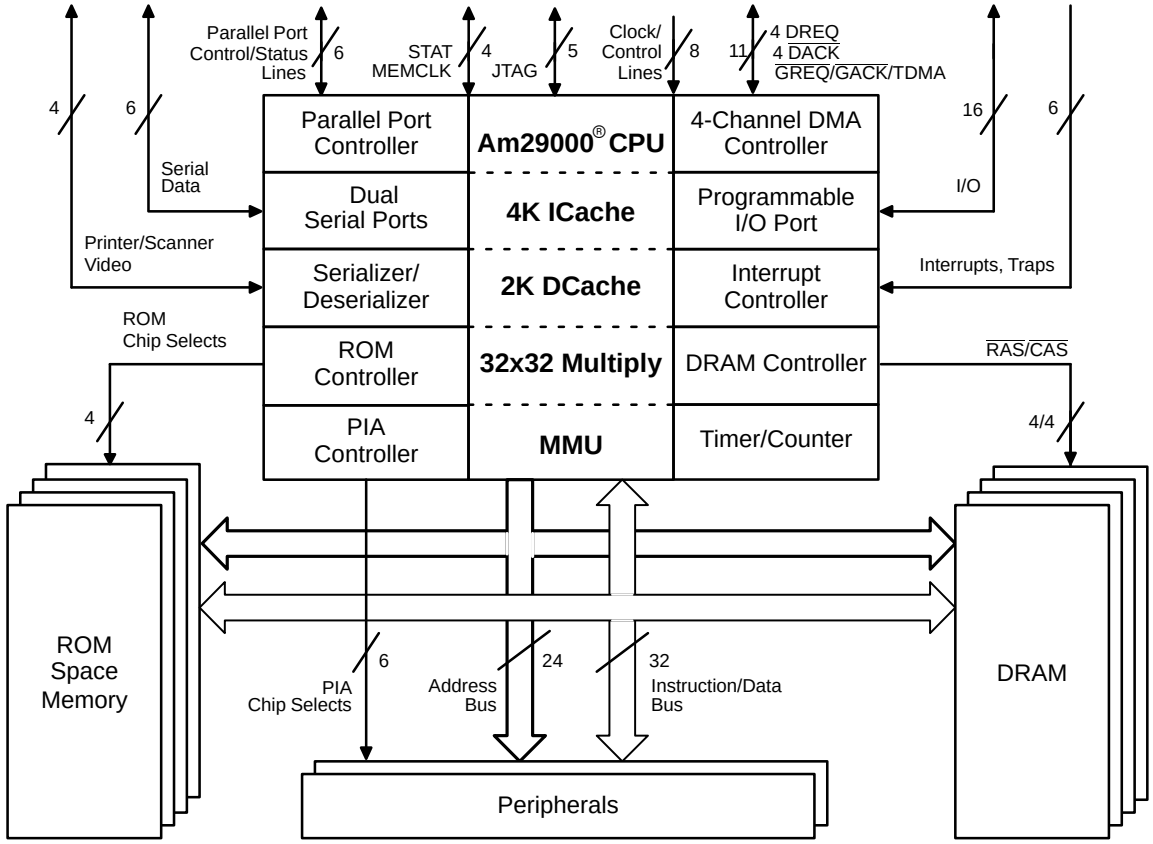

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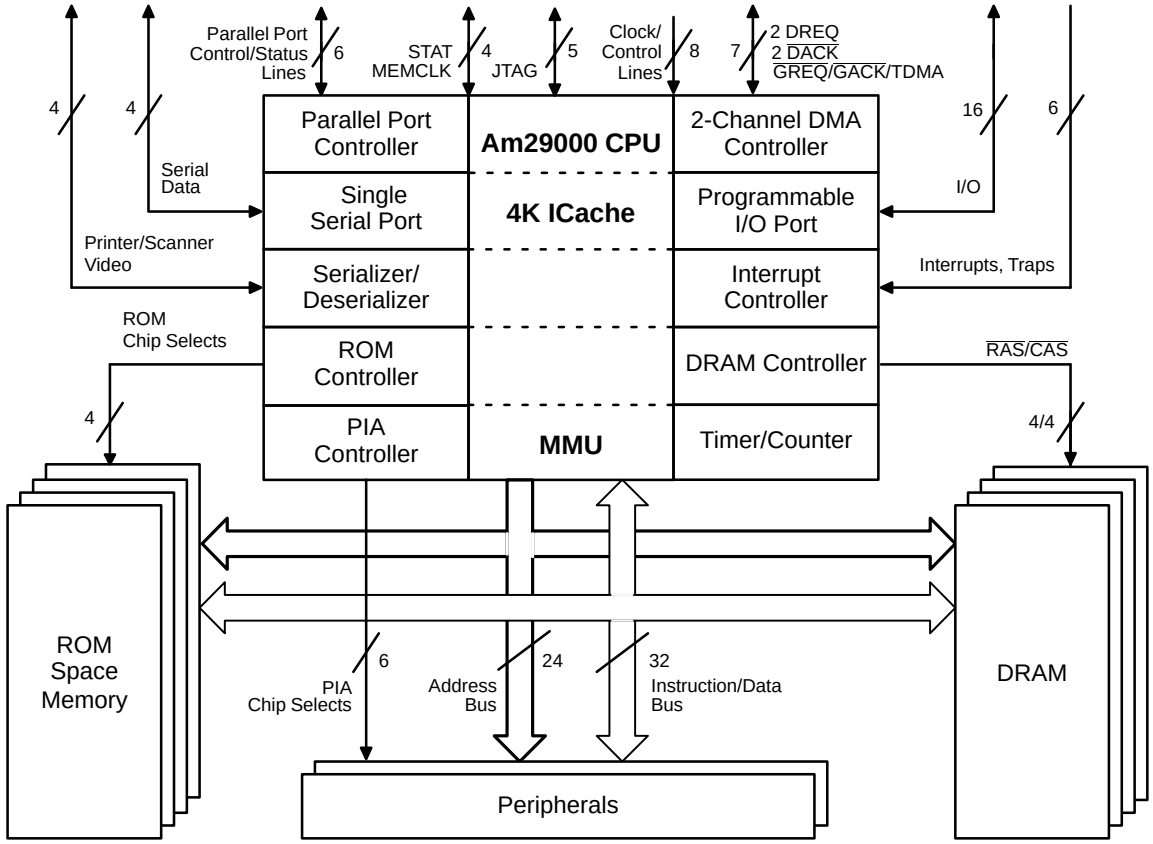
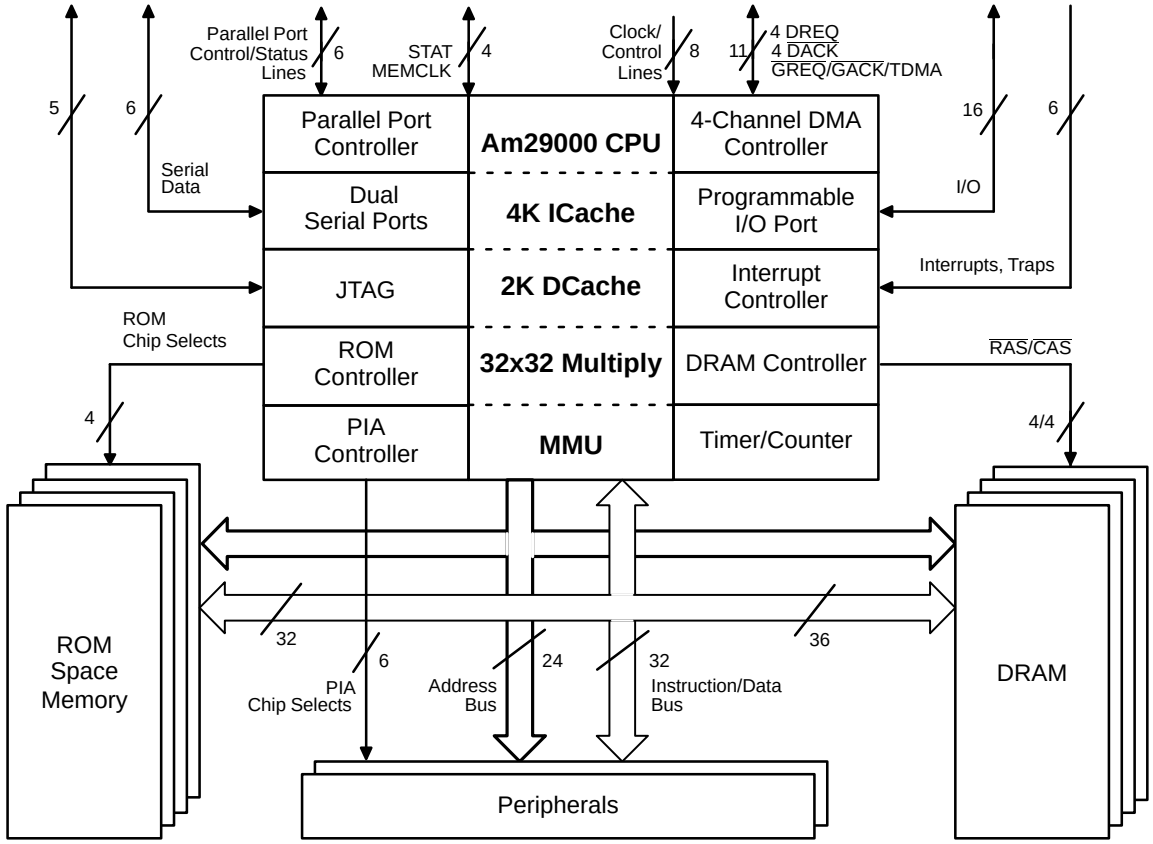


Am29243 MICROCONTROLLER BLOCK DIAGRAM



CUSTOMER SERVICE

AMD's customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from AMD's worldwide staff of field application engineers and factory support staff.

Hotline, E-mail, and Bulletin Board Support

For answers to technical questions, AMD® provides a toll-free number for direct access to our engineering support staff. For overseas customers, the easiest way to reach the engineering support staff with your questions is via fax with a short description of your question. AMD 29K family customers also receive technical support through electronic mail. This worldwide service is available to 29K family product users via the international Internet e-mail service. Also available is the AMD bulletin board service, which provides the latest 29K family product information, including technical information and data on upcoming product releases.

Engineering Support Staff

(800) 292-9263, ext. 2	toll-free for U.S.
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Product Information

A simple phone call gets you free printed publications, such as data books, user's manuals, data sheets, application notes, the Fusion29K Partner Solutions Catalog and Newsletter, and other literature. Internationally, contact your local AMD sales office for complete 29K family literature. For electronic copies of the most current product information and publications on the 29K family, visit AMD's worldwide web site on the Internet.

Literature Request

(800) 292-9263, ext. 3	toll-free for U.S.
(512) 602-5651	direct dial worldwide
(512) 602-7639	fax for U.S.
(800) 222-9323, option 2	AMD Facts-On-Demand™ fax information service toll-free for U.S.
http://www.amd.com	worldwide web

GENERAL DESCRIPTION

The Am29240 microcontroller series is an enhanced bus-compatible extension of the Am29200™ RISC microcontroller family, with two to four times the performance. The Am29240 microcontroller series includes the Am29240 microcontroller, the low-cost Am29245 microcontroller, and the Am29243 data microcontroller. The on-chip caches, MMU, faster integer math, and extended DMA addressing capability of the Am29240 microcontroller series allow the embedded systems designer to provide increasing levels of performance and software compatibility throughout a range of products (see Table 1 on page 7).

Based on a static low-voltage design, these CMOS-technology devices offer a complete set of system peripherals and interfaces commonly used in embedded applications. Compared to CISC processors, the Am29240 microcontroller series offers better performance, more efficient use of low-cost memories, lower system cost, and complete design flexibility for the designer. Coupled with hardware and software development tools from AMD and the AMD Fusion29K® partners, the Am29240 microcontroller series provides the embedded product designer with the cost and performance edge required by today's marketplace.

Am29240 Microcontroller

For general-purpose embedded applications, such as mass-storage controllers, communications, digital signal processing, networking, industrial control, pen-based systems, and multimedia, the Am29240 microcontroller provides a high-performance solution with a low total-system cost. The memory interface of the Am29240 microcontroller provides even faster direct memory access than the Am29200 microcontroller. This performance improvement minimizes the effect of memory latency, allowing designers to use low-cost memory with simpler memory designs. On-chip instruction and data caches provide even better performance for time-critical code.

Other on-chip functions include: a ROM controller, DRAM controller, peripheral interface adapter controller, DMA controller, programmable I/O port, parallel port controller, serial ports, and an interrupt controller. For a complete description of the technical features, on-chip peripherals, programming interface, and instruction set, please refer to the *Am29240, Am29245, and Am29243 RISC Microcontrollers User's Manual* (order #17741).

Am29245 Microcontroller

The low-cost Am29245 microcontroller is designed for embedded applications in which cost and space constraints, along with increased performance requirements, are primary considerations.

The Am29245 microcontroller also provides an easy upgrade path for Am29200, Am29202™, and Am29205™ microcontroller-based products.

Am29243 Microcontroller

With DRAM parity support and a full MMU, the Am29243 data microcontroller is recommended for communications applications that require high-speed data movement and fast protocol processing in a fault-tolerant environment.

Both the Am29243 and Am29240 microcontrollers support fly-by DMA at 100 Mbytes/s for LANs and switching applications, and a two-cycle Multiply Accumulate function for DSP applications. The low power requirements make either microcontroller a good choice for field-deployed devices.

29K Family Development Support Products

Contact your local AMD representative for information on the complete set of development support tools. The following software and hardware development products are available on several hosts:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators
- Execution boards

Third-Party Development Support Products

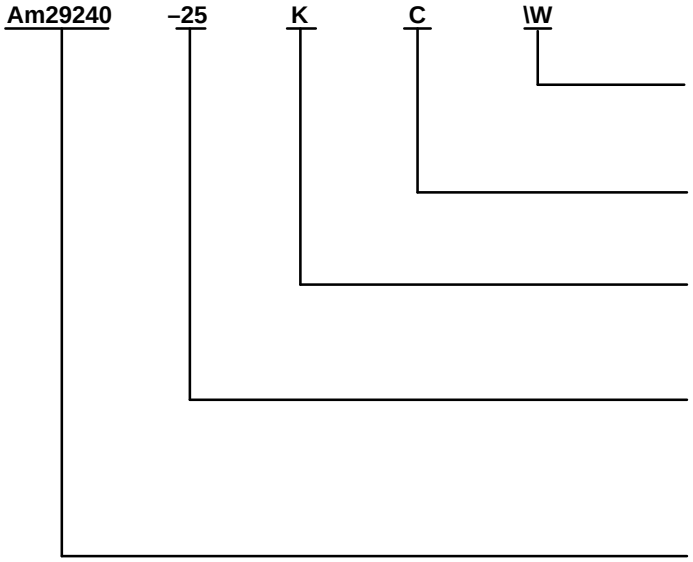
The Fusion29K Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs. Products/solutions available from the AMD Fusion29K partners include the following:

- Silicon products
- Software generation and debug tools
- Hardware development tools
- Board-level products
- Laser-printer solutions
- Multiuser, kernel, and real-time operating systems
- Graphics solutions
- Networking and communication solutions
- Manufacturing support
- Custom software consulting, support, and training

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



PROCESSING
\W = Trimmed and Formed (PQB 196)

TEMPERATURE RANGE
C = Commercial (T_C = 0°C to +85°C)

PACKAGE TYPE
K = 196-Lead Plastic Quad Flat Pack (PQB 196)

SPEED OPTION
–25 = 25 MHz
–20 = 20 MHz
–16 = 16 MHz

DEVICE NUMBER/DESCRIPTION
Am29240 RISC Microcontroller
Am29245 RISC Microcontroller
Am29243 RISC Data Microcontroller

Valid Combinations	
Am29240–20 Am29240–25	KC\W
Am29243–20 Am29243–25	KC\W
Am29245–16	KC\W

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

RELATED AMD PRODUCTS

29K Family Devices

Product	Description
Am29000®	32-bit RISC microprocessor
Am29005™	Low-cost 32-bit RISC microprocessor with no MMU and no branch target cache
Am29030™	32-bit RISC microprocessor with 8-Kbyte instruction cache
Am29035™	32-bit RISC microprocessor with 4-Kbyte instruction cache
Am29040™	32-bit RISC microprocessor with 8-Kbyte instruction cache and 4-Kbyte data cache
Am29050™	32-bit RISC microprocessor with on-chip floating point
Am29200™	32-bit RISC microcontroller
Am29202™	Low-cost 32-bit RISC microcontroller with IEEE-1284-compliant parallel interface
Am29205™	Low-cost 32-bit RISC microcontroller

Table 1. Product Comparison—Am29200 Microcontroller Family

FEATURE	Am29205 Controller	Am29202 Controller	Am29200 Controller	Am29245 Controller	Am29240 Controller	Am29243 Controller
Instruction Cache	—	—	—	4 Kbytes	4 Kbytes	4 Kbytes
Data Cache	—	—	—	—	2 Kbytes	2 Kbytes
Cache Associativity	—	—	—	2-way	2-way	2-way
Integer Multiplier	Software	Software	Software	Software	32 x 32-bit	32 x 32-bit
Memory Management Unit (MMU)	—	—	—	1 TLB 16 Entry	1 TLB 16 Entry	2 TLBs 32 Entry
Data Bus Width						
Internal	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
External	16 bits	32 bits	32 bits	32 bits	32 bits	32 bits
ROM Interface						
Banks	3	4	4	4	4	4
Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
ROM Size (Max/Bank)	4 Mbytes	4 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes
Boot-Up ROM Width	16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Burst-Mode Access	Not Supported	Not Supported	Supported	Supported	Supported	Supported
DRAM Interface						
Banks	4	4	4	4	4	4
Width	16 bits only	16, 32 bits	16, 32 bits	16, 32 bits	16, 32 bits	16, 32 bits
Size: 32-Bit Mode	—	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank
Size: 16-Bit Mode	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank
Video DRAM	Not Supported	Not Supported	Supported	Supported	Supported	Not Supported
Access Cycles						
Initial/Burst	3/2	3/2	3/2	3/1	3/1	3/1
DRAM Parity	No	No	No	No	No	Yes
On-Chip DMA						
Width (ext. peripherals)	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Total Number of Channels	2	2	2	2	4	4
Externally Controlled	1	1	2	2	4	4
External Master Access	No	No	Yes	Yes	Yes	Yes
External Master Burst	No	No	No	Yes	Yes	Yes
External Terminate Signal	No	No	Yes	Yes	Yes	Yes
Scalable Clocking Double-Frequency CPU Option	No	No	No	No	Yes	Yes
Low-Voltage Operation	No	No	No	Yes	Yes	Yes
Peripheral Interface Adapter (PIA)						
PIA Ports	2	2	6	6	6	6
Data Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Min. Cycles Access	3	3	3	1	1	1
Programmable I/O Port (PIO)						
Signals	8	12	16	16	16	16
Signals programmable for interrupt generation	8	8	8	8	8	8
Serial Ports						
Ports	1 Port	1 Port	1 Port	1 Port	2 Ports	2 Ports
$\overline{DSR}/\overline{DTR}$	PIO signals	PIO signals	Supported	Supported	1 Port Supported	1 Port Supported
Interrupt Controller						
External Interrupt Pins	2	2	4	4	4	4
External Trap and Warn Pins	0	0	3	3	3	3
Parallel Port Controller	Yes	Yes	Yes	Yes	Yes	Yes
32-Bit Transfer	No	Yes	Yes	Yes	Yes	Yes
IEEE-1284 Interface	No	Yes	No	No	No	No
JTAG Debug Support	No	Yes	Yes	Yes	Yes	Yes
Serializer/Deserializer	Yes	Yes	Yes	Yes	Yes	No
Pin Count and Package	100 PQFP	132 PQFP	168 PQFP	196 PQFP	196 PQFP	196 PQFP
Operating Voltage						
V_{CC}	5 V	5 V	5 V	5 V	5 V	5 V
I/O Tolerance	5 V	5 V	5 V	5 V	5 V	5 V
Processor Clock Rate	12, 16 MHz	12, 16, 20 MHz	16, 20 MHz	16 MHz	20, 25 MHz	20, 25 MHz

KEY FEATURES AND BENEFITS

The Am29240 microcontroller series extends the line of RISC microcontrollers based on 29K family architecture, providing performance upgrades to the Am29205 and Am29200 microcontrollers. The RISC microcontroller product line allows users to benefit from the very high performance of the 29K family architecture, while also capitalizing on the very low system cost made possible by integrating processor and peripherals.

The Am29240 microcontroller series expands the price/performance range of systems that can be built with the 29K family. The Am29240 microcontroller series is fully software compatible with the Am29000, Am29005, Am29030, Am29035, Am29040, and Am29050 microprocessors, as well as the Am29200 and Am29205 microcontrollers. It can be used in existing 29K family microcontroller applications without software modifications.

On-Chip Caches

The Am29240 microcontroller series incorporates a 4-Kbyte, two-way instruction cache that supplies most processor instructions without wait states at the processor frequency. For best performance, the instruction cache supports critical-word-first reloading with fetch-through, so that the processor receives the required instruction and the pipeline restarts with minimum delay. The instruction cache has a valid bit per word to minimize the reload overhead. All cache array elements are visible to software for testing and preload.

The Am29240 and Am29243 microcontrollers incorporate a 2-Kbyte, two-way set-associative data cache. The data cache appears in the execute stage of the processor pipeline, so that loaded data is available immediately to the next instruction. This provides the maximum performance for loads without requiring load scheduling. The data cache performs critical-word-first, wrap-around, and burst-mode refill with load-through. This minimizes the time the processor waits on external data as well as minimizing the reload time. The data cache uses a write-through policy with a two-entry write buffer. Byte, half-word, and word reads and writes are supported. All cache array elements are visible to software for testing and preload.

Single-Cycle Multiplier

The Am29240 and Am29243 microcontrollers incorporate a full combinatorial multiplier that accepts two 32-bit input operands and produces a 32-bit result in a single cycle. The multiplier can produce a 64-bit result in two cycles. The multiplier permits maximum performance without requiring instruction scheduling, since the latency of the multiply is the same as the latency of other integer operations. High-performance multiplication benefits imaging, signal processing, and state modeling applications.

Complete Set of Common Peripherals

The Am29240 microcontroller series minimizes system cost by incorporating a complete set of system facilities commonly found in embedded applications, eliminating the cost of additional components. The on-chip functions include: a ROM controller, a DRAM controller, a peripheral interface adapter, a DMA controller, a programmable I/O port, a parallel port, up to two serial ports, and an interrupt controller. A video interface is also included in the Am29240 and Am29245 microcontrollers for printer, scanner, and other imaging applications. These facilities allow many simple systems to be built using only the Am29240 microcontroller series, external ROM, and/or DRAM memory.

ROM Controller

The ROM controller supports four individual banks of ROM or other static memory, each with its own timing characteristics. Each ROM bank may be a different size and may be either 8, 16, or 32 bits wide. The ROM banks can appear as a contiguous memory area of up to 64 Mbytes in size. The ROM controller also supports byte, half-word, and word writes to the ROM memory space for devices such as flash EPROMs and SRAMs.

DRAM Controller

The DRAM controller supports four separate banks of dynamic memory. Each bank may be a different size and may be either 16 or 32 bits wide. The DRAM banks can appear as a contiguous memory area of up to 64 Mbytes in size. The DRAM controller supports three-cycle accesses, with single-cycle page-mode and burst-mode accesses.

Peripheral Interface Adapter

The Peripheral Interface Adapter (PIA) permits glueless interfacing to as many as six external peripheral chips. The PIA allows for additional system features implemented by external peripheral chips.

DMA Controller

The DMA controller provides up to four channels for transferring data between the DRAM and internal or external peripherals. The DMA channels are double buffered to relax constraints on reload time.

I/O Port

The I/O port permits direct access to 16 individually programmable external input/output signals. Eight of these signals can be configured to cause interrupts.

Parallel Port

The parallel port implements a bidirectional IBM PC-compatible parallel interface to a host processor.

Serial Port

The serial port implements up to two full-duplex UARTs.

Serializer/Deserializer

The serializer/deserializer (video interface) on the Am29240 and Am29245 microcontrollers permits direct connection to a number of laser-marking engines, video displays, or raster input devices such as scanners.

Interrupt Controller

The interrupt controller generates and reports the status of interrupts caused by on-chip peripherals.

Wide Range of Price/Performance Points

To reduce design costs and time-to-market, the product designer can use the Am29200 microcontroller family and one basic system design as the foundation for an entire product line. From this design, numerous implementations of the product at various levels of price and performance may be derived with minimum time, effort, and cost.

The Am29240 RISC microcontroller series supports this capability through various combinations of on-chip caches, programmable memory widths, programmable wait states, burst-mode and page-mode access support, bus compatibility, and 29K family software compatibility. A system can be upgraded using various memory architectures without hardware and software redesign.

Within the Am29240 microcontroller series, the external interfaces and the processor operate at frequencies in the range of 16 to 25 MHz. Using the Scalable Clocking feature on the Am29240 and Am29243 microcontrollers, the internal processor core can operate either at the interface frequency or twice this frequency. For example, the processor can operate at 25 MHz while the interface operates at 12.5 MHz.

The ROM controller accommodates memories that are either 8, 16, or 32 bits wide, and the DRAM controller accommodates dynamic memories that are either 16 or 32 bits wide. This unique feature provides a flexible interface to low-cost memory, as well as a convenient, flexible upgrade path. For example, a system can start with a 16-bit memory design and can subsequently improve performance by migrating to a 32-bit memory design. One particular advantage is the ability to add memory in half-megabyte increments. This provides significant cost savings for applications that do not require larger memory upgrades.

The Am29200, Am29202, Am29205, Am29240, Am29245, and Am29243 microcontrollers allow users to address an extremely wide range of cost performance points, with higher performance and lower cost than existing designs based on CISC microprocessors.

Glueless System Interfaces

The Am29240 microcontroller series also minimizes system cost by providing a glueless attachment to external ROMs, DRAMs, and other peripheral components. Processor outputs have edge-rate control that allows them to drive a wide range of load capacitances with low noise and ringing. This eliminates the cost of external logic and buffering.

Bus and Software Compatibility

Compatibility within a processor family is critical for achieving a rational, easy upgrade path. Processors in the Am29240 microcontroller series are all members of a bus-compatible family of RISC microcontrollers. All members of this family—the Am29205, Am29202, Am29200, Am29240, Am29245, and Am29243 microcontrollers—allow improvements in price, performance, and system capabilities without requiring that users redesign their system hardware or software. Bus compatibility ensures a convenient upgrade path for future systems.

The Am29240 microcontroller series is available in a 196-pin plastic quad flat-pack (PQFP) package. The Am29240 microcontroller series is signal-compatible with the Am29200 and the Am29205 microcontrollers.

Moreover, the Am29240 microcontroller series is binary compatible with existing RISC microcontrollers and other members of the 29K family (the Am29000, Am29005, Am29030, Am29035, Am29040, and Am29050 microprocessors, as well as the Am29200, Am29202, and Am29205 microcontrollers). The Am29240 microcontroller series provides a migration path to low-cost, high-performance, highly integrated systems from other 29K family members, without requiring expensive rewrites of application software.

Complete Development and Support Environment

A complete development and support environment is vital for reducing a product's time-to-market. Advanced Micro Devices has created a standard development environment for the 29K family of processors. In addition, the Fusion29K third-party support organization provides the most comprehensive customer/partner program in the embedded processor market.

Advanced Micro Devices offers a complete set of hardware and software tools for design, integration, debugging, and benchmarking. These tools, which are available now for the 29K family, include the following:

- Software development kit that includes the High C® 29K™ optimizing C compiler with assembler, linker, ANSI library functions, 29K family architectural simulator, and MiniMON29K® debug monitor
- XRAY29K™ source-level debugger
- A complete family of demonstration and development boards

In addition, Advanced Micro Devices has developed a standard host interface (HIF) specification for operating system services, the Universal Debugger Interface (UDI) for seamless connection of debuggers to ICEs and target hardware, and extensions for the UNIX common object file format (COFF).

This support is augmented by an engineering hotline, an on-line bulletin board, and field application engineers.

Debugging and Testing

The Am29240 microcontroller series provides debugging and testing features at both the software and hardware levels.

Software debugging is facilitated by the instruction trace facility and instruction breakpoints. Instruction tracing is accomplished by forcing the processor to trap after each instruction has been executed. Instruction breakpoints are implemented by the HALT instruction or by a software trap.

The processor provides several additional features to assist system debugging and testing:

- The Test/Development Interface is composed of a group of pins that indicate the state of the processor and control the operation of the processor.
- A Traceable Cache feature permits a hardware-development system to track accesses to the on-chip caches, permitting a high level of visibility into processor operation.
- An IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port and Boundary-Scan Architecture. The Test Access Port provides a scan interface for testing processor and system hardware in a production environment, and contains extensions that allow a hardware-development system to control and observe the processor without interposing hardware between the processor and system.

PERFORMANCE OVERVIEW

The Am29240 microcontroller series offers a significant margin of performance over CISC microprocessors in existing embedded designs, since the majority of processor features were defined for the maximum achievable performance at very low cost. This section describes the features of the Am29240 microcontroller series from the point of view of system performance.

Instruction Timing

The Am29240 microcontroller series uses an arithmetic/logic unit, a field shift unit, and a prioritizer to execute most instructions. Each of these is organized to operate on 32-bit operands and provide a 32-bit result. All operations are performed in a single cycle.

The performance degradation of load and store operations is minimized in the Am29240 microcontroller series by overlapping them with instruction execution, by taking advantage of pipelining, by an on-chip data cache, and by organizing the flow of external data into the processor so that the impact of external accesses is minimized.

Pipelining

Instruction operations are overlapped with instruction fetch, instruction decode and operand fetch, instruction execution, and result write-back to the Register File. Pipeline forwarding logic detects pipeline dependencies and routes data as required, avoiding delays that might arise from these dependencies. Pipeline interlocks are implemented by processor hardware. Except for a few special cases, it is not necessary to rearrange programs to avoid pipeline dependencies, although this is sometimes desirable for performance.

On-Chip Instruction and Data Caches

On-chip instruction and data caches satisfy most processor fetches without wait states, even when the processor operates at twice the system frequency. The caches are pipelined for best performance. The reload policies minimize the amount of time spent waiting for reload, while optimizing the benefit of locality of reference.

Burst-Mode and Page-Mode Memories

The Am29240 microcontroller series directly supports burst-mode memories. The burst-mode memory supplies instructions at the maximum bandwidth, without the complexity of an external cache or the performance degradation due to cache misses.

The processor can also use the page-mode capability of common DRAMs to improve the access time in cases where page-mode accesses can be used. This is particularly useful in very low-cost systems with 16-bit-wide DRAMs, where the DRAM must be accessed twice for each 32-bit operand.

Instruction Set Overview

All 29K family members employ a three-address instruction set architecture. The compiler or assembly-language programmer is given complete freedom to allocate register usage. There are 192 general-purpose registers, allowing the retention of intermediate calculations and avoiding needless data destruction. Instruction operands may be contained in any of the general-purpose registers, and the results may be stored into any of the general-purpose registers.

The Am29240 microcontroller series instruction set contains 117 instructions that are divided into nine classes. These classes are integer arithmetic, compare, logical, shift, data movement, constant, floating point, branch, and miscellaneous. The floating-point instructions are not executed directly, but are emulated by trap handlers.

All directly implemented instructions are capable of executing in one processor cycle, with the exception of interrupt returns, loads, and stores.

Data Formats

The Am29240 microcontroller series defines a word as 32 bits of data, a half-word as 16 bits, and a byte as 8 bits. The hardware provides direct support for word-integer (signed and unsigned), word-logical, word-Boolean, half-word integer (signed and unsigned), and character data (signed and unsigned).

Word-Boolean data is based on the value contained in the most significant bit of the word. The values TRUE and FALSE are represented by the most significant bit values 1 and 0, respectively.

Other data formats, such as character strings, are supported by instruction sequences. Floating-point formats (single and double precision) are defined for the processor; however, there is no direct hardware support for these formats in the Am29240 microcontroller series.

Protection

The Am29240 microcontroller series offers two mutually exclusive modes of execution—the User and Supervisor modes—that restrict or permit accesses to certain processor registers and external storage locations.

The register file may be configured to restrict accesses to Supervisor-mode programs on a bank-by-bank basis.

Memory Management Unit

The Am29240 microcontroller series provides a memory-management unit (MMU) for translating virtual addresses into physical addresses. The page size for translation ranges from 1 Kbyte to 16 Mbytes in powers of 4. The Am29245 and Am29240 microcontrollers each have a single, 16-entry TLB. The Am29243 microcontroller has dual 16-entry TLBs, each capable of mapping pages of different size.

Interrupts and Traps

When a member of the Am29240 microcontroller series takes an interrupt or trap, it does not automatically save its current state information in memory. This lightweight interrupt and trap facility greatly improves the performance of temporary interruptions such as simple operating-system calls that require no saving of state information.

In cases where the processor state must be saved, the saving and restoring of state information is under the control of software. The methods and data structures used to handle interrupts—and the amount of state saved—may be tailored to the needs of a particular system.

Interrupts and traps are dispatched through a 256-entry vector table that directs the processor to a routine that handles a given interrupt or trap. The vector table may be relocated in memory by the modification of a processor register. There may be multiple vector tables in the system, though only one is active at any given time.

The vector table is a table of pointers to the interrupt and trap handlers, and requires only 1 Kbyte of memory. The processor performs a vector fetch every time an interrupt or trap is taken. The vector fetch requires at least three cycles, in addition to the number of cycles required for the basic memory access.

PIN DESCRIPTIONS

A23–A0

Address Bus (output, synchronous)

The Address Bus supplies the byte address for all accesses, except for DRAM accesses. For DRAM accesses, multiplexed row and column addresses are provided on A14–A1. A2–A0 are also used to provide a clock to an optional burst-mode EPROM.

BOOTW

Boot ROM Width (input, asynchronous)

This input configures the width of ROM Bank 0, so the ROM can be accessed before the ROM configuration has been set by the system initialization software. The BOOTW signal is sampled during and after a processor reset. If BOOTW is High before and after reset (tied High), the boot ROM is 32 bits wide. If BOOTW is Low before and after reset (tied Low), the boot ROM is 16 bits wide. If BOOTW is Low before reset and High after reset (tied to $\overline{\text{RESET}}$), the boot ROM is 8 bits wide. This signal has special hardening against metastable states, allowing it to be driven with a slow-rise-time signal and permitting it to be tied to $\overline{\text{RESET}}$.

$\overline{\text{BURST}}$

Burst-Mode Access (output, synchronous)

This signal is asserted to perform sequential accesses from a burst-mode device.

$\overline{\text{CAS}}3–\overline{\text{CAS}}0$

Column Address Strobes, Byte 3–0 (output, synchronous)

A High-to-Low transition on these signals causes the DRAM selected by $\overline{\text{RAS}}3–\overline{\text{RAS}}0$ to latch the column address and complete the access. To support byte and half-word writes, column address strobes are provided for individual DRAM bytes. $\overline{\text{CAS}}3$ is the column address strobe for the DRAMs, in all banks, attached to ID31–ID24. $\overline{\text{CAS}}2$ is for the DRAMs attached to ID23–ID16, and so on. These signals are also used in other special DRAM cycles.

CNTL1–CNTL0

CPU Control
(input, asynchronous, internal pull-ups)

These inputs specify the processor mode: Load Test Instruction, Step, Halt, or Normal.

$\overline{\text{DACK}}$D–$\overline{\text{DACK}}$A

DMA Acknowledge D through A
(output, synchronous)

These signals acknowledge an external transfer on a DMA channel. DMA acknowledgments are not dedicated to a particular DMA channel—each channel specifies which acknowledge line, if any, it is using. Only one channel at a time can use either $\overline{\text{DACK}}$D, $\overline{\text{DACK}}$C, $\overline{\text{DACK}}$B, or $\overline{\text{DACK}}$A, and the same channel uses the respective DREQD–DREQA signal for transfer requests. DMA transfers can occur to and from internal peripherals independent of these acknowledgments. The $\overline{\text{DACK}}$D and $\overline{\text{DACK}}$C signals are supported on the Am29240 and Am29243 microcontrollers only.

DREQD–DREQA

DMA Request D through A
(input, asynchronous, pull-up resistors)

These inputs request an external transfer on a DMA channel. DMA requests are not dedicated to a particular channel—each channel specifies which request line, if any, it is using. Only one channel at a time can use either DREQD, DREQC, DREQB, or DREQA. This channel acknowledges a transfer using the respective $\overline{\text{DACK}}$D–$\overline{\text{DACK}}$A signal. These requests are individually programmable to be either level- or edge-sensitive for either polarity of level or edge. DMA transfers can occur to and from internal peripherals independent of these requests.

The DMA request/acknowledge pairs DREQA/$\overline{\text{DACK}}$A and DREQB/$\overline{\text{DACK}}$B correspond to the Am29200 microcontroller signals DREQ0/$\overline{\text{DACK}}$0 and DREQ1/$\overline{\text{DACK}}$1, respectively. The pin placement reflects this correspondence, and a processor reset dedicates these request/acknowledge pairs to DMA channels 0 and 1, respectively. This permits backward-compatible upgrade to an Am29200 microcontroller. The DREQD and DREQC signals are supported on the Am29240 and Am29243 microcontrollers only.

$\overline{\text{DSR}}$A

Data Set Ready, Port A (output, synchronous)

This indicates to the host that the serial port is ready to transmit or receive data on Serial Port A.

$\overline{\text{DTR}}$A

Data Terminal Ready, Port A
(input, asynchronous)

This indicates to the processor that the host is ready to transmit or receive data on Serial Port A.

$\overline{\text{GACK}}$

External Memory Grant Acknowledge
(output, synchronous)

This signal indicates to an external device that it has been granted an access to the processor's ROM or DRAM, and that the device should provide an address.

The processor can be placed into a slave configuration that allows tracing of a master processor. In this configuration, $\overline{\text{GACK}}$ is used to indicate that the processor pipeline was held during the previous processor cycle.

$\overline{\text{GREQ}}$

External Memory Grant Request
(input, synchronous, pull-up resistor)

This signal is used by an external device to request an access to the processor's ROM or DRAM. To perform this access, the external device supplies an address to the ROM controller or DRAM controller.

To support a hardware-development system, $\overline{\text{GREQ}}$ should be either tied High or held at a high-impedance state during a processor reset.

ID31–ID0

Instruction/Data Bus (bidirectional, synchronous)

The Instruction/Data Bus (ID Bus) transfers instructions to, and data to and from the processor.

IDP3–IDP0

Instruction/Data Parity
(bidirectional, synchronous)

If parity checking is enabled by the PCE bit of the DRAM Control Register, IDP3–IDP0 are parity bits for the ID Bus during DRAM accesses. IDP3 is the parity bit for ID31–ID24, IDP2 is the parity bit for ID23–ID16, and so on. If parity is enabled, the processor drives IDP3–IDP0 with valid parity during DRAM writes, and expects IDP3–IDP0 to be driven with valid parity during DRAM reads. These signals are supported on the Am29243 microcontroller only.

INCLK

Input Clock (input)

This is an oscillator input at twice the system operating frequency. The processor operates either at the system operating frequency or at the INCLK frequency, as controlled by the TBO bit in the Configuration Register. The processor can operate at the INCLK frequency only if MEMCLK is an output.

$\overline{\text{INTR}}$3–$\overline{\text{INTR}}$0

Interrupt Requests 3–0
(input, asynchronous, internal pull-up resistors)

These inputs generate prioritized interrupt requests. The interrupt caused by $\overline{\text{INTR}}$0 has the highest priority,

and the interrupt caused by $\overline{\text{INTR}}$3 has the lowest priority. The interrupt requests are masked in prioritized order by the Interrupt Mask field in the Current Processor Status Register and are disabled by the DA and DI bits of the Current Processor Status Register. These signals have special hardening against metastable states, allowing them to be driven with slow-transition-time signals.

LSYNC

Line Synchronization (input, asynchronous)

This signal indicates the start of a raster line. This signal is supported on the Am29240 and Am29245 microcontrollers only.

MEMCLK

Memory Clock (input/output)

This is either a clock output or an input from an external clock generator, as determined by the MEMDRV input. It operates at the system operating frequency, which is half of the INCLK frequency. Most processor inputs and outputs are synchronous to MEMCLK. MEMCLK must be driven with CMOS levels. MEMCLK must be an output if the processor operates at the INCLK frequency.

MEMDRV

MEMCLK Drive Enable
(input, internal pull-up resistor)

This input determines whether MEMCLK is an output or an input. If this pin is High, the processor generates a clock on the MEMCLK output. If this pin is Low, the processor accepts a clock generated by the system on the MEMCLK input. This signal is tied High through an internal pull-up resistor so the signal can be left unconnected to configure MEMCLK as an output.

PACK

Parallel Port Acknowledge (output, synchronous)

This signal is used by the processor to acknowledge a transfer from the host or to indicate to the host that data has been placed on the port.

PAUTOFD

Parallel Port Autofeed (input, asynchronous)

This signal is used by the host to indicate how line feeds should be performed or is used to indicate that the host is busy and cannot accept a data transfer.

$\overline{\text{PBUSY}}$

Parallel Port Busy (output, synchronous)

This indicates to the host that the Parallel Port is busy and cannot accept a data transfer.

$\overline{\text{PIACS}}$5–$\overline{\text{PIACS}}$0

Peripheral Chip Selects, Regions 5–0
(output, synchronous)

These signals are used to select individual peripheral devices. DMA channels may be programmed to use dedicated chip selects during an external peripheral access.

$\overline{\text{PIAOE}}$

Peripheral Output Enable (output, synchronous)

This signal enables the selected peripheral device to drive the ID bus.

$\overline{\text{PIAWE}}$

Peripheral Write Enable (output, synchronous)

This signal causes data on the ID bus to be written into the selected peripheral.

PIO15–PIO0

Programmable Input/Output
(input/output, asynchronous)

These signals are available for direct software control and inspection. PIO15–PIO8 may be individually programmed to cause processor interrupts. These signals have special hardening against metastable states, allowing them to be driven with slow-transition-time signals.

The PIO signals are sampled during a processor reset. After reset, the sampled value is held in the PIO Input Register. This sampled value is supplied the first time this register is read, unless the read is preceded by write to the PIO Input Register or by a read or write of any other PIO register. This may be used to indicate system configuration information to the processor during a reset.

$\overline{\text{POE}}$

Parallel Port Output Enable (output, synchronous)

This signal enables an external data buffer containing data from the host to drive the ID Bus.

PSTROBE

Parallel Port Strobe (input, asynchronous)

This signal is used by the host to indicate that data is on the Parallel Port or to acknowledge a transfer from the processor.

PSYNC

Page Synchronization
(input/output, asynchronous)

This signal indicates the beginning of a raster page. This signal is supported on the Am29240 and Am29245 microcontrollers only.

$\overline{\text{PWE}}$

Parallel Port Write Enable (output, synchronous)

This signal writes a buffer with data on the ID Bus. Then, the buffer drives data to the host.

R/$\overline{\text{W}}$

Read/Write (output, synchronous)

During an external ROM, DRAM, DMA, or PIA access, this signal indicates the direction of transfer: High for a read and Low for a write.

$\overline{\text{RAS}}$3–$\overline{\text{RAS}}$0

Row Address Strobe, Banks 3–0 (output, synchronous)

A High-to-Low transition on one of these signals causes a DRAM in the corresponding bank to latch the row address and begin an access. $\overline{\text{RAS}}$3 starts an access in DRAM Bank 3, and so on. These signals also are used in other special DRAM cycles.

$\overline{\text{RESET}}$

Reset (input, asynchronous)

This input places the processor in the Reset mode. This signal has special hardening against metastable states, allowing it to be driven with a slow-rise-time signal.

$\overline{\text{ROMCS}}$3–$\overline{\text{ROMCS}}$0

ROM Chip Selects, Banks 3–0 (output, synchronous)

A Low level on one of these signals selects the memory devices in the corresponding ROM bank. $\overline{\text{ROMCS}}$3 selects devices in ROM Bank 3, and so on. The timing and access parameters of each bank are individually programmable.

$\overline{\text{ROMOE}}$

ROM Output Enable (output, synchronous)

This signal enables the selected ROM Bank to drive the ID bus. It is used to prevent bus contention when switching between different ROM banks or switching between a ROM bank and another device or DRAM bank.

$\overline{\text{RSWE}}$

ROM Space Write Enable (output, synchronous)

This signal is used to write an alterable memory in a ROM bank (such as an SRAM or Flash EPROM).

RXDA

Receive Data, Port A (input, asynchronous)

This input is used to receive serial data to Serial Port A.

RXDB

Receive Data, Port B (input, asynchronous)

This input is used to receive data to Serial Port B. This signal is supported on the Am29240 and Am29243 microcontrollers only.

STAT2–STAT0

CPU Status (output, synchronous)

These outputs indicate information about the processor or the current access for the purposes of hardware debug.

TCK

Test Clock Input (input, asynchronous, pull-up resistor)

This input is used to operate the Test Access Port. The state of the Test Access Port must be held if this clock is held either High or Low. This clock is internally synchronized to MEMCLK for certain operations of the Test Access Port controller, so signals internally driven and sampled by the Test Access Port are synchronous to processor internal clocks.

TDI

Test Data Input (input, synchronous to TCK, pull-up resistor)

This input supplies data to the test logic from an external source. It is sampled on the rising edge of TCK. If it is not driven, it appears High internally.

TDMA

Terminate DMA (input/output, synchronous)

This signal is either an input or an output as controlled by the corresponding DMA Control Register. As an input, this signal can be asserted during an external DMA transfer (non-fly-by) to terminate the transfer after the current access. The TDMA input is ignored during fly-by transfers. As an output, this signal is asserted to indicate the final transfer of a sequence.

TDO

Test Data Output (three-state output, synchronous to TCK)

This output supplies data from the test logic to an external destination. It changes on the falling edge of TCK. It is in the high-impedance state except when scanning is in progress.

TMS

Test Mode Select (input, synchronous to TCK, pull-up resistor)

This input is used to control the Test Access Port. If it is not driven, it appears High internally.

$\overline{TR}$/$\overline{OE}$

Video DRAM Transfer/Output Enable (output, synchronous)

This signal is used with video DRAMs to transfer data to the video shift register. It is also used as an output enable in normal video DRAM read cycles. This signal is supported on the Am29240 and Am29245 microcontrollers only.

$\overline{TRAP}$1–$\overline{TRAP}$0

Trap Requests 1–0 (input, asynchronous, internal pull-ups)

These inputs generate prioritized trap requests. The trap caused by $\overline{TRAP}$0 has the highest priority. These trap requests are disabled by the DA bit of the Current Processor Status Register. These signals have special hardening against metastable states, allowing them to be driven with slow-transition-time signals.

$\overline{TRIST}$

Three-State Control (input, asynchronous, pull-up resistor)

This input is asserted to force all processor outputs into the high-impedance state. This signal is tied High through an internal pull-up resistor.

Note: $\overline{TRIST}$ *does not control the* MEMCLK *pin. To three-state* MEMCLK*, the user must drive* MEMDRV *Low.*

$\overline{TRST}$

Test Reset Input (input, asynchronous, pull-up resistor)

This input asynchronously resets the Test Access Port. If $\overline{TRST}$ is not driven, it appears High internally. $\overline{TRST}$ must be tied to $\overline{RESET}$, even if the Test Access Port is not being used.

TXDA

Transmit Data, Port A (output, asynchronous)

This output is used to transmit serial data from Serial Port A.

TXDB

Transmit Data, Port B (output, asynchronous)

This output is used to transmit data from Serial Port B. This signal is supported on the Am29240 and Am29243 microcontrollers only.

UCLK

UART Clock (input)

This is an oscillator input for generating the UART (Serial Port) clock. To generate the UART clock, the oscillator frequency may be divided by any amount up to 65,536. The UART clock operates at 16 times the Serial Port's baud rate. As an option, UCLK may be driven with MEMCLK or INCLK. It can be driven with TTL levels.

VCLK

Video Clock (input, asynchronous)

This clock is used to synchronize the transfer of video data. As an option, VCLK may be driven with MEMCLK or INCLK. It can be driven with TTL levels. This signal is supported on the Am29240 and Am29245 microcontrollers only.

VDAT

Video Data (input/output, synchronous to VCLK)

This is serial data to or from the video device. This signal is supported on the Am29240 and Am29245 microcontrollers only.

$\overline{WAIT}$

Add Wait States (input, synchronous, internal pull-up)

External accesses are normally timed by the processor. However, the $\overline{WAIT}$ signal may be asserted during a PIA, ROM, or DMA access to extend the access indefinitely.

$\overline{WARN}$

Warn (input, asynchronous, edge-sensitive, internal pull-up)

A High-to-Low transition on this input causes a nonmaskable $\overline{WARN}$ trap to occur. This trap bypasses the normal trap vector fetch sequence, and is useful in situations where the vector fetch may not work (e.g., when data memory is faulty). This signal has special hardening against metastable states, allowing it to be driven with a slow-transition-time signal.

$\overline{WE}$

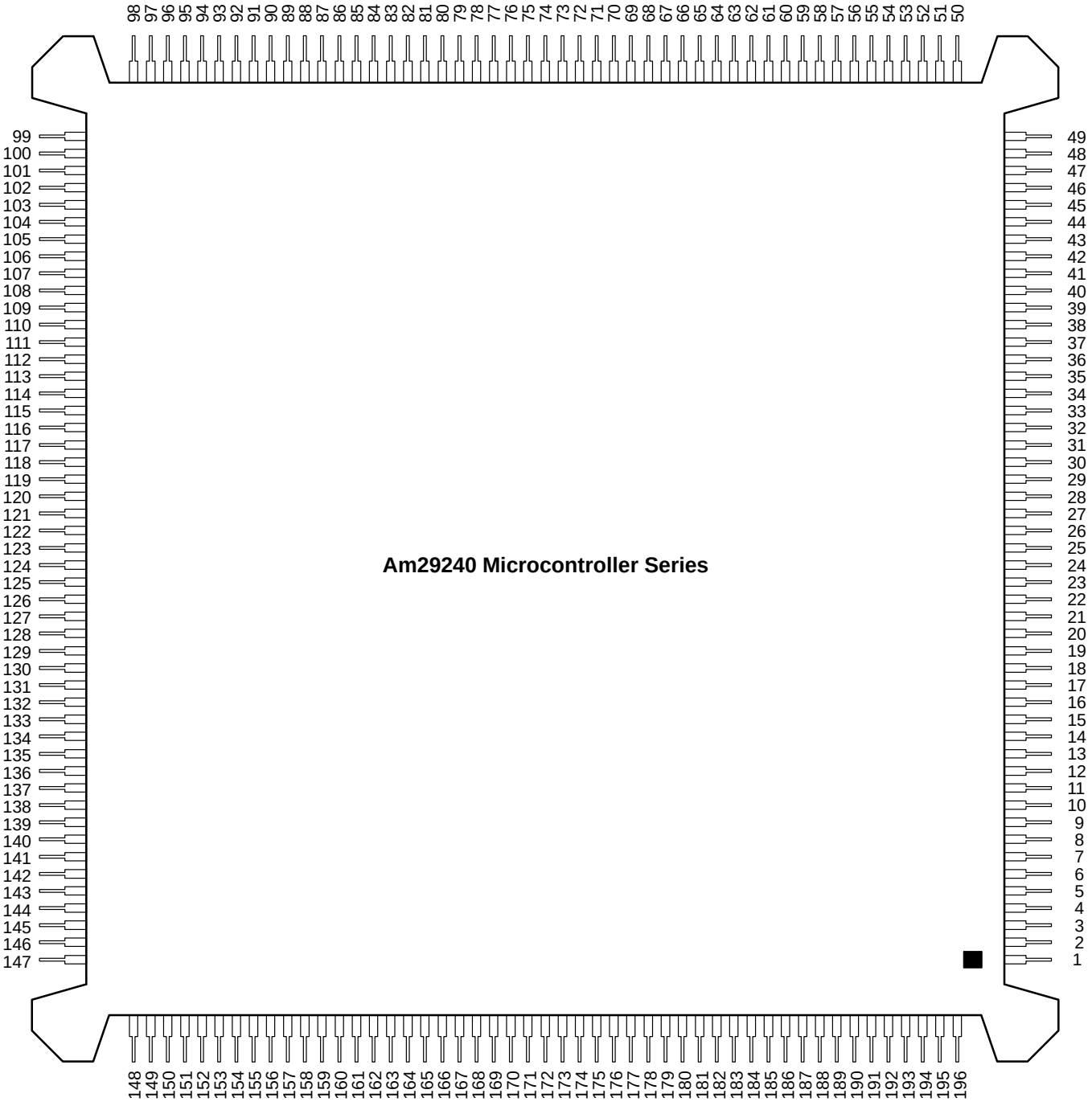
Write Enable (output, synchronous)

This signal is used to write the selected DRAM bank. "Early write" cycles are used so the DRAM data inputs and outputs can be tied to the common ID Bus.

CONNECTION DIAGRAM

196-Pin PQFP

Top Side View



Note:

Pin 1 marked for orientation.

PQFP PIN DESIGNATIONS (Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	**50**	V_{CC}	**99**	V_{CC}	**148**	V_{CC}
2	MEMCLK	**51**	Reserved	**100**	Reserved	**149**	Reserved
3	MEMDRV	**52**	Reserved	**101**	Reserved	**150**	PIO12
4	INCLK	**53**	TXDB [3]	**102**	A23	**151**	PIO11
5	ID31	**54**	RXDB [3]	**103**	A22	**152**	PIO10
6	ID30	**55**	$\overline{\text{DTR}}$A	**104**	A21	**153**	PIO9
7	ID29	**56**	RXDA	**105**	A20	**154**	PIO8
8	ID28	**57**	UCLK	**106**	A19	**155**	PIO7
9	ID27	**58**	$\overline{\text{DSR}}$A	**107**	A18	**156**	PIO6
10	ID26	**59**	TXDA	**108**	A17	**157**	PIO5
11	ID25	**60**	$\overline{\text{ROMCS}}$3	**109**	A16	**158**	PIO4
12	ID24	**61**	$\overline{\text{ROMCS}}$2	**110**	GND	**159**	GND
13	GND	**62**	$\overline{\text{ROMCS}}$1	**111**	V_{CC}	**160**	V_{CC}
14	V_{CC}	**63**	$\overline{\text{ROMCS}}$0	**112**	A15	**161**	PIO3
15	ID23	**64**	V_{CC}	**113**	A14	**162**	PIO2
16	ID22	**65**	GND	**114**	A13	**163**	PIO1
17	ID21	**66**	$\overline{\text{BURST}}$	**115**	A12	**164**	PIO0
18	ID20	**67**	$\overline{\text{RSWE}}$	**116**	A11	**165**	TDO
19	ID19	**68**	$\overline{\text{ROMOE}}$	**117**	A10	**166**	STAT2
20	ID18	**69**	$\overline{\text{RAS}}$3	**118**	A9	**167**	STAT1
21	ID17	**70**	$\overline{\text{RAS}}$2	**119**	A8	**168**	STAT0
22	ID16	**71**	$\overline{\text{RAS}}$1	**120**	GND	**169**	VDAT [2]
23	GND	**72**	$\overline{\text{RAS}}$0	**121**	V_{CC}	**170**	PSYNC [2]
24	V_{CC}	**73**	$\overline{\text{CAS}}$3	**122**	A7	**171**	GND
25	ID15	**74**	$\overline{\text{CAS}}$2	**123**	A6	**172**	V_{CC}
26	ID14	**75**	V_{CC}	**124**	A5	**173**	$\overline{\text{GREQ}}$
27	ID13	**76**	GND	**125**	A4	**174**	DREQB
28	ID12	**77**	$\overline{\text{CAS}}$1	**126**	A3	**175**	DREQA
29	ID11	**78**	$\overline{\text{CAS}}$0	**127**	A2	**176**	TDMA
30	ID10	**79**	$\overline{\text{TR}}$/$\overline{\text{OE}}$	**128**	A1	**177**	$\overline{\text{TRAP}}$0
31	ID9	**80**	$\overline{\text{WE}}$	**129**	A0	**178**	$\overline{\text{TRAP}}$1
32	ID8	**81**	$\overline{\text{GACK}}$	**130**	GND	**179**	$\overline{\text{INTR}}$0
33	GND	**82**	$\overline{\text{PIACS}}$5	**131**	V_{CC}	**180**	$\overline{\text{INTR}}$1
34	V_{CC}	**83**	$\overline{\text{PIACS}}$4	**132**	BOOTW	**181**	$\overline{\text{INTR}}$2
35	ID7	**84**	$\overline{\text{PIACS}}$3	**133**	$\overline{\text{WAIT}}$	**182**	$\overline{\text{INTR}}$3
36	ID6	**85**	$\overline{\text{PIACS}}$2	**134**	PAUTOFD	**183**	GND
37	ID5	**86**	V_{CC}	**135**	PSTROBE	**184**	V_{CC}
38	ID4	**87**	GND	**136**	$\overline{\text{PWE}}$	**185**	$\overline{\text{WARN}}$
39	ID3	**88**	$\overline{\text{PIACS}}$1	**137**	$\overline{\text{POE}}$	**186**	VCLK [2]
40	ID2	**89**	$\overline{\text{PIACS}}$0	**138**	PACK	**187**	LSYNC [2]
41	ID1	**90**	$\overline{\text{PIAWE}}$	**139**	$\overline{\text{PBUSY}}$	**188**	TMS
42	ID0	**91**	$\overline{\text{PIAOE}}$	**140**	GND	**189**	$\overline{\text{TRST}}$
43	GND	**92**	R/$\overline{\text{W}}$	**141**	V_{CC}	**190**	TCK
44	V_{CC}	**93**	$\overline{\text{DACK}}$B	**142**	PIO15	**191**	TDI
45	IDP3 [1, 3]	**94**	$\overline{\text{DACK}}$A	**143**	PIO14	**192**	$\overline{\text{RESET}}$
46	IDP2 [1, 3]	**95**	$\overline{\text{DACK}}$D [3]	**144**	PIO13	**193**	CNTL1
47	IDP1 [1, 3]	**96**	$\overline{\text{DACK}}$C [3]	**145**	DREQD [3]	**194**	CNTL0
48	IDP0 [1, 3]	**97**	Reserved	**146**	DREQC [3]	**195**	$\overline{\text{TRIST}}$
49	GND	**98**	GND	**147**	GND	**196**	GND

Notes: *All values are typical and preliminary.*

1. *Defined as a no-connect on the Am29240 microcontroller.*
2. *Defined as a no-connect on the Am29243 microcontroller.*
3. *Defined as a no-connect on the Am29245 microcontroller.*

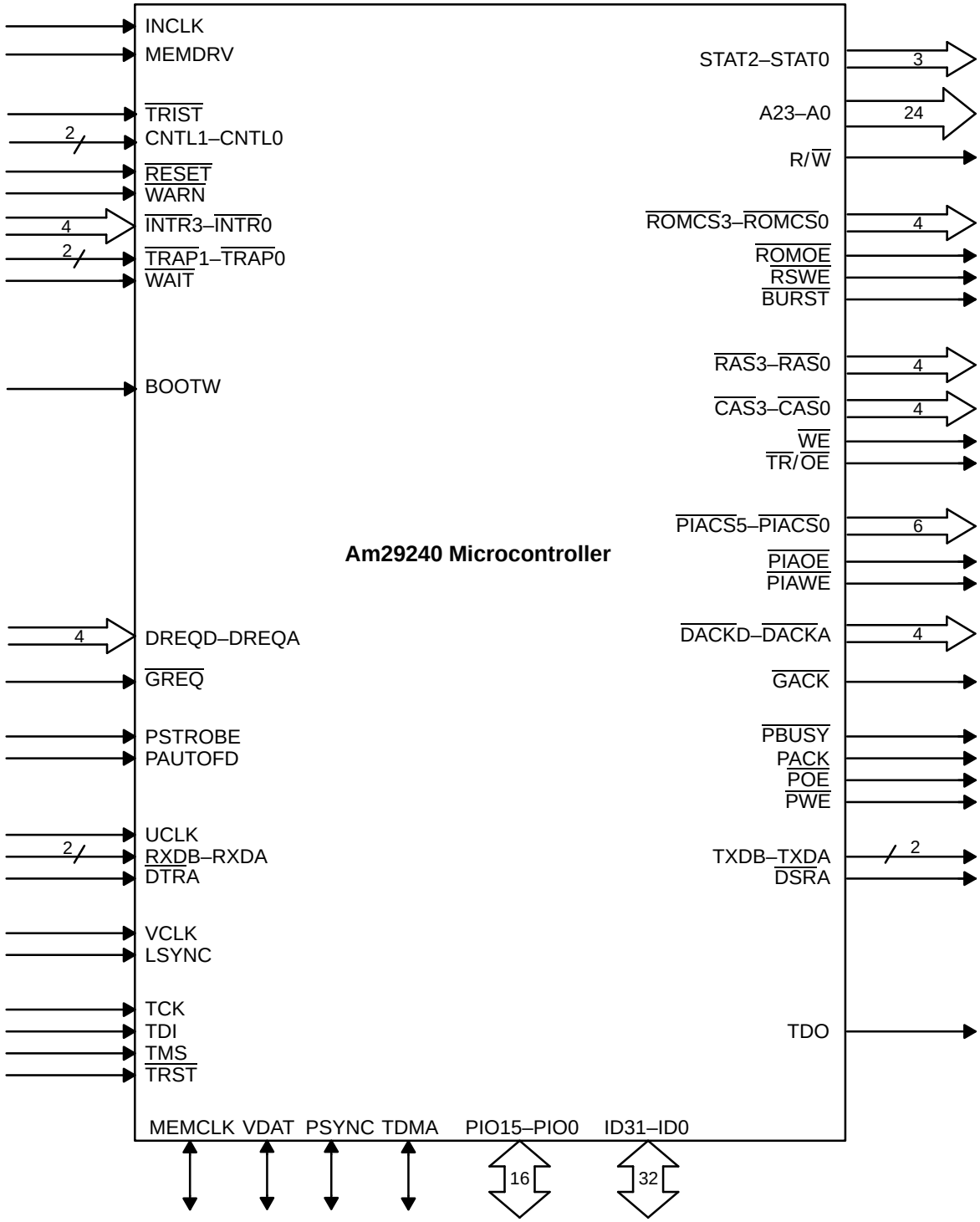
PQFP PIN DESIGNATIONS (Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	129	**GND**	76	**INCLK**	4	**Reserved**	149
A1	128	**GND**	87	**$\overline{\text{INTR}}$0**	179	**$\overline{\text{RESET}}$**	192
A2	127	**GND**	98	**$\overline{\text{INTR}}$1**	180	**$\overline{\text{ROMCS}}$0**	63
A3	126	**GND**	110	**$\overline{\text{INTR}}$2**	181	**$\overline{\text{ROMCS}}$1**	62
A4	125	**GND**	120	**$\overline{\text{INTR}}$3**	182	**$\overline{\text{ROMCS}}$2**	61
A5	124	**GND**	130	**LSYNC** [2]	187	**$\overline{\text{ROMCS}}$3**	60
A6	123	**GND**	140	**MEMCLK**	2	**$\overline{\text{ROMOE}}$**	68
A7	122	**GND**	147	**MEMDRV**	3	**$\overline{\text{RSWE}}$**	67
A8	119	**GND**	159	**PACK**	138	**RXDA**	56
A9	118	**GND**	171	**PAUTOFD**	134	**RXDB** [3]	54
A10	117	**GND**	183	**$\overline{\text{PBUSY}}$**	139	**STAT0**	168
A11	116	**GND**	196	**$\overline{\text{PIACS}}$0**	89	**STAT1**	167
A12	115	**$\overline{\text{GREQ}}$**	173	**$\overline{\text{PIACS}}$1**	88	**STAT2**	166
A13	114	**ID0**	42	**$\overline{\text{PIACS}}$2**	85	**TCK**	190
A14	113	**ID1**	41	**$\overline{\text{PIACS}}$3**	84	**TDI**	191
A15	112	**ID2**	40	**$\overline{\text{PIACS}}$4**	83	**TDMA**	176
A16	109	**ID3**	39	**$\overline{\text{PIACS}}$5**	82	**TDO**	165
A17	108	**ID4**	38	**$\overline{\text{PIAOE}}$**	91	**TMS**	188
A18	107	**ID5**	37	**$\overline{\text{PIAWE}}$**	90	**$\overline{\text{TR}}$/$\overline{\text{OE}}$**	79
A19	106	**ID6**	36	**PIO0**	164	**$\overline{\text{TRAP}}$0**	177
A20	105	**ID7**	35	**PIO1**	163	**$\overline{\text{TRAP}}$1**	178
A21	104	**ID8**	32	**PIO2**	162	**$\overline{\text{TRIST}}$**	195
A22	103	**ID9**	31	**PIO3**	161	**$\overline{\text{TRST}}$**	189
A23	102	**ID10**	30	**PIO4**	158	**TXDA**	59
BOOTW	132	**ID11**	29	**PIO5**	157	**TXDB** [3]	53
$\overline{\text{BURST}}$	66	**ID12**	28	**PIO6**	156	**UCLK**	57
$\overline{\text{CAS}}$0	78	**ID13**	27	**PIO7**	155	**V_{CC}**	1
$\overline{\text{CAS}}$1	77	**ID14**	26	**PIO8**	154	**V_{CC}**	14
$\overline{\text{CAS}}$2	74	**ID15**	25	**PIO9**	153	**V_{CC}**	24
$\overline{\text{CAS}}$3	73	**ID16**	22	**PIO10**	152	**V_{CC}**	34
CNTL0	194	**ID17**	21	**PIO11**	151	**V_{CC}**	44
CNTL1	193	**ID18**	20	**PIO12**	150	**V_{CC}**	50
$\overline{\text{DACK}}$A	94	**ID19**	19	**PIO13**	144	**V_{CC}**	64
$\overline{\text{DACK}}$B	93	**ID20**	18	**PIO14**	143	**V_{CC}**	75
$\overline{\text{DACK}}$C [3]	96	**ID21**	17	**PIO15**	142	**V_{CC}**	86
$\overline{\text{DACK}}$D [3]	95	**ID22**	16	**$\overline{\text{POE}}$**	137	**V_{CC}**	99
DREQA	175	**ID23**	15	**PSTROBE**	135	**V_{CC}**	111
DREQB	174	**ID24**	12	**PSYNC** [2]	170	**V_{CC}**	121
DREQC [3]	146	**ID25**	11	**$\overline{\text{PWE}}$**	136	**V_{CC}**	131
DREQD [3]	145	**ID26**	10	**R/$\overline{\text{W}}$**	92	**V_{CC}**	141
$\overline{\text{DSR}}$A	58	**ID27**	9	**$\overline{\text{RAS}}$0**	72	**V_{CC}**	148
$\overline{\text{DTR}}$A	55	**ID28**	8	**$\overline{\text{RAS}}$1**	71	**V_{CC}**	160
$\overline{\text{GACK}}$	81	**ID29**	7	**$\overline{\text{RAS}}$2**	70	**V_{CC}**	172
GND	13	**ID30**	6	**$\overline{\text{RAS}}$3**	69	**V_{CC}**	184
GND	23	**ID31**	5	**Reserved**	51	**VCLK** [2]	186
GND	33	**IDP0** [1, 3]	48	**Reserved**	52	**VDAT** [2]	169
GND	43	**IDP1** [1, 3]	47	**Reserved**	97	**$\overline{\text{WAIT}}$**	133
GND	49	**IDP2** [1, 3]	46	**Reserved**	100	**$\overline{\text{WARN}}$**	185
GND	65	**IDP3** [1, 3]	45	**Reserved**	101	**$\overline{\text{WE}}$**	80

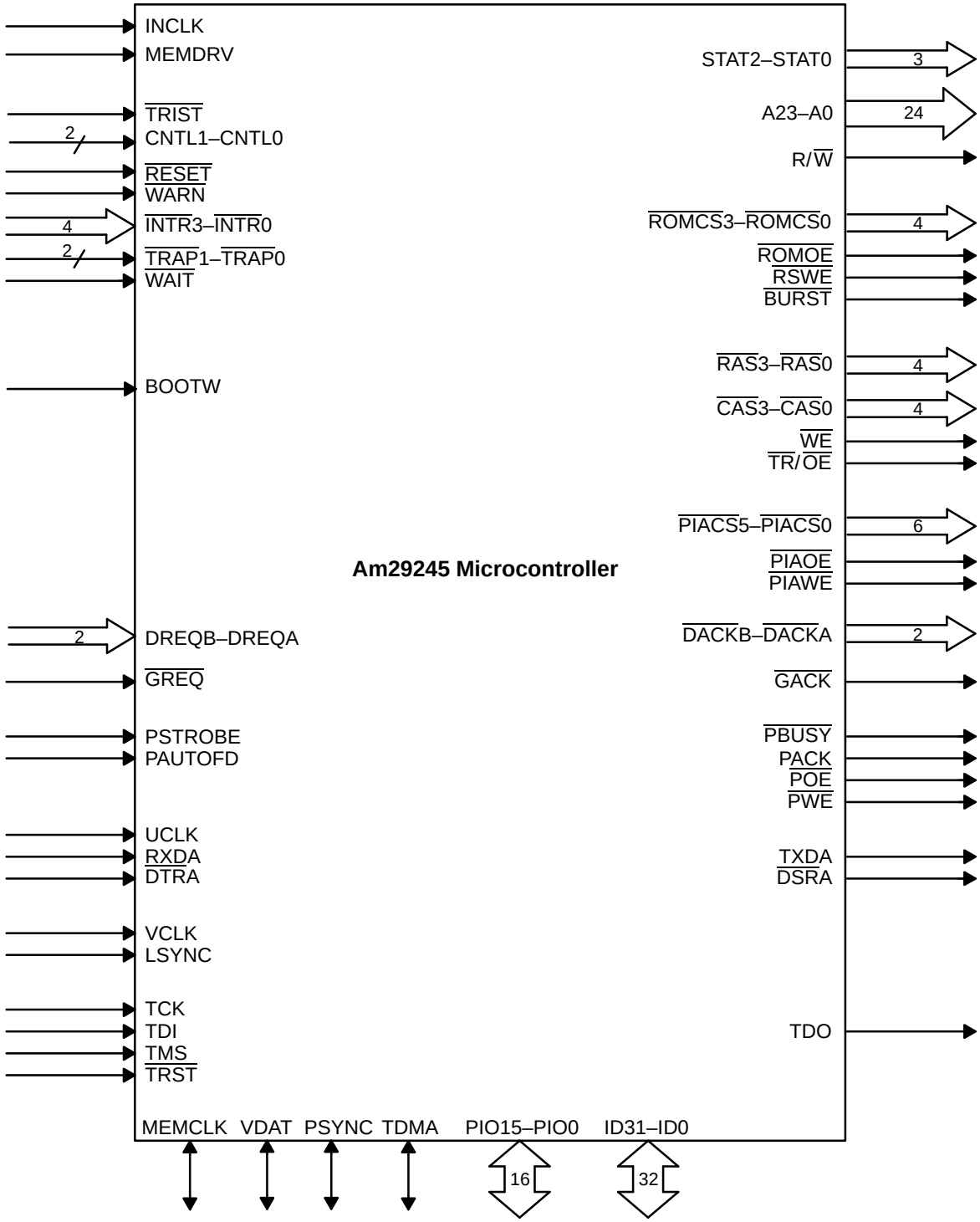
Notes: *All values are typical and preliminary.*

1. *Defined as a no-connect on the Am29240 microcontroller.*
2. *Defined as a no-connect on the Am29243 microcontroller.*
3. *Defined as a no-connect on the Am29245 microcontroller.*

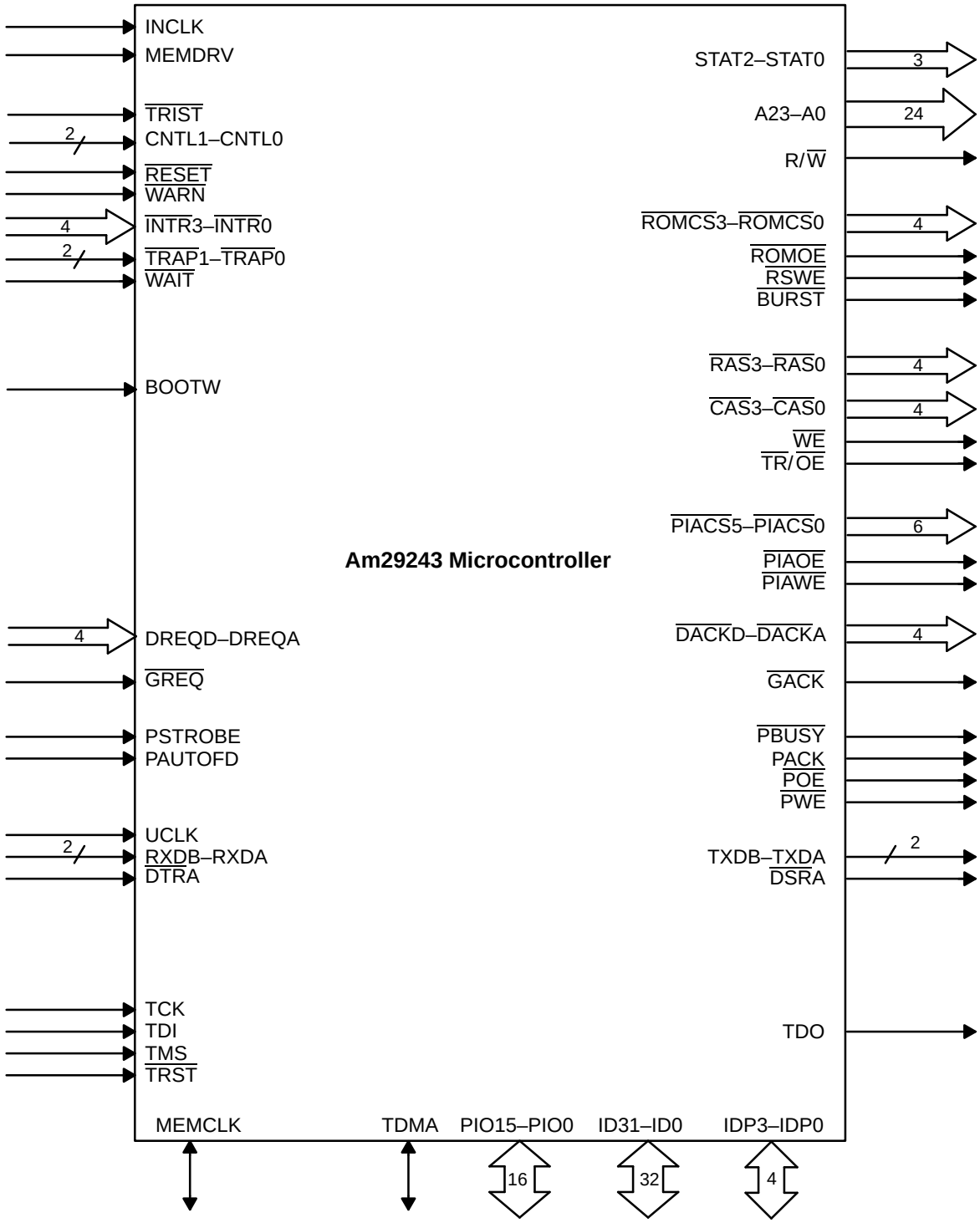
Am29240 MICROCONTROLLER LOGIC SYMBOL



Am29245 MICROCONTROLLER LOGIC SYMBOL



Am29243 MICROCONTROLLER LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +125°C
Voltage on any Pin
with Respect to GND . . . . . –0.5 V to V_{CC} +0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) . . . . . 0°C to +85°C
Supply Voltage (V_{CC}) . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL Operating Ranges

Symbol	Parameter Description	Test Conditions	Advance Information		Unit
			Min	Max	
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage	Note 1	–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage	Note 1	V_{CC} –0.8	V_{CC} +0.5	V
V_{OL}	Output Low Voltage for All Outputs except MEMCLK	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage for All Outputs except MEMCLK	I_{OH} = –400 µA	2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V Note 2		±10 or +10/–200	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.45 V		±10	µA
I_{CCOP}	Operating Power-Supply Current with respect to MEMCLK	V_{CC} = 5.25 V, Outputs Floating; Holding $\overline{RESET}$ active at 25 MHz		14	mA/MHz
V_{OLC}	MEMCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	MEMCLK Output High Voltage	I_{OHC} = –20 mA	V_{CC} –0.6		V
I_{OSGND}	MEMCLK GND Short Circuit Current	V_{CC} = 5.0 V	100		mA
I_{OSVCC}	MEMCLK V_{CC} Short Circuit Current	V_{CC} = 5.0 V	100		mA

Notes:
1. *INCLK is driven with CMOS input levels.*
2. *The Low input leakage current for the inputs* CNTL1–CNTL0, $\overline{INTR}$3–$\overline{INTR}$0, $\overline{TRAP}$1–$\overline{TRAP}$0, DREQD–DREQA, TCK, TDI, $\overline{TRST}$, TMS, $\overline{GREQ}$, $\overline{WARN}$, MEMDRV, $\overline{WAIT}$, *and* $\overline{TRIST}$ *is –200* µA. *These pins have internal pull-up resistors.*

CAPACITANCE

Symbol	Parameter Description	Test Conditions	Advance Information		Unit
			Min	Max	
C_{IN}	Input Capacitance	fC = 10 MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			15	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note: *Limits guaranteed by characterization.*

SWITCHING CHARACTERISTICS over COMMERCIAL Operating Ranges

No.	Parameter Description	Test Conditions [1, 8]	Advance Information						Unit
			16 MHz		20 MHz		25 MHz		
			Min	Max	Min	Max	Min	Max	
1	INCLK Period (=0.5T)	Notes 9, 10, 11	30	∞	25	∞	20	∞	ns
2	INCLK High Time	Note 9	12	∞	10	∞	8	∞	ns
3	INCLK Low Time	Note 9	12	∞	10	∞	8	∞	ns
4	INCLK Rise Time	Note 9	1	7	1	7	1	7	ns
5	INCLK Fall Time	Note 9	1	7	1	7	1	7	ns
6	MEMCLK Delay from INCLK	MEMCLK Output Notes 3, 8	1	7	1	7	1	7	ns
8	MEMCLK High Time	MEMCLK Output Notes 3, 8	0.5T–3	∞	0.5T–3	∞	0.5T–3	∞	ns
9	MEMCLK Low Time	MEMCLK Output Notes 3, 8	0.5T–3	∞	0.5T–3	∞	0.5T–3	∞	ns
10	MEMCLK Rise Time	Notes 3, 8	1	4	1	4	1	4	ns
11	MEMCLK Fall Time	Notes 3, 8	1	4	1	4	1	4	ns
12a	Synchronous Output Valid Delay from MEMCLK Rising Edge								
	PIO15–PIO0, STAT2–STAT0, and $\overline{\text{PIACS}}$5–$\overline{\text{PIACS}}$0	MEMCLK Output Note 1A	1	13	1	12	1	11	ns
	$\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0 Rising Edge/ $\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0 Falling Edge	MEMCLK Output Notes 1B, 4B	1	17/11	1	15/9	1	13/7	ns
	All others	MEMCLK Output Note 1B	1	12	1	11	1	10	ns
12b	Synchronous Output Valid from MEMCLK Falling Edge								
	PIO15–PIO0, STAT2–STAT0, and $\overline{\text{PIACS}}$5–$\overline{\text{PIACS}}$0	MEMCLK Output Note 1A	1	12	1	11	1	10	ns
	$\overline{\text{CAS}}$3–$\overline{\text{CAS}}$0 Falling Edge	MEMCLK Output Notes 1B, 4B	1	11	1	9	1	7	ns
	All others	MEMCLK Output Note 1B	1	11	1	10	1	9	ns
13	Synchronous Output Disable Delay from MEMCLK Rising Edge	MEMCLK Output	1	12	1	11	1	10	ns
14	Synchronous Input Setup Time to MEMCLK Rising Edge								
	ID31–ID0 and IDP3–IDP0 for DRAM access	Parity Enabled Note 4A	18		16		15		ns
	ID31–ID0 for DRAM access	Parity Disabled Note 4A	10		8		7		ns
	All others		10		8		7		ns
15	Available CAS Access Time ($T\overline{\text{CAS}}$–T_{Setup})	Notes 4A, 4B		24		23		18	ns
16a	Synchronous Input Hold Time to MEMCLK Rising Edge	Note 4A	0		0		0		ns
16b	Synchronous Input Hold Time to $\overline{\text{CAS}}$ Rising Edge	Note 4B	3		3		3		ns

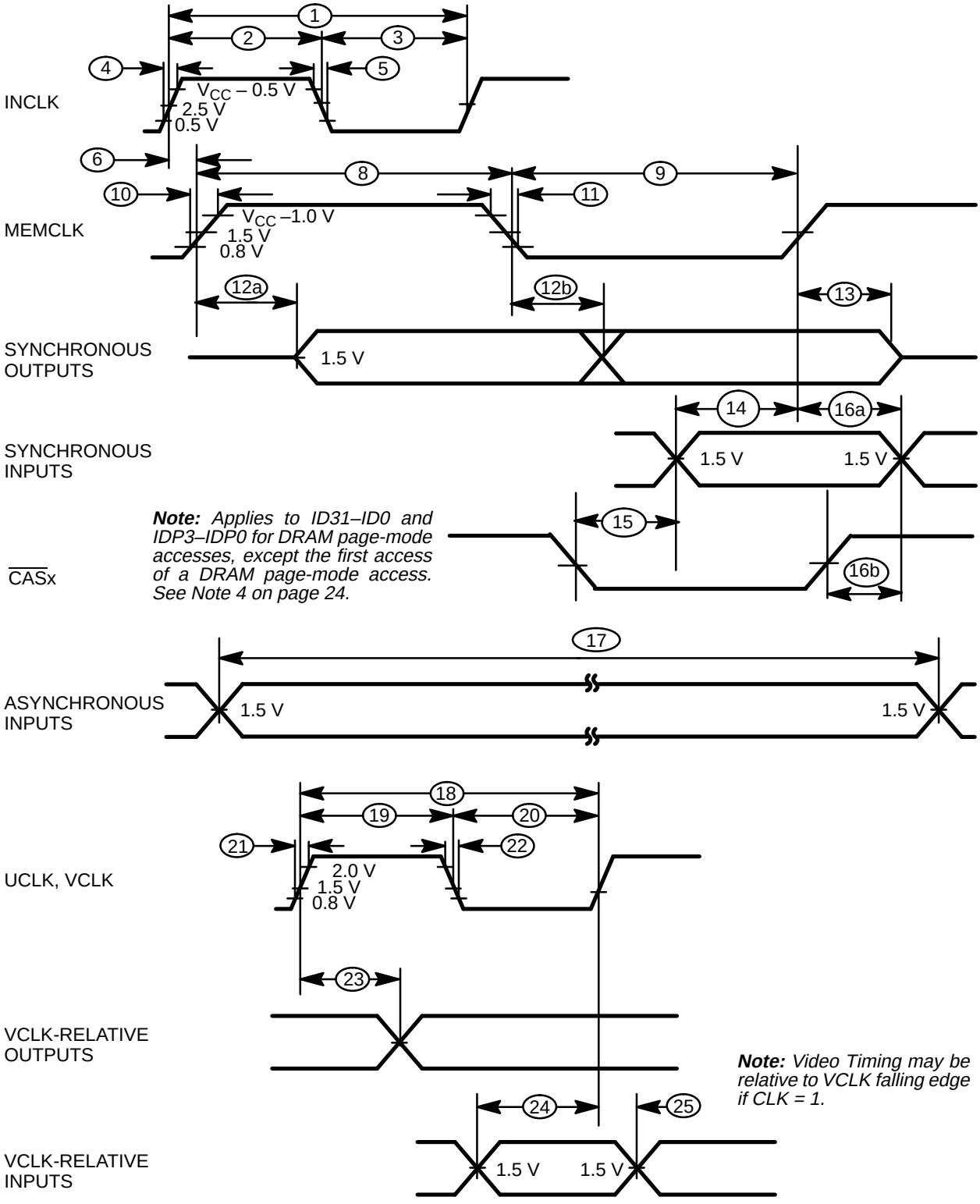
SWITCHING CHARACTERISTICS over COMMERCIAL Operating Ranges (continued)

No.	Parameter Description	Test Conditions [1, 8]	Advance Information						Unit
			16 MHz		20 MHz		25 MHz		
			Min	Max	Min	Max	Min	Max	
17	Asynchronous Input Pulse Width								
	LSYNC and PSYNC		Note 5		Note 5		Note 5		
	All others		4T		4T		4T		ns
18	UCLK Period	Note 2	30		25		20		ns
	VCLK Period	Note 2	25		20		15		ns
19	UCLK High Time	Note 2	10		8		6		ns
	VCLK High Time	Note 2	8		6		4		ns
20	UCLK Low Time	Note 2	10		8		6		ns
	VCLK Low Time	Note 2	8		6		4		ns
21	UCLK Rise time	Note 2	0	3	0	3	0	3	ns
	VCLK Rise time	Note 2	0	3	0	3	0	3	ns
22	UCLK Fall Time	Note 2	0	3	0	3	0	3	ns
	VCLK Fall Time	Note 2	0	3	0	3	0	3	ns
23	Synchronous Output Valid Delay from VCLK Rise and Fall	Note 6	1	16	1	14	1	14	ns
24	Input Setup Time to VCLK Rise and Fall	Notes 6, 7	10		9		9		ns
25	Input Hold Time to VCLK Rise and Fall	Notes 6, 7	0		0		0		ns

Notes:

1. *All outputs driving 80 pF, measured at V_{OL} = 1.5 V and V_{OH} = 1.5 V. For higher capacitance:*
   A. *Add 1-ns output delay per 15 pF loading up to 150-pF total. The minimum delay from $\overline{\text{PIAOE}}$ to $\overline{\text{PIACS}}x$ is 0 ns if the capacitance loading on $\overline{\text{PIACS}}x$ is equal to or higher than the capacitance loading on $\overline{\text{PIAOE}}$.*
   B. *Add 1-ns output delay per 25 pF loading up to 300-pF total.*
2. *VCLK and UCLK can be driven with TTL inputs. UCLK must be tied High if it is unused.*
3. *MEMCLK can drive an external load of 100 pF.*
4. *ID31–ID0 and IDP3–IDP0 are sampled on the rising edge of MEMCLK for all non-DRAM accesses, simple DRAM accesses, and the first access of a DRAM page-mode access. ID31–ID0 and IDP3–IDP0 are sampled on the rising edge of $\overline{\text{CAS}}x$ for all DRAM page-mode accesses, except the first access of a DRAM page-mode access. (See Figures 1–4 on pages 26–27.)*
   A. *Applies to ID31–ID0 and IDP3–IDP0 for simple DRAM accesses and the first access of a DRAM page-mode access.*
   B. *Applies to ID31–ID0 and IDP3–IDP0 for DRAM page-mode accesses, except the first access of a DRAM page-mode access. When ID31–ID0 and IDP3–IDP0 are sampled on $\overline{\text{CAS}}x$, there is no additional setup time required for ID31–ID0 and IDP3–IDP0 when the parity is enabled.*
5. *LSYNC and PSYNC minimum width is two bit-times. A bit-time is one period of the internal video clock, which is determined by the CLKDIV field in the Video Control Register and VCLK.*
6. *Active VCLK edge depends on the CLKI bit in the Video Control Register.*
7. *LSYNC and PSYNC can be treated as synchronous signals by meeting the setup and hold times, though the synchronization delay still applies.*
8. *The MEMCLK as an input option (i.e., MEMDRV pin is connected to GND) is not supported.*
9. *INCLK is driven with CMOS input levels.*
10. *When the user sets the TBO bit, the INCLK period must not be greater than the operating frequency of the part.*
11. *For the 25 MHz part, INCLK = 20 ns minimum (50 MHz maximum) when turbo mode is disabled. When turbo mode is enabled, INCLK = 30 ns minimum (33 MHz maximum).*

SWITCHING WAVEFORMS



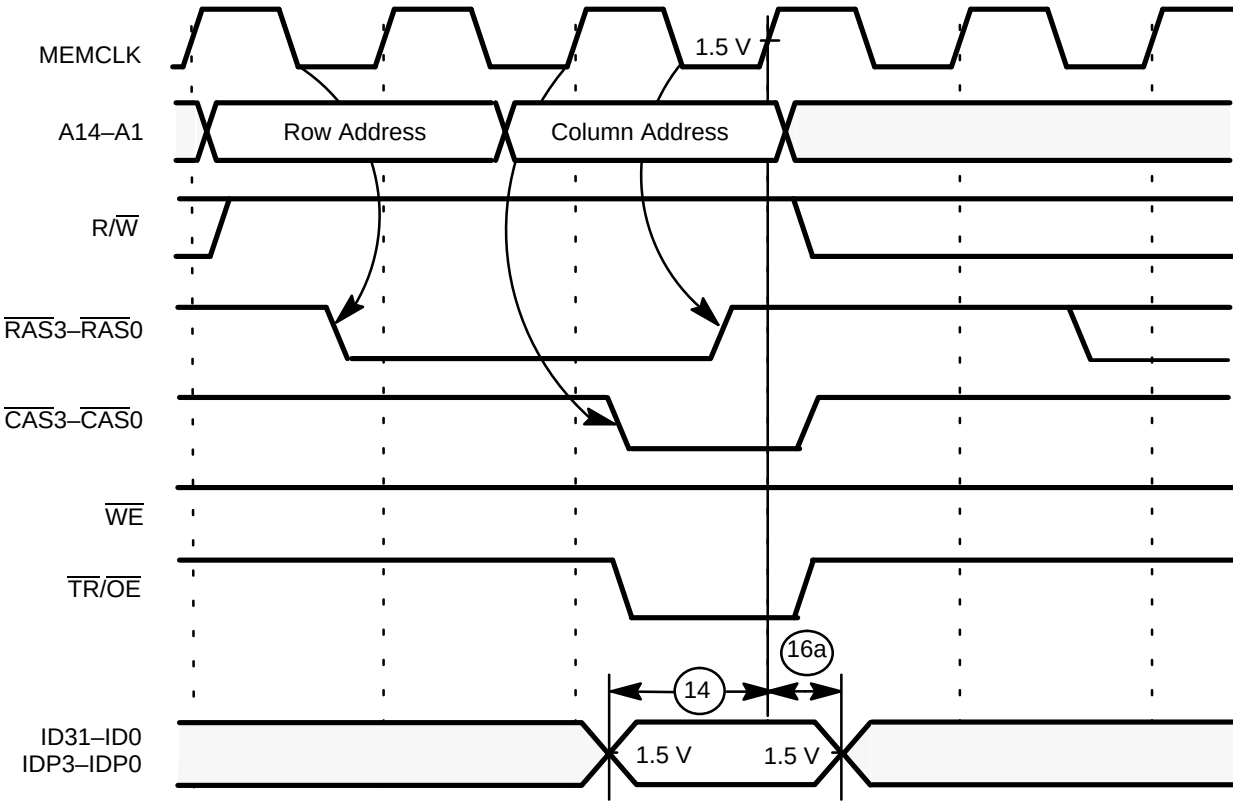
Note: *Applies to ID31–ID0 and IDP3–IDP0 for DRAM page-mode accesses, except the first access of a DRAM page-mode access. See Note 4 on page 24.*

Note: *Video Timing may be relative to VCLK falling edge if CLK = 1.*

Note:

During AC testing, all inputs are driven at V_{IL} = 0.4 V, V_{IH} = 2.4 V.

SWITCHING WAVEFORMS (continued)



Note: The RAS3–RAS0 *signals are asserted and deasserted on the falling edge of* MEMCLK.

Figure 1. Simple 3/1 DRAM Read Cycle, Am29240 Microcontroller Series

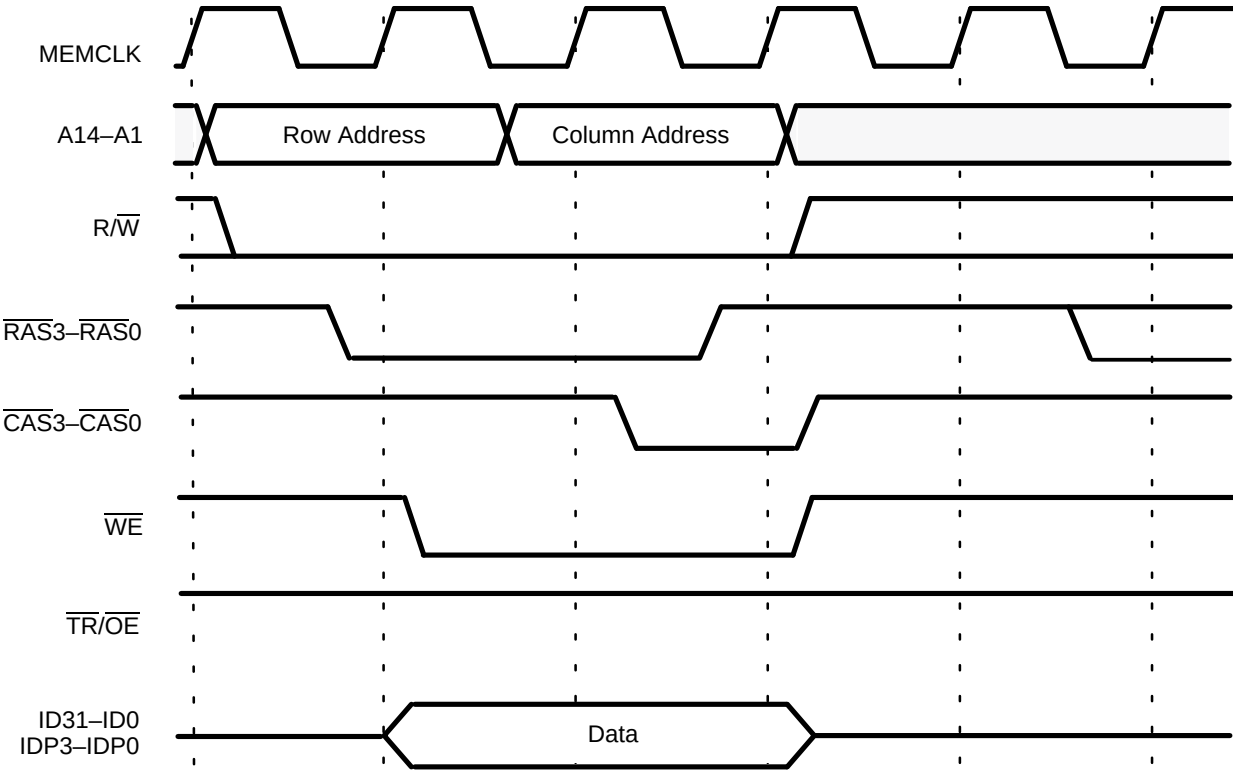
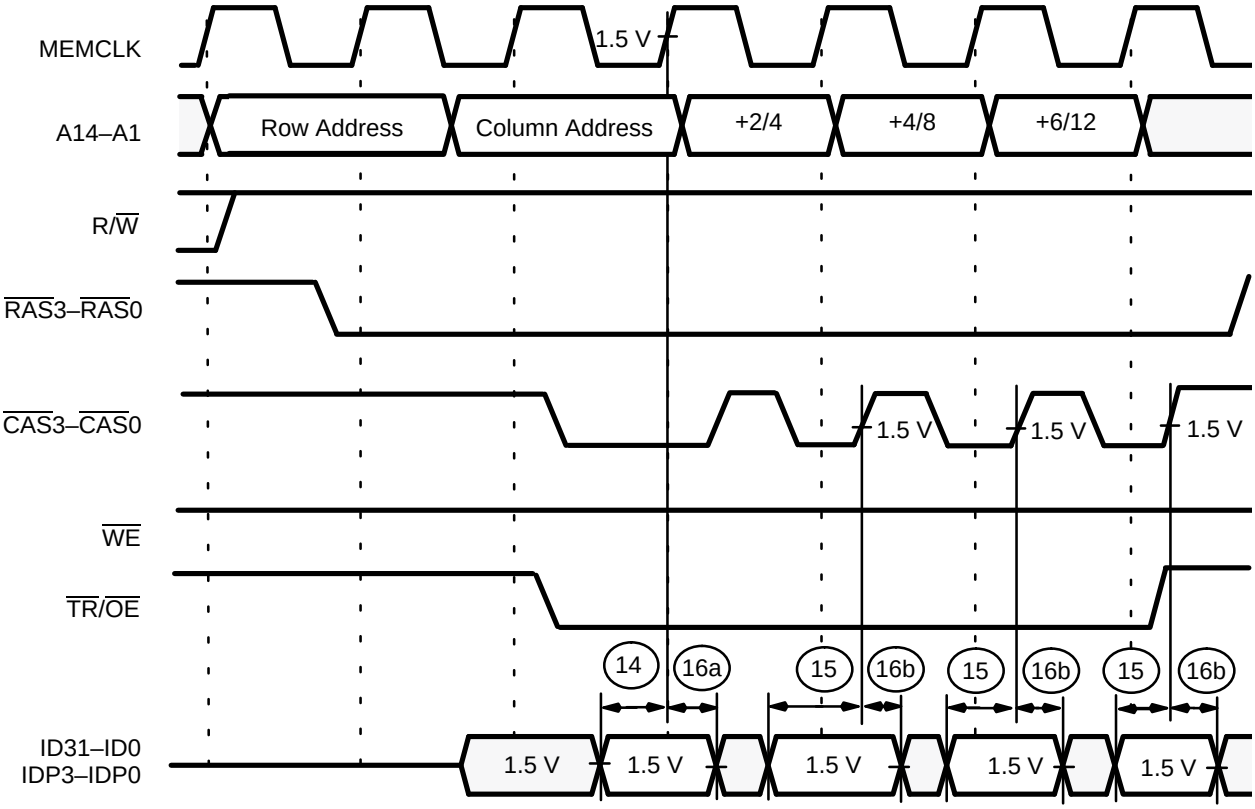


Figure 2. Simple 3/1 DRAM Write Cycle, Am29240 Microcontroller Series

SWITCHING WAVEFORMS (continued)



Note: The RAS3–RAS0 signals are *asserted and deasserted on the falling edge of* MEMCLK.

Figure 3. 3/1 DRAM Page-Mode Read, Am29240 Microcontroller Series

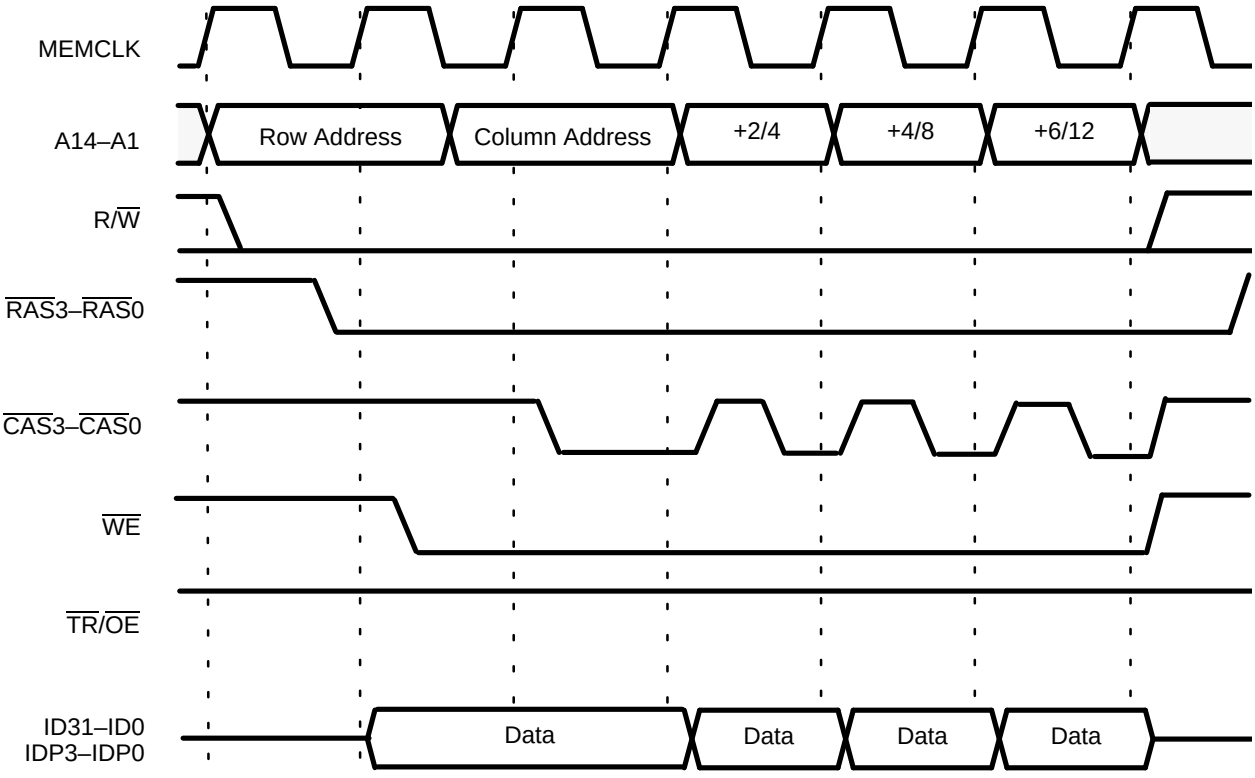
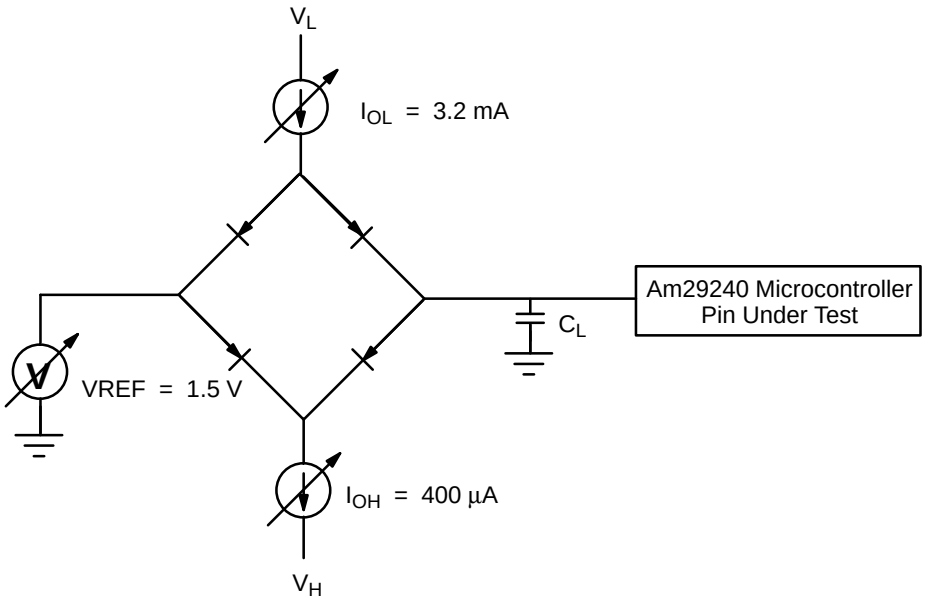


Figure 4. 3/1 DRAM Page-Mode Write, Am29240 Microcontroller Series

SWITCHING TEST CIRCUIT



THERMAL CHARACTERISTICS

The Am29240 microcontroller series is specified for operation with case temperature ranges for a commercial temperature device. Case temperature is measured at the top center of the PQFP package as shown in Figure 5.

The various temperatures and thermal resistances can be determined using the equations shown in Figure 6 along with information given in Table 2. (The variable *P* is power in watts.)

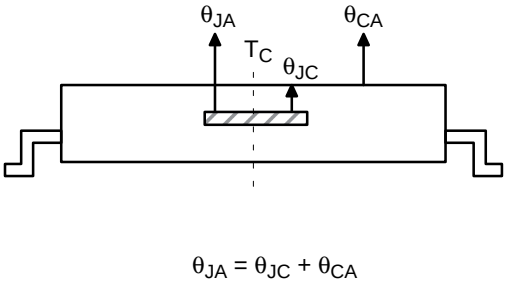


Figure 5. Thermal Resistance — °C/Watt

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

$P = I_{CCOP} \cdot freq \cdot V_{CC}$

$T_J = T_C + P \cdot \theta_{JC}$

$T_J = T_A + P \cdot \theta_{JA}$

$T_C = T_J - P \cdot \theta_{JC}$

$T_C = T_A + P \cdot \theta_{CA}$

$T_A = T_J - P \cdot \theta_{JA}$

$T_A = T_C - P \cdot \theta_{CA}$

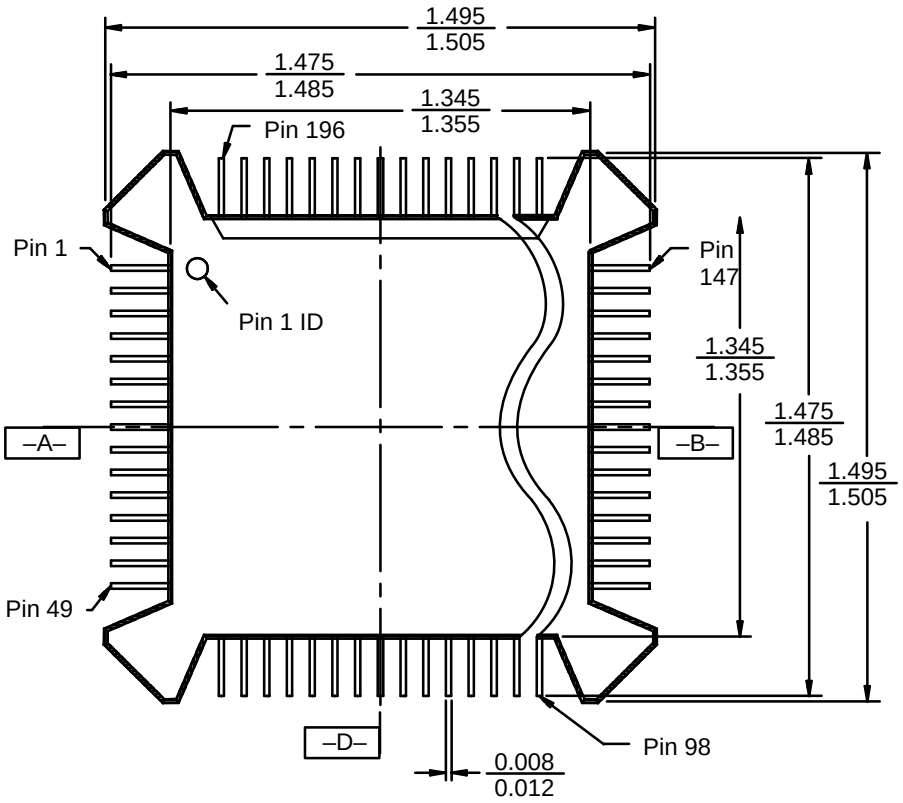
Figure 6. Thermal Characteristics Equations

Table 2. Thermal Characteristics (°C/Watt) Surface Mounted

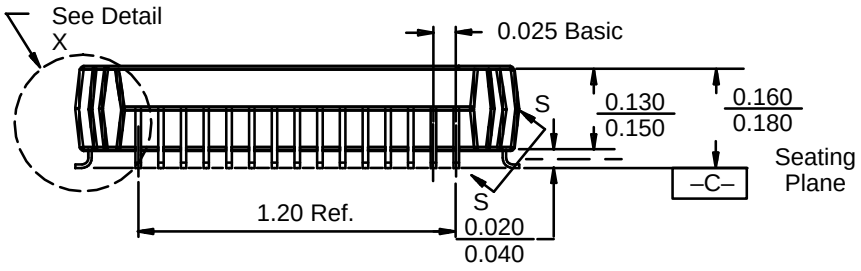
Parameter		°C/Watt
θ_{JA}	Junction-to-Ambient	38
θ_{JC}	Junction-to-Case	8
θ_{CA}	Case-to-Ambient	30

PHYSICAL DIMENSIONS

PQB 196, Trimmed and Formed
Plastic Quad Flat Pack (measured in inches)



Top View

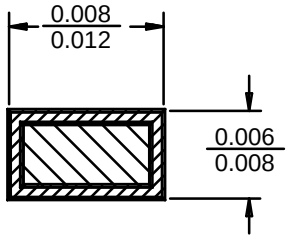


Side View

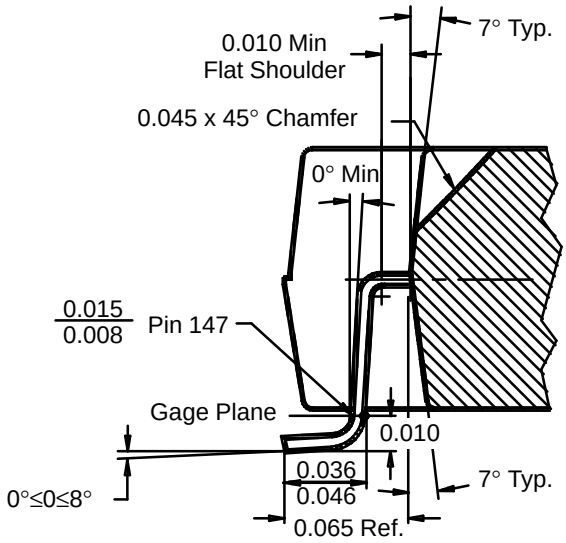
Note:
Not to scale. For reference only.

PHYSICAL DIMENSIONS (continued)

PQB 196, Trimmed and Formed
Plastic Quad Flat Pack (measured in inches)



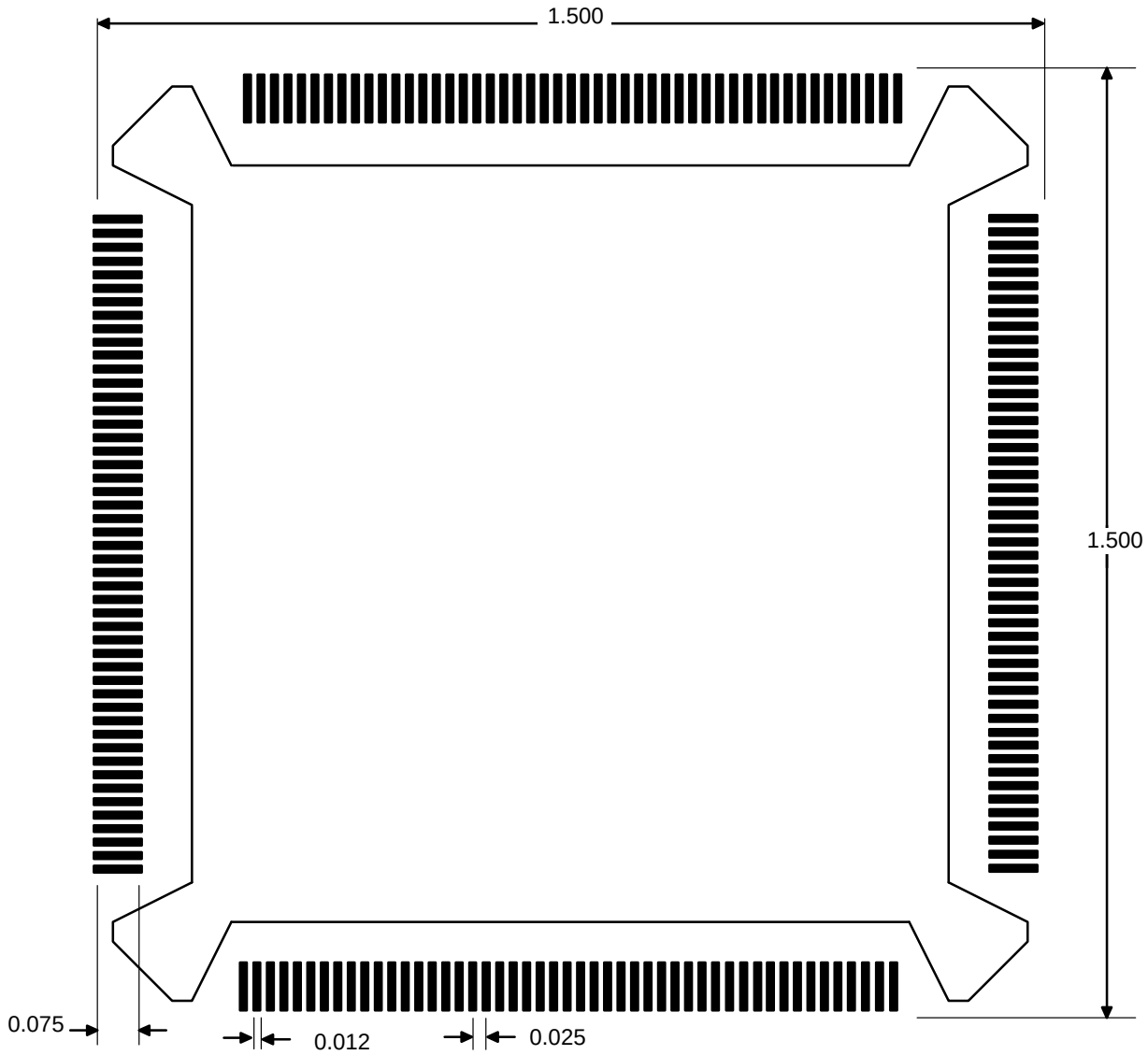
Section S–S



Detail X

Note:
Not to scale. For reference only.

PHYSICAL DIMENSIONS (continued)
Solder Land Recommendations—196-Lead PQFP



Note:
Not to scale. For reference only.