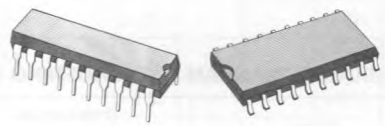
SGS-THOMSON MICROELECTRONICS

AM6012
AM6012A

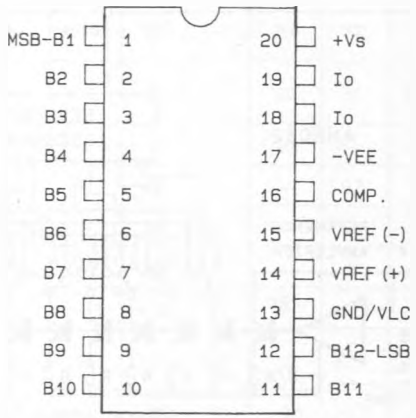
12-BIT HIGH SPEED D/A CONVERTERS

- ALL GRADES 12-BIT MONOTONIC OVER TEMPERATURE
- DIFFERENTAL NONLINEARITY TO ±0.012% (13 BITS) MAX OVER TEMPERATURE (A GRADES)
- 250ns TYPICAL SETTLING TIME
- FULL SCALE CURRENT 4mA
- HIGH SPEED MULTIPLYING CAPABILITY
- TTL/CMOS/ECL/HTL COMPATIBLE
- HIGH OUTPUT COMPLIANCE: −5V TO +10V
- COMPLEMENTARY CURRENT OUTPUTS
- LOW POWER CONSUMPTION: 230mW



DIP-20 Plastic SO-20L

PIN CONNECTIONS



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DESCRIPTION

The AM6012 is an industry standard monolithic 12-bit digital-to analog converter. Complementary current output and high speed multiplying capability make the AM6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures. The AM6012 is packaged in a 20-pin plastic DIP and is SO-20L for surface mounting. Although tested and specified at ±15V, the AM6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts. The AM6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as high as 0.012% (13 bits) for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range.

Guaranteed monotonicity and low cost make the AM6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

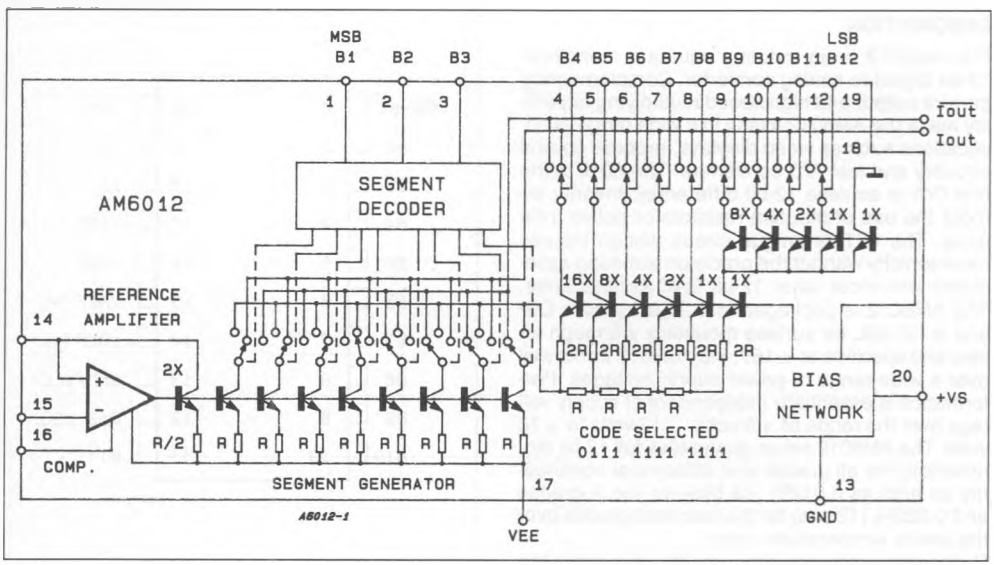
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to 70	°C
Storage Temperature	−65 to + 125	°C
Power Supply Voltage	±18	V
Logic Inputs	−5 to +18	V
Voltage at Current Outputs Pins	−8 to +12	V
Reference Inputs	$+V_S$ to $-V_{EE}$ ±18V max Differential	V
Reference Input Current	1.25	mA

CONNECTION DIAGRAM AND ORDERING INFORMATION

Type	Differential linearity (%)	Temperature Range (°C)	Package
AM6012PC	0.025	0 to 70	DIP.20
AM6012APC	0.012		
AM6012 D	0.025	0 to 70	SO.20L
AM6012 AD	0.012		

BLOCK DIAGRAM



THERMAL DATA

$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = +15V$, $V_{EE} = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	—	—	±.012	—	—	±.025	%FS
			13	—	—	12	—	—	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	—	—	±.05	—	—	±0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Temp.Co.		—	±5	±20	—	±10	±40	ppm°C
			—	±.0005	±.002		±.001	±.004	%FS°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohme typ.	−5	—	+10	−5	—	+10	V
I_{FSS}	Full Scale Symmetry	I_{FS}-I_{FS}	—	±0.2	±1.0	—	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		—	—	0.10	—	—	0.10	μA
t_S	Setting Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	—	250	500	—	250	500	nSec
t_{PLH} t_{PHL}	Propagation Delay - all bits	50% to 50%	—	25	50	—	25	50	nSec
C_{OUT}	Output Capacitance		—	20	—	—	20	—	pF
V_{IL}	Logic Input Levels — Logic "0"		—	—	0.8	—	—	0.8	V
V_{IH}	Logic Input Levels — Logic "1"		2.0	—	—	2.0	—	—	V
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	—	—	40	—	—	40	μA
V_{IS}	Logic Input Swing	$V_{EE} = -15V$	−5	—	+18	−5	—	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
di/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = OpF	4.0	8.0	—	4.0	8.0	—	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$V_S = (+13.5V$ to $+16.5V)$ $V_{EE} = -15V$	—	±.00005	±.001	—	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		$V_{EE} = -13.5V$ to $-16.5V$ $V_S = +15V$	—	±.00025	±.001	—	±.00025	±.001	
V_S	Power Supply Range	$V_{OUT} = 0V$	4.5	—	18	4.5	—	18	V
V_{EE}			−18	—	−10.8	−18	—	−10.8	
I+	Power Supply Current	$V_S = +5V$, $V_{EE} = -15V$	—	5.7	8.5	—	5.7	8.5	mA
I−			—	−13.7	−18.0	–	−13.7	−18.0	
I+		$V_S = +15V$, $V_{EE} = -15V$		5.7	8.5	—	5.7	8.5	
I−			—	−13.7	−18.0	–	−13.7	−18.0	
P_D	Power Dissipation	$V_S = +5V$, $V_{EE} = -15V$	—	234	312	—	234	312	mW
		$V_S = +15V$, $V_{EE} = -15V$	—	291	397	—	291	397	

Fig. 1 - Relative Accuracy Error

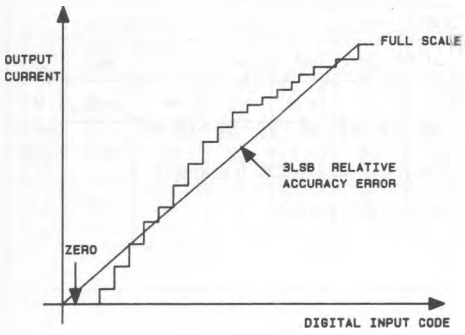


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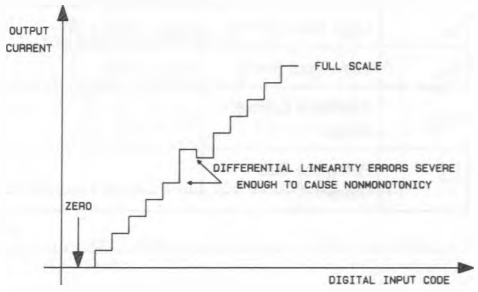
Fig. 2 - Example of Nonmonotonic Behavior



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APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The segmented design of the AM6012, shown in the block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AM6012.

In a conventional R-2R type DAC, when the input code is increemented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AM6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time. For example, consider the MSB carry in an AM6012. In the initial state of 011111111111 as shown in the block diagram, the switches in the segment generator are set in such a way that currents I_O, I_1 and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "1", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

RELATIVE ACCURACY VS. DIFFERENTIAL NONLINEARITY

We defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 1 has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a ILSB change in digital input code.

For example, for a 4mA full scale output, a change of ILSB in digital input code should result in a 0.98μA change in the analog output current (ILSB = 4mA x 1/4096 = 0.98μA). If in actual use, however, a ILSB change in the input code results ina change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The AM6012 has very good differential linearity in spite of the porr relative accuracy. Conversely, the DAC of Figure 1 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be nonmonotonic at one or more of the major carries. In most case the worst differential linearity error will occur at the MSB transition point.

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. Differential linearity is verified on all AM6012s with 100% final testing. In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit onverters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AM6012 is especially well suited for these applications since it has inherently low differential linearity error.

APPLICATION INFORMATION (Continued)

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + I_{\overline{O}} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increase $I_{\overline{O}}$ as in a negative or inverter logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin one.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures fro guidance. For example, operation at −9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and mononicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is flight, typically ±10ppm/°C with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ms. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu A$, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be octained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATION INFORMATION (Continued)

REFERENCE AMPLIFIER SETUP

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{RF} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 3).

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5 OkΩ; minimum values of C_C are 5, 12 and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin (See Figure 4 and 5).

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven be a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to I_{REF} = 1mA in 250ns.

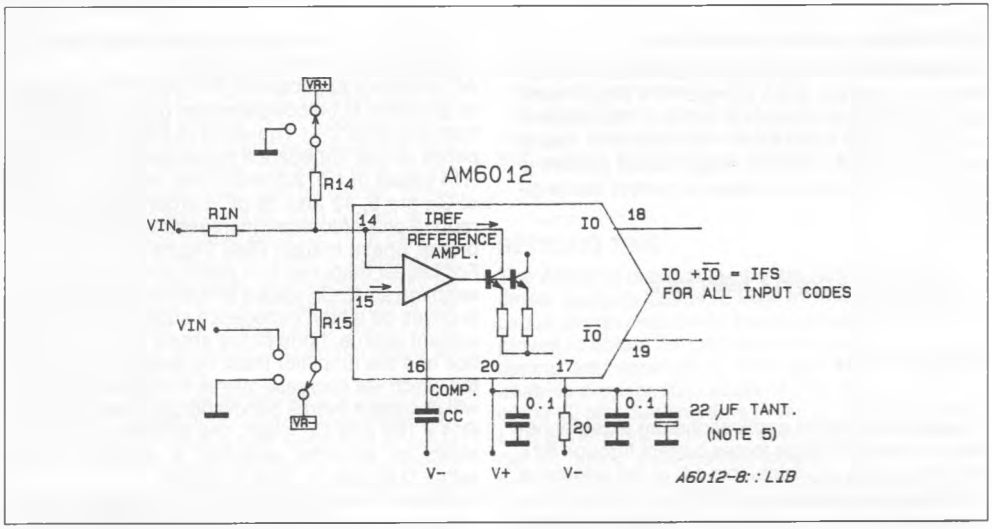
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and $C_C = 0$. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic inputs may swing between −5 and +10V.

This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended. For interfacing other logic families, see block titled "Interfacing with Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 1.1mA typical, external circuitry should be designed to accommodate this current (Figure 6).

Fig. 3 - Reference amplifier biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01µF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01µF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V - with 20Ω and bypass with 22µF tantulum capacitor.
6. Reference current and reference resistor - there is a 1 to 4 schale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4mA} = 10k\Omega \quad R_{14} = R_{15}$$

Fig. 4 - Minimum size compensation capacitor (I_{FS} = 4mA, I_{REF} = 1.0mA)

$R_{14(EQ)}$(KΩ)	C_C(pF)
10	50
5	25
2	10
1	5
5	0

Note: A 0.01 μF capacitor is recommended for fixed reference operation.

Fig. 5 - Reference Amplifier Frequency response

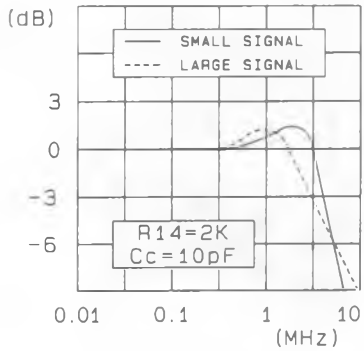


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Fig. 6 - Interfacing Circuits

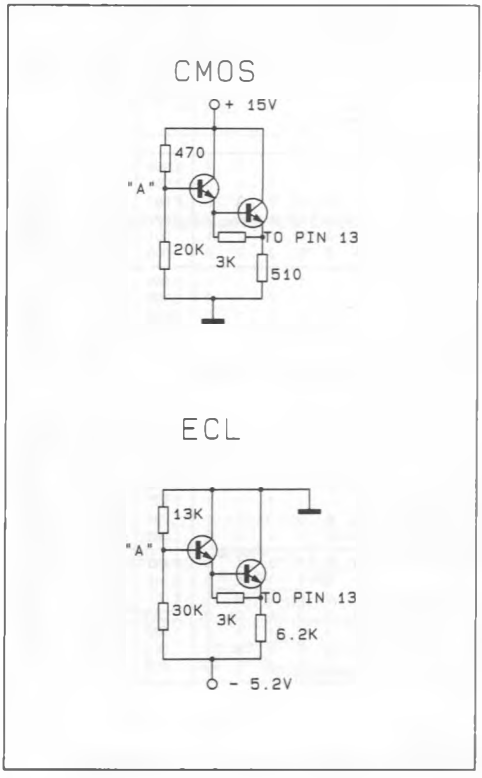


Fig. 7 - Accomodating Bipolar Reference

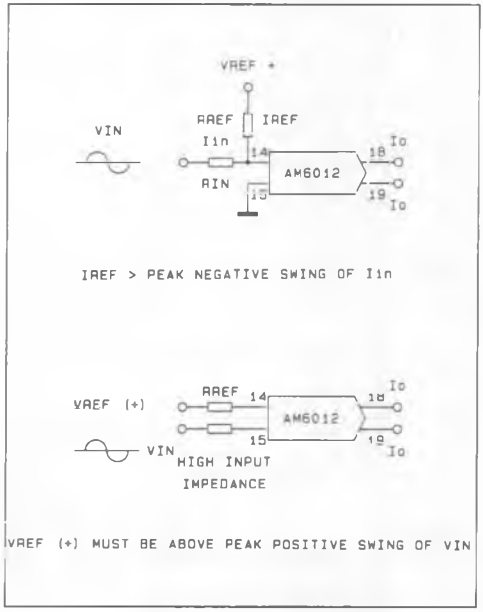
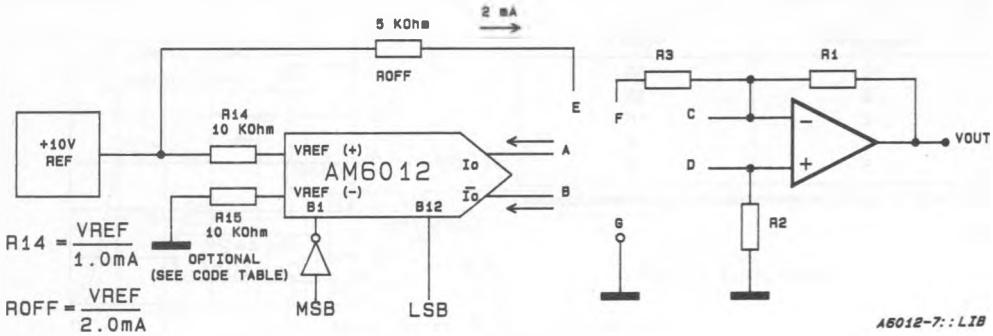


Fig. 8 - AM6012 Logic Inputs



Code Format		Connec.	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0	$\overline{I_0}$	V_{OUT}
Unipolar	Straight bynary one polarity with true input code, true zero output	a-c b-g $R_1 = R2 = 2.5K$	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9978
			Positive full scale-LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary one polarity with complementary input code, true zero output	a-g b-c R1 = R2 = 2.5K	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
			Positive full scale-LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
			Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
Symmetrical Offset	Straight offset binary; offset half scale, symmetrical about zero, no true zero output	a-c b-d f-0 R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale-LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(-) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0024
			Negative full scale-LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-9.9976
	1's complement offset half scale symmetrical about zero, no true zero output MSB complemented (need inverter at B1)	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale-LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(-) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0024
			Negative full scale-LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-9.9976
Offset with True Zero	Offset binary, offset half scale, true zero output	e-a-c b-g R1 = R2 = 5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale-LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			-LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-.0049
			Negative full scale+LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	-9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-10.000
	2's complement offset half scale true zero output MSB complemented (need inverter at B1)	e-a-c b-g R1 = R2 = 5K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
			Positive full scale-LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			-1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.049
			Negative full scale+LSB	1	0	0	0	0	0	0	0	0	0	0	1	001	3.998	-9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	-10.000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

Fig. 9 - Basic Negative Reference Operation

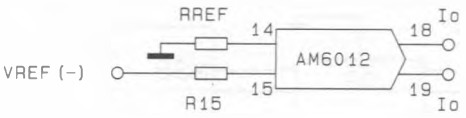


Fig. 10 - Recommended Full-scale Adjustment Circuit

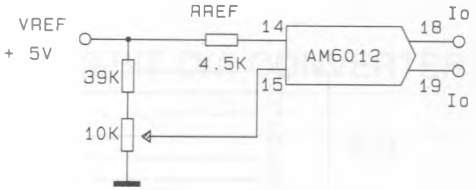


Fig. 11 - CRT Display Driver

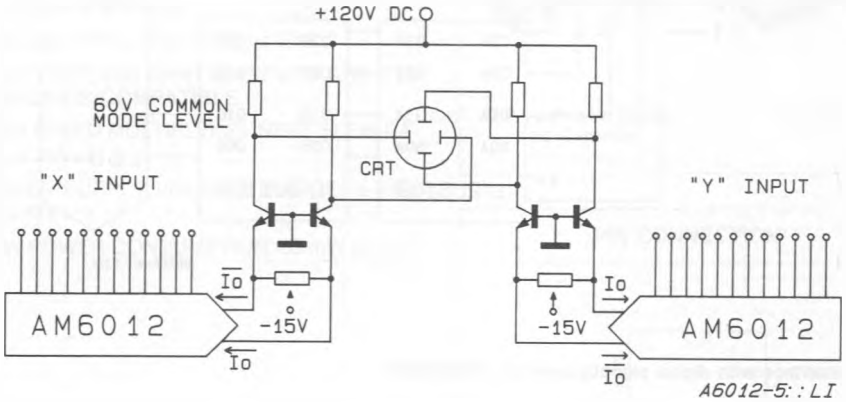


Fig. 12 - 12-BIT High-Speed A/D Converter

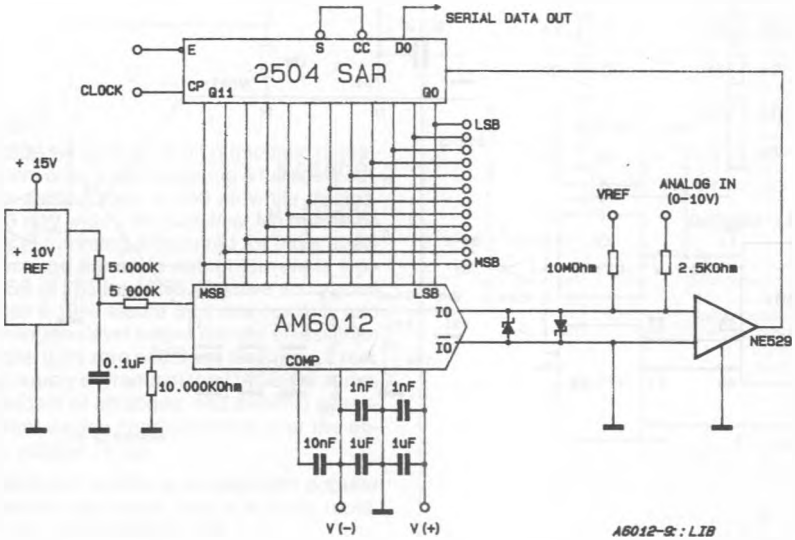


Fig. 13 - Interface with 8-bit Microprocessor Bus

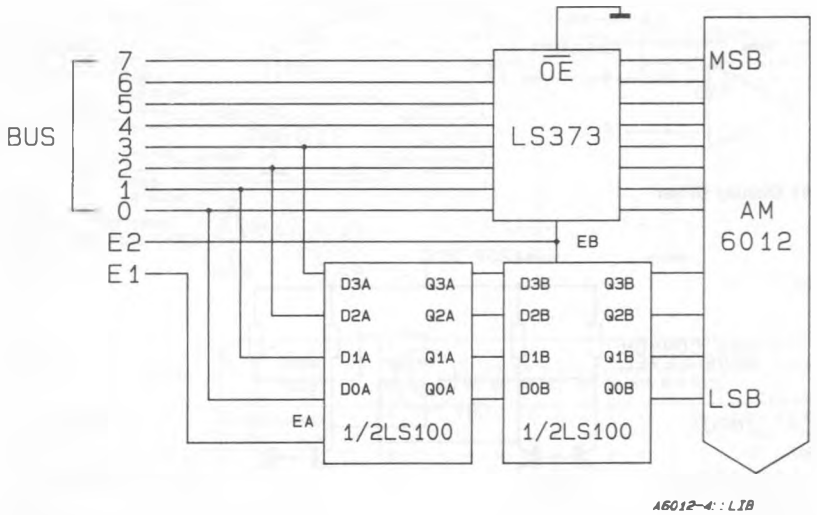


Fig. 14 - Interface with digital signal processor TS68930/31