

AMD Athlon™ MP

Processor Model 6

OPGA Data Sheet

for Multiprocessor

Platforms



Preliminary Information

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Contents

Revision History	xi
1 Overview	1
1.1 AMD Athlon™ MP Processor Key Microarchitecture Summary	2
2 Interface Signals	5
2.1 Overview	5
2.2 Signaling Technology	5
2.3 Push–Pull (PP) Drivers	6
2.4 AMD Athlon System Bus Signals	6
3 Logic Symbol Diagram	7
4 Power Management	9
4.1 Power Management States	9
Working State	10
Halt State	10
Stop Grant States	10
Probe State	12
4.2 Connect and Disconnect Protocol	13
Connect Protocol	13
4.3 Clock Control	19
5 CPUID Support	21
6 Thermal Design	23
7 Electrical Data	25
7.1 Conventions	25
7.2 Interface Signal Groupings	25
7.3 Voltage Identification (VID[4:0])	26
7.4 Frequency Identification (FID[3:0])	27
7.5 VCCA AC and DC Characteristics	27
7.6 Decoupling	27
7.7 VCC_CORE Characteristics	28
7.8 Absolute Ratings	30
7.9 VCC_CORE Voltage and Current	30
7.10 SYSCLK and SYSCLK# AC and DC Characteristics	31
7.11 AMD Athlon™ System Bus AC and DC Characteristics	33
7.12 General AC and DC Characteristics	35
7.13 Thermal Diode Characteristics	37
7.14 APIC Pins AC and DC Characteristics	38

8	Signal and Power-Up Requirements	39
8.1	Power-Up Requirements	39
	Signal Sequence and Timing Description	39
	Clock Multiplier Selection (FID[3:0])	42
8.2	Processor Warm Reset Requirements	42
	Northbridge Reset Pins	42
9	Mechanical Data	43
9.1	Introduction	43
9.2	Die Loading	43
9.3	OPGA Package Description	44
10	Pin Descriptions	47
10.1	Pin Diagram and Pin Name Abbreviations	47
10.2	Pin List	56
10.3	Detailed Pin Descriptions	64
	A20M# Pin	64
	AMD Pin	64
	AMD Athlon System Bus Pins	64
	Analog Pin	64
	APIC Pins, PICCLK, PICD[1:0]#	64
	CLKFWRST Pin	64
	CLKIN, RSTCLK (SYSCLK) Pins	64
	CONNECT Pin	65
	COREFB and COREFB# Pins	65
	CPU_PRESENCE# Pin	65
	DBRDY and DBREQ# Pins	65
	FERR Pin	65
	FID[3:0] Pins	65
	FLUSH# Pin	67
	IGNNE# Pin	67
	INIT# Pin	67
	INTR Pin	67
	JTAG Pins	67
	K7CLKOUT and K7CLKOUT# Pins	67
	Key Pins	67
	NC Pins	67
	NMI Pin	67
	PGA Orientation Pins	68
	PLL Bypass and Test Pins	68
	PWROK Pin	68
	SADDIN[1:0]# and SADDOUT[1:0]# Pins	68
	Scan Pins	68
	SCHECK[7:0]# Pins	68
	SMI# Pin	68
	STPCLK# Pin	68
	SYSCLK and SYSCLK#	69

	THERMDA and THERMDC Pins	69
	VCCA Pin	69
	VID[4:0] Pins	69
	VREFSYS Pin	70
	ZN and ZP Pins	70
11	Ordering Information	71
	Standard AMD Athlon MP Processor Products	71
	Appendix A Conventions and Abbreviations	73
	Signals and Bits	73
	Data Terminology	74
	Abbreviations and Acronyms	75

List of Figures

Figure 1.	Logic Symbol Diagram	7
Figure 2.	AMD Athlon™ MP Processor Power Management States	9
Figure 3.	AMD Athlon System Bus Disconnect Sequence in the Stop Grant State	15
Figure 4.	Exiting the Stop Grant State and Bus Connect Sequence	16
Figure 5.	Northbridge Connect State Diagram	17
Figure 6.	Processor Connect State Diagram	18
Figure 7.	VCC_CORE Voltage Waveform	29
Figure 8.	SYSCLK and SYSCLK# Differential Clock Signals	31
Figure 9.	SYSCLK Waveform	32
Figure 10.	Signal Relationship Requirements During Power-Up Sequence	39
Figure 11.	AMD Athlon MP Processor OPGA Package	45
Figure 12.	AMD Athlon MP Processor Pin Diagram— Topside View	48
Figure 13.	AMD Athlon MP Processor Pin Diagram— Bottomside View	49
Figure 14.	OPN Example for the AMD Athlon MP Processor, OPGA Package	71

List of Tables

Table 1.	Maximum Thermal Power	23
Table 2.	Interface Signal Groupings	25
Table 3.	VID[4:0] DC Characteristics	26
Table 4.	FID[3:0] DC Characteristics	27
Table 5.	VCCA AC and DC Characteristics	27
Table 6.	VCC_CORE Characteristics	28
Table 7.	Absolute Ratings	30
Table 8.	VCC_CORE Voltage and Current.	30
Table 9.	SYSClk and SYSClk# DC Characteristics	31
Table 10.	SYSClk and SYSClk# AC Characteristics	32
Table 11.	AMD Athlon™ System Bus DC Characteristics	33
Table 12.	AMD Athlon System Bus AC Characteristics	34
Table 13.	General AC and DC Characteristics.	35
Table 14.	Thermal Diode Characteristics.	37
Table 15.	APIC Pin AC and DC Characteristics.	38
Table 16.	Mechanical Loading for the OPGA Package	43
Table 17.	Dimensions for the AMD Athlon MP Processor OPGA Package	44
Table 18.	Pin Name Abbreviations	50
Table 19.	Cross-Reference by Pin Location	56
Table 20.	FID[3:0] Clock Multiplier Encodings	66
Table 21.	VID[4:0] Code to Voltage Definition	69
Table 22.	Abbreviations	75
Table 23.	Acronyms.	76

Revision History

Date	Rev	Description
October 2001	A	Initial release of the <i>AMD Athlon™ MP Processor Model 6 OPGA Data Sheet for Multiprocessor Platforms</i> , order# 25480.

1 Overview

The AMD Athlon™ MP Processor powers the next generation in computing platforms, delivering compelling performance for cutting-edge applications and an unprecedented computing experience.

The AMD Athlon™ MP processor continues to deliver breakthrough performance in the multiprocessing server and workstation markets. This processor is designed to meet the reliability and computation-intensive requirements of cutting-edge software applications required by workstations and servers.

Delivered in an OPGA package, the AMD Athlon MP processor delivers the integer, floating-point, and 3D multimedia performance for enterprise applications running on x86 system platforms. The AMD Athlon MP processor offers compelling performance for productivity software, including workstation-class Digital Content Creation (DCC), Electronic Design Automation (EDA), and Computer-Aided Design (CAD), as well as infrastructure and collaborative server applications. It also offers the scalability and reliability that IT managers and business users require for mission-critical computing.

The AMD Athlon MP processor features the seventh-generation microarchitecture, including a high-speed execution core that includes multiple x86 instruction decoders; a dual-ported, 128-Kbyte, split level-one (L1) cache; a 256-Kbyte on-chip L2 cache; three independent integer pipelines, three address calculation pipelines; and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The integrated L2 cache supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The processor also features the advanced MOESI cache coherency protocol to ensure efficient cache integrity in a multiprocessing environment. The floating-point engine is capable of delivering excellent performance on the numerically complex applications typical of servers and workstations.

The key features of the AMD Athlon MP processor include QuantiSpeed™ architecture, a high-performance full-speed cache, a 266-MHz, 2.1-Gigabyte per second system bus,

3DNow!™ Professional technology, and fully featured logic implementation for the multiprocessor configuration.

The AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling. The point-to-point front-side bus architecture provides a more efficient, higher bandwidth bus that allows each processor, in a multiprocessor configuration, to communicate to the system chipset through two, full-speed, independent buses rather than through a common, shared bus. Combined with the AMD-760MP™ chipset, the processor and the system bus interface with Double-Data Rate (DDR) memory subsystems, providing scalable headroom for bandwidth-hungry applications such as large databases, CAD/CAM modeling, and simulation engines.

The front-side bus of the AMD Athlon MP processor also provides multiple-bit error detection and single-bit error correction with 8-bit Error Correcting Code (ECC). The front-side bus with 8-bit ECC delivers the high reliability and consistency demanded by mission-critical applications.

The AMD Athlon MP processor is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow! technologies. Using a data format and Single-Instruction Multiple-Data (SIMD) operations based on the MMX instruction model, the AMD Athlon MP processor can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The 3DNow! professional technology implemented in the AMD Athlon MP processor includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for Digital Signal Processing (DSP)/communications applications.

1.1 AMD Athlon™ MP Processor Key Microarchitecture Summary

The following features summarize the AMD Athlon MP processor microarchitecture:

- QuantiSpeed architecture:
 - An advanced nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for increased

Instructions Per Clock cycle (IPC) and high clock frequencies

- Fully pipelined floating-point unit that executes all x87 (floating-point), MMX and 3DNow! professional instructions
 - Hardware data pre-fetch that increases and optimizes performance on high-end software applications that utilize high-bandwidth system capability
 - Advanced two-level Translation Look-aside Buffer (TLB) structures for enhanced data and instruction address translation. The AMD Athlon MP processor with QuantiSpeed architecture incorporates three TLB optimizations: the L1 DTLB increases from 32 to 40 entries, the L2 ITLB and L2 DTLB both use exclusive architecture, and the TLB entries can be speculatively loaded.
- 3DNow! professional technology with new instructions to enable improved integer-math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications
 - 266-MHz AMD Athlon system bus enabling leading-edge system bandwidth for data movement-intensive applications
 - Point-to-point front-side bus architecture allowing each processor in a multi-processor configuration to communicate to the system chipsets through two, full speed, independent buses
 - High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, 256-Kbyte on-chip L2 cache for a total of 384 Kbytes of on-chip cache
 - Multiple-bit error detection and single-bit error correction with 8-bit Error Correcting Code (ECC)
 - Full featured MP Local APIC implementation
 - Advanced MOESI cache coherency protocol to ensure efficient cache integrity in a multiprocessing environment

The AMD Athlon MP processor delivers excellent system performance in a cost-effective, industry-standard form factor. The AMD Athlon MP processor is compatible with motherboards based on Socket A.

2 Interface Signals

2.1 Overview

The AMD Athlon™ system bus architecture is designed to deliver superior data movement bandwidth for next-generation x86 platforms as well as the high-performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel, including 8-bit Error Code Correction [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull, low-voltage, swing-signaling technology contained within the Socket A socket.

For more information, see “AMD Athlon™ System Bus Signals” on page 6, “Pin Descriptions” on page 47, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

2.2 Signaling Technology

The AMD Athlon system bus uses a low-voltage, swing-signaling technology, that has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers, that require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance-matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, “Pin Descriptions” on page 47.

2.3 Push-Pull (PP) Drivers

The AMD Athlon MP processor supports Push-Pull (PP) drivers. The system logic configures the processor with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins.

See “ZN and ZP Pins” on page 70 for more information.

2.4 AMD Athlon™ System Bus Signals

The AMD Athlon system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Chapter 7, “Electrical Data” on page 25 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

3 Logic Symbol Diagram

Figure 1 is the logic symbol diagram of the processor. This diagram shows the logical grouping of the input and output signals.

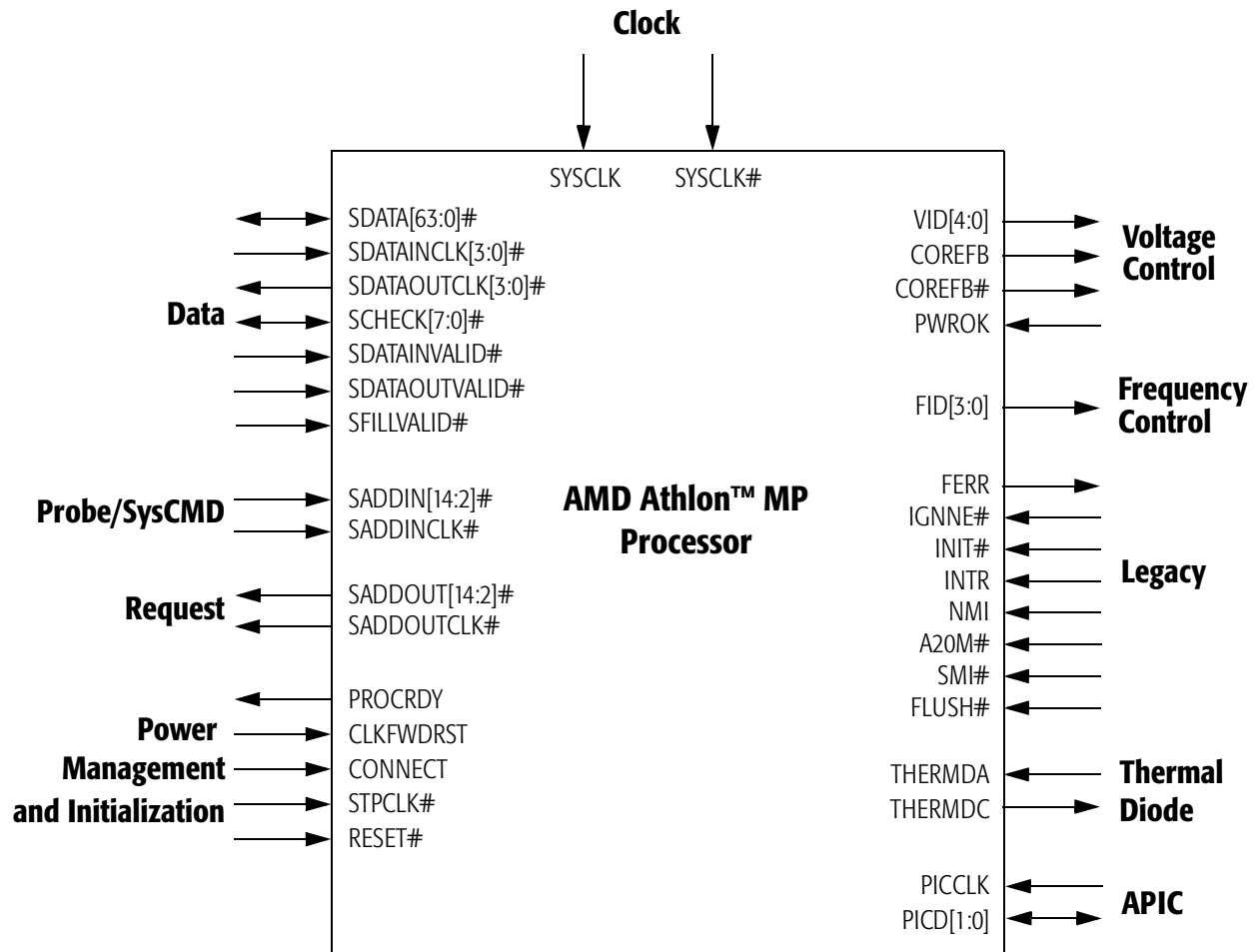


Figure 1. Logic Symbol Diagram

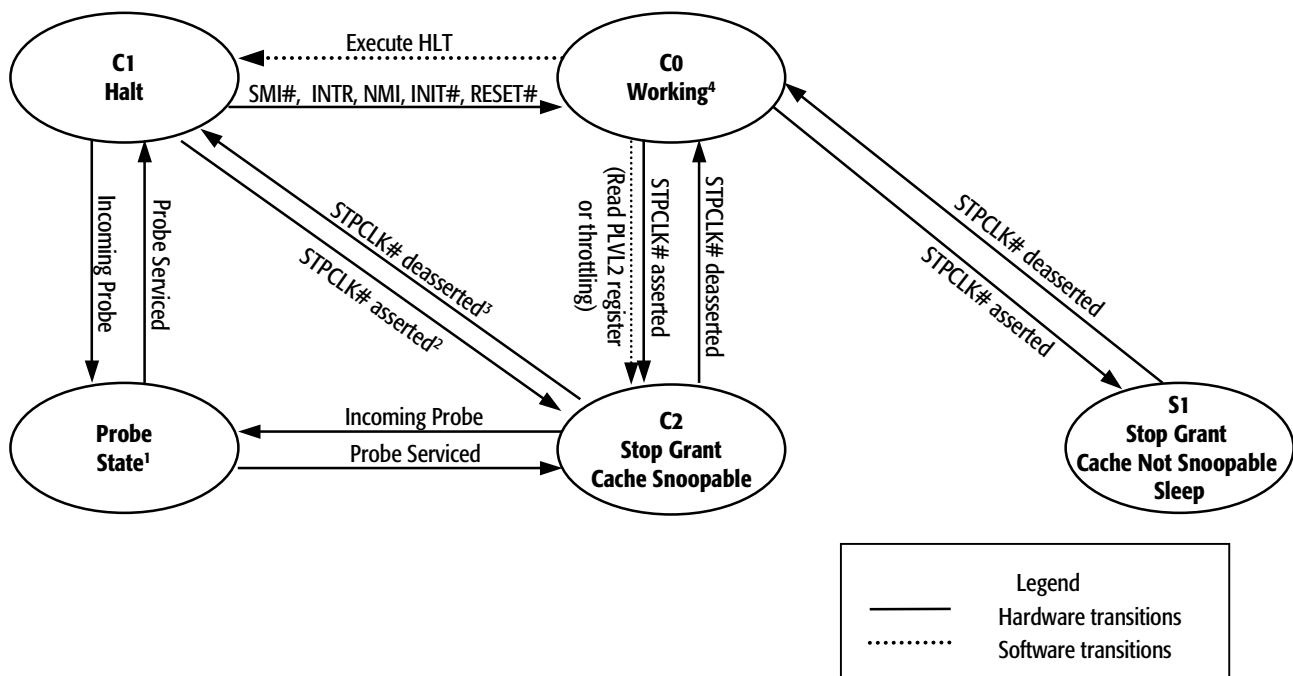
4 Power Management

This chapter describes the power management control system of the AMD Athlon™ MP processor. The power management features of the processor are compliant with the ACPI 1.0b and ACPI 2.0 specifications.

4.1 Power Management States

The AMD Athlon MP processor supports low-power Halt and Stop Grant states. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems for processor power management.

Figure 2 shows the power management states of the processor. The figure includes the ACPI “Cx” naming convention for these states.



Note: The AMD Athlon™ System Bus is connected during the following states:

- 1) The Probe state
- 2) During transitions between the Halt state and the C2 Stop Grant state
- 3) During transitions between the C2 Stop Grant state and the Halt state
- 4) C0 Working state

Figure 2. AMD Athlon™ MP Processor Power Management States

The following sections provide an overview of the power management states. For more details, refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

Note: In all power management states that the processor is powered, the system must not stop the system clock (SYSCLK/SYSClk#) to the processor.

Working State

The Working state is the state in which the processor is executing instructions.

Halt State

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD Athlon system bus. The processor only enters the low power state dictated by the CLK_Ctl MSR if the system controller (Northbridge) disconnects the AMD Athlon system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor will exit the Halt state and enter the Stop Grant state. The processor will initiate a system bus connect, if it is disconnected, then issue a Stop Grant special cycle. When STPCLK# is deasserted, the processor will exit the Stop Grant state and re-enter the Halt state. The processor will issue a Halt special cycle when re-entering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, RESET#, SMI#, or an interrupt via the INTR or NMI pins, or via a local APIC interrupt message. When the Halt state is exited, the processor will initiate an AMD Athlon system bus connect if it is disconnected.

Stop Grant States

The processor enters the Stop Grant state upon recognition of assertion of STPCLK# input. After entering the Stop Grant state, the processor issues a Stop Grant special bus cycle on the AMD Athlon system bus. The processor is not in a low-power state at this time, because the AMD Athlon system bus is still connected. After the Northbridge disconnects the AMD Athlon system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK_Ctl MSR. If the Northbridge needs to probe the processor during the Stop Grant state while the system bus is disconnected, it

must first connect the system bus. Connecting the system bus places the processor into the higher power probe state. After the Northbridge has completed all probes of the processor, the Northbridge must disconnect the AMD Athlon system bus again so that the processor can return to the low-power state. During the Stop Grant states, the processor latches INIT#, INTR, NMI, SMI#, or a local APIC interrupt message, if they are asserted.

The Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. When STPCLK# is deasserted, the processor initiates a connect of the AMD Athlon system bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized. If RESET# is sampled asserted during the Stop Grant state, the processor exits the Stop Grant state and the reset process begins.

There are two mechanisms for asserting STPCLK#—hardware and software.

The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until THERM# is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge.

The operating system places the processor into the C2 Stop Grant state by reading the P_LVL2 register in the Southbridge.

If an ACPI Thermal Zone is defined for the processor, the operating system can initiate throttling with STPCLK# using the ACPI defined P_CNT register in the Southbridge. The Northbridge connects the AMD Athlon system bus, and the processor enters the Probe state to service cache snoops during Stop Grant for C2 or throttling.

In C2, probes are allowed, as shown in Figure 2 on page 9

The Stop Grant state is also entered for the S1, Powered On Suspend, system sleep state based on a write to the SLP_TYP and SLP_EN fields in the ACPI-defined Power Management 1 control register in the Southbridge. During the S1 Sleep state, system software ensures no bus master or probe activity occurs. The Southbridge deasserts STPCLK# and brings the processor out of the S1 Stop Grant state when any enabled resume event occurs.

Probe State

The Probe state is entered when the Northbridge connects the AMD Athlon system bus to probe the processor (for example, to snoop the processor caches) when the processor is in the Halt or Stop Grant state. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state. When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). When probe activity is completed the processor only returns to a low-power state after the Northbridge disconnects the AMD Athlon system bus again.

4.2 Connect and Disconnect Protocol

Significant power savings of the processor only occur if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Athlon system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWRST signals and a Connect special cycle.

AMD Athlon system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# deassertion, or by the Northbridge to service a probe.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWRST in anticipation of reestablishing a connection at some later point.

Note: *The Northbridge must disconnect the processor from the AMD Athlon system bus before issuing the Stop Grant special cycle to the PCI bus, or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

This note applies to current chipset implementation—alternate chipset implementations that do not require this are possible.

Note: *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted).

For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 3 shows STPCLK# assertion resulting in the processor in the Stop Grant state and the AMD Athlon system bus disconnected.

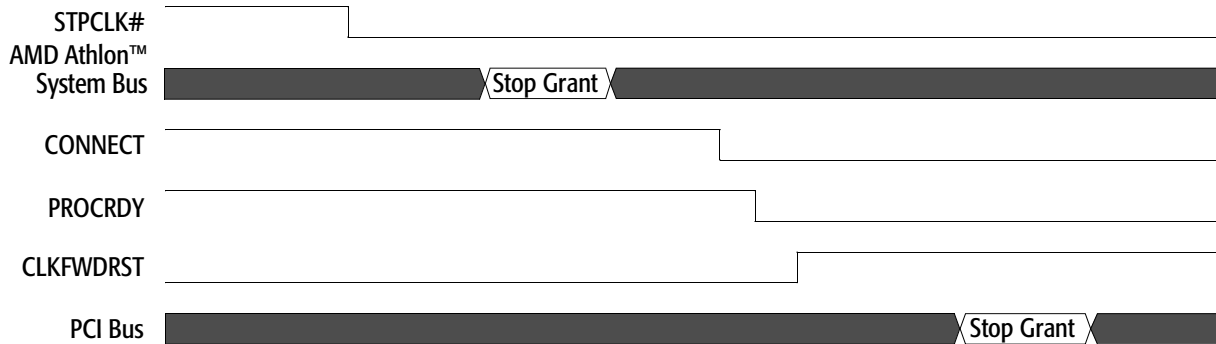


Figure 3. AMD Athlon™ System Bus Disconnect Sequence in the Stop Grant State

An example of the AMD Athlon system bus disconnect sequence is as follows:

1. The peripheral controller (Southbridge) asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted, it enters the Stop Grant state and then issues a Stop Grant special cycle.
3. When the special cycle is received by the Northbridge, it deasserts CONNECT, assuming no probes are pending, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY.
5. The Northbridge asserts CLKFWRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the processor enters a low-power state. The Northbridge passes the Stop Grant special cycle along to the Southbridge.

Figure 4 shows the signal sequence of events that takes the processor out of the Stop Grant state, connects the processor to the AMD Athlon system bus, and puts the processor into the Working state.

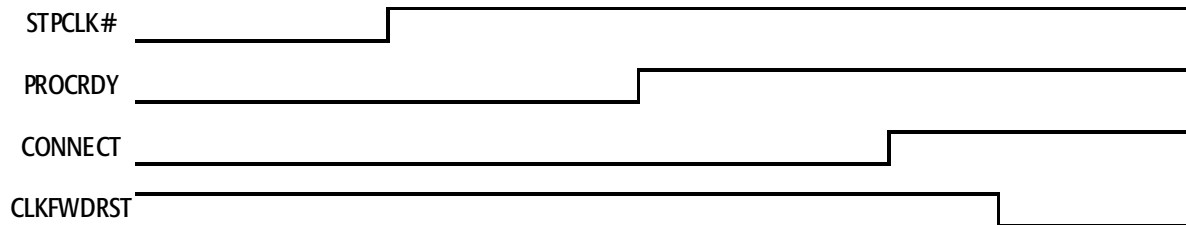
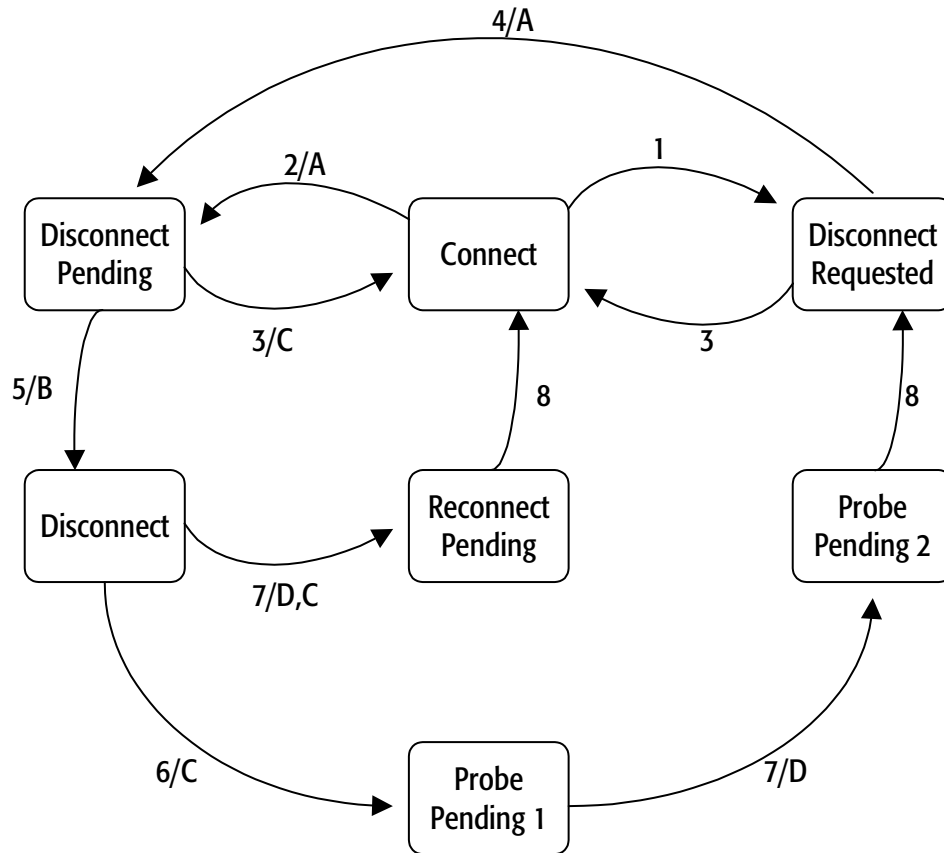


Figure 4. Exiting the Stop Grant State and Bus Connect Sequence

The following sequence of events removes the processor from the Stop Grant state and connects it to the system bus:

1. The Southbridge deasserts STPCLK#, informing the processor of a wake event.
2. When the processor recognizes STPCLK# deassertion, it exits the low-power state and asserts PROCRDY, notifying the Northbridge to connect to the bus.
3. The Northbridge asserts CONNECT.
4. The Northbridge deasserts CLKFWRST, synchronizing the forwarded clocks between the processor and the Northbridge.
5. The processor issues a Connect special cycle on the system bus and resumes operating system and application code execution.

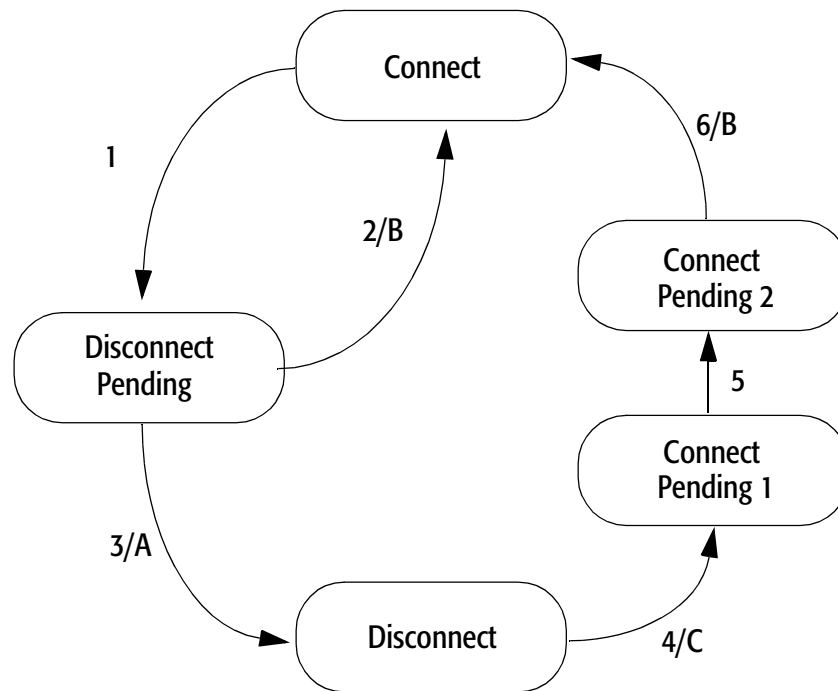
Figure 5 and Figure 6 on page 18 describe the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending.
2	A disconnect is requested and no probes are pending.
3	A Connect special cycle from the processor.
4	No probes are pending.
5	PROCRDY is deasserted.
6	A probe needs service.
7	PROCRDY is asserted.
8	Three SYSCLK periods after CLKFWDRST is deasserted. <i>Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.</i>

	Action
A	Deassert CONNECT eight SYSCLK periods after last SysDC sent.
B	Assert CLKFWDRST.
C	Assert CONNECT.
D	Deassert CLKFWDRST.

Figure 5. Northbridge Connect State Diagram



	Condition	Action
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).	A CLKFWRST is asserted by the Northbridge.
2	Processor receives a wake-up event and must cancel the disconnect request.	B Issue a Connect special cycle.*
3	Deassert PROCRDY and slow down internal clocks.	C Return internal clocks to full speed and assert PROCRDY.
4	Processor wake-up event or CONNECT asserted by Northbridge.	* The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Athlon™ system bus is connected so the Northbridge can probe the processor, a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).
5	CLKFWRST is deasserted by the Northbridge.	
6	Forward clocks start three SYCLK periods after CLKFWRST is deasserted.	

Figure 6. Processor Connect State Diagram

4.3 Clock Control

The processor implements a Clock Control (CLK_Ctl) MSR (address C001_001Bh) that determines the internal clock divisor when the AMD Athlon system bus is disconnected.

Refer to the *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656, for more details on the CLK_Ctl register.

5 CPUID Support

AMD Athlon™ MP processor version and feature set recognition can be performed through the use of the CPUID instruction, that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction see the following document:

- *AMD Processor Recognition Application Note*, order# 20734

6 Thermal Design

The AMD Athlon™ MP Processor provides a diode that can be used in conjunction with an external temperature sensor to determine the die temperature of the processor.

The diode anode (THERMDA) and cathode (THERMDC) are available as pins on the processor.

Refer to “THERMDA and THERMDC Pins” on page 69 for more details.

For information about thermal design for the AMD Athlon MP processor, including layout and airflow considerations, see the *AMD Processor Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794, and the cooling guidelines on <http://www.amd.com>.

Table 1 shows the thermal design power specifications.

Table 1. Maximum Thermal Power

Model Number	Frequency (MHz)	Nominal Voltage	Maximum Thermal Power ¹	Typical Thermal Power	Max Die Temperature
1500+	1333	1.75 V	60.0 W	53.8 W	95°C
1600+	1400		62.8 W	56.3 W	
1800+	1533		66.0 W	59.2 W	
Notes: 1. The maximum thermal power represents the maximum sustained power dissipated while executing publicly available software or instruction sequences under normal system operation at nominal VCC_CORE. Thermal solutions must monitor the processor temperature to prevent the processor from exceeding its maximum die temperature.					

7 Electrical Data

7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group.

Table 2 defines each group and the signals contained in each group.

Table 2. Interface Signal Groupings

Signal Group	Signals	Notes
Power	VID[4:0], VCCA, VCC_CORE, COREFB, COREFB#	See "Absolute Ratings" on page 30, "Voltage Identification (VID[4:0])" on page 26, "VID[4:0] Pins" on page 69, "VCCA AC and DC Characteristics" on page 27, "VCCA Pin" on page 69, and "COREFB and COREFB# Pins" on page 65.
Frequency	FID[3:0]	See "Frequency Identification (FID[3:0])" on page 27 and "FID[3:0] Pins" on page 65.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See Table 9, "SYSCLK and SYSCLK# DC Characteristics," on page 31, Table 10, "SYSCLK and SYSCLK# AC Characteristics," on page 32, Table , "SYSCLK and SYSCLK#," on page 69, and Table , "PLL Bypass and Test Pins," on page 68.
AMD Athlon™ System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, SCHECK[7:0]#, CLKFWRDST, PROCRDY, CONNECT	See "AMD Athlon™ System Bus AC and DC Characteristics" on page 33, and "CLKFWRDST Pin" on page 64.

Table 2. Interface Signal Groupings (Continued)

Signal Group	Signals	Notes
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See “General AC and DC Characteristics” on page 35, “INTR Pin” on page 67, “NMI Pin” on page 67, “SMI# Pin” on page 68, “INIT# Pin” on page 67, “A20M# Pin” on page 64, “FERR Pin” on page 65, “IGNNE# Pin” on page 67, “STPCLK# Pin” on page 68, and “FLUSH# Pin” on page 67.
JTAG	TMS, TCK, TRST#, TDI, TDO	See “General AC and DC Characteristics” on page 35.
Test	PLLBYPASS#, PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See “General AC and DC Characteristics” on page 35, “PLL Bypass and Test Pins” on page 68, “Scan Pins” on page 68, “Analog Pin” on page 64.
Miscellaneous	DBREQ#, DBRDY, PWROK	See “General AC and DC Characteristics” on page 35, “DBRDY and DBREQ# Pins” on page 65, “PWROK Pin” on page 68.
APIC	PICD[1:0]#, PICCLK	See “APIC Pins AC and DC Characteristics” on page 38, and “APIC Pins, PICCLK, PICD[1:0]#” on page 64.
Thermal	THERMDA, THERMDC	Table 14, “Thermal Diode Characteristics,” on page 37, and “THERMDA and THERMDC Pins” on page 69.

7.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC Characteristics. For more information on VID[4:0] DC Characteristics, see “VID[4:0] Pins” on page 69.

Table 3. VID[4:0] DC Characteristics

Parameter	Description	Min	Max
I _{OL}	Output Current Low	16 mA	
V _{OH}	Output High Voltage	–	2.625 V*
Note: * The VID pins must not be pulled above this voltage by an external pullup resistor.			

7.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see “FID[3:0] Pins” on page 65.

Table 4. FID[3:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
V_{OH}	Output High Voltage	–	2.625 V *
Note: * The FID pins must not be pulled above this voltage by an external pullup resistor.			

7.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see “VCCA Pin” on page 69.

Table 5. VCCA AC and DC Characteristics

Symbol	Parameter	Min	Nominal	Max	Units	Notes
V_{VCCA}	VCCA Pin Voltage	2.25	2.5	2.75	V	1
I_{VCCA}	VCCA Pin Current	0		50	mA/GHz	2
Notes: 1. Minimum and Maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted. 2. Measured at 2.5 V.						

7.6 Decoupling

See the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Athlon™ MP processor.

7.7 VCC_CORE Characteristics

The AMD Athlon MP processor is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 6, which also shows the AC and DC characteristics for VCC_CORE. See Figure 7 on page 29 for a graphical representation of the VCC_CORE waveform.

Table 6. VCC_CORE Characteristics

Parameter	Description	Min ¹		Nominal ¹	Max ¹		Units
		AC	DC		DC	AC	
VCC_CORE@ 1.75 V	Processor core supply	1.65	1.70	1.75	1.80	1.90	V
VCC_CORE _{SLEEP} ²	Processor core supply in sleep state	1.20	1.25	1.30	1.35	1.45	V
t _{MAX_AC} ³	Positive excursion time for AC transients					10	μs
t _{MIN_AC} ³	Negative excursion time for AC transients					5	μs
T _{DIE}	Temperature of processor die				95		°C
Notes:							
1. All voltage measurements are taken differentially at the COREFB/COREFB# pins.							
2. Sleep voltage can be used for the S1 sleep state.							
3. Excursion time is defined as the length of time a signal exceeds the DC threshold level.							

Figure 7 shows the processor core voltage (V_{CC_CORE}) waveform response to perturbation. The t_{MIN_AC} (negative AC transient excursion time) and t_{MAX_AC} (positive AC transient excursion time) represent the maximum allowable time below or above the DC tolerance thresholds.

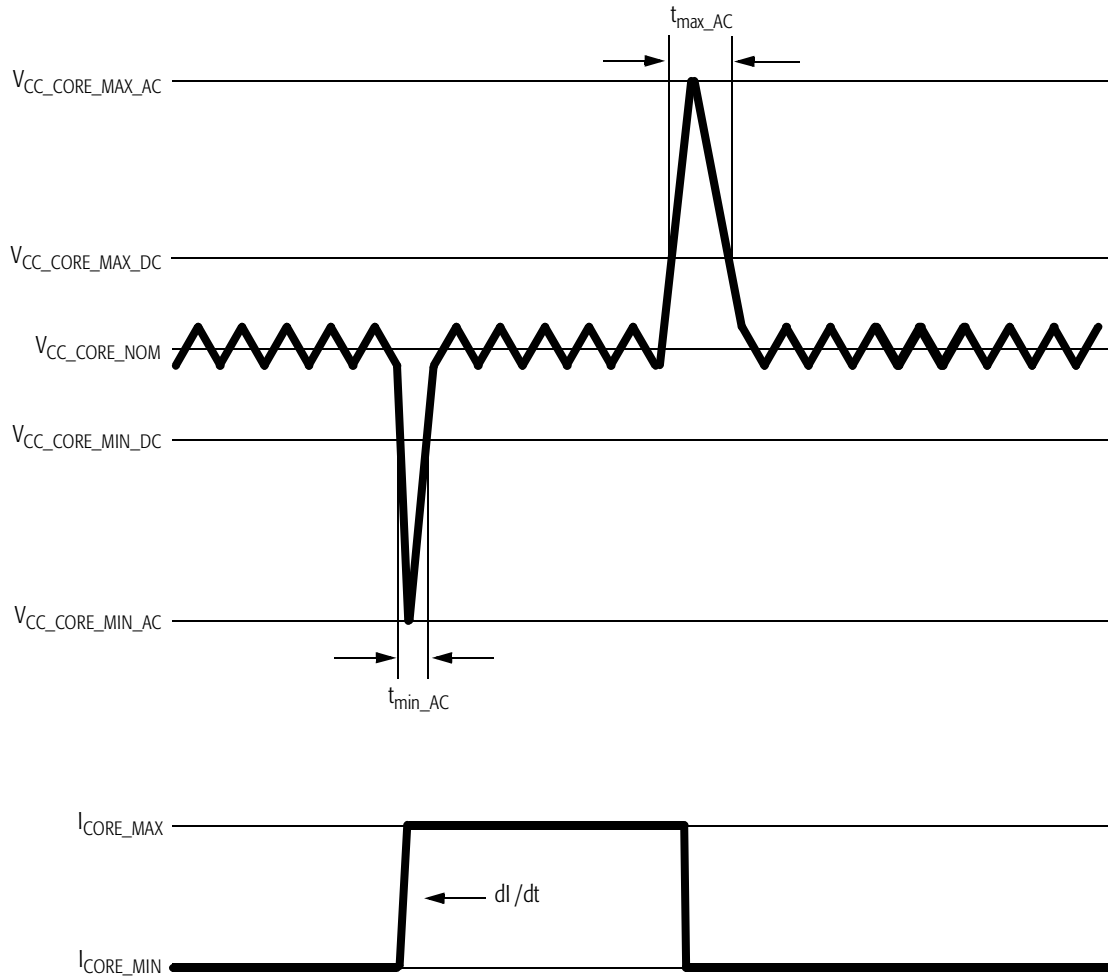


Figure 7. V_{CC_CORE} Voltage Waveform

7.8 Absolute Ratings

The AMD Athlon MP processor should not be subjected to conditions exceeding the absolute ratings, as such conditions can adversely affect long-term reliability or result in functional damage.

Table 7 lists the maximum absolute ratings of operation for the AMD Athlon MP processor.

Table 7. Absolute Ratings

Parameter	Description	Min	Max
VCC_CORE	AMD Athlon™ MP Processor core supply	–0.5 V	VCC_CORE Max + 0.5 V
VCCA	AMD Athlon MP Processor PLL supply	–0.5 V	VCCA Max + 0.5 V
V _{PIN}	Voltage on any signal pin	–0.5 V	VCC_CORE Max + 0.5 V
T _{STORAGE}	Storage temperature of processor	–40° C	100° C

7.9 VCC_CORE Voltage and Current

Table 8 shows the power and current for the AMD Athlon MP processor during normal and reduced power states.

Table 8. VCC_CORE Voltage and Current

Model Number	Frequency (MHz)	Nominal Voltage	Stop Grant (Maximum)	Maximum I _{CC} (Power Supply Current) ¹	Die Temperature
1500+	1333	1.75 V	5 W	34.3 A	95°C
1600+	1400			35.9 A	
1800+	1533			37.7 A	
Note: 1. Measured at the nominal voltage.					

7.10 SYSCLK and SYSCLK# AC and DC Characteristics

Table 9 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together.

Table 9. SYSCLK and SYSCLK# DC Characteristics

Symbol	Description	Min	Max	Units
$V_{\text{Threshold-DC}}$	Crossing before transition is detected (DC)	400		mV
$V_{\text{Threshold-AC}}$	Crossing before transition is detected (AC)	450		mV
$I_{\text{LEAK_P}}$	Leakage current through P-channel pullup to VCC_CORE	-1		mA
$I_{\text{LEAK_N}}$	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
V_{CROSS}	Differential signal crossover		$V_{\text{CC_CORE}}/2 \pm 100$	mV
C_{PIN}	Capacitance*	4	12*	pF

Note:
 * The following processor inputs have twice the listed capacitance because they connect to two input pads—SYSCLK and SYSCLK#. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#.

Figure 8 shows the DC characteristics of the SYSCLK and SYSCLK# signals.

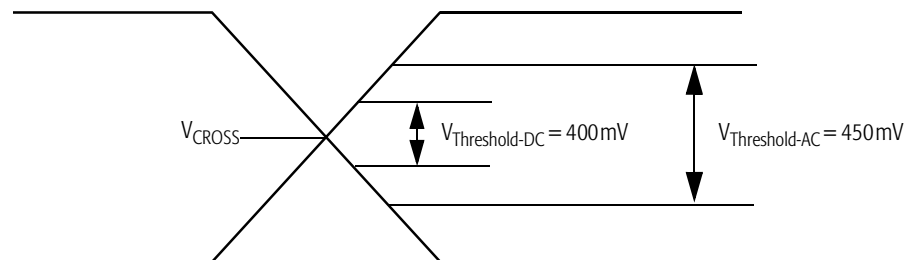


Figure 8. SYSCLK and SYSCLK# Differential Clock Signals

Table 10 shows the SYSCLK/SYSCLK# differential clock AC characteristics of the AMD Athlon MP processor.

Table 10. SYSCLK and SYSCLK# AC Characteristics

Symbol	Parameter Description	Minimum	Maximum	Units	Notes
	Clock Frequency	133	133	MHz	3
	Duty Cycle	30%	70%		
t_1	Period	7.5		ns	1, 2
t_2	High Time	1.05		ns	
t_3	Low Time	1.05		ns	
t_4	Fall Time		2	ps	
t_5	Rise Time		2	ps	
	Period Stability		± 300	ps	
Notes: <ol style="list-style-type: none"> 1. Circuitry driving the AMD Athlon™ system bus clock inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The -20dB attenuation point, as measured into a 10- or 20-pF load must be less than 500 KHz. 2. Circuitry driving the AMD Athlon system bus clock inputs may purposely alter the AMD Athlon system bus clock period (spread spectrum clock generators). In no cases can the AMD Athlon system bus period violate the minimum specification above. AMD Athlon system bus clock inputs can vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 KHz. 3. Minimum Clock Frequency is 50 MHz. 					

Figure 9 on page 32 shows a sample waveform of the SYSCLK signal.

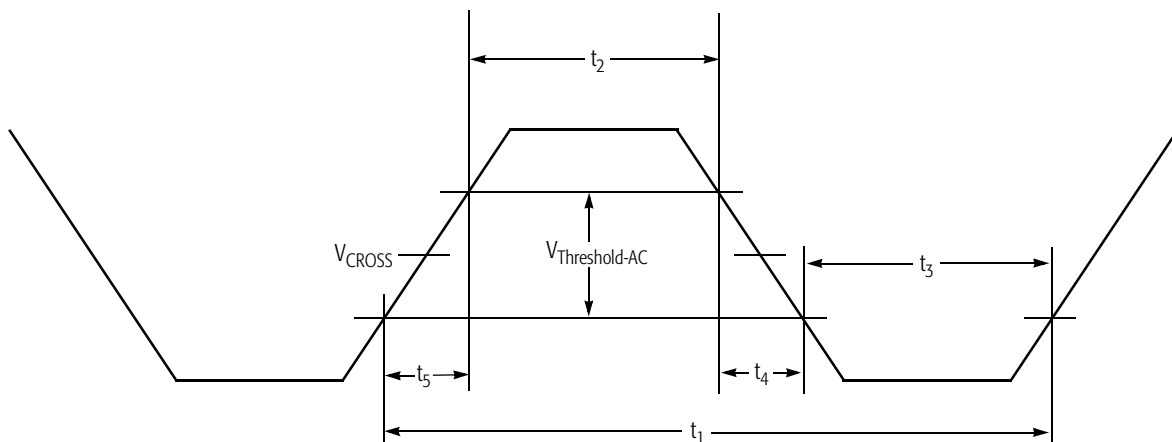


Figure 9. SYSCLK Waveform

7.11 AMD Athlon™ System Bus AC and DC Characteristics

Table 11 shows the DC characteristics of the AMD Athlon system bus used by the AMD Athlon MP processor. See Table 6, “VCC_CORE Characteristics,” on page 28 for information on T_{DIE} and VCC_CORE. For information about SYSCLK and SYSCLK#, see “SYSCLK and SYSCLK#” on page 69 and Table 18, “Pin Name Abbreviations,” on page 50.

Table 11. AMD Athlon™ System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		$(0.5 \cdot VCC_CORE) - 50$	$(0.5 \cdot VCC_CORE) + 50$	mV	1
$I_{VREF_LEAK_P}$	V_{REF} Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	-100		μA	
$I_{VREF_LEAK_N}$	V_{REF} Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		100	μA	
V_{IH}	Input High Voltage		$V_{REF} + 200$	$VCC_CORE + 500$	mV	
V_{IL}	Input Low Voltage		-500	$V_{REF} - 200$	mV	
V_{OH}	Output High Voltage	$I_{OUT} = -200 \mu A$	$0.85 VCC_CORE$	$VCC_CORE + 500$	mV	2
V_{OL}	Output Low Voltage	$I_{OUT} = 1 \text{ mA}$	-500	400	mV	2
I_{LEAK_P}	Tristate Leakage Pullup	$V_{IN} = VSS$ (Ground)	-1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	$V_{IN} = VCC_CORE$ Nominal		1	mA	
C_{IN}	Input Pin Capacitance		4	12	pF	

Notes:

- V_{REF} is nominally set to 50% of VCC_CORE with actual values that are specific to motherboard design implementation. V_{REF} must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the $\pm 50 \text{ mV}$ specification listed above.
- Specified at the T_{DIE} and VCC_CORE specifications in this document.

The AC characteristics of the AMD Athlon system bus are shown in Table 12 on page 34. The parameters are grouped based on the source or destination of the signals involved.

Table 12. AMD Athlon™ System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770	ps	2
	T_{SU}	Input Data Setup Time	300		ps	3
	T_{HD}	Input Data Hold Time	300		ps	3
	C_{IN}	Capacitance on input Clocks	4	12	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync	T_{VAL}	RSTCLK to Output Valid	250	2000	ps	4, 5
	T_{SU}	Setup to RSTCLK	500		ps	4, 6
	T_{HD}	Hold from RSTCLK	1000		ps	4, 6

Notes:

1. Rise and fall time ranges are guidelines over which the I/O has been characterized.
2. $T_{SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.
 $T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.
4. The synchronous signals include PROC RDY, CONNECT, and CLK FWD RST.
5. T_{VAL} is RSTCLK rising edge to output valid for PROC RDY. Test Load is 25 pF.
6. T_{SU} is setup of CONNECT/CLK FWD RST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLK FWD RST from rising edge of RSTCLK.

7.12 General AC and DC Characteristics

Table 13 shows the AMD Athlon MP processor AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

Table 13. General AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V _{IH}	Input High Voltage		(VCC_CORE/2) + 200 mV	VCC_CORE + 300 mV	V	1, 2
V _{IL}	Input Low Voltage		–300	350	mV	1, 2
V _{OH}	Output High Voltage		VCC_CORE – 400	VCC_CORE + 300	mV	
V _{OL}	Output Low Voltage		–300	400	mV	
I _{LEAK_P}	Tristate Leakage Pullup	V _{IN} = VSS (Ground)	–1		mA	
I _{LEAK_N}	Tristate Leakage Pulldown	V _{IN} = VCC_CORE Nominal		600	μA	
I _{OH}	Output High Current			–16	mA	3
I _{OL}	Output Low Current		16		mA	3
T _{SU}	Sync Input Setup Time		2.0		ns	4, 5
T _{HD}	Sync Input Hold Time		0.0		ps	4, 5
T _{DELAY}	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T _{BIT}	Input Time to Acquire		20.0		ns	7, 8
T _{RPT}	Input Time to Reacquire		40.0		ns	9–13

Notes:

1. Characterized across DC supply voltage range.
2. Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE minimum and VCC_CORE maximum.
3. I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.
4. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.
5. These are aggregate numbers.
6. Edge rates indicate the range over which inputs were characterized.
7. In asynchronous operation, the signal must persist for this time to enable capture.
8. This value assumes RSTCLK period is 10 ns \Rightarrow T_{BIT} = 2*f_{RST}.
9. The approximate value for standard case in normal mode operation.
10. This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.
11. Reassertions of the signal within this time are not guaranteed to be seen by the core.
12. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
13. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.

Table 13. General AC and DC Characteristics (Continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T _{RISE}	Signal Rise Time		1.0	3.0	V/ns	6
T _{FALL}	Signal Fall Time		1.0	3.0	V/ns	6
C _{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. Characterized across DC supply voltage range.
2. Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE minimum and VCC_CORE maximum.
3. I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.
4. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.
5. These are aggregate numbers.
6. Edge rates indicate the range over which inputs were characterized.
7. In asynchronous operation, the signal must persist for this time to enable capture.
8. This value assumes RSTCLK period is 10 ns \Rightarrow TBIT = 2*fRST.
9. The approximate value for standard case in normal mode operation.
10. This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.
11. Reassertions of the signal within this time are not guaranteed to be seen by the core.
12. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
13. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.

7.13 Thermal Diode Characteristics

Table 14 shows the AMD Athlon MP processor characteristics of the on-board thermal diode.

Table 14. Thermal Diode Characteristics

Symbol	Parameter Description	Min	Nom	Max	Units	Notes
I_{fw}	Forward bias current	5		300	μA	1
n	Diode ideality factor	1.002	1.008	1.016		2, 3, 4, 5

Notes:

1. The sourcing current should always be used in forward bias only.
2. Characterized at 95°C with a forward bias current pair of 10 μA and 100 μA .
3. Not 100% tested. Specified by design and limited characterization.
4. The diode ideality factor, n , is a correction factor to the ideal diode equation.

For the following equations, use the following variables and constants:

n	Diode ideality factor
k	Boltzmann constant
q	Electron charge constant
T	Diode temperature (Kelvin)
V_{BE}	Voltage from base to emitter
I_C	Collector current
I_S	Saturation current
N	Ratio of collector currents

The equation for V_{BE} is:

$$V_{BE} = \frac{nkT}{q} \cdot \ln\left(\frac{I_C}{I_S}\right)$$

By sourcing two currents and using the above equation, a difference in base emitter voltage can be found that leads to the following equation for temperature:

$$T = \frac{\Delta V_{BE}}{n \cdot \ln(N) \cdot \frac{k}{q}}$$

5. If a different sourcing current pair is used other than 10 μA and 100 μA , the following equation should be used to correct the temperature. Subtract this offset from the temperature measured by the temperature sensor.

For the following equations, use the following variables and constants:

I_{high}	High sourcing current
I_{low}	Low sourcing current

T_{offset} (in °C) can be found using the following equation:

$$T_{offset} = (6.0 \cdot 10^4) \cdot \frac{(I_{high} - I_{low})}{\ln\left(\frac{I_{high}}{I_{low}}\right)} - 2.34$$

7.14 APIC Pins AC and DC Characteristics

Table 15 shows the AMD Athlon MP processor AC and DC characteristics of the APIC pins.

Table 15. APIC Pin AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		1.7	2.625	V	1, 3
V_{IL}	Input Low Voltage		–300	700	mV	1, 2
V_{OH}	Output High Voltage			2.625	V	3
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	$V_{IN} = V_{SS}$ (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	$V_{IN} = 2.5\text{ V}$		1	mA	
I_{OL}	Output Low Current	V_{OL} Max	12		mA	
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	4
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	4
C_{PIN}	Pin Capacitance		4	12	pF	
Notes: <ol style="list-style-type: none"> 1. Characterized across DC supply voltage range 2. 2.625 V = 2.5 V + 5% maximum 3. Edge rates indicate the range over which inputs were characterized 						

8 Signal and Power-Up Requirements

This chapter describes the AMD Athlon™ MP processor power-up requirements during system power-up and warm resets.

8.1 Power-Up Requirements

Signal Sequence and Timing Description

Figure 10 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

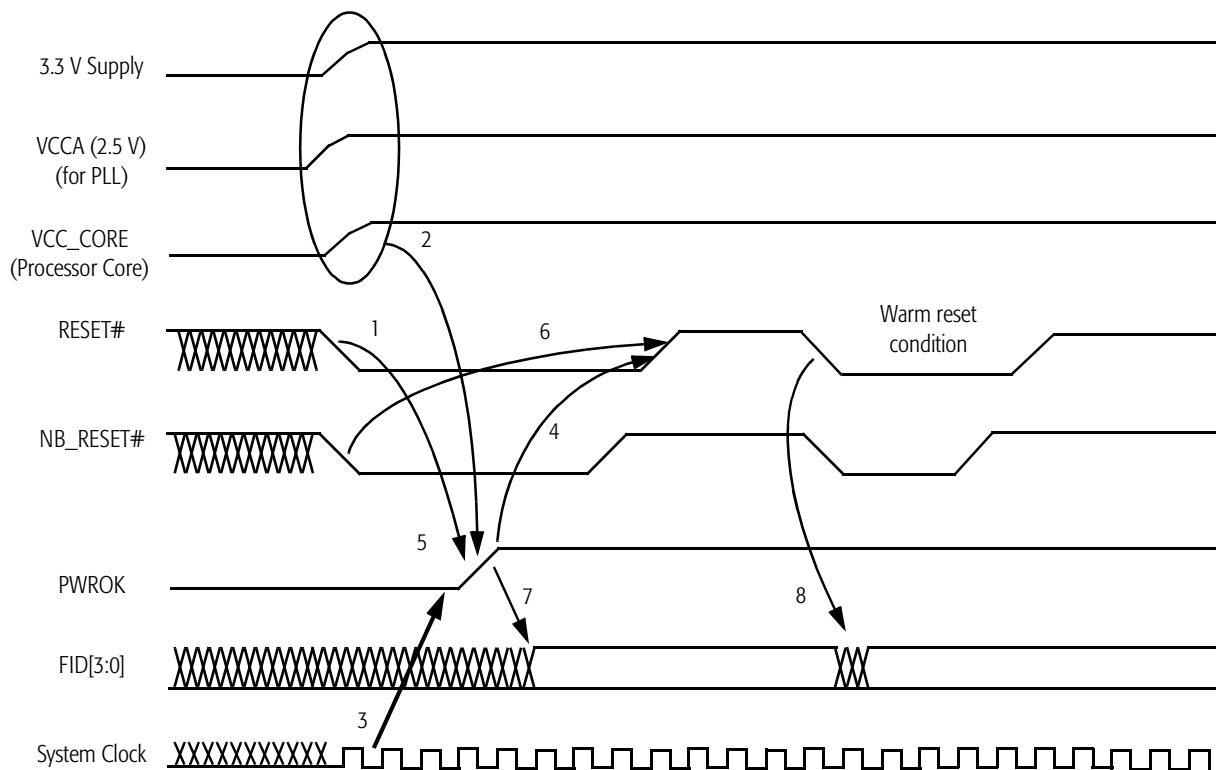


Figure 10. Signal Relationship Requirements During Power-Up Sequence

- Note:**
1. Figure 10 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.
 2. Requirements 1–8 in Figure 10 are described in “Power-Up Timing Requirements.” on page 40.

Power-Up Timing Requirements. The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted.
The AMD Athlon MP processor does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 nanoseconds** prior to the assertion of PWROK. In practice, Southbridges will assert RESET# milliseconds before PWROK is deasserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that VCC_CORE and all other voltage planes in the system are within specification.

The motherboard is required to delay PWROK assertion for a minimum of three milliseconds from the 3.3 V supply being within specification. This ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

The processor core voltage, VCC_CORE, must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the AMD Athlon MP processor is clocked by a ring oscillator.

The processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within specification at least five microseconds before PWROK is asserted.

In practice VCCA, VCC_CORE, and all other voltage planes must be within specification for several milliseconds before PWROK is asserted.

After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running before PWROK is asserted.

When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system

clock must be valid at this time. The system clocks are designed to be running after 3.3 V has been within specification for three milliseconds.

4. PWROK assertion to deassertion of RESET#

The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1 ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0 milliseconds**. Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# deassertion.

5. PWROK must be monotonic and meet the timing requirements as defined in Table 13, “General AC and DC Characteristics,” on page 35. The processor should not switch between the rising oscillator and the PLL after the initial assertion of PWROK.

6. NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

If NB_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP transfer. There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

7. The FID[3:0] signals are valid after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

8. The FID[3:0] signals become valid 10 system clocks after RESET# is asserted. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

Clock Multiplier Selection (FID[3:0])

The chipset samples the FID[3:0] signals in a chipset-specific manner from the processor and uses this information to determine the correct Serial Initialization Packet (SIP). The chipset then sends the SIP information to the processor for configuration of the AMD Athlon system bus for the clock multiplier that determines the processor frequency indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWRST signals, that are synchronous to SYSCLK.

For more information, see “FID[3:0] Pins” on page 65.

Serial Initialization Packet (SIP) Protocol. Refer to *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol.

8.2 Processor Warm Reset Requirements

Northbridge Reset Pins

RESET# cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same as PCI RESET#. The minimum assertion for PCI RESET# is one millisecond. Southbridges enforce a minimum assertion of RESET# for the processor, Northbridge, and PCI of 1.5 to 2.0 milliseconds.

9 Mechanical Data

9.1 Introduction

The AMD Athlon™ MP processor connects to the motherboard through a Pin Grid Array (PGA) socket named Socket A. This processor utilizes the Organic Pin Grid Array (OPGA) package type, described in “OPGA Package Description” on page 44. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

9.2 Die Loading

The processor die on OPGA packages is exposed at the top of the package. This feature facilitates heat transfer from the die to an approved heat sink. Any heat sink design should avoid loads on corners and edges of die. The OPGA package has compliant pads that serve to bring surfaces in planar contact. Tool-assisted zero insertion force sockets should be designed so that no load is placed on the substrate of the package.

Table 16 shows the mechanical loading specifications for the processor die. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 16.

Table 16. Mechanical Loading for the OPGA Package

Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	1
Die Edge	10	10	lbf	2
Notes: 1. Load specified for coplanar contact to die surface. 2. Load defined for a surface at no more than a two degree angle of inclination to die surface.				

9.3 OPGA Package Description

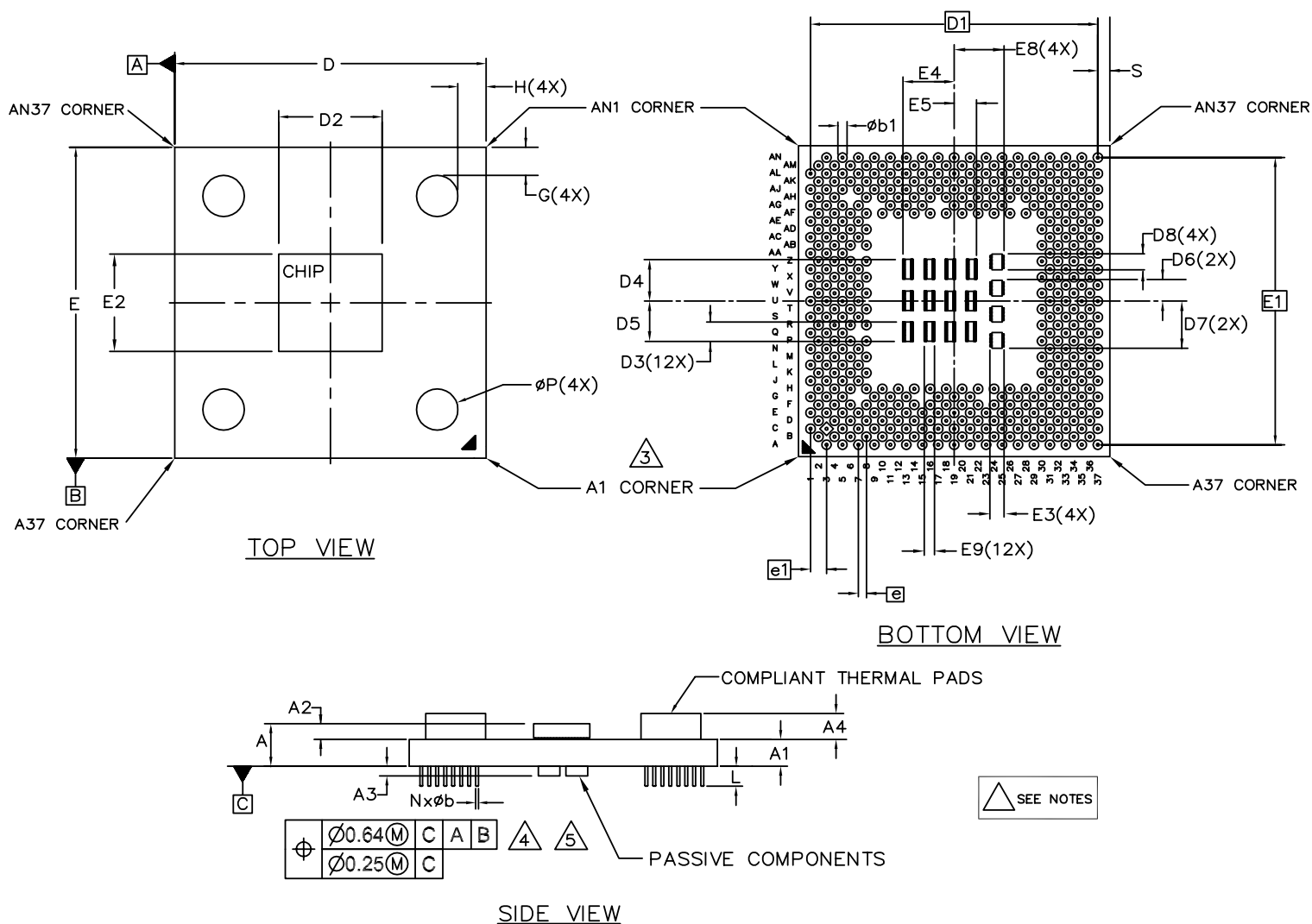
Figure 11 on page 45 shows a diagram and notes for the AMD Athlon MP processor OPGA package. Table 17 provides the dimensions in millimeters assigned to the letters and symbols shown in the Figure 11 diagram.

Table 17. Dimensions for the AMD Athlon™ MP Processor OPGA Package

Letter or Symbol	Minimum Dimension ¹	Maximum Dimension ¹	Letter or Symbol	Minimum Dimension ¹	Maximum Dimension ¹
D/E	49.27	49.78	G/H	–	4.50
D1/E1	45.72 BSC		A	1.942 REF	
D2	11.698 REF		A1	1.00	1.20
D3	3.30	3.60	A2	0.80	0.88
D4	6.40	6.95	A3	0.116	–
D5	6.40	6.95	A4	–	1.90
D6	3.35	3.90	φP	–	6.60
D7	7.48	8.03	φb	0.43	0.50
D8	3.05	3.35	φb1	1.40 REF	
E2	11.01 REF		S	1.435	2.375
E3	2.35	2.65	L	3.05	3.31
E4	7.90	8.45	M	37	
E5	3.29	3.84	N	453	
E8	7.94	8.49	e	1.27 BSC	
E9	1.66	1.96	e1	2.54 BSC	

Note:

1. Dimensions are given in millimeters.



GENERAL NOTES:

1. All dimensions are specified in millimeter (mm).
2. Dimensioning and tolerancing per ASME—Y14.5M—1994.
3. This corner is marked with a triangle on both sides of the package to identify the pin A1 corner for orientation purposes.
4. Pin tips should have radius.
5. Symbol "M" determines pin matrix size and "N" is number of pins.
6. For staggered pin configuration, pins on the same row are on a 2.54 mm grid. Adjacent rows offset by 1.27 mm.

Figure 11. AMD Athlon™ MP Processor OPGA Package

10 Pin Descriptions

10.1 Pin Diagram and Pin Name Abbreviations

Figure 12 on page 48 shows the staggered Pin Grid Array (PGA) for the AMD Athlon™ MP processor. Because some of the pin names are too long to fit in the grid, they are abbreviated. Figure 13 on page 49 shows the bottomside view of the array. Table 18 on page 50 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37						
A			SA0#12		SA0#5		SA0#3	SA0#55	VSS		SA0#61	SA0#53	VSS	SA0#3	VCC	SA0#62	SA0#7	SA0#57	SA0#59	SA0#35	SA0#34		SA0#47		VSS		VCC		SA0#43		SA0#45		SA0#42		SA0#41		SA0#30	A	SA0#30				
B		VSS		VCC		VSS				VSS		VCC		VSS		VCC		VSS		VCC			VCC		VCC		VSS				VSS												
C	SA0#7		SA0#9		SA0#6		SA0#2		SA0#54		SA0#3		SA0#6		SA0#51		SA0#60	SA0#9	SA0#59	SA0#56	SA0#57		SA0#47		SA0#38		SA0#38		SA0#43		SA0#45		SA0#42		SA0#41		SA0#30	C	SA0#30				
D		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		VCC		VSS		VCC		VSS		VSS		VSS		VSS			D	SA0#30			
E	SA0#11		SA0#6		SA0#4		SA0#6		SA0#52		SA0#50		SA0#49		SA0#36		SA0#48	SA0#58	SA0#58	SA0#36	SA0#46		SA0#44		SA0#42		SA0#42		SA0#32		SA0#33		SA0#31		SA0#30		SA0#22	E	SA0#22				
F		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		VCC		VSS		VCC		NC		NC		SA0#23		VCC			F	SA0#22			
G	SA0#10		SA0#14		SA0#13		KEY				NC		NC		KEY		KEY	NC	NC	NC	KEY		KEY		KEY		NC		NC		NC		SA0#20		SA0#23				G	SA0#21			
H		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		NC		NC		VSS		VSS				H	SA0#21		
J	SA0#0		SA0#1		NC		VD[4]																						NC		NC		SA0#19		SA0#17				J	SA0#29			
K		VSS		VSS		VSS		NC																				VCC		NC		VCC		VCC		VCC			K	SA0#28			
L	VD[0]		VD[1]		VD[2]		VD[3]																						NC		NC		SA0#26		SA0#22					L	SA0#28		
M		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS				M	SA0#28		
N	PICLK		PICLK		PICLK		KEY																							NC		NC		SA0#25		SA0#27					N	SA0#18	
P		VSS		VSS		VSS		VSS																				VCC		VCC		VCC		VCC		VCC		VCC			P	SA0#16	
Q	TCK		TMS		VCC		KEY																							NC		NC		SA0#24		SA0#17					Q	SA0#16	
R		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		VSS			R	SA0#6	
S	SCINCK1		SCINCK		SCINCK2		THDA																							NC		NC		SA0#7		SA0#15					S	SA0#6	
T		VSS		VSS		VSS		VSS																				VCC		VCC		VCC		VCC		VCC		VCC			T	SA0#10	
U	TDI		TRST#		TD0		THDC																							NC		NC		SA0#5		SA0#4					U	SA0#10	
V		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		VSS			V	SA0#1	
W	FD[0]		FD[1]		VREF_S		NC																							NC		NC		SA0#0		SA0#2					W	SA0#1	
X		VSS		VSS		VSS		VSS																				VCC		VCC		VCC		VCC		VCC		VCC			X	SA0#1	
Y	FD[2]		FD[3]		NC		KEY																							NC		NC		SA0#1		SA0#3					Y	SA0#12	
Z		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		VSS			Z	SA0#12	
AA	DBRDY		DBRDY#		NC		KEY																							NC		NC		SA0#8		SA0#0					AA	SA0#13	
AB		VSS		VSS		VSS		VSS																				VCC		VCC		VCC		VCC		VCC		VCC			AB	SA0#11	
AC	STPC#		PLTST#		ZN		NC																							NC		NC		SA0#10		SA0#14					AC	SA0#11	
AD		VCC		VCC		VCC		NC																						NC		NC		VSS		VSS		VSS			AD	SA0#11	
AE	A20M#		PWR0K		2P		NC																								NC		NC		SA0#5		SA0#0#0					AE	SA0#9
AF		VSS		VSS		NC		NC																						NC		NC		VCC		VCC		VCC			AF	SA0#9	
AG	FERR		RESET#		NC		KEY		KEY																					NC		NC		SA0#2		SA0#11					AG	SA0#7	
AH		VCC		VCC		AMD																								NC		NC		VSS		VSS		VSS			AH	SA0#7	
AJ	IGAME#		INT#		VCC		NC		NC																									SA0#0		SA0#6					AJ	SA0#3	
AK		VSS		VSS		CPW		NC																					VCC		VCC		VCC		VCC		VCC		VCC			AK	SA0#3
AL	INTR		FLUSH#		VCC		NC		NC																									SA0#8		SA0#4					AL	SA0#10	
AM		VCC		VSS		VSS		NC																							VCC		VCC		SA0#9		SA0#4					AM	SA0#9
AN			NMI		SM#		NC		NC																									SA0#14		SA0#13					AN	SA0#9	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37						

AMD Athlon™ MP Processor

Topside View

AMD Athlon™ MP Processor Topside View

Figure 12. AMD Athlon™ MP Processor Pin Diagram – Topside View

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN						
1			SA0P7		SA0P11		SA0P10			SA0P0		WDI[0]			PKCLK	TK		SA0C0		TDI		FDI[0]		FDI[2]		DBRDY		STPC#		AZ0M#		FERR		IGNIE#		INTR			1					
2		VSS		VCC		VSS		VCC			VSS		VCC		VSS		VCC		VSS		TRST#		FDI[1]		FDI[3]		DBREQ#				PWROK		RESET#		INIT#		FLUSH#		NMI	3				
3	SA0P12	SA0P9			SA0C#		SA0P4		VCC		SA0P1		WDI[1]		PKCH0	TMS		SA0M#																					4					
4		VCC		VCC		VSS		VCC			VSS		WDI[2]		PKCH1	SA0C#		SA0P13		TDI		VCC		NC		NC		Z#		ZP		NC		VCC		VCC		SA0P#	5					
5	SA0P5	SA0P8			SA0P4					NC		WDI[3]				SA0C#		SA0C2		TDI		VCC		VSS		VCC		VSS				NC		AMD		CPH#		VSS		6				
6		VSS		VSS		VSS		NC			VSS					VSS		TH0A		TH0C		NC		KEY		KEY					NC		KEY		NC		NC		NC	7				
7	SA0P3	SA0P2			SA0P6		KEY					WDI[4]			KEY		KEY																						8					
8		VCC		VCC		NC		NC			NC					VSS		VCC				VCC		VSS		VCC													9					
9	SA0P55	SA0P54			SA0P22		KEY																																	10				
10		VSS		VSS		VSS		NC																																11				
11	SA0P61	SA0C#3			SA0P30		NC																																	12				
12		VCC		VCC		VCC		VCC																																13				
13	SA0P53	SA0P46			SA0P49		NC																																	14				
14		VSS		VSS		VSS		VSS																																	15			
15	SA0P63	SA0P51			SA0C#3		KEY																																	16				
16		VCC		VCC		VCC		VCC																																	17			
17	SA0P62	SA0P60			SA0P48		KEY																																		18			
18		VSS		VSS		VSS		VSS																																	19			
19	SA0P67	SA0P59			SA0P38		NC																																		20			
20		VCC		VCC		VCC		VCC																																	21			
21	SA0P57	SA0P56			SA0P36		NC																																		22			
22		VSS		VSS		VSS		VSS																																		23		
23	SA0P59	SA0P37			SA0P46		KEY																																		24			
24		VCC		VCC		VCC		VCC																																		25		
25	SA0P35	SA0P47			SA0P44		KEY																																			26		
26		VSS		VSS		VSS		VSS																																		27		
27	SA0P34	SA0P38			SA0C#2		NC																																			28		
28		VCC		VCC		VCC		VCC																																		29		
29	SA0P44	SA0P45			SA0P33		NC																																			30		
30		VSS		VSS		VSS		NC																																		31		
31	SA0P5	SA0P43			SA0P22		NC																																				32	
32		VCC		VCC		VCC		NC																																			33	
33	SA0C#2	SA0P42			SA0P43		SA0P20																																					34
34		VSS		VSS		VCC		VSS																																				35
35	SA0P40	SA0P41			SA0P31		SA0P23																																					36
36		VCC		VSS		VCC		VSS																																				37
37	SA0P30	SA0C#1			SA0P22		SA0P21																																					

AMD Athlon™ MP Processor
Bottomside View

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AMD Athlon™ MP Processor Bottomside View

Figure 13. AMD Athlon™ MP Processor Pin Diagram – Bottomside View

Table 18. Pin Name Abbreviations

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	A20M#	AE1		NC	F8
	AMD	AH6		NC	F30
ANLOG	ANALOG	AJ13		NC	G11
CLKFR	CLKFWRST	AJ21		NC	G13
	CLKIN	AN17		NC	G19
	CLKIN#	AL17		NC	G21
CNNCT	CONNECT	AL23		NC	G27
	COREFB	AG11		NC	G29
	COREFB#	AG13		NC	G31
CPR#	CPU_PRESENCE#	AK6		NC	H6
	DBRDY	AA1		NC	H8
	DBREQ#	AA3		NC	H10
	FERR	AG1		NC	H28
	FID[0]	W1		NC	H30
	FID[1]	W3		NC	H32
	FID[2]	Y1		NC	J5
	FID[3]	Y3		NC	J31
	FLUSH#	AL3		NC	K8
	IGNNE#	AJ1		NC	K30
	INIT#	AJ3		NC	L31
	INTR	AL1		NC	N31
K7CO	K7CLKOUT	AL21		NC	Q31
K7CO#	K7CLKOUT#	AN21		NC	S31
	KEY	G7		NC	U31
	KEY	G9		NC	W7
	KEY	G15		NC	W31
	KEY	G17		NC	Y5
	KEY	G23		NC	Y31
	KEY	G25		NC	AA5
	KEY	N7		NC	AA31
	KEY	Q7		NC	AC7
	KEY	Y7		NC	AC31
	KEY	AA7		NC	AD8
	KEY	AG7		NC	AD30
	KEY	AG9		NC	AE7
	KEY	AG15		NC	AE31
	KEY	AG17		NC	AF6
	KEY	AG27		NC	AF8
	KEY	AG29		NC	AF10

Table 18. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AF28	PLTST#	PLLTEST#	AC3
	NC	AF30	PRCRDY	PROCREADY	AN23
	NC	AF32		PWROK	AE3
	NC	AG5		RESET#	AG3
	NC	AG19	RCLK	RSTCLK	AN19
	NC	AG21	RCLK#	RSTCLK#	AL19
	NC	AG23	SAI#0	SADDIN[0]#	AJ29
	NC	AG25	SAI#1	SADDIN[1]#	AL29
	NC	AG31	SAI#2	SADDIN[2]#	AG33
	NC	AH8	SAI#3	SADDIN[3]#	AJ37
	NC	AH30	SAI#4	SADDIN[4]#	AL35
	NC	AJ7	SAI#5	SADDIN[5]#	AE33
	NC	AJ9	SAI#6	SADDIN[6]#	AJ35
	NC	AJ11	SAI#7	SADDIN[7]#	AG37
	NC	AJ15	SAI#8	SADDIN[8]#	AL33
	NC	AJ17	SAI#9	SADDIN[9]#	AN37
	NC	AJ19	SAI#10	SADDIN[10]#	AL37
	NC	AJ27	SAI#11	SADDIN[11]#	AG35
	NC	AK8	SAI#12	SADDIN[12]#	AN29
	NC	AL7	SAI#13	SADDIN[13]#	AN35
	NC	AL9	SAI#14	SADDIN[14]#	AN31
	NC	AL11	SAIC#	SADDINCLK#	AJ33
	NC	AL25	SAO#0	SADDOUT[0]#	J1
	NC	AL27	SAO#1	SADDOUT[1]#	J3
	NC	AM8	SAO#2	SADDOUT[2]#	C7
	NC	AN7	SAO#3	SADDOUT[3]#	A7
	NC	AN9	SAO#4	SADDOUT[4]#	E5
	NC	AN11	SAO#5	SADDOUT[5]#	A5
	NC	AN25	SAO#6	SADDOUT[6]#	E7
	NC	AN27	SAO#7	SADDOUT[7]#	C1
	NMI	AN3	SAO#8	SADDOUT[8]#	C5
	PICCLK	N1	SAO#9	SADDOUT[9]#	C3
PICD#0	PICD[0]#	N3	SAO#10	SADDOUT[10]#	G1
PICD#1	PICD[1]#	N5	SAO#11	SADDOUT[11]#	E1
PLBYP#	PLLBYPASS#	AJ25	SAO#12	SADDOUT[12]#	A3
PLBYC	PLLBYPASSCLK	AN15	SAO#13	SADDOUT[13]#	G5
PLBYC#	PLLBYPASSCLK#	AL15	SAO#14	SADDOUT[14]#	G3
PLMN1	PLLMON1	AN13	SAOC#	SADDOUTCLK#	E3
PLMN2	PLLMON2	AL13	SCNCK1	SCANCLK1	S1

Table 18. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SCNCK2	SCANCLK2	S5	SD#28	SDATA[28]#	L37
SCNINV	SCANINTEVAL	S3	SD#29	SDATA[29]#	J37
SCNSN	SCANSHIFTEN	Q5	SD#30	SDATA[30]#	A37
SCK#0	SCHECK[0]#	U37	SD#31	SDATA[31]#	E35
SCK#1	SCHECK[1]#	Y33	SD#32	SDATA[32]#	E31
SCK#2	SCHECK[2]#	L35	SD#33	SDATA[33]#	E29
SCK#3	SCHECK[3]#	E33	SD#34	SDATA[34]#	A27
SCK#4	SCHECK[4]#	E25	SD#35	SDATA[35]#	A25
SCK#5	SCHECK[5]#	A31	SD#36	SDATA[36]#	E21
SCK#6	SCHECK[6]#	C13	SD#37	SDATA[37]#	C23
SCK#7	SCHECK[7]#	A19	SD#38	SDATA[38]#	C27
SD#0	SDATA[0]#	AA35	SD#39	SDATA[39]#	A23
SD#1	SDATA[1]#	W37	SD#40	SDATA[40]#	A35
SD#2	SDATA[2]#	W35	SD#41	SDATA[41]#	C35
SD#3	SDATA[3]#	Y35	SD#42	SDATA[42]#	C33
SD#4	SDATA[4]#	U35	SD#43	SDATA[43]#	C31
SD#5	SDATA[5]#	U33	SD#44	SDATA[44]#	A29
SD#6	SDATA[6]#	S37	SD#45	SDATA[45]#	C29
SD#7	SDATA[7]#	S33	SD#46	SDATA[46]#	E23
SD#8	SDATA[8]#	AA33	SD#47	SDATA[47]#	C25
SD#9	SDATA[9]#	AE37	SD#48	SDATA[48]#	E17
SD#10	SDATA[10]#	AC33	SD#49	SDATA[49]#	E13
SD#11	SDATA[11]#	AC37	SD#50	SDATA[50]#	E11
SD#12	SDATA[12]#	Y37	SD#51	SDATA[51]#	C15
SD#13	SDATA[13]#	AA37	SD#52	SDATA[52]#	E9
SD#14	SDATA[14]#	AC35	SD#53	SDATA[53]#	A13
SD#15	SDATA[15]#	S35	SD#54	SDATA[54]#	C9
SD#16	SDATA[16]#	Q37	SD#55	SDATA[55]#	A9
SD#17	SDATA[17]#	Q35	SD#56	SDATA[56]#	C21
SD#18	SDATA[18]#	N37	SD#57	SDATA[57]#	A21
SD#19	SDATA[19]#	J33	SD#58	SDATA[58]#	E19
SD#20	SDATA[20]#	G33	SD#59	SDATA[59]#	C19
SD#21	SDATA[21]#	G37	SD#60	SDATA[60]#	C17
SD#22	SDATA[22]#	E37	SD#61	SDATA[61]#	A11
SD#23	SDATA[23]#	G35	SD#62	SDATA[62]#	A17
SD#24	SDATA[24]#	Q33	SD#63	SDATA[63]#	A15
SD#25	SDATA[25]#	N33	SDIC#0	SDATAINCLK[0]#	W33
SD#26	SDATA[26]#	L33	SDIC#1	SDATAINCLK[1]#	J35
SD#27	SDATA[27]#	N35	SDIC#2	SDATAINCLK[2]#	E27

Table 18. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SDIC#3	SDATAINCLK[3]#	E15	VCC	VCC_CORE	F28
SDINV#	SDATAINVALID#	AN33	VCC	VCC_CORE	F32
SDOC#0	SDATAOUTCLK[0]#	AE35	VCC	VCC_CORE	F34
SDOC#1	SDATAOUTCLK[1]#	C37	VCC	VCC_CORE	F36
SDOC#2	SDATAOUTCLK[2]#	A33	VCC	VCC_CORE	H2
SDOC#3	SDATAOUTCLK[3]#	C11	VCC	VCC_CORE	H4
SDOV#	SDATAOUTVALID#	AL31	VCC	VCC_CORE	H12
SFILLV#	SFILLVALID#	AJ31	VCC	VCC_CORE	H16
	SMI#	AN5	VCC	VCC_CORE	H20
STPC#	STPCLK#	AC1	VCC	VCC_CORE	H24
	TCK	Q1	VCC	VCC_CORE	K32
	TDI	U1	VCC	VCC_CORE	K34
	TDO	U5	VCC	VCC_CORE	K36
THDA	THERMDA	S7	VCC	VCC_CORE	M2
THDC	THERMDC	U7	VCC	VCC_CORE	M4
	TMS	Q3	VCC	VCC_CORE	M6
	TRST#	U3	VCC	VCC_CORE	M8
VCC	VCC_CORE	B4	VCC	VCC_CORE	P30
VCC	VCC_CORE	B8	VCC	VCC_CORE	P32
VCC	VCC_CORE	B12	VCC	VCC_CORE	P34
VCC	VCC_CORE	B16	VCC	VCC_CORE	P36
VCC	VCC_CORE	B20	VCC	VCC_CORE	R2
VCC	VCC_CORE	B24	VCC	VCC_CORE	R4
VCC	VCC_CORE	B28	VCC	VCC_CORE	R6
VCC	VCC_CORE	B32	VCC	VCC_CORE	R8
VCC	VCC_CORE	B36	VCC	VCC_CORE	T30
VCC	VCC_CORE	D2	VCC	VCC_CORE	T32
VCC	VCC_CORE	D4	VCC	VCC_CORE	T34
VCC	VCC_CORE	D8	VCC	VCC_CORE	T36
VCC	VCC_CORE	D12	VCC	VCC_CORE	V2
VCC	VCC_CORE	D16	VCC	VCC_CORE	V4
VCC	VCC_CORE	D20	VCC	VCC_CORE	V6
VCC	VCC_CORE	D24	VCC	VCC_CORE	V8
VCC	VCC_CORE	D28	VCC	VCC_CORE	X30
VCC	VCC_CORE	D32	VCC	VCC_CORE	X32
VCC	VCC_CORE	F12	VCC	VCC_CORE	X34
VCC	VCC_CORE	F16	VCC	VCC_CORE	X36
VCC	VCC_CORE	F20	VCC	VCC_CORE	Z2
VCC	VCC_CORE	F24	VCC	VCC_CORE	Z4

Table 18. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
VCC	VCC_CORE	Z6	VCC	VCC_CORE	AM26
VCC	VCC_CORE	Z8	VCC	VCC_CORE	AM30
VCC	VCC_CORE	AB30	VCC	VCC_CORE	AM34
VCC	VCC_CORE	AB32		VCCA	AJ23
VCC	VCC_CORE	AB34		VID[0]	L1
VCC	VCC_CORE	AB36		VID[1]	L3
VCC	VCC_CORE	AD2		VID[2]	L5
VCC	VCC_CORE	AD4		VID[3]	L7
VCC	VCC_CORE	AD6		VID[4]	J7
VCC	VCC_CORE	AF14	VREF_S	VREF_SYS	W5
VCC	VCC_CORE	AF18		VSS	B2
VCC	VCC_CORE	AF22		VSS	B6
VCC	VCC_CORE	AF26		VSS	B10
VCC	VCC_CORE	AF34		VSS	B14
VCC	VCC_CORE	AF36		VSS	B18
VCC	VCC_CORE	AH2		VSS	B22
VCC	VCC_CORE	AH4		VSS	B26
VCC	VCC_CORE	AH10		VSS	B30
VCC	VCC_CORE	AH14		VSS	B34
VCC	VCC_CORE	AH18		VSS	D6
VCC	VCC_CORE	AH22		VSS	D10
VCC	VCC_CORE	AH26		VSS	D14
VCC	VCC_CORE	AK10		VSS	D18
VCC	VCC_CORE	AK14		VSS	D22
VCC	VCC_CORE	AK18		VSS	D26
VCC	VCC_CORE	AK22		VSS	D30
VCC	VCC_CORE	AK26		VSS	D34
VCC	VCC_CORE	AK30		VSS	D36
VCC	VCC_CORE	AK34		VSS	F2
VCC	VCC_CORE	AK36		VSS	F4
VCC	VCC_CORE	AJ5		VSS	F6
VCC	VCC_CORE	AL5		VSS	F10
VCC	VCC_CORE	AM2		VSS	F14
VCC	VCC_CORE	AM10		VSS	F18
VCC	VCC_CORE	AM14		VSS	F22
VCC	VCC_CORE	AM18		VSS	F26
VCC	VCC_CORE	AM22		VSS	H14
VCC	VCC_CORE	AM26		VSS	H18
VCC	VCC_CORE	AM22		VSS	H22

Table 18. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	VSS	H26		VSS	AD34
	VSS	H34		VSS	AD36
	VSS	H36		VSS	AF2
	VSS	K2		VSS	AF4
	VSS	K4		VSS	AF12
	VSS	K6		VSS	AF16
	VSS	M30		VSS	AH12
	VSS	M32		VSS	AH16
	VSS	M34		VSS	AH20
	VSS	M36		VSS	AH24
	VSS	P2		VSS	AH28
	VSS	P4		VSS	AH32
	VSS	P6		VSS	AH34
	VSS	P8		VSS	AH36
	VSS	R30		VSS	AK2
	VSS	R32		VSS	AK4
	VSS	R34		VSS	AK12
	VSS	R36		VSS	AK16
	VSS	T2		VSS	AK20
	VSS	T4		VSS	AK24
	VSS	T6		VSS	AK28
	VSS	T8		VSS	AK32
	VSS	V30		VSS	AM4
	VSS	V32		VSS	AM6
	VSS	V34		VSS	AM12
	VSS	V36		VSS	AM16
	VSS	X2		VSS	AM20
	VSS	X4		VSS	AM24
	VSS	X6		VSS	AM28
	VSS	X8		VSS	AM32
	VSS	Z30		VSS	AM36
	VSS	Z32		ZN	AC5
	VSS	Z34		ZP	AE5
	VSS	Z36			
	VSS	AB2			
	VSS	AB8			
	VSS	AB4			
	VSS	AB6			
	VSS	AD32			

10.2 Pin List

Table 19 cross-references Socket A pin location to signal name.

The “L” (Level) column shows the electrical specification for this pin. “P” indicates a push-pull mode driven by a single source. “O” indicates open-drain mode that allows devices to share the pin.

Note: The Socket A AMD Athlon MP processor supports push-pull drivers. For more information, see “Push–Pull (PP) Drivers” on page 6.

The “P” (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The “R” (Reference) column indicates if this signal should be referenced to VSS (G) or VCC_CORE (P) planes for the purpose of signal routing with respect to the current return paths.

Table 19. Cross-Reference by Pin Location

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
A1	No Pin	page 68	-	-	-	B2	VSS		-	-	-
A3	SADDOUT[12]#		P	O	G	B4	VCC_CORE		-	-	-
A5	SADDOUT[5]#		P	O	G	B6	VSS		-	-	-
A7	SADDOUT[3]#		P	O	G	B8	VCC_CORE		-	-	-
A9	SDATA[55]#		P	B	P	B10	VSS		-	-	-
A11	SDATA[61]#		P	B	P	B12	VCC_CORE		-	-	-
A13	SDATA[53]#		P	B	G	B14	VSS		-	-	-
A15	SDATA[63]#		P	B	G	B16	VCC_CORE		-	-	-
A17	SDATA[62]#		P	B	G	B18	VSS		-	-	-
A19	SCHECK[7]#	page 68	P	B	G	B20	VCC_CORE		-	-	-
A21	SDATA[57]#		P	B	G	B22	VSS		-	-	-
A23	SDATA[39]#		P	B	G	B24	VCC_CORE		-	-	-
A25	SDATA[35]#		P	B	P	B26	VSS		-	-	-
A27	SDATA[34]#		P	B	P	B28	VCC_CORE		-	-	-
A29	SDATA[44]#		P	B	G	B30	VSS		-	-	-
A31	SCHECK[5]#	page 68	P	B	G	B32	VCC_CORE		-	-	-
A33	SDATAOUTCLK[2]#		P	O	P	B34	VSS		-	-	-
A35	SDATA[40]#		P	B	G	B36	VCC_CORE		-	-	-
A37	SDATA[30]#		P	B	P	C1	SADDOUT[7]#		P	O	G

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
C3	SADDOUT[9]#		P	O	G	D34	VSS		-	-	-
C5	SADDOUT[8]#		P	O	G	D36	VSS		-	-	-
C7	SADDOUT[2]#		P	O	G	E1	SADDOUT[11]#		P	O	P
C9	SDATA[54]#		P	B	P	E3	SADDOUTCLK#		P	O	G
C11	SDATAOUTCLK[3]#		P	O	G	E5	SADDOUT[4]#		P	O	P
C13	SCHECK[6]#	page 68	P	B	G	E7	SADDOUT[6]#		P	O	G
C15	SDATA[51]#		P	B	P	E9	SDATA[52]#		P	B	P
C17	SDATA[60]#		P	B	G	E11	SDATA[50]#		P	B	P
C19	SDATA[59]#		P	B	G	E13	SDATA[49]#		P	B	G
C21	SDATA[56]#		P	B	G	E15	SDATAINCLK[3]#		P	I	G
C23	SDATA[37]#		P	B	P	E17	SDATA[48]#		P	B	P
C25	SDATA[47]#		P	B	G	E19	SDATA[58]#		P	B	G
C27	SDATA[38]#		P	B	G	E21	SDATA[36]#		P	B	P
C29	SDATA[45]#		P	B	G	E23	SDATA[46]#		P	B	P
C31	SDATA[43]#		P	B	G	E25	SCHECK[4]#	page 68	P	B	P
C33	SDATA[42]#		P	B	G	E27	SDATAINCLK[2]#		P	I	G
C35	SDATA[41]#		P	B	G	E29	SDATA[33]#		P	B	P
C37	SDATAOUTCLK[1]#		P	O	G	E31	SDATA[32]#		P	B	P
D2	VCC_CORE		-	-	-	E33	SCHECK[3]#	page 68	P	B	P
D4	VCC_CORE		-	-	-	E35	SDATA[31]#		P	B	P
D6	VSS		-	-	-	E37	SDATA[22]#		P	B	G
D8	VCC_CORE		-	-	-	F2	VSS		-	-	-
D10	VSS		-	-	-	F4	VSS		-	-	-
D12	VCC_CORE		-	-	-	F6	VSS		-	-	-
D14	VSS		-	-	-	F8	NC Pin	page 67	-	-	-
D16	VCC_CORE		-	-	-	F10	VSS		-	-	-
D18	VSS		-	-	-	F12	VCC_CORE		-	-	-
D20	VCC_CORE		-	-	-	F14	VSS		-	-	-
D22	VSS		-	-	-	F16	VCC_CORE		-	-	-
D24	VCC_CORE		-	-	-	F18	VSS		-	-	-
D26	VSS		-	-	-	F20	VCC_CORE		-	-	-
D28	VCC_CORE		-	-	-	F22	VSS		-	-	-
D30	VSS		-	-	-	F24	VCC_CORE		-	-	-
D32	VCC_CORE		-	-	-	F26	VSS		-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
F28	VCC_CORE		-	-	-	H22	VSS		-	-	-
F30	NC Pin	page 67	-	-	-	H24	VCC_CORE		-	-	-
F32	VCC_CORE		-	-	-	H26	VSS		-	-	-
F34	VCC_CORE		-	-	-	H28	NC Pin	page 67	-	-	-
F36	VCC_CORE		-	-	-	H30	NC Pin	page 67	-	-	-
G1	SADDOUT[10]#		P	O	P	H32	NC Pin	page 67	-	-	-
G3	SADDOUT[14]#		P	O	G	H34	VSS		-	-	-
G5	SADDOUT[13]#		P	O	G	H36	VSS		-	-	-
G7	Key Pin	page 67	-	-	-	J1	SADDOUT[0]#	page 68	P	O	-
G9	Key Pin	page 67	-	-	-	J3	SADDOUT[1]#	page 68	P	O	-
G11	NC Pin	page 67	-	-	-	J5	NC Pin	page 67	-	-	-
G13	NC Pin	page 67	-	-	-	J7	VID[4]	page 69	O	O	-
G15	Key Pin	page 67	-	-	-	J31	NC Pin	page 67	-	-	-
G17	Key Pin	page 67	-	-	-	J33	SDATA[19]#		P	B	G
G19	NC Pin	page 67	-	-	-	J35	SDATAINCLK[1]#		P	I	P
G21	NC Pin	page 67	-	-	-	J37	SDATA[29]#		P	B	P
G23	Key Pin	page 67	-	-	-	K2	VSS		-	-	-
G25	Key Pin	page 67	-	-	-	K4	VSS		-	-	-
G27	NC Pin	page 67	-	-	-	K6	VSS		-	-	-
G29	NC Pin	page 67	-	-	-	K8	NC Pin	page 67	-	-	-
G31	NC Pin	page 67	-	-	-	K30	NC Pin	page 67	-	-	-
G33	SDATA[20]#		P	B	G	K32	VCC_CORE		-	-	-
G35	SDATA[23]#		P	B	G	K34	VCC_CORE		-	-	-
G37	SDATA[21]#		P	B	G	K36	VCC_CORE		-	-	-
H2	VCC_CORE		-	-	-	L1	VID[0]	page 69	O	O	-
H4	VCC_CORE		-	-	-	L3	VID[1]	page 69	O	O	-
H6	NC Pin	page 67	-	-	-	L5	VID[2]	page 69	O	O	-
H8	NC Pin	page 67	-	-	-	L7	VID[3]	page 69	O	O	-
H10	NC Pin	page 67	-	-	-	L31	NC Pin	page 67	-	-	-
H12	VCC_CORE		-	-	-	L33	SDATA[26]#		P	B	P
H14	VSS		-	-	-	L35	SCHECK[2]#	page 68	P	B	G
H16	VCC_CORE		-	-	-	L37	SDATA[28]#		P	B	P
H18	VSS		-	-	-	M2	VCC_CORE		-	-	-
H20	VCC_CORE		-	-	-	M4	VCC_CORE		-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
M6	VCC_CORE		-	-	-	R30	VSS		-	-	-
M8	VCC_CORE		-	-	-	R32	VSS		-	-	-
M30	VSS		-	-	-	R34	VSS		-	-	-
M32	VSS		-	-	-	R36	VSS		-	-	-
M34	VSS		-	-	-	S1	SCANCLK1	page 68	P	I	-
M36	VSS		-	-	-	S3	SCANINTEVAL	page 68	P	I	-
N1	PICCLK	page 64	O	I	-	S5	SCANCLK2	page 68	P	I	-
N3	PICD#[0]	page 64	O	B	-	S7	THERMDA	page 69	-	-	-
N5	PICD#[1]	page 64	O	B	-	S31	NC Pin	page 67	-	-	-
N7	Key Pin	page 67	-	-	-	S33	SDATA[7]#		P	B	G
N31	NC Pin	page 67	-	-	-	S35	SDATA[15]#		P	B	P
N33	SDATA[25]#		P	B	P	S37	SDATA[6]#		P	B	G
N35	SDATA[27]#		P	B	P	T2	VSS		-	-	-
N37	SDATA[18]#		P	B	G	T4	VSS		-	-	-
P2	VSS		-	-	-	T6	VSS		-	-	-
P4	VSS		-	-	-	T8	VSS		-	-	-
P6	VSS		-	-	-	T30	VCC_CORE		-	-	-
P8	VSS		-	-	-	T32	VCC_CORE		-	-	-
P30	VCC_CORE		-	-	-	T34	VCC_CORE		-	-	-
P32	VCC_CORE		-	-	-	T36	VCC_CORE		-	-	-
P34	VCC_CORE		-	-	-	U1	TDI	page 67	P	I	-
P36	VCC_CORE		-	-	-	U3	TRST#	page 67	P	I	-
Q1	TCK	page 67	P	I	-	U5	TDO	page 67	P	O	-
Q3	TMS	page 67	P	I	-	U7	THERMDC	page 69	-	-	-
Q5	SCANSHIFTEN	page 68	P	I	-	U31	NC Pin	page 67	-	-	-
Q7	Key Pin	page 67	-	-	-	U33	SDATA[5]#		P	B	G
Q31	NC Pin	page 67	-	-	-	U35	SDATA[4]#		P	B	G
Q33	SDATA[24]#		P	B	P	U37	SCHECK[0]#	page 68	P	B	G
Q35	SDATA[17]#		P	B	G	V2	VCC_CORE		-	-	-
Q37	SDATA[16]#		P	B	G	V4	VCC_CORE		-	-	-
R2	VCC_CORE		-	-	-	V6	VCC_CORE		-	-	-
R4	VCC_CORE		-	-	-	V8	VCC_CORE		-	-	-
R6	VCC_CORE		-	-	-	V30	VSS		-	-	-
R8	VCC_CORE		-	-	-	V32	VSS		-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
V34	VSS		-	-	-	AA1	DBRDY	page 65	P	O	-
V36	VSS		-	-	-	AA3	DBREQ#	page 65	P	I	-
W1	FID[0]	page 66	O	O	-	AA5	NC		-	-	-
W3	FID[1]	page 66	O	O	-	AA7	Key Pin	page 67	-	-	-
W5	VREFSYS	page 69	P	-	-	AA31	NC Pin	page 67	-	-	-
W7	NC Pin	page 67	-	-	-	AA33	SDATA[8]#		P	B	P
W31	NC Pin	page 67	-	-	-	AA35	SDATA[0]#		P	B	G
W33	SDATAINCLK[0]#		P	I	G	AA37	SDATA[13]#		P	B	G
W35	SDATA[2]#		P	B	G	AB2	VSS		-	-	-
W37	SDATA[1]#		P	B	P	AB4	VSS		-	-	-
X2	VSS		-	-	-	AB6	VSS		-	-	-
X4	VSS		-	-	-	AB8	VSS		-	-	-
X6	VSS		-	-	-	AB30	VCC_CORE		-	-	-
X8	VSS		-	-	-	AB32	VCC_CORE		-	-	-
X30	VCC_CORE		-	-	-	AB34	VCC_CORE		-	-	-
X32	VCC_CORE		-	-	-	AB36	VCC_CORE		-	-	-
X34	VCC_CORE		-	-	-	AC1	STPCLK#	page 68	P	I	-
X36	VCC_CORE		-	-	-	AC3	PLLTEST#	page 68	P	I	-
Y1	FID[2]	page 66	O	O	-	AC5	ZN	page 70	P	-	-
Y3	FID[3]	page 66	O	O	-	AC7	NC		-	-	-
Y5	NC Pin	page 67	-	-	-	AC31	NC Pin	page 67	-	-	-
Y7	Key Pin	page 67	-	-	-	AC33	SDATA[10]#		P	B	P
Y31	NC Pin	page 67	-	-	-	AC35	SDATA[14]#		P	B	G
Y33	SCHECK[1]#	page 68	P	B	P	AC37	SDATA[11]#		P	B	G
Y35	SDATA[3]#		P	B	G	AD2	VCC_CORE		-	-	-
Y37	SDATA[12]#		P	B	P	AD4	VCC_CORE		-	-	-
Z2	VCC_CORE		-	-	-	AD6	VCC_CORE		-	-	-
Z4	VCC_CORE		-	-	-	AD8	NC Pin	page 67	-	-	-
Z6	VCC_CORE		-	-	-	AD30	NC Pin	page 67	-	-	-
Z8	VCC_CORE		-	-	-	AD32	VSS		-	-	-
Z30	VSS		-	-	-	AD34	VSS		-	-	-
Z32	VSS		-	-	-	AD36	VSS		-	-	-
Z34	VSS		-	-	-	AE1	A20M#		P	I	-
Z36	VSS		-	-	-	AE3	PWROK		P	I	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AE5	ZP	page 70	P	-	-	AG21	NC Pin	page 67	-	-	-
AE7	NC		-	-	-	AG23	NC Pin	page 67	-	-	-
AE31	NC Pin	page 67	-	-	-	AG25	NC Pin	page 67	-	-	-
AE33	SADDIN[5]#		P	I	G	AG27	Key Pin	page 67	-	-	-
AE35	SDATAOUTCLK[0]#		P	O	P	AG29	Key Pin	page 67	-	-	-
AE37	SDATA[9]#		P	B	G	AG31	NC Pin	page 67	-	-	-
AF2	VSS		-	-	-	AG33	SADDIN[2]#		P	I	G
AF4	VSS		-	-	-	AG35	SADDIN[11]#		P	I	G
AF6	NC Pin	page 67	-	-	-	AG37	SADDIN[7]#		P	I	P
AF8	NC Pin	page 67	-	-	-	AH2	VCC_CORE		-	-	-
AF10	NC Pin	page 67	-	-	-	AH4	VCC_CORE		-	-	-
AF12	VSS		-	-	-	AH6	AMD Pin	page 64	-	-	-
AF14	VCC_CORE		-	-	-	AH8	NC Pin	page 67	-	-	-
AF16	VSS		-	-	-	AH10	VCC_CORE		-	-	-
AF18	VCC_CORE		-	-	-	AH12	VSS		-	-	-
AF20	VSS		-	-	-	AH14	VCC_CORE		-	-	-
AF22	VCC_CORE		-	-	-	AH16	VSS		-	-	-
AF24	VSS		-	-	-	AH18	VCC_CORE		-	-	-
AF26	VCC_CORE		-	-	-	AH20	VSS		-	-	-
AF28	NC Pin	page 67	-	-	-	AH22	VCC_CORE		-	-	-
AF30	NC Pin	page 67	-	-	-	AH24	VSS		-	-	-
AF32	NC Pin	page 67	-	-	-	AH26	VCC_CORE		-	-	-
AF34	VCC_CORE		-	-	-	AH28	VSS		-	-	-
AF36	VCC_CORE		-	-	-	AH30	NC Pin	page 67	-	-	-
AG1	FERR	page 65	P	O	-	AH32	VSS		-	-	-
AG3	RESET#		-	I	-	AH34	VSS		-	-	-
AG5	NC Pin	page 67	-	-	-	AH36	VSS		-	-	-
AG7	Key Pin	page 67	-	-	-	AJ1	IGNNE#	page 67	P	I	-
AG9	Key Pin	page 67	-	-	-	AJ3	INIT#	page 67	P	I	-
AG11	COREFB	page 65	-	-	-	AJ5	VCC_CORE		-	-	-
AG13	COREFB#	page 65	-	-	-	AJ7	NC Pin	page 67	-	-	-
AG15	Key Pin	page 67	-	-	-	AJ9	NC Pin	page 67	-	-	-
AG17	Key Pin	page 67	-	-	-	AJ11	NC Pin	page 67	-	-	-
AG19	NC Pin	page 67	-	-	-	AJ13	Analog	page 64	-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AJ15	NC Pin	page 67	-	-	-	AL9	NC Pin	page 67	-	-	-
AJ17	NC Pin	page 67	-	-	-	AL11	NC Pin	page 67	-	-	-
AJ19	NC Pin	page 67	-	-	-	AL13	PLLMON2	page 68	O	O	-
AJ21	CLKFWRST	page 64	P	I	P	AL15	PLLBYPASSCLK#	page 68	P	I	-
AJ23	VCCA	page 69	-	-	-	AL17	CLKIN#	page 64	P	I	P
AJ25	PLLBYPASS#	page 68	P	I	-	AL19	RSTCLK#	page 64	P	I	P
AJ27	NC Pin	page 67	-	-	-	AL21	K7CLKOUT	page 67	P	O	-
AJ29	SADDIN[0]#	page 68	P	I	-	AL23	CONNECT	page 65	P	I	P
AJ31	SFILLVALID#		P	I	G	AL25	NC Pin	page 67	-	-	-
AJ33	SADDINCLK#		P	I	G	AL27	NC Pin	page 67	-	-	-
AJ35	SADDIN[6]#		P	I	P	AL29	SADDIN[1]#	page 68	P	I	-
AJ37	SADDIN[3]#		P	I	G	AL31	SDATAOUTVALID#		P	O	P
AK2	VSS		-	-	-	AL33	SADDIN[8]#		P	I	P
AK4	VSS		-	-	-	AL35	SADDIN[4]#		P	I	G
AK6	CPU_PRESENCE#	page 65	-	-	-	AL37	SADDIN[10]#		P	I	G
AK8	NC Pin	page 67	-	-	-	AM2	VCC_CORE		-	-	-
AK10	VCC_CORE		-	-	-	AM4	VSS		-	-	-
AK12	VSS		-	-	-	AM6	VSS		-	-	-
AK14	VCC_CORE		-	-	-	AM8	NC Pin	page 67	-	-	-
AK16	VSS		-	-	-	AM10	VCC_CORE		-	-	-
AK18	VCC_CORE		-	-	-	AM12	VSS		-	-	-
AK20	VSS		-	-	-	AM14	VCC_CORE		-	-	-
AK22	VCC_CORE		-	-	-	AM16	VSS		-	-	-
AK24	VSS		-	-	-	AM18	VCC_CORE		-	-	-
AK26	VCC_CORE		-	-	-	AM20	VSS		-	-	-
AK28	VSS		-	-	-	AM22	VCC_CORE		-	-	-
AK30	VCC_CORE		-	-	-	AM24	VSS		-	-	-
AK32	VSS		-	-	-	AM26	VCC_CORE		-	-	-
AK34	VCC_CORE		-	-	-	AM28	VSS		-	-	-
AK36	VCC_CORE		-	-	-	AM30	VCC_CORE		-	-	-
AL1	INTR	page 67	P	I	-	AM32	VSS		-	-	-
AL3	FLUSH#	page 67	P	I	-	AM34	VCC_CORE		-	-	-
AL5	VCC_CORE		-	-	-	AM36	VSS		-	-	-
AL7	NC Pin	page 67	-	-	-	AN1	No Pin	page 68	-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AN3	NMI		P	I	-
AN5	SMI#		P	I	-
AN7	NC Pin	page 67	-	-	-
AN9	NC Pin	page 67	-	-	-
AN11	NC Pin	page 67	-	-	-
AN13	PLLMON1	page 68	O	B	-
AN15	PLLBYPASSCLK	page 68	P	I	-
AN17	CLKIN	page 64	P	I	P
AN19	RSTCLK	page 64	P	I	P
AN21	K7CLKOUT#	page 67	P	O	-
AN23	PROCRDY		P	O	P
AN25	NC Pin	page 67	-	-	-
AN27	NC Pin	page 67	-	-	-
AN29	SADDIN[12]#		P	I	G
AN31	SADDIN[14]#		P	I	G
AN33	SDATAINVALID#		P	I	P
AN35	SADDIN[13]#		P	I	G
AN37	SADDIN[9]#		P	I	G

10.3 Detailed Pin Descriptions

The information in this section pertains to Table 19 on page 56.

A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

AMD Pin

AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.

AMD Athlon™ System Bus Pins

See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SCHECK[7:0]#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.

Analog Pin

Treat this pin as a NC.

APIC Pins, PICCLK, PICD[1:0]#

The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge, a dedicated I/O APIC, or another multiprocessing-enabled AMD Athlon MP processor. The pin, PICCLK, must be driven with a valid clock input.

For more information, see Table 15, “APIC Pin AC and DC Characteristics,” on page 38.

CLKFWRST Pin

CLKFWRST resets clock-forward circuitry for both the system and processor.

CLKIN, RSTCLK (SYSCLK) Pins

Connect CLKIN with RSTCLK and name it SYSCLK. Connect CLKIN# with RSTCLK# and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.

See “SYSCLK and SYSCLK#” on page 69 for more information.

CONNECT Pin

CONNECT is an input from the system used for power management and clock-forward initialization at reset.

**COREFB and
COREFB# Pins**

COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.

CPU_PRESENCE# Pin

CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor in the Socket A-style socket.

**DBRDY and DBREQ#
Pins**

DBRDY and DBREQ# are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.

FERR Pin

FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the “Required Circuits” chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

FID[3:0] Pins

FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio.

Table 20 on page 66 describes the encodings of the clock multipliers on FID[3:0].

Table 20. FID[3:0] Clock Multiplier Encodings

FID[3]	FID[2]	FID[1]	FID[0]	Processor Clock to SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	≥ 12.5*
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5
Note: *All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.				

The FID[3:0] signals are open drain processor outputs that are pulled High on the motherboard and sampled by the chipset to determine the SIP (Serialization Initialization Packet) that is sent to the processor. The FID[3:0] signals are valid after PWROK is asserted. The FID[3:0] signals must not be sampled until they become valid. See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for more information about Serialization Initialization Packets and SIP protocol.

The processor FID[3:0] outputs are open drain and 2.5 V tolerant. To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor. For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

See “Frequency Identification (FID[3:0])” on page 27 for the DC characteristics for FID[3:0].

FLUSH# Pin	FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.
IGNNE# Pin	IGNNE# is an input from the system that tells the processor to ignore numeric errors.
INIT# Pin	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.
INTR Pin	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
JTAG Pins	TCK, TMS, TDI, TRST#, and TDO are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pull TDI, TCK, TMS, and TRST# up to VCC_CORE with pullup resistors.
K7CLKOUT and K7CLKOUT# Pins	K7CLKOUT and K7CLKOUT# are each run for two to three inches and then terminated with a resistor pair: 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.
Key Pins	These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (No Connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.
NC Pins	The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.
NMI Pin	NMI is an input from the system that causes a non-maskable interrupt.

PGA Orientation Pins	<p>No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.</p> <p>For more information, see the <i>AMD Athlon™ Processor-Based Motherboard Design Guide</i>, order# 24363.</p>
PLL Bypass and Test Pins	<p>PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.</p>
PWROK Pin	<p>The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.</p> <p>For more information, see “Signal and Power-Up Requirements” on page 39.</p>
SADDIN[1:0]# and SADDOUT[1:0]# Pins	<p>The AMD Athlon MP processor does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the <i>AMD Athlon™ and AMD Duron™ System Bus Specification</i>, order# 21902.</p>
Scan Pins	<p>SCANSHIFTEN, SCANCLK1, SCANINTEVAL, and SCANCLK2 are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.</p>
SCHECK[7:0]# Pins	<p>For systems that do not support ECC, the SCHECK[7:0]# pins should be treated as NC pins.</p>
SMI# Pin	<p>SMI# is an input that causes the processor to enter the system management mode.</p>
STPCLK# Pin	<p>STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.</p>

SYSCLK and SYSCLK# SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system-clock generator.

See “CLKIN, RSTCLK (SYSCLK) Pins” on page 64 for more information.

**THERMDA and
THERMDC Pins**

Thermal Diode anode and cathode pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system.

VCCA Pin

VCCA is the processor PLL supply. For information about the VCCA pin, see “VCCA AC and DC Characteristics” on page 27 and the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

VID[4:0] Pins

The VID[4:0] (Voltage Identification) outputs are used to dictate the VCC_CORE voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor package. The VID[4:0] pins are pulled-up on the motherboard and used by the VCC_CORE DC/DC converter.

Table 21. VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE(V)	VID[4:0]	VCC_CORE (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

VREFSYS Pin

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

ZN and ZP Pins

ZN (AC5) and ZP (AE5) are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z_0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z_0 of the transmission line.

11 Ordering Information

Standard AMD Athlon™ MP Processor Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) are formed by a combination of the elements, as shown in Figure 14 .

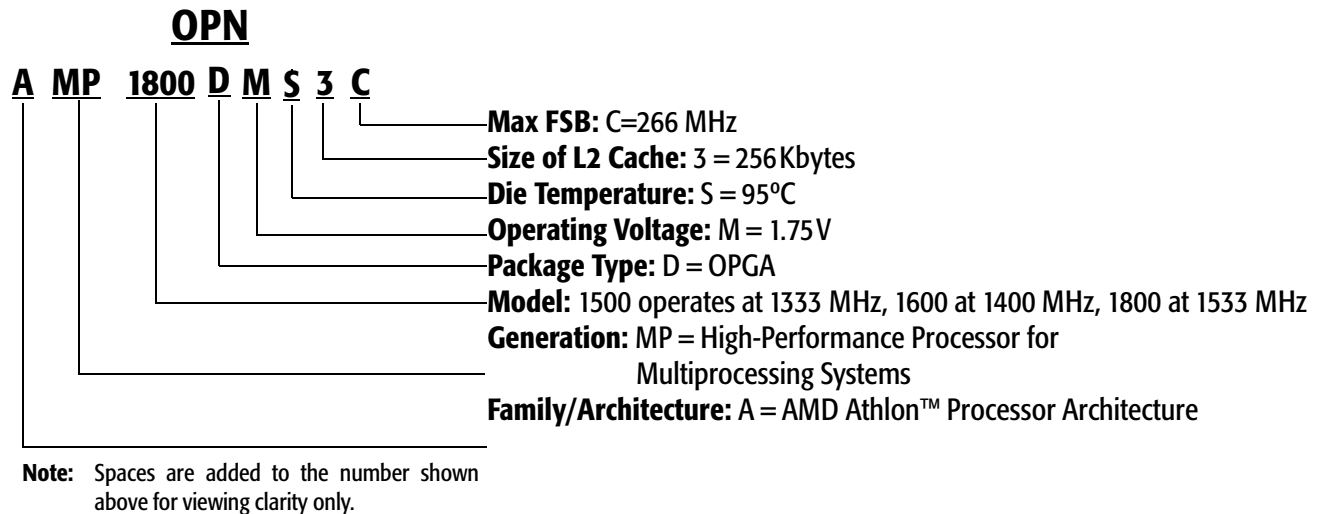


Figure 14. OPN Example for the AMD Athlon™ MP Processor, OPGA Package

Appendix A

Conventions and Abbreviations

This section contains information about the conventions and abbreviations used in this document.

Signals and Bits

- **Active-Low Signals**—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- **Signal Ranges**—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- **Reserved Bits and Signals**—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- **Three-State**—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
 - A *word* is two bytes (16 bits)
 - A *doubleword* is four bytes (32 bits)
 - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
 - Kilo (K, as in 4-Kbyte page)
 - Mega (M, as in 4 Mbits/sec)
 - Giga (G, as in 4 Gbytes of memory space)

See Table 22 on page 75 for more abbreviations.

- Little-Endian Convention—The byte with the address *xx...xx00* is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 22 contains the definitions of abbreviations used in this document.

Table 22. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
GHz	Gigahertz
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
lbf	Foot-pound
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
μ	Micro-
μA	Microampere
μF	Microfarad
μH	Microhenry
μs	Microsecond
μV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm

Table 22. Abbreviations (Continued)

Abbreviation	Meaning
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 23 contains the definitions of acronyms used in this document.

Table 23. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
CPGA	Ceramic Pin Grid Array
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic

Table 23. Acronyms (Continued)

Abbreviation	Meaning
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-Drain
OPGA	Organic Pin Grid Array
PA	Physical Address
PBGA	Plastic Ball Grid Array
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PGA	Pin Grid Array
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SCSI	Small Computer System Interface
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIMD	Single Instruction Multiple Data
SIP	Serial Initialization Packet
SMBus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory

Table 23. Acronyms (Continued)

Abbreviation	Meaning
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer