0.35 Micron CMOS Pad Library Datasheets
AMI350XXPF 3.3/5.0 Volt
Section 4

AMI350XXPF 0.35 micron CMOS Pad Library

Input Drive Pieces

Pull Pieces

AMI350XXPF 0.35 micron CMOS Pad Library

Output Drive Pieces

Pad Selection Guide

AMI350XXPF 0.35 micron CMOS Pad Library

Power Pad Cells

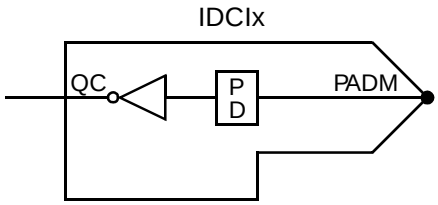
Special Pad Cells

DATASHEETS

Description

IDCIx is a family of inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

HDL Syntax

Verilog ..... IDCIx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCIx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCI3	IDCI6
PADM (pF)	4.99	4.99

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCI3	1.0	4.722	10.4
IDCI6	1.0	8.179	16.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

IDCI3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.400 0.456	0.493 0.544	0.578 0.621	0.655 0.683	0.736 0.742
IDCI6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.440 0.482	0.519 0.592	0.589 0.666	0.662 0.720	0.739 0.763

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IDCIC

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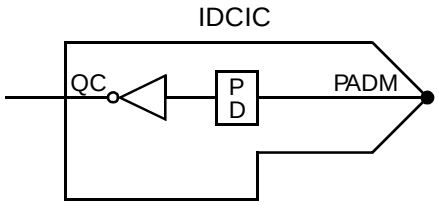
Description

IDCIC is an inverting 5 volt capable (cascode-gate), CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCIC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCIC port map (QC, PADM);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.120	nA
EQL_{pd}	26.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

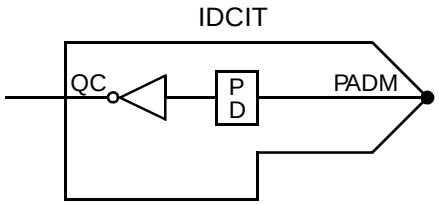
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	1.099 0.835	1.160 0.949	1.228 1.045	1.300 1.120	1.376 1.179

Description

IDCIT is an inverting 5 volt tolerant, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCIT *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCIT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.206	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.574 0.543	0.648 0.651	0.720 0.724	0.797 0.777	0.884 0.819

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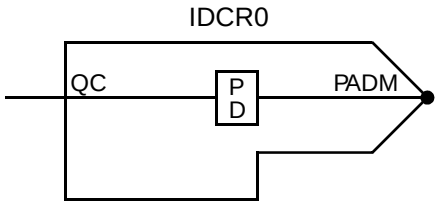
Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.088	nA
EQL_{pd}	1.6	Eq-load

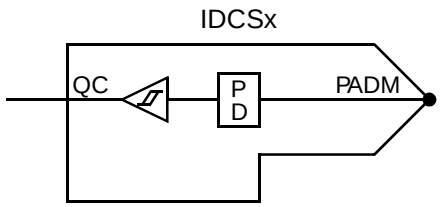
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCSx is a family of non-inverting, CMOS-level Schmitt trigger input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

HDL Syntax

Verilog ..... IDCSx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCSx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCS3	IDCS6
PADM (pF)	4.99	4.99

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCS3	1.0	4.483	14.2
IDCS6	1.0	7.076	18.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	10	21	32	42 (max)
IDCS3	From: PADM	t_{PLH}	0.920	1.007	1.107	1.199	1.276
	To: QC	t_{PHL}	0.831	0.931	1.035	1.120	1.180
	Number of Equivalent Loads		**1**	**20**	**40**	**60**	**80 (max)**
IDCS6	From: PADM	t_{PLH}	1.214	1.337	1.420	1.481	1.530
	To: QC	t_{PHL}	1.018	1.151	1.254	1.352	1.450

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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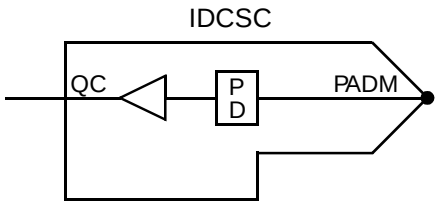
Description

IDCSC is a 5 volt cascoded-gate non-inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCSC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCSC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.849	nA
EQL_{pd}	34.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

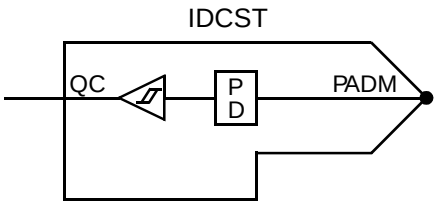
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.906 1.048	1.013 1.138	1.083 1.198	1.138 1.243	1.184 1.278

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDCST is a 5 volt tolerant non-inverting, CMOS Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCST *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCST port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.476	nA
EQL_{pd}	23.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	1.570 1.812	1.700 1.893	1.776 1.957	1.838 2.004	1.906 2.039

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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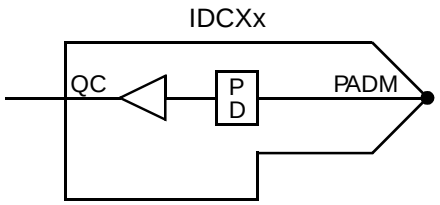
Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.99	4.99

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	1.0	3.858	8.4
IDCX6	1.0	7.555	14.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

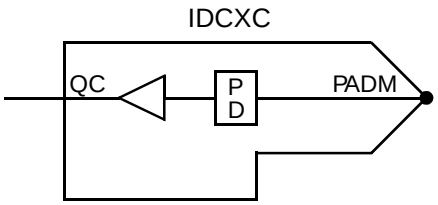
IDCX3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.382 0.332	0.502 0.460	0.602 0.555	0.680 0.631	0.758 0.691
IDCX6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.364 0.310	0.475 0.430	0.566 0.514	0.646 0.587	0.719 0.653

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Description

IDCXC is a 5 volt cascoded-gate non-inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCXC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.849	nA
EQL_{pd}	30.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.870 1.109	1.004 1.170	1.073 1.221	1.126 1.284	1.171 1.360

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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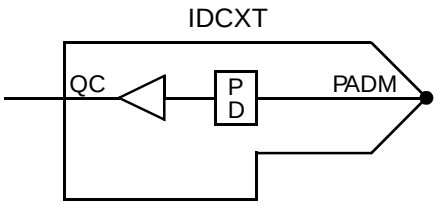
Description

IDCXT is a 5 volt tolerant non-inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDCXT *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	23.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH}	0.545	0.677	0.766	0.831	0.882
		t_{PHL}	0.508	0.642	0.732	0.797	0.849

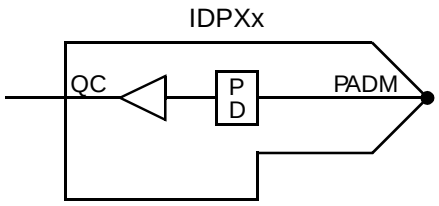
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

IDPXx is a family of non-inverting, PCI-level input buffer pieces. IDPXx is intended to be used in conjunction with the 33MHz PCI ODPSXE33 piece whereas IDPX6 is intended to be used with the 66MHz PCI ODPHXE66 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDPX3	IDPX6
PADM (pF)	4.99	4.99

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	1.0	3.618	9.0
IDPX6	1.0	7.107	15.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

IDPX3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.396 0.337	0.520 0.435	0.623 0.512	0.703 0.586	0.780 0.646
IDPX6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.366 0.342	0.451 0.445	0.533 0.515	0.615 0.578	0.698 0.642

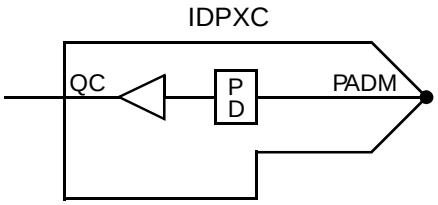
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

IDPXC is a 5 volt capable (cascode-gate) non-inverting, 33MHz PCI-level input buffer piece to be used in conjunction with 33MHz PCI ODPSCE33 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDPXC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPXC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	25.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

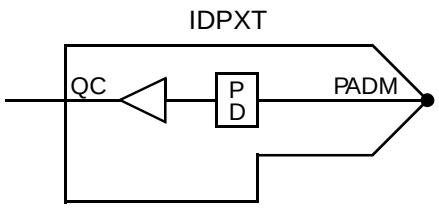
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.449 0.490	0.618 0.603	0.696 0.679	0.755 0.735	0.820 0.779

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPXT is a 5 volt tolerant non-inverting, 33MHz PCI-level input buffer piece to be used in conjunction with 33MHz PCI ODPHTE66 piece

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDPXT *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPXT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	25.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.459 0.506	0.612 0.612	0.682 0.682	0.751 0.736	0.825 0.781

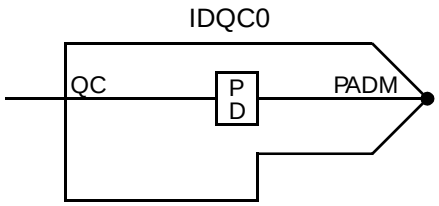
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);

VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.088	nA
EQL_{pd}	1.6	Eq-load

See page 2-13 for power equation.

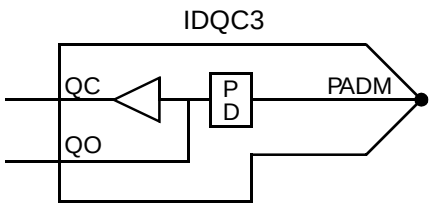
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

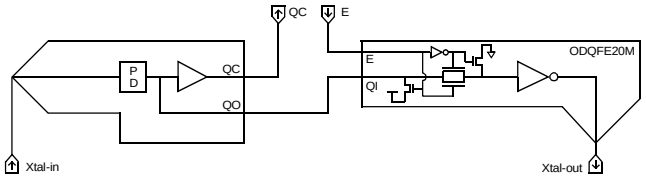
Description

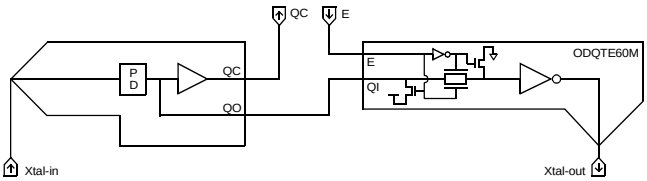
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.99 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.858	nA
EQL_{pd}	9.8	Eq-load

See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.389 0.361	0.517 0.483	0.621 0.575	0.701 0.654	0.779 0.719
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

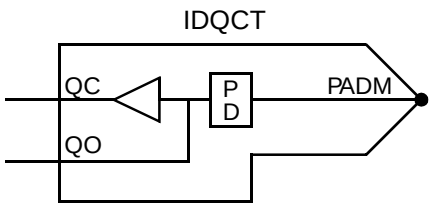
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes: The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

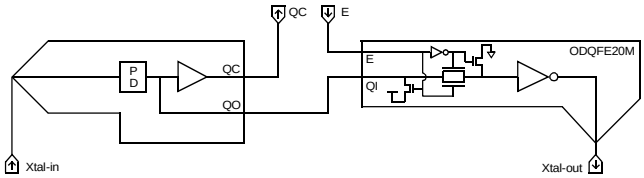
Description

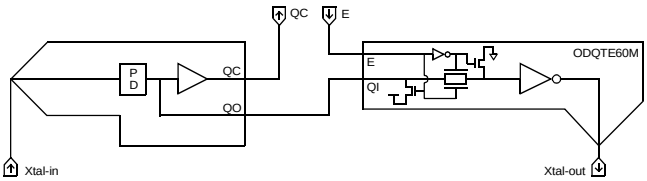
IDQCT is a 5-volt tolerant crystal oscillator input receiver pad piece with a non-inverting, CMOS clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.99 pF

Pad Logic

HDL Syntax

Verilog ..... IDQCT *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQCT port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	25.0	Eq-load

See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.567 0.579	0.624 0.633	0.690 0.698	0.744 0.763	0.779 0.821
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

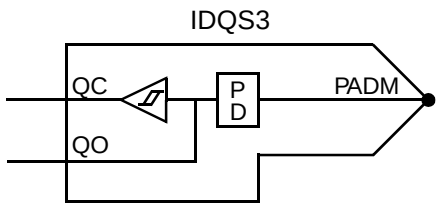
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes: The IDQCT is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator

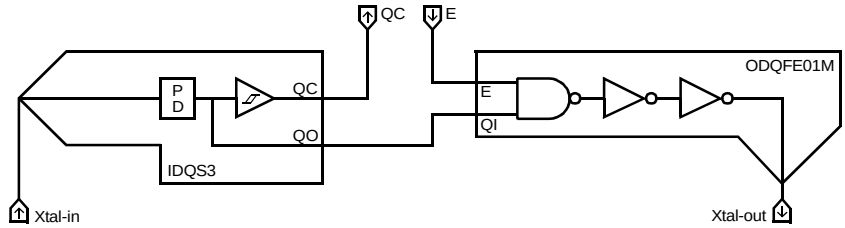
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS Schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.483	nA
EQL_{pd}	15.4	Eq-load

See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.933 0.851	1.020 0.946	1.119 1.047	1.211 1.132	1.287 1.194
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

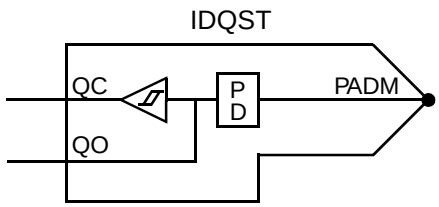
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes: The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

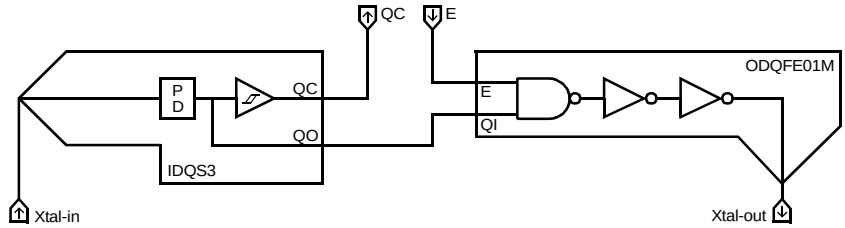
Description

IDQST is a 5-volt tolerant crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS Schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.99 pF

Pad Logic

HDL Syntax

Verilog ..... IDQST *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQST port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.476	nA
EQL_{pd}	24.6	Eq-load

See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	1.797 1.836	1.836 1.842	1.878 1.873	1.926 1.935	1.978 2.024
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

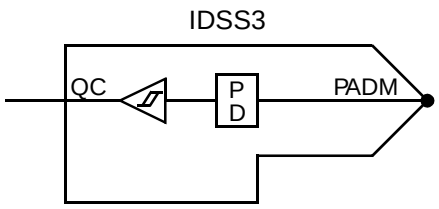
Design Notes:

The IDQST is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator

Description

IDSS3 is a non-inverting, SCSI-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDSS3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDSS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.659	nA
EQL_{pd}	16.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	1.092 1.360	1.185 1.502	1.287 1.647	1.377 1.760	1.448 1.835

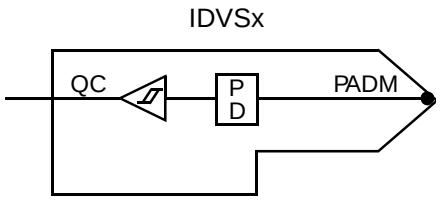
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

IDVSx is a family of non-inverting, LVTTL-level Schmitt input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDVSx inst_IDVSx (QC, PADM);

VHDL..... inst_IDVSx : IDVSx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDVS3	IDVS6
PADM (pF)	4.99	4.99

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDVS3	1.0	4.483	13.9
IDVS6	1.0	7.076	18.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

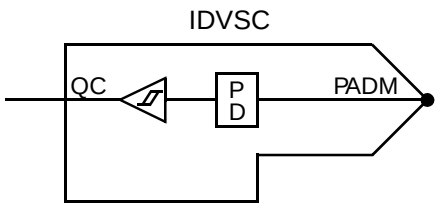
IDVS3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM	t_{PLH}	0.615	0.759	0.869	0.946	1.023
	To: QC	t_{PHL}	0.715	0.816	0.918	0.999	1.053
IDVS6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM	t_{PLH}	0.816	0.934	1.024	1.114	1.207
	To: QC	t_{PHL}	0.935	1.047	1.110	1.200	1.322

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDVSC is a 5-volt capable (cascode-gate) non-inverting, LVTTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDVSC inst_IDVSC (QC, PADM);

VHDL..... inst_IDVSC : IDVSC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.700	nA
EQL_{pd}	25.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH}	1.102	1.173	1.236	1.313	1.405
		t_{PHL}	0.987	1.086	1.153	1.201	1.239

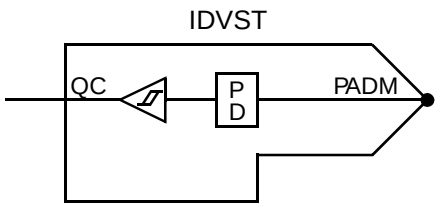
Delay will vary with input conditions. See page 2-15 for interconnect estimates

AMI350XXPF 0.35 micron CMOS Pad Library

Description

IDVST is 5 volt tolerant non-inverting, LVTTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDVST inst_IDVST (QC, PADM);

VHDL..... inst_IDVST : IDVST port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.700	nA
EQL_{pd}	25.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

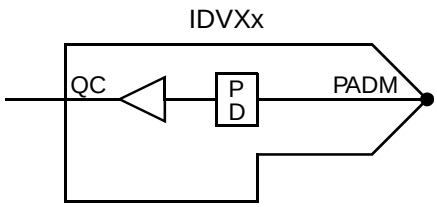
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	1.085 1.045	1.195 1.112	1.269 1.157	1.322 1.190	1.365 1.216

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Description

IDVXx is family of non-inverting, LVTTL-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

Pin Name	Load	
	IDVX3	IDVX6
PADM (pF)	4.99	4.99

HDL Syntax

Verilog ..... IDVXx inst_IDVXx (QC, PADM);

VHDL..... inst_IDVXx : IDVXx port map (QC, PADM);

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDVX3	1.0	3.618	8.3
IDVX6	1.0	7.075	14.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	10	21	32	42 (max)
IDVX3	From: PADM To: QC	t_{PLH} t_{PHL}	0.348 0.360	0.464 0.455	0.562 0.538	0.640 0.604	0.717 0.668
	Number of Equivalent Loads		**1**	**10**	**21**	**32**	**42 (max)**
IDVX6	From: PADM To: QC	t_{PLH} t_{PHL}	0.329 0.327	0.375 0.386	0.437 0.433	0.493 0.467	0.527 0.496

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

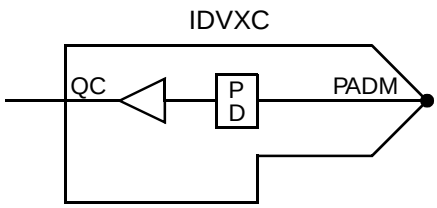
IDVXC

AMI350XXPF 0.35 micron CMOS Pad Library

Description

IDVXC is a 5-volt capable (cascode-gate) non-inverting, LVTTL-level input buffer piece

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDVXC inst_IDVXC (QC, PADM);

VHDL..... inst_IDVXC : IDVXC port map (QC, PADM);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	24.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

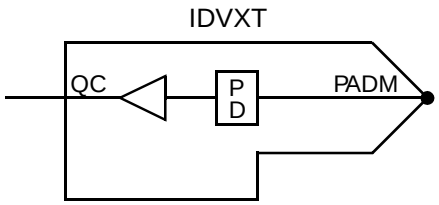
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.541 0.466	0.606 0.515	0.673 0.546	0.726 0.579	0.762 0.612

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Description

IDVXT is a 5-volt tolerant non-inverting, LVTTL-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.99 pF

HDL Syntax

Verilog ..... IDVXT inst_IDVXT (QC, PADM);

VHDL..... inst_IDVXT : IDVXT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	24.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.541 0.455	0.606 0.496	0.673 0.549	0.726 0.602	0.762 0.651

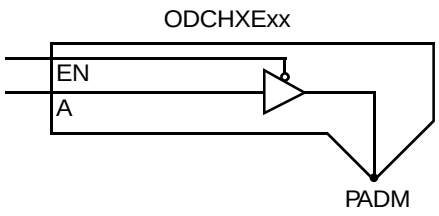
Delay will vary with input conditions. See page 2-15 for interconnect estimates

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCHXExx is a family of 8 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enable outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCHXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODCHXE08	ODCHXE12	ODCHXE16	ODCHXE24
A (eq-load)	5.2	5.2	5.2	5.2
EN (eq-load)	7.6	7.6	7.6	7.6
PADM (pF)	5.02	5.04	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCHXE08	8	129.838	305.4
ODCHXE12	12	129.838	329.3
ODCHXE16	16	129.838	352.6
ODCHXE24	24	129.838	369.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCHXE08	From: A To: PADM	t_{PLH} t_{PHL}	0.910 0.672	1.870 1.271	3.243 2.127	5.987 3.839	8.732 5.550
	From: EN To: PADM	t_{ZH} t_{ZL}	0.844 0.698	1.805 1.297	3.177 2.153	5.922 3.864	8.667 5.576
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.763 0.606	1.400 1.011	2.310 1.586	4.129 2.726	5.948 3.852
	From: EN To: PADM	t_{ZH} t_{ZL}	0.700 0.630	1.337 1.036	2.246 1.612	4.065 2.752	5.884 3.877
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.705 0.586	1.192 0.900	1.889 1.343	3.281 2.210	4.673 3.051
	From: EN To: PADM	t_{ZH} t_{ZL}	0.641 0.608	1.128 0.923	1.824 1.368	3.217 2.236	4.609 3.077
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE24	From: A To: PADM	t_{PLH} t_{PHL}	0.710 0.563	1.197 0.790	1.893 1.104	3.284 1.699	4.676 2.250
	From: EN To: PADM	t_{ZH} t_{ZL}	0.640 0.587	1.128 0.816	1.824 1.132	3.217 1.728	4.609 2.277

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

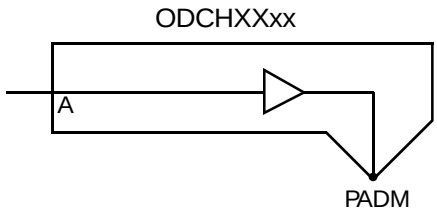
Delay (ns) From	To	Parameter	Cell ODCHXE08	ODCHXE12	ODCHXE16	ODCHXE24
EN	PADM	t_{HZ} t_{LZ}	0.318 0.465	0.359 0.505	0.406 0.543	0.406 0.595

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCHXXxx is a family of 8 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCHXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXXxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCHXX08	ODCHXX12	ODCHXX16	ODCHXX24
A (eq-load)	18.9	18.9	18.9	18.9

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCHXX08	8	109.576	254.3
ODCHXX12	12	109.576	278.2
ODCHXX16	16	109.576	301.4
ODCHXX24	24	109.576	317.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.637 0.474	1.598 1.072	2.971 1.927	5.715 3.635	8.460 5.344
ODCHXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.503 0.417	1.139 0.814	2.048 1.381	3.864 2.515	5.681 3.649
ODCHXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.451 0.398	0.937 0.704	1.631 1.139	3.019 1.999	4.407 2.846
ODCHXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.479 0.353	0.960 0.566	1.650 0.866	3.038 1.449	4.436 2.010

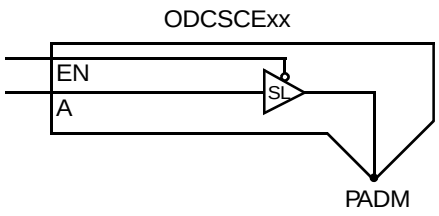
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCSCExx is a family of 4 to 12 mA, 5-volt capable (cascode-gate), non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSCExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSCExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSCE04	ODCSCE08	ODCSCE12
A (eq-load)	2.9	2.9	2.9
EN (eq-load)	2.3	2.3	2.3
PADM (pF)	5.05	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSCE04	4	108.509	463.8
ODCSCE08	8	108.509	505.3
ODCSCE12	12	108.509	524.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSCE04	From: A To: PADM	t_{PLH} t_{PHL}	4.453 3.870	6.337 5.247	9.002 6.914	14.236 9.651	19.344 12.420
	From: EN To: PADM	t_{ZH} t_{ZL}	4.471 1.618	6.354 2.482	9.020 3.400	14.262 5.012	19.385 6.529
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSCE08	From: A To: PADM	t_{PLH} t_{PHL}	3.793 3.460	4.840 4.267	6.287 5.317	9.006 7.055	11.492 8.310
	From: EN To: PADM	t_{ZH} t_{ZL}	3.855 1.254	4.906 1.874	6.355 2.576	9.070 3.562	11.539 4.397
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSCE12	From: A To: PADM	t_{PLH} t_{PHL}	3.789 3.349	4.838 4.020	6.286 4.878	9.007 6.246	11.493 7.148
	From: EN To: PADM	t_{ZH} t_{ZL}	3.856 1.260	4.907 1.710	6.355 2.284	9.069 3.189	11.539 3.769

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

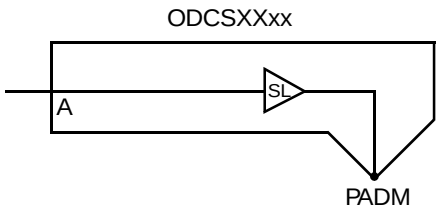
Delay (ns) From	To	Parameter	Cell ODCSCE04	ODCSCE08	ODCSCE12
EN	PADM	t_{HZ} t_{LZ}	2.531 1.137	2.841 1.322	2.841 1.520

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCSCXxx is a family of 4 to 12 mA, non-inverting, 5-volt capable (cascode-gate), CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSCXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSCXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSCX04	ODCSCX08	ODCSCX12
A (eq-load)	3.9	3.9	3.9

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSCX04	4	107.020	455.5
ODCSCX08	8	107.020	497.0
ODCSCX12	12	107.020	516.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSCX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.252 3.778	6.133 5.155	8.797 6.826	14.037 9.578	19.162 12.374
ODCSCX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.609 3.389	4.653 4.200	6.096 5.254	8.812 6.995	11.302 8.245
ODCSCX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.603 3.291	4.649 3.961	6.095 4.818	8.814 6.186	11.302 7.089

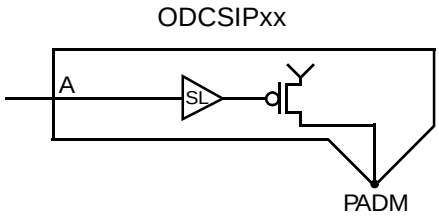
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCSIPxx is a family of 4 to 16 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCSIP04	ODCSIP08	ODCSIP12	ODCSIP16
A (eq-load)	3.0	4.5	4.5	4.5
PADM (pF)	5.01	5.02	5.04	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	98.537	329.0
ODCSIP08	8	99.641	342.2
ODCSIP12	12	99.641	357.0
ODCSIP16	16	99.641	369.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.286	4.291	7.123	12.676	18.079
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.652	2.834	4.366	7.121	9.910
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.553	2.455	3.560	5.408	7.279
ODCSIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.570	2.324	3.150	4.638	6.052

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

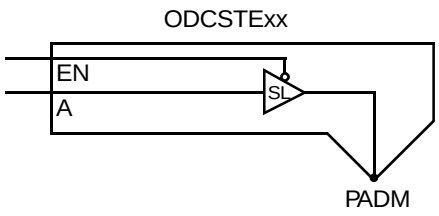
Delay (ns) From	To	Parameter	Cell			
			ODCSIP04	**ODCSIP08**	**ODCSIP12**	**ODCSIP16**
A	PADM	t_{HZ}	0.923	0.739	0.574	0.678

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCSTExx is a family of 4 to 8 mA, 5-volt tolerant, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load	
	ODCSTE04	ODCSTE08
A (eq-load)	2.4	2.4
EN (eq-load)	7.9	7.9
PADM (pF)	5.05	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSTE04	4	113.300	482.4
ODCSTE08	8	113.300	501.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSTE04	From: A To: PADM	t_{PLH} t_{PHL}	3.142 2.229	5.154 3.566	7.996 5.079	13.560 7.892	18.967 10.638
	From: EN To: PADM	t_{ZH} t_{ZL}	2.934 2.107	4.944 3.493	7.781 5.025	13.342 7.844	18.749 10.594
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSTE08	From: A To: PADM	t_{PLH} t_{PHL}	2.445 1.684	3.550 2.632	5.077 3.703	7.954 5.242	10.594 6.693
	From: EN To: PADM	t_{ZH} t_{ZL}	2.269 1.524	3.371 2.497	4.895 3.596	7.768 5.165	10.408 6.616

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

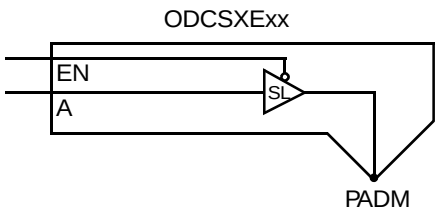
Delay (ns) From	To	Parameter	Cell ODCSTE04	Cell ODCSTE08
EN	PADM	t_{HZ} t_{LZ}	8.406 0.697	9.238 0.798

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCSXExx is a family of 4 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16	ODCSXE24
A (eq-load)	2.4	2.5	2.4	2.4	2.4
EN (eq-load)	6.2	6.2	6.2	6.2	6.2
PADM (pF)	5.01	5.02	5.04	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	113.278	372.2
ODCSXE08	8	113.278	395.0
ODCSXE12	12	113.278	419.0
ODCSXE16	16	113.278	442.2
ODCSXE24	24	113.278	458.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.520 2.986	4.586 4.155	7.485 5.997	13.097 9.603	18.463 13.081
	From: EN To: PADM	t_{ZH} t_{ZL}	2.440 2.493	4.464 4.071	7.319 6.071	12.899 9.570	18.306 13.112
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.963 1.617	3.172 2.958	4.646 4.146	7.456 6.004	10.235 7.826
	From: EN To: PADM	t_{ZH} t_{ZL}	1.865 2.067	3.043 3.070	4.577 4.186	7.355 6.076	10.162 7.783
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.715 1.396	2.715 2.430	3.800 3.541	5.678 4.967	7.557 6.231
	From: EN To: PADM	t_{ZH} t_{ZL}	1.731 1.897	2.623 2.746	3.726 3.694	5.587 5.026	7.475 6.272
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.441 1.362	2.231 2.263	3.121 3.242	4.397 4.502	5.614 5.528
	From: EN To: PADM	t_{ZH} t_{ZL}	1.596 1.866	2.295 2.626	3.105 3.462	4.335 4.589	5.542 5.589
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.436 1.314	2.225 2.099	3.114 2.878	4.394 3.960	5.610 4.755
	From: EN To: PADM	t_{ZH} t_{ZL}	1.596 1.881	2.295 2.524	3.105 3.159	4.335 4.102	5.542 4.851

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

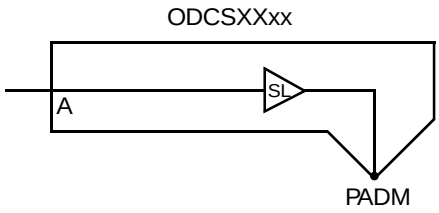
Delay (ns) From	To	Parameter	Cell				
			ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16	ODCSXE24
ENPADM		t_{HZ} t_{LZ}	0.515 0.470	0.604 0.513	0.689 0.562	0.779 0.605	0.779 0.668

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCSXXxx is a family of 4 to 24 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCSXX04	ODCSXX08	ODCSXX12	ODCSXX16	ODCSXX24
A (eq-load)	3.8	3.8	3.8	3.8	3.8

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	110.684	363.2
ODCSXX08	8	110.684	386.0
ODCSXX12	12	110.684	409.9
ODCSXX16	16	110.684	433.2
ODCSXX24	24	110.684	449.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.203 2.238	4.289 3.979	7.208 5.845	12.825 9.430	18.148 12.923
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.768 1.482	2.911 2.763	4.367 3.934	7.191 5.863	9.950 7.622
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.460 1.233	2.402 2.250	3.451 3.355	5.391 4.804	7.223 6.062
ODCSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.322 1.214	2.189 2.092	3.113 3.060	4.629 4.339	6.066 5.364
ODCSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.264 1.151	2.137 1.894	3.140 2.714	4.636 3.791	6.096 4.623

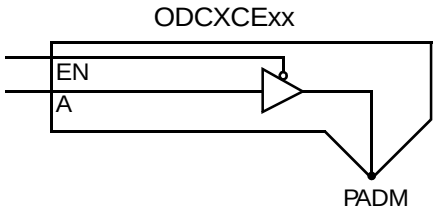
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCXCExx is a family of 1 to 12 mA, 5-volt capable (cascode-gate), non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXCExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXCExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXCE01	ODCXCE02	ODCXCE04	ODCXCE08	ODCXCE12
A (eq-load)	2.9	2.9	2.9	2.9	2.9
EN (eq-load)	2.3	2.3	2.3	2.3	2.3
PADM (pF)	5.05	5.06	5.05	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXCE01	1	110.714	318.7
ODCXCE02	2	110.714	329.8
ODCXCE04	4	110.714	352.0
ODCXCE08	8	110.714	393.6
ODCXCE12	12	110.714	413.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXCE01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	7.125 4.735	9.226 5.841	11.326 6.946	14.477 8.605	19.730 11.368
	From: EN To: PADM	t_{ZH} t_{ZL}	7.212 1.818	9.315 2.423	11.419 3.029	14.574 3.937	19.833 5.452
ODCXCE02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.681 3.484	8.303 5.420	10.890 6.802	13.478 8.185	18.654 10.950
	From: EN To: PADM	t_{ZH} t_{ZL}	4.763 1.141	8.391 2.201	10.982 2.958	13.573 3.716	18.755 5.230
ODCXCE04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.534 2.886	5.345 3.844	7.932 5.209	13.108 7.924	18.285 10.621
	From: EN To: PADM	t_{ZH} t_{ZL}	3.618 0.841	5.432 1.367	8.023 2.117	13.205 3.610	18.387 5.096
ODCXCE08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.997 2.680	3.904 3.169	5.200 3.864	7.793 5.234	10.386 6.582
	From: EN To: PADM	t_{ZH} t_{ZL}	3.087 0.764	3.994 1.042	5.290 1.435	7.881 2.197	10.473 2.930
ODCXCE12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.005 2.681	3.912 3.030	5.209 3.518	7.802 4.454	10.396 5.338
	From: EN To: PADM	t_{ZH} t_{ZL}	3.090 0.790	3.997 1.001	5.293 1.291	7.883 1.827	10.474 2.307

AMI350XXPF 0.35 micron CMOS Pad Library

Tristate Timing

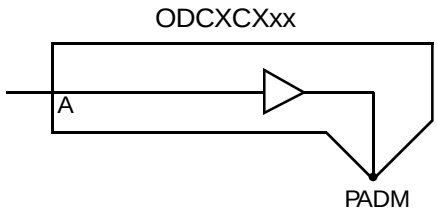
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXCE01	ODCXCE02	ODCXCE04	ODCXCE08	ODCXCE12
EN	PADM	t_{HZ} t_{LZ}	1.619 0.437	1.691 0.498	1.849 0.598	2.143 0.776	2.145 0.966

Description

ODCXCXxx is a family of 1 to 12 mA, 5-volt capable (cascode-gate), non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXCXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXCXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXCX01	ODCXCX02	ODCXCX04	ODCXCX08	ODCXCX12
A (eq-load)	3.7	3.7	3.7	3.7	3.7

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXCX01	1	109.225	312.6
ODCXCX02	2	109.225	323.8
ODCXCX04	4	109.225	346.0
ODCXCX08	8	109.225	387.5
ODCXCX12	12	109.225	406.9

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

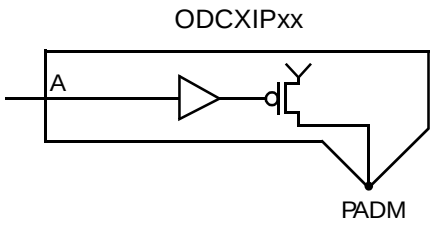
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXCX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	6.941 4.725	9.040 5.826	11.138 6.932	14.285 8.595	19.530 11.384
ODCXCX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.473 3.449	8.101 5.385	10.692 6.769	13.283 8.151	18.465 10.917
ODCXCX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.323 2.849	5.137 3.801	7.728 5.160	12.911 7.878	18.094 10.596
ODCXCX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.812 2.613	3.719 3.096	5.015 3.784	7.608 5.149	10.200 6.501
ODCXCX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.813 2.584	3.721 2.919	5.017 3.392	7.610 4.313	10.204 5.205

Description

ODCXIPxx is a family of 1 to 16 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12	ODCXIP16
A (eq-load)	2.5	2.6	2.6	4.0	5.6	5.6
PADM (pF)	5.00	5.00	5.01	5.02	5.04	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXIP01	1	98.535	206.1
ODCXIP02	2	99.639	211.1
ODCXIP04	4	100.743	218.9
ODCXIP08	8	102.952	233.9
ODCXIP12	12	106.264	250.8
ODCXIP16	16	106.264	263.3

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXIP01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZH}	4.313	6.516	8.718	12.022	17.528
ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	2.279	6.101	8.831	11.561	17.022
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.305	3.214	5.942	11.397	16.852
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.759	1.720	3.092	5.836	8.580
ODCXIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.585	1.222	2.131	3.949	5.768
ODCXIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.534	1.021	1.718	3.110	4.503

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

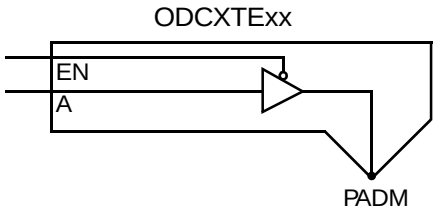
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**	**ODCXIP12**	**ODCXIP16**
A	PADM	t_{HZ}	0.446	0.379	0.406	0.433	0.421	0.504

Description

ODCXTExx is a family of 1 to 8 mA 5-volt tolerant, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODCXTE01	ODCXTE02	ODCXTE04	ODCXTE08
A (eq-load)	2.4	2.4	2.4	2.4
EN (eq-load)	7.9	7.9	7.9	7.9
PADM (pF)	5.05	5.05	5.05	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXTE01	1	116.610	360.6
ODCXTE02	2	116.610	365.1
ODCXTE04	4	116.610	374.4
ODCXTE08	8	116.610	393.5

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODCXTE01	From: A To: PADM	t_{PLH} t_{PHL}	5.118 2.610	7.322 3.716	9.526 4.823	12.832 6.482	18.338 9.248
	From: EN To: PADM	t_{ZH} t_{ZL}	4.973 2.567	7.179 3.674	9.385 4.780	12.695 6.440	18.211 9.206
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODCXTE02	From: A To: PADM	t_{PLH} t_{PHL}	2.823 1.516	6.653 3.436	9.388 4.807	12.124 6.178	17.594 8.921
	From: EN To: PADM	t_{ZH} t_{ZL}	2.685 1.473	6.515 3.393	9.250 4.765	11.985 6.137	17.455 8.880
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXTE04	From: A To: PADM	t_{PLH} t_{PHL}	1.719 1.008	3.631 1.964	6.364 3.329	11.829 6.059	17.294 8.789
	From: EN To: PADM	t_{ZH} t_{ZL}	1.581 0.962	3.493 1.919	6.225 3.285	11.690 6.017	17.154 8.749
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXTE08	From: A To: PADM	t_{PLH} t_{PHL}	1.216 0.814	2.170 1.289	3.533 1.967	6.260 3.323	8.986 4.680
	From: EN To: PADM	t_{ZH} t_{ZL}	1.077 0.756	2.031 1.237	3.394 1.921	6.120 3.282	8.845 4.633

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

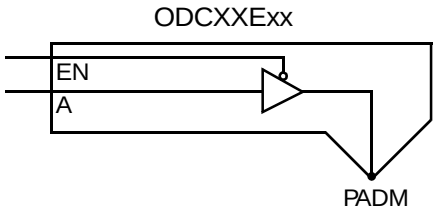
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCXTE01	ODCXTE02	ODCXTE04	ODCXTE08
EN	PADM	t_{HZ} t_{LZ}	0.620 0.415	0.739 0.441	0.991 0.495	1.637 0.595

Description

ODCXXExx is a family of 1 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
A (eq-load)	6.7	9.6	9.6	2.4	5.2	5.2	5.2
EN (eq-load)	4.5	6.0	6.0	5.5	7.6	7.6	7.6
PADM (pF)	5.00	5.00	5.01	5.02	5.04	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	100.935	213.7
ODCXXE02	2	104.440	225.5
ODCXXE04	4	104.440	237.0
ODCXXE08	8	118.795	292.9
ODCXXE12	12	129.838	329.3
ODCXXE16	16	129.838	352.5
ODCXXE24	24	129.838	368.9

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	4.269 2.916	6.471 4.308	8.674 5.699	11.978 7.786	17.484 11.265
	From: EN To: PADM	t_{ZH} t_{ZL}	4.351 2.910	6.554 4.302	8.756 5.693	12.059 7.781	17.565 11.260
ODCXXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.207 1.563	6.035 3.999	8.770 5.740	11.504 7.480	16.973 10.960
	From: EN To: PADM	t_{ZH} t_{ZL}	2.313 1.559	6.135 3.996	8.865 5.736	11.595 7.477	17.055 10.958
ODCXXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.256 1.036	3.165 2.269	5.893 4.025	11.349 7.515	16.806 10.978
	From: EN To: PADM	t_{ZH} t_{ZL}	1.358 1.026	3.267 2.261	5.995 4.019	11.450 7.511	16.906 10.973
ODCXXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.097 0.830	2.058 1.429	3.431 2.285	6.176 3.997	8.921 5.710
	From: EN To: PADM	t_{ZH} t_{ZL}	0.958 0.747	1.919 1.350	3.291 2.209	6.036 3.923	8.781 5.628
ODCXXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	0.778 0.617	1.414 1.023	2.324 1.599	4.143 2.740	5.962 3.865
	From: EN To: PADM	t_{ZH} t_{ZL}	0.712 0.640	1.348 1.047	2.258 1.624	4.077 2.766	5.896 3.890
ODCXXE16	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	0.723 0.598	1.210 0.913	1.906 1.358	3.299 2.226	4.691 3.068
	From: EN To: PADM	t_{ZH} t_{ZL}	0.656 0.620	1.143 0.938	1.840 1.384	3.233 2.255	4.626 3.094
ODCXXE24	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	0.730 0.575	1.216 0.805	1.912 1.123	3.302 1.722	4.693 2.272
	From: EN To: PADM	t_{ZH} t_{ZL}	0.655 0.600	1.143 0.832	1.839 1.151	3.232 1.752	4.625 2.301

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

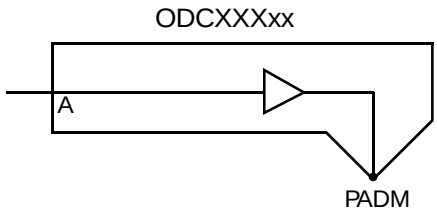
Delay (ns) From	To	Parameter	Cell						
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
EN	PADM	t_{HZ} t_{LZ}	0.613 0.234	0.504 0.198	0.630 0.266	0.403 0.479	0.381 0.523	0.433 0.566	0.433 0.626

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODCXXXxx is a family of 1 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12	ODCXXX16	ODCXXX24
A (eq-load)	4.6	4.6	7.4	10.1	10.1	10.1	10.1

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	98.533	206.8
ODCXXX02	2	98.533	213.2
ODCXXX04	4	100.741	224.9
ODCXXX08	8	102.950	249.5
ODCXXX12	12	102.950	273.4
ODCXXX16	16	102.950	296.7
ODCXXX24	24	102.950	313.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.203 2.766	6.404 4.156	8.605 5.546	11.907 7.632	17.411 11.108
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.227 1.579	6.052 4.011	8.784 5.748	11.517 7.486	16.983 10.960
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.194 0.892	3.104 2.110	5.834 3.849	11.293 7.326	16.753 10.804
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.708 0.575	1.667 1.181	3.037 2.043	5.778 3.757	8.518 5.458
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.602 0.560	1.237 0.970	2.143 1.550	3.956 2.693	5.769 3.814
ODCXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.577 0.578	1.062 0.902	1.755 1.355	3.140 2.231	4.525 3.065
ODCXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.621 0.526	1.102 0.801	1.791 1.119	3.177 1.693	4.575 2.267

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

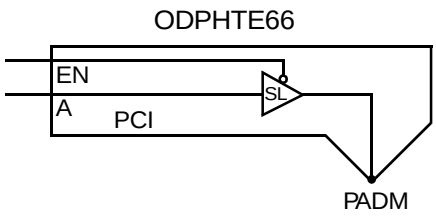
ODPHTE66

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODPHTE66 is a 3.3v drive ONLY, (33/66) MHz PSEUDO PCI compliant, 5V-Tolerant, non-inverting, tri-state buffer pad piece with controlled slew rate output. There is no high clamp diode (Ich) in this cell.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	6.2 eql
EN	8.5 eql
PADM	5.05 pF

HDL Syntax

Verilog ..... ODPHTE66 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPHTE66 port map (PADM, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	107.392	nA
EQL_{pd}	356.3	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

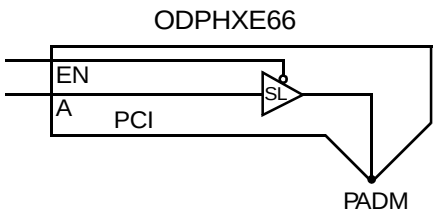
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.315 1.407	2.161 2.295	3.351 3.541	5.660 5.955	7.877 8.265
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	2.480 0.421 1.384 1.391	 2.227 2.285	 3.412 3.538	 5.713 5.963	 7.923 8.278

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODPHXE66 is a 3.3v drive ONLY, NON-5V tolerant, (33/66) MHz, PCI compliant, non-inverting, tri-state buffer piece with controlled slew rate output.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	9.1 eql
EN	9.2 eql
PADM	5.03 pF

HDL Syntax

Verilog ..... ODPHXE66 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPHXE66 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	106.268	nA
EQL_{pd}	384.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.975 1.112	1.838 1.835	3.034 2.809	5.293 4.552	7.376 6.023
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.734 0.937 1.118 1.224	 1.959 2.041	 3.127 3.025	 5.351 4.610	 7.423 6.166

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

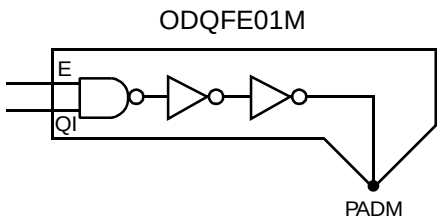
ODQFE01M

AMI350XXPF 0.35 micron CMOS Pad Library

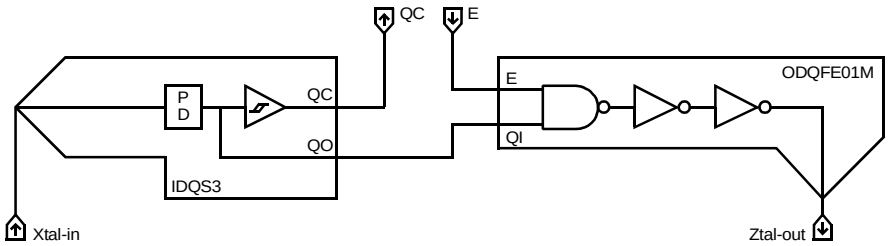
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	4.3 eql
QI	3.2 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	98.534	nA
EQL_{pd}	211.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	4.415 3.241	6.616 4.631	8.818 6.022	12.120 8.108	17.624 11.585
QI	PADM	t_{PLH} t_{PHL}	4.470 3.270	6.672 4.657	8.875 6.044	12.178 8.125	17.684 11.593

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

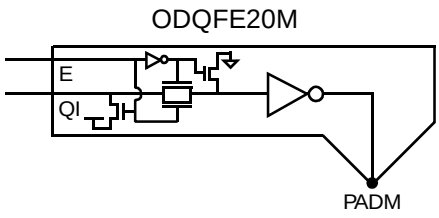
ODQFE20M

AMI350XXPF 0.35 micron CMOS Pad Library

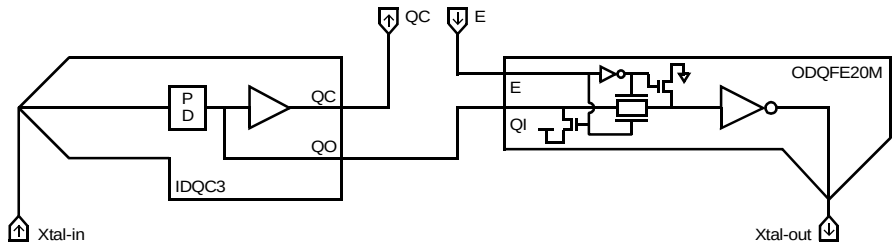
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	7.6 eql
QI	6.3 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	98.719	nA
EQL_{pd}	227.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	2.678 1.470	6.499 3.904	9.228 5.642	11.957 7.381	17.417 10.858
QI	PADM	t_{PLH} t_{PHL}	2.127 1.485	5.950 3.922	8.681 5.661	11.411 7.400	16.873 10.873

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

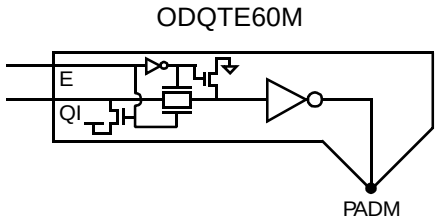
ODQTE60M

AMI350XXPF 0.35 micron CMOS Pad Library

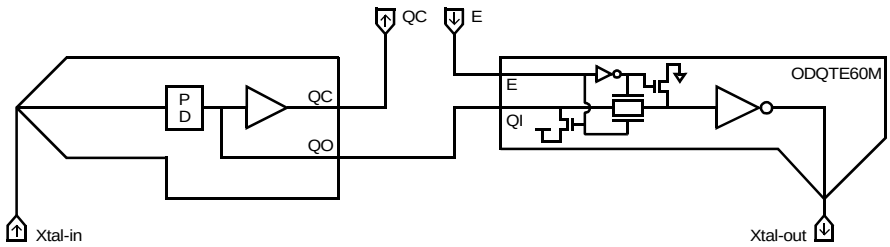
Description

ODQTE60M is an third-overtone mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	7.6 eql
QI	6.3 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	98.719	nA
EQL_{pd}	239.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	1.818 0.869	3.729 2.085	6.459 3.824	11.918 7.300	17.378 10.777
QI	PADM	t_{PLH} t_{PHL}	1.166 0.916	3.077 2.137	5.806 3.880	11.264 7.362	16.722 10.836

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

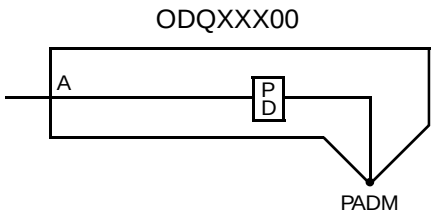
ODQXXX00

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.3 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

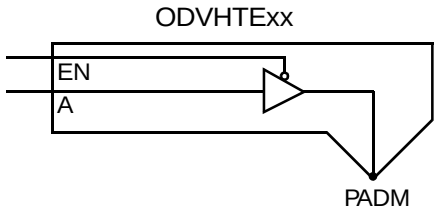
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	96.229	nA
EQL_{pd}	196.0	Eq-load

See page 2-13 for power equation.

Description

ODVHTExx is a 8 mA, 5 volt tolerant , high performance, non-inverting, LVTTL-level, tristate output buffer piece with active low enable output.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVHTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVHTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load
	ODVHTE08
A (eq-load)	2.4
EN (eq-load)	7.9
PADM (pF)	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHTE08	8	116.610	393.6

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHTE08	From: A To: PADM	t_{PLH} t_{PHL}	1.109 0.862	1.903 1.430	3.037 2.242	5.305 3.866	7.573 5.490
	From: EN To: PADM	t_{ZH} t_{ZL}	0.970 0.805	1.764 1.378	2.897 2.195	5.165 3.824	7.432 5.444

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

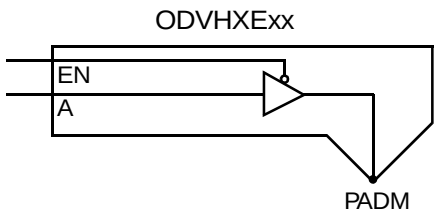
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns)		Parameter	Cell
From	To		ODVHTE08
EN	PADM	t_{HZ} t_{LZ}	1.577 0.578

Description

ODVHXExx is a family of 8 to 24 mA, non-inverting. TTL-level, tristate output buffer pieces with active low enable outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVHXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVHXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODVHXEODVHTE12	ODVHXE12	ODVHXE16	ODVHXE24
A (eq-load)	5.2	5.2	5.2	5.2
EN (eq-load)	7.6	7.6	7.6	7.6
PADM (pF)	5.02	5.04	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHXE08	8	129.838	305.4
ODVHXE12	12	129.838	329.3
ODVHXE16	16	129.838	352.6
ODVHXE24	24	129.838	369.0

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHXE08	From: A To: PADM	t_{PLH} t_{PHL}	0.824 0.735	1.622 1.453	2.762 2.478	5.041 4.530	7.321 6.581
	From: EN To: PADM	t_{ZH} t_{ZL}	0.758 0.760	1.556 1.478	2.696 2.504	4.976 4.556	7.256 6.607
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.709 0.652	1.239 1.134	1.995 1.821	3.507 3.185	5.020 4.538
	From: EN To: PADM	t_{ZH} t_{ZL}	0.643 0.676	1.173 1.159	1.929 1.847	3.441 3.212	4.954 4.563
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.664 0.621	1.068 0.992	1.644 1.518	2.798 2.554	3.951 3.568
	From: EN To: PADM	t_{ZH} t_{ZL}	0.597 0.643	1.001 1.016	1.578 1.544	2.732 2.582	3.886 3.593
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHXE24	From: A To: PADM	t_{PLH} t_{PHL}	0.670 0.592	1.073 0.856	1.649 1.224	2.802 1.930	3.954 2.596
	From: EN To: PADM	t_{ZH} t_{ZL}	0.597 0.615	1.001 0.881	1.578 1.252	2.732 1.959	3.886 2.623

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

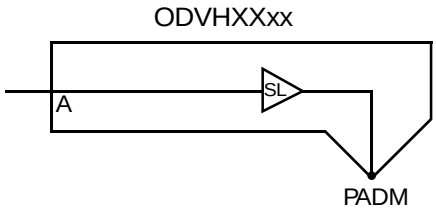
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ODVHXE08	ODVHXE12	ODVHXE16	ODVHXE24
EN	PADM	t_{HZ} t_{LZ}	0.318 0.465	0.361 0.508	0.409 0.544	0.409 0.598

Description

ODVHXXxx is a family of 4 to 24 mA, non-inverting, LVTTL-level, output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVHXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVHXXxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODVHXX08	ODVHXX12	ODVHXX16	ODVHXX24
A (eq-load)	18.9	18.9	18.9	18.9

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHXX08	8	109.576	254.3
ODVHXX12	12	109.576	278.2
ODVHXX16	16	109.576	301.4
ODVHXX24	24	109.576	317.8

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

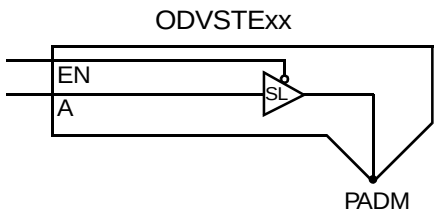
ODVHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.551	1.349	2.489	4.768	7.047
	To: PADM	t_{PLH}	0.533	1.251	2.277	4.329	6.381
ODVHXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.445	0.974	1.729	3.241	4.752
	To: PADM	t_{PLH}	0.459	0.935	1.615	2.974	4.333
ODVHXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.405	0.808	1.384	2.535	3.687
	To: PADM	t_{PLH}	0.433	0.798	1.316	2.344	3.362
ODVHXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.433	0.835	1.408	2.554	3.701
	To: PADM	t_{PLH}	0.377	0.630	0.985	1.680	2.354

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODVSTExx is a family of 4 to 8 mA, 5 volt tolerant, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVSTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVSTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load	
	ODVSTE04	ODVSTE08
A (eq-load)	2.4	2.4
EN (eq-load)	7.9	7.9
PADM (pF)	5.05	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSTE04	4	113.300	482.4
ODVSTE08	8	113.300	501.5

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVSTE04	From: A To: PADM	t_{PLH} t_{PHL}	2.872 2.313	4.568 3.851	6.955 5.770	11.603 9.051	16.084 12.356
	From: EN To: PADM	t_{ZH} t_{ZL}	2.663 2.258	4.356 3.804	6.741 5.560	11.385 8.915	15.865 12.189
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSTE08	From: A To: PADM	t_{PLH} t_{PHL}	2.241 1.910	3.289 2.920	4.608 4.026	6.894 5.861	9.210 7.464
	From: EN To: PADM	t_{ZH} t_{ZL}	2.062 1.492	3.107 2.798	4.425 3.925	6.716 5.704	9.039 7.423

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

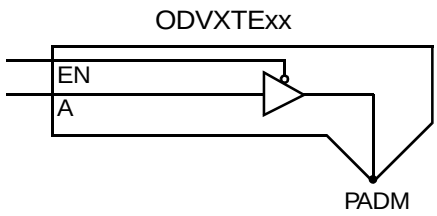
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODVSTE04	Cell ODVSTE08
EN	PADM	t_{HZ} t_{LZ}	8.406 0.697	9.238 0.798

Description

ODVXTExx is a family of 1 to 8 mA, 5-volt tolerant, non-inverting, LVTTL-level, tristate output buffer pieces with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVXTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVXTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODVXTE01	ODVXTE02	ODVXTE04	ODVXTE08
A (eq-load)	2.4	2.4	2.4	2.4
EN (eq-load)	7.9	7.9	7.9	7.9
PADM (pF)	5.05	5.05	5.05	5.05

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXTE01	1	116.610	360.6
ODVXTE02	2	116.610	365.1
ODVXTE04	4	116.610	374.4
ODVXTE08	8	116.610	393.5

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODVXTE01	From: A To: PADM	t_{PLH} t_{PHL}	4.343 3.072	6.179 4.393	8.016 5.714	10.771 7.695	15.363 10.998
	From: EN To: PADM	t_{ZH} t_{ZL}	4.208 3.031	6.044 4.352	7.881 5.672	10.635 7.653	15.226 10.955
	Capacitive Load (pF)		15	50	75	100	150 (max)
ODVXTE02	From: A To: PADM	t_{PLH} t_{PHL}	2.442 1.739	5.629 4.038	7.905 5.680	10.182 7.322	14.734 10.606
	From: EN To: PADM	t_{ZH} t_{ZL}	2.305 1.695	5.491 3.995	7.767 5.637	10.043 7.280	14.595 10.566
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVXTE04	From: A To: PADM	t_{PLH} t_{PHL}	1.527 1.119	3.118 2.264	5.390 3.899	9.934 7.169	14.479 10.440
	From: EN To: PADM	t_{ZH} t_{ZL}	1.388 1.072	2.979 2.218	5.251 3.854	9.795 7.127	14.339 10.400
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVXTE08	From: A To: PADM	t_{PLH} t_{PHL}	1.118 0.868	1.912 1.437	3.046 2.249	5.315 3.873	7.583 5.498
	From: EN To: PADM	t_{ZH} t_{ZL}	0.978 0.810	1.772 1.385	2.906 2.203	5.174 3.832	7.442 5.452

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

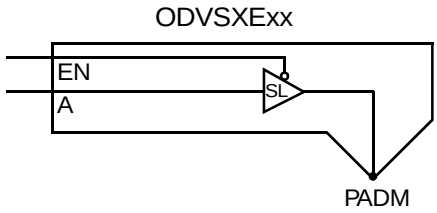
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODVXTE01	ODVXTE02	ODVXTE04	ODVXTE08
EN	PADM	t_{HZ} t_{LZ}	0.620 0.415	0.739 0.441	0.991 0.495	1.638 0.594

Description

ODVSXExx is a family of 4 to 24 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODVSXE04	ODVSXE08	ODVSXE12	ODVSXE16	ODVSXE24
A (eq-load)	2.4	2.5	2.4	2.4	2.4
EN (eq-load)	6.2	6.2	6.2	6.2	6.2
PADM (pF)	5.01	5.02	5.04	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXE04	4	113.278	372.2
ODVSXE08	8	113.278	395.0
ODVSXE12	12	113.278	419.0
ODVSXE16	16	113.278	442.2
ODVSXE24	24	113.278	458.6

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.279 2.424	4.028 4.550	6.473 6.855	11.168 11.018	15.604 15.307
	From: EN To: PADM	t_{ZH} t_{ZL}	2.213 2.713	3.916 4.497	6.311 6.823	10.969 11.029	15.450 15.255
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.793 1.871	2.827 3.225	4.111 4.523	6.502 6.713	8.723 8.842
	From: EN To: PADM	t_{ZH} t_{ZL}	1.733 2.174	2.756 3.327	4.061 4.642	6.366 6.736	8.706 8.929
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.501 1.736	2.393 2.831	3.428 3.872	5.010 5.512	6.580 6.930
	From: EN To: PADM	t_{ZH} t_{ZL}	1.626 2.049	2.416 2.964	3.368 4.003	4.925 5.522	6.503 6.995
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.443 1.541	2.232 2.575	3.121 3.564	4.397 4.890	5.613 6.053
	From: EN To: PADM	t_{ZH} t_{ZL}	1.597 2.014	2.296 2.831	3.105 3.736	4.335 4.987	5.542 6.148
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.436 1.383	2.225 2.313	3.114 3.177	4.394 4.241	5.610 5.179
	From: EN To: PADM	t_{ZH} t_{ZL}	1.596 1.978	2.295 2.667	3.105 3.420	4.335 4.417	5.542 5.281

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

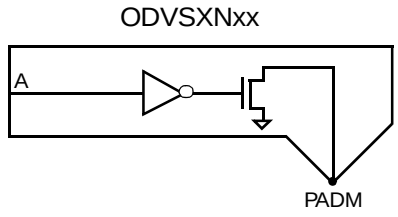
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODVSXE04	ODVSXE08	ODVSXE12	ODVSXE16	ODVSXE24
EN	PADM	t_{HZ} t_{LZ}	0.515 0.470	0.603 0.515	0.689 0.562	0.779 0.606	0.779 0.668

Description

ODVSXNxx is a family of 4 to 24 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODVSXN04	ODVSXN08	ODVSXN12	ODVSXN16	ODVSXN24
A (eq-load)	6.0	6.0	6.0	6.0	6.0
PADM (pF)	5.00	5.00	5.00	5.00	5.00

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXN04	4	102.953	324.3
ODVSXN08	8	102.953	334.7
ODVSXN12	12	102.953	346.3
ODVSXN16	16	102.953	357.0
ODVSXN24	24	102.953	373.4

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVSXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.615	4.245	6.517	10.859	14.931
ODVSXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.083	3.147	4.441	6.570	8.705
ODVSXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.942	2.814	3.818	5.330	6.803
ODVSXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.915	2.691	3.566	4.812	5.973
ODVSXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.896	2.544	3.266	4.255	5.110

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

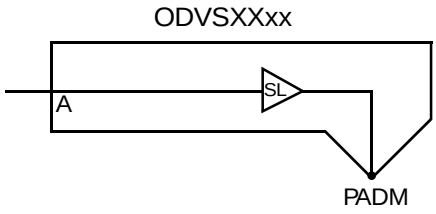
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODVSXN04	**ODVSXN08**	**ODVSXN12**	**ODVSXN16**	**ODVSXN24**
A	PADM	t_{HZ}	0.190	0.236	0.290	0.341	0.409

Description

ODVSXXxx is a family of 4 to 24 mA, non-inverting, LVTTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog..... ODVSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODVSXX04	ODVSXX08	ODVSXX12	ODVSXX16	ODVSXX24
A (eq-load)	3.8	3.8	3.8	3.8	3.8

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXX04	4	110.684	363.2
ODVSXX08	8	110.684	386.0
ODVSXX12	12	110.684	409.9
ODVSXX16	16	110.684	433.2
ODVSXX24	24	110.684	449.6

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

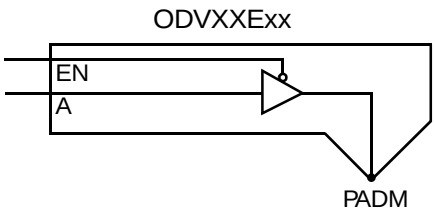
ODVSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.918 2.400	3.805 4.371	6.284 6.669	10.819 10.857	15.387 15.127
ODVSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.447 1.657	2.549 3.050	3.841 4.359	6.206 6.553	8.470 8.685
ODVSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.187 1.497	2.085 2.593	3.130 3.677	4.726 5.345	6.294 6.723
ODVSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.144 1.340	1.929 2.338	2.820 3.405	4.113 4.758	5.328 5.937
ODVSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.155 1.265	1.933 2.116	2.821 3.027	4.117 4.154	5.331 5.052

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODVXXExx is a family of 1 to 24 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	XXE01	ODVXXE02	ODVXXE04	ODVXXE08	ODVXXE12	ODVXXE16	ODVXXE24
A (eq-load)	6.7	9.6	9.6	2.4	5.2	5.2	5.2
EN (eq-load)	4.5	6.0	6.0	5.5	7.6	7.6	7.6
PADM (pF)	5.00	5.00	5.01	5.02	5.04	5.06	5.06

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXE01	1	100.935	213.7
ODVXXE02	2	104.440	225.5
ODVXXE04	4	104.440	237.0
ODVXXE08	8	118.795	292.9
ODVXXE12	12	129.838	329.3
ODVXXE16	16	129.838	352.5
ODVXXE24	24	129.838	368.9

a. See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	3.593 3.420	5.424 5.087	7.255 6.754	10.001 9.255	14.579 13.423
	From: EN To: PADM	t_{ZH} t_{ZL}	3.676 3.414	5.507 5.081	7.338 6.749	10.084 9.249	14.662 13.417
ODVXXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.871 1.816	5.056 4.734	7.332 6.819	9.608 8.903	14.159 13.072
	From: EN To: PADM	t_{ZH} t_{ZL}	1.969 1.812	5.153 4.730	7.428 6.815	9.702 8.900	14.251 13.069
ODVXXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.062 1.165	2.653 2.638	4.926 4.737	9.471 8.915	14.016 13.069
	From: EN To: PADM	t_{ZH} t_{ZL}	1.181 1.155	2.771 2.630	5.042 4.730	9.583 8.911	14.125 13.063
ODVXXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.011 0.893	1.810 1.611	2.950 2.637	5.230 4.689	7.510 6.741
	From: EN To: PADM	t_{ZH} t_{ZL}	0.872 0.813	1.670 1.532	2.810 2.558	5.090 4.611	7.370 6.663
ODVXXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	0.720 0.661	1.249 1.145	2.006 1.833	3.518 3.199	5.031 4.550
	From: EN To: PADM	t_{ZH} t_{ZL}	0.654 0.686	1.184 1.170	1.940 1.859	3.453 3.225	4.966 4.576
ODVXXE16	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	0.678 0.632	1.082 1.006	1.659 1.534	2.813 2.572	3.967 3.584
	From: EN To: PADM	t_{ZH} t_{ZL}	0.607 0.655	1.014 1.031	1.594 1.561	2.749 2.600	3.898 3.611
ODVXXE24	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	0.685 0.602	1.088 0.869	1.664 1.242	2.817 1.952	3.969 2.616
	From: EN To: PADM	t_{ZH} t_{ZL}	0.607 0.627	1.014 0.896	1.594 1.271	2.749 1.982	3.898 2.645

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

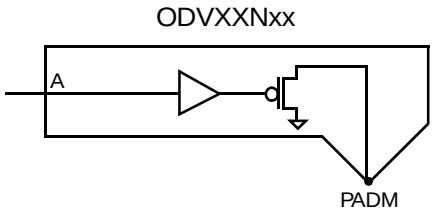
Delay (ns) From	To	Parameter	Cell						
			ODVXXE01	ODVXXE02	ODVXXE04	ODVXXE08	ODVXXE12	ODVXXE16	ODVXXE24
EN	PADM	t_{HZ}	0.613	0.504	0.630	0.403	0.381	0.433	0.433
		t_{LZ}	0.234	0.198	0.266	0.479	0.523	0.566	0.626

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODVXXNxx is a family of 1 to 24 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVXXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODVXXN01	ODVXXN02	ODVXXN04	ODVXXN08	ODVXXN12	ODVXXN16	ODVXXN24
A (eq-load)	4.8	4.8	4.8	7.3	7.3	10.2	10.2
PADM (pF)	4.99	5.00	5.00	5.00	5.00	5.00	5.00

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXN01	1	98.533	201.3
ODVXXN02	2	98.533	204.2
ODVXXN04	4	98.533	210.1
ODVXXN08	8	100.741	221.5
ODVXXN12	12	100.741	233.1
ODVXXN16	16	102.950	244.8
ODVXXN24	24	102.950	261.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXXN01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZL}	3.155	4.821	6.488	8.988	13.155
ODVXXN02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZL}	1.681	4.598	6.682	8.766	12.934
ODVXXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.996	2.456	4.541	8.712	12.883
ODVXXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.566	1.284	2.309	4.359	6.409
ODVXXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.490	0.976	1.666	3.033	4.381
ODVXXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.399	0.769	1.293	2.326	3.340
ODVXXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.361	0.641	1.003	1.693	2.375

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

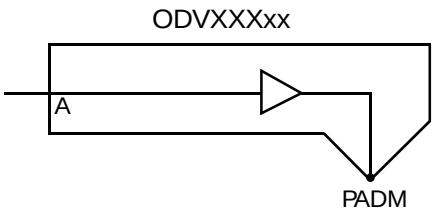
Delay (ns) From	To	Parameter	Cell						
			ODVXXN01	**ODVXXN02**	**ODVXXN04**	**ODVXXN08**	**ODVXXN12**	**ODVXXN16**	**ODVXXN24**
A	PADM	t_{HZ}	0.139	0.171	0.240	0.218	0.282	0.262	0.320

AMI350XXPF 0.35 micron CMOS Pad Library

Description

ODVXXXxx is a family of 1 to 24 mA, non-inverting, LVTTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODVXXX01	ODVXXX02	ODVXXX04	ODVXXX08	ODVXXX12	ODVXXX16	ODVXXX24
A (eq-load)	4.6	4.6	7.4	10.1	10.1	10.1	10.1

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXX01	1	98.533	206.8
ODVXXX02	2	98.533	213.2
ODVXXX04	4	100.741	224.9
ODVXXX08	8	102.950	249.5
ODVXXX12	12	102.950	273.4
ODVXXX16	16	102.950	296.7
ODVXXX24	24	102.950	313.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

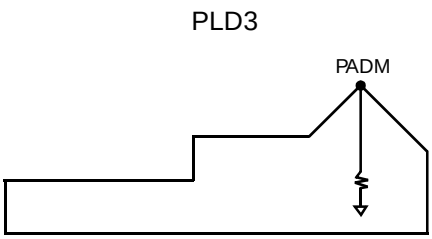
ODVXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.528 3.267	5.360 4.932	7.193 6.596	9.941 9.092	14.523 13.253
ODVXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.876 1.836	5.059 4.752	7.333 6.834	9.607 8.917	14.155 13.082
ODVXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.011 1.019	2.600 2.477	4.870 4.561	9.411 8.727	13.952 12.893
ODVXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.621 0.642	1.417 1.364	2.556 2.394	4.832 4.447	7.108 6.490
ODVXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.542 0.602	1.070 1.092	1.824 1.786	3.332 3.155	4.840 4.497
ODVXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.529 0.612	0.931 0.995	1.506 1.534	2.655 2.579	3.803 3.581
ODVXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.575 0.567	0.973 0.843	1.543 1.224	2.691 1.942	3.849 2.602

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

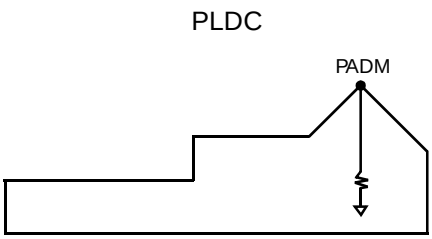
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.598	nA
EQL_{pd}	196.9	Eq-load

See page 2-13 for power equation.

Description

PLDC is a 5-volt capable (cascode-gate) active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLDC *inst_name* (PADM);

VHDL..... *inst_name*: PLDC port map (PADM);

Power Characteristics

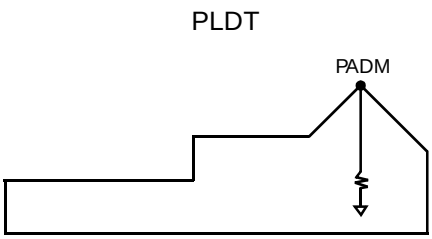
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.448	nA
EQL_{pd}	175.9	Eq-load

See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

PLDT is a 5-volt tolerant active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLDT *inst_name* (PADM);

VHDL..... *inst_name*: PLDT port map (PADM);

Power Characteristics

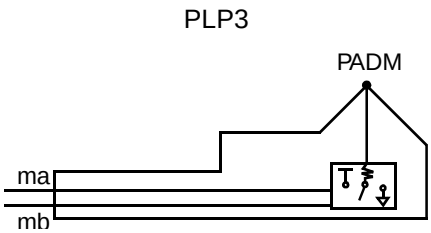
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.453	nA
EQL_{pd}	176.0	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.0 eql
MB	2.7 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.598	nA
EQL_{pd}	193.1	Eq-load

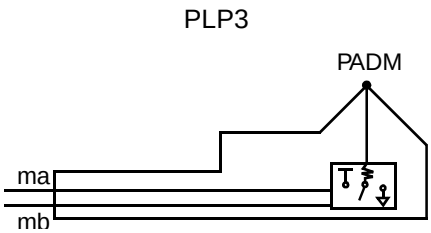
See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

PLPT is a programmable pull-up/pull-down buffer piece for use in 5 volt tolerant applications.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	1.6 eql
MB	1.3 eql

HDL Syntax

Verilog ..... PLPT *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLPT port map (PADM, MA, MB);

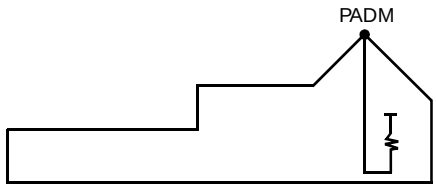
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.053	nA
EQL_{pd}	182.9	Eq-load

See page 2-13 for power equation.

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3  	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

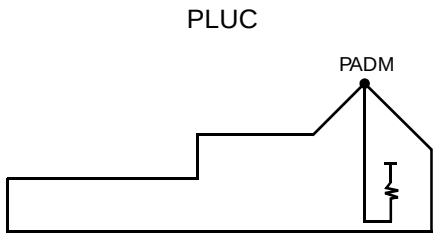
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.598	nA
EQL_{pd}	196.7	Eq-load

See page 2-13 for power equation.

AMI350XXPF 0.35 micron CMOS Pad Library

Description

PLUC is a 5-volt capable (cascode-gate) active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLUC *inst_name* (PADM);

VHDL..... *inst_name*: PLUC port map (PADM);

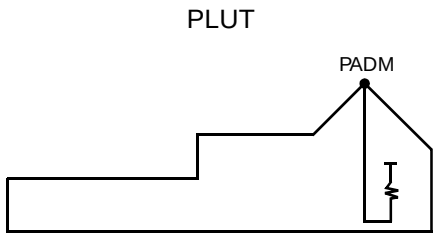
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.709	nA
EQL_{pd}	171.9	Eq-load

See page 2-13 for power equation.

Description

PLUT is a 5-volt tolerant active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLUT *inst_name* (PADM);

VHDL..... *inst_name*: PLUT port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.709	nA
EQL_{pd}	171.9	Eq-load

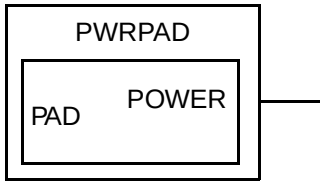
See page 2-13 for power equation.

PWRPAD

AMI350XXPF 0.35 micron CMOS Pad Library

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

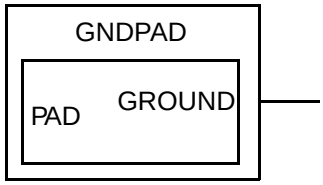
```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses
- VDD_5V is the chip port name
- SS1 is the chip port name

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
         port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses

VSS1 is the chip port name

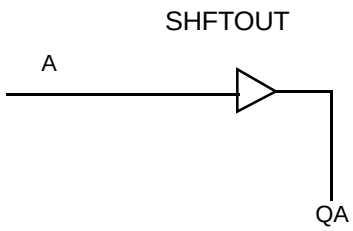
SHFTOUT

AMI350XXPF 0.35 micron CMOS Pad Library

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	5.3

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.904	nA
EQL_{pd}	10.5	eql

Propagation Delays *See note at beginning of section to compute total delay.

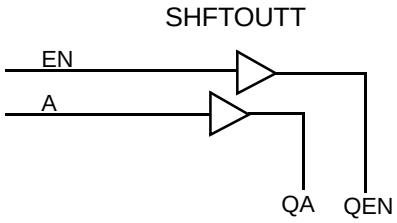
Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	6	12	17	23 (max)
A	QA	t_{PLH} t_{PHL}	0.117 0.094	0.155 0.128	0.201 0.163	0.240 0.191	0.287 0.228

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	4.1
EN(eql)	3.8

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.905	nA
EQL_{pd}	12.0	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.129 0.193	0.160 0.265	0.207 0.370	0.269 0.505	0.316 0.604
EN	QEN	t_{PLH} t_{PHL}	0.122 0.187	0.154 0.262	0.202 0.366	0.265 0.497	0.311 0.591%%%Created