0.35 Micron CMOS Core Library
Standard Cell Datasheets
AMI350LXSC 3.3 Volt
Section 3
Revision 1.1

Simple Gates

Complex Gates

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AMI350LXSC 0.35 micron CMOS Standard Cell

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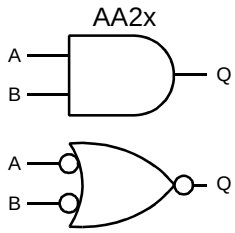
DATASHEETS

Description

AA2x is a family of 2-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... AA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: AA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	AA21	AA22	AA24	AA26
A	1.0	1.0	2.0	2.0
B	1.0	1.0	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA21	1.2	1.089	2.2
AA22	1.2	1.489	3.4
AA24	2.0	2.978	6.1
AA26	2.2	3.778	8.6

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

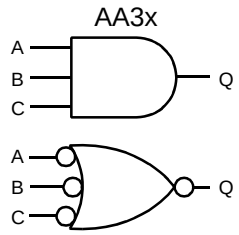
AA21	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.186 0.184	0.320 0.319	0.495 0.483	0.710 0.682	0.881 0.843
AA22	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.182 0.187	0.334 0.348	0.498 0.510	0.638 0.647	0.795 0.799
AA24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.151 0.162	0.299 0.323	0.449 0.471	0.584 0.604	0.720 0.743
AA26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.174 0.164	0.326 0.349	0.465 0.498	0.598 0.624	0.739 0.745

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA3x is a family of 3-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

HDL Syntax

Verilog ..... AA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AA31	AA32	AA34	AA36
A	1.1	1.1	2.0	3.0
B	1.0	1.1	2.0	2.9
C	1.1	1.1	2.1	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA31	1.5	1.313	2.6
AA32	1.5	1.713	4.0
AA34	3.0	3.427	8.2
AA36	4.2	5.140	11.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} =3.3V Typical Process

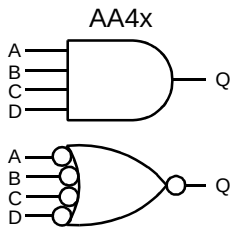
AA31	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.216 0.220	0.350 0.356	0.527 0.514	0.747 0.707	0.922 0.871
AA32	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.225 0.223	0.381 0.392	0.549 0.559	0.692 0.696	0.853 0.846
AA34	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.184 0.186	0.334 0.354	0.487 0.491	0.623 0.622	0.768 0.771
AA36	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.172 0.172	0.330 0.347	0.469 0.487	0.596 0.612	0.725 0.736

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA4x is a family of 4-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

HDL Syntax

Verilog ..... AA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AA41	AA42	AA44	AA46
A	1.0	1.0	3.0	3.0
B	1.1	1.1	2.9	2.9
C	1.1	1.1	2.9	2.9
D	1.1	1.1	2.9	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQLpd (Eq-load)
AA41	1.7	1.490	3.0
AA42	1.7	1.890	4.3
AA44	4.5	4.868	10.4
AA46	4.8	5.668	12.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

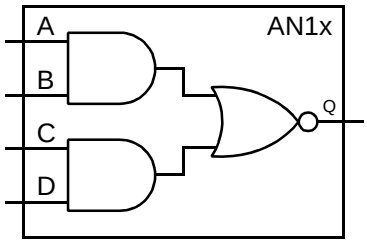
AA41	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.231 0.235	0.370 0.380	0.551 0.553	0.773 0.756	0.950 0.911
AA42	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.250 0.252	0.409 0.429	0.581 0.592	0.727 0.728	0.891 0.883
AA44	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.216 0.171	0.339 0.332	0.477 0.485	0.616 0.619	0.767 0.755
AA46	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.205 0.208	0.366 0.359	0.512 0.494	0.643 0.625	0.776 0.766

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN1x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

HDL Syntax

Verilog ..... AN1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN11	AN12	AN14	AN16
A	1.1	1.0	1.1	2.0
B	1.1	1.0	1.1	2.0
C	1.0	1.0	1.0	2.0
D	1.1	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN11	1.5	1.387	2.0
AN12	2.5	2.466	5.8
AN14	2.7	2.866	7.5
AN16	5.0	5.732	14.6

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

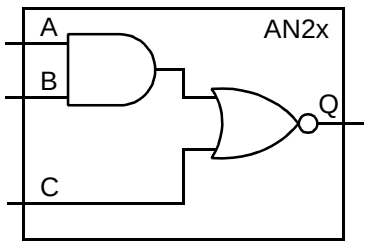
AN11	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.195 0.185	0.294 0.251	0.582 0.425	0.858 0.594	1.037 0.711
AN12	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.257 0.281	0.389 0.413	0.561 0.583	0.776 0.788	0.949 0.950
AN14	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.274 0.305	0.416 0.466	0.579 0.631	0.722 0.769	0.887 0.922
AN16	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.215 0.251	0.359 0.417	0.510 0.569	0.648 0.702	0.793 0.839

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN2x is a family of AND-NOR circuits consisting of one 2-input AND gate and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

HDL Syntax

Verilog ..... AN2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AN2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AN21	AN22	AN24	AN26
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN21	1.2	0.609	1.6
AN22	2.2	2.178	5.6
AN24	2.5	2.578	7.2
AN26	4.0	4.755	13.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

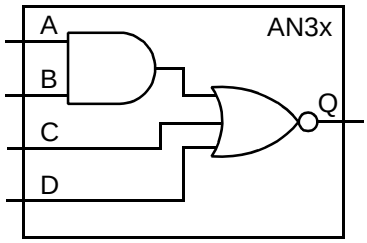
AN21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.155 0.198	0.235 0.276	0.467 0.490	0.695 0.700	0.846 0.841
AN22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.258 0.283	0.393 0.421	0.567 0.591	0.781 0.793	0.950 0.950
AN24	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.272 0.304	0.419 0.469	0.584 0.636	0.727 0.774	0.890 0.927
AN26	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.215 0.246	0.367 0.418	0.512 0.563	0.646 0.699	0.793 0.847

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN3x is a family of AND-NOR circuits consisting of one 2-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... AN3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN31	AN32	AN34	AN36
A	1.0	1.0	1.1	2.0
B	1.0	1.0	1.1	2.0
C	1.1	1.0	1.1	2.0
D	1.0	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN31	1.5	0.817	1.9
AN32	2.5	2.194	6.0
AN34	2.7	2.594	7.5
AN36	4.2	5.188	14.9

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

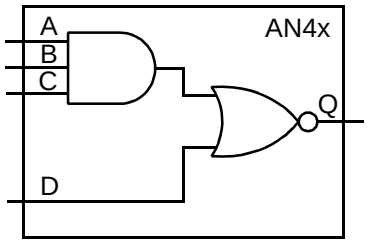
AN31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.174 0.239	0.281 0.335	0.490 0.515	0.592 0.601	0.793 0.771
AN32	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.266 0.299	0.395 0.430	0.569 0.597	0.788 0.799	0.964 0.959
AN34	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.265 0.299	0.414 0.463	0.577 0.628	0.718 0.764	0.877 0.913
AN36	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.226 0.261	0.374 0.419	0.515 0.569	0.652 0.702	0.806 0.839

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN4x is a family of AND-NOR circuits consisting of one 3-input AND gate, and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

HDL Syntax

Verilog ..... AN4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN41	AN42	AN44	AN46
A	1.0	1.1	1.0	2.0
B	1.0	1.1	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.1	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN41	1.5	0.657	2.3
AN42	2.5	2.402	6.0
AN44	2.7	2.802	7.7
AN46	4.8	5.204	14.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

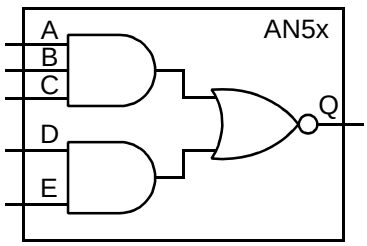
AN41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.185 0.241	0.276 0.331	0.450 0.498	0.534 0.582	0.698 0.764
AN42	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.292 0.315	0.425 0.445	0.597 0.616	0.807 0.828	0.974 0.997
AN44	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.303 0.339	0.448 0.495	0.610 0.660	0.750 0.801	0.909 0.958
AN46	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.239 0.351	0.390 0.521	0.533 0.668	0.667 0.796	0.817 0.938

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN5x is a family of AND-NOR circuits consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN52	AN54	AN56
A	1.0	1.1	2.0
B	1.0	1.1	2.0
C	1.0	1.0	2.0
D	1.1	1.1	2.0
E	1.0	1.1	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN52	2.7	2.690	6.4
AN54	3.0	3.090	8.0
AN56	5.8	6.181	16.3

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

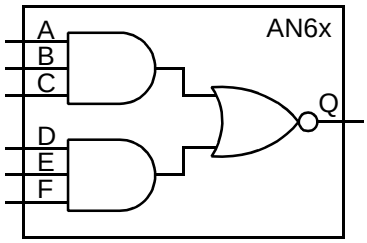
AN52	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.296 0.329	0.428 0.463	0.601 0.630	0.819 0.831	0.995 0.987
AN54	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.304 0.346	0.451 0.508	0.616 0.674	0.759 0.812	0.921 0.966
AN56	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.251 0.303	0.403 0.455	0.543 0.594	0.677 0.729	0.836 0.881

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN6x is a family of AND-NOR circuits consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN62	AN64	AN66
A	1.1	1.0	2.0
B	1.1	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.1	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN62	3.0	2.915	7.0
AN64	3.2	3.315	8.4
AN66	6.2	6.630	17.0

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

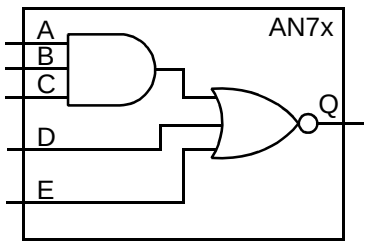
AN62	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.318 0.339	0.443 0.470	0.608 0.635	0.819 0.837	0.991 0.997
AN64	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.306 0.347	0.458 0.507	0.621 0.671	0.758 0.809	0.912 0.961
AN66	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.247 0.290	0.402 0.450	0.543 0.595	0.676 0.731	0.822 0.873

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN7x is a family of AND-NOR circuits consisting of one 3-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN72	AN74	AN76
A	1.1	1.0	2.0
B	1.0	1.0	2.0
C	1.1	1.0	2.0
D	1.0	1.1	2.0
E	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN72	2.7	2.418	6.6
AN74	3.0	2.818	8.1
AN76	5.0	5.636	15.7

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

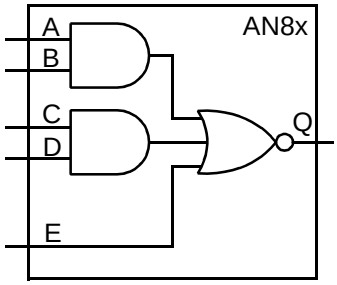
AN72	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.301 0.329	0.430 0.461	0.606 0.631	0.829 0.840	1.006 1.005
AN74	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.308 0.347	0.443 0.515	0.608 0.683	0.755 0.821	0.926 0.972
AN76	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.251 0.294	0.402 0.451	0.547 0.607	0.676 0.744	0.810 0.885

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN8x is a family of AND-NOR circuits consisting of two 2-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN82	AN84	AN86
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.1	1.0	2.0
D	1.1	1.1	2.0
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN82	3.2	3.091	8.1
AN84	3.5	3.491	9.8
AN86	6.0	6.981	18.7

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

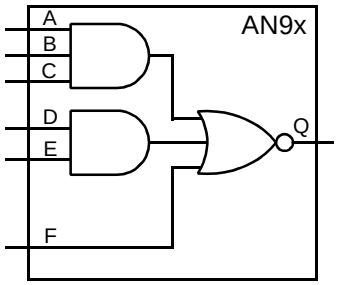
AN82	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.298 0.326	0.434 0.462	0.608 0.631	0.820 0.833	0.986 0.990
AN84	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.303 0.333	0.451 0.490	0.618 0.661	0.764 0.806	0.930 0.969
AN86	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.244 0.279	0.402 0.458	0.560 0.604	0.700 0.736	0.845 0.884

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN9x is a family of AND-NOR circuits consisting of one 3-input AND gate, one 2-input AND gate, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN92	AN94	AN96
A	1.1	1.0	2.0
B	1.1	1.0	2.0
C	1.1	1.0	2.0
D	1.0	1.0	2.1
E	1.1	1.1	2.1
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN92	3.5	3.315	8.7
AN94	3.5	3.715	10.0
AN96	6.8	7.430	19.5

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

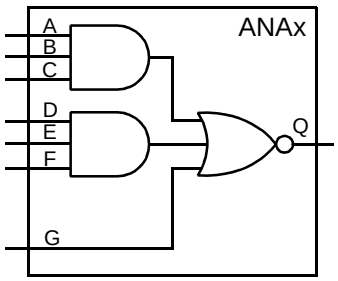
AN92	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.331 0.368	0.467 0.501	0.642 0.670	0.854 0.875	1.021 1.037
AN94	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.330 0.371	0.484 0.542	0.651 0.708	0.793 0.841	0.953 0.987
AN96	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.268 0.304	0.419 0.484	0.562 0.629	0.701 0.761	0.856 0.913

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANAx is a family of AND-NOR circuits consisting of two 3-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANAx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANA2	ANA4	ANA6
A	1.1	1.0	2.0
B	1.1	1.0	2.0
C	1.0	1.0	2.0
D	1.1	1.1	2.0
E	1.1	1.1	2.0
F	1.1	1.1	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANA2	3.8	3.539	9.1
ANA4	3.8	3.939	10.6
ANA6	7.5	7.879	20.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

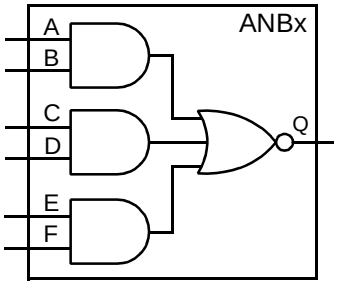
ANA2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.324 0.366	0.458 0.502	0.635 0.669	0.856 0.870	1.031 1.031
ANA4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.333 0.376	0.488 0.544	0.654 0.712	0.795 0.849	0.953 1.000
ANA6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.279 0.303	0.444 0.476	0.592 0.638	0.726 0.769	0.876 0.918

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANBx is a family of AND-NOR circuits consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... ANBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ANBx port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ANB2	ANB4	ANB6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.1	2.0
D	1.1	1.0	2.0
E	1.0	1.1	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANB2	3.5	3.379	8.4
ANB4	3.8	3.779	10.1
ANB6	7.0	7.558	19.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

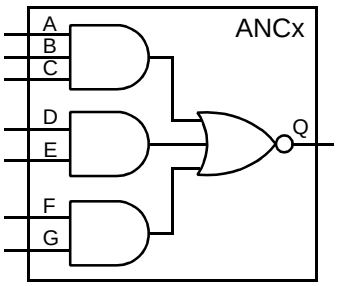
ANB2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.298 0.325	0.433 0.461	0.607 0.632	0.825 0.839	0.999 1.002
ANB4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.306 0.339	0.462 0.510	0.627 0.677	0.766 0.814	0.923 0.963
ANB6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.244 0.284	0.406 0.455	0.560 0.614	0.695 0.752	0.834 0.894

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANCx is a family of AND-NOR circuits consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANC2	ANC4	ANC6
A	1.1	1.0	2.0
B	1.1	1.0	2.0
C	1.1	1.0	2.0
D	1.0	1.0	2.0
E	1.1	1.1	2.0
F	1.1	1.1	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANC2	4.0	3.603	8.9
ANC4	4.0	4.003	10.4
ANC6	7.8	8.007	20.1

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

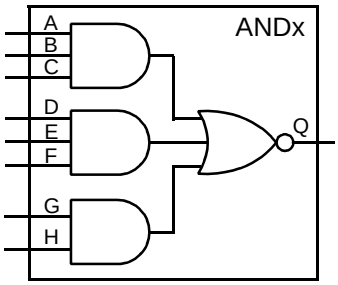
ANC2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.326 0.363	0.459 0.502	0.633 0.672	0.848 0.873	1.018 1.028
ANC4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.333 0.378	0.491 0.540	0.659 0.706	0.800 0.844	0.958 0.997
ANC6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.259 0.312	0.413 0.478	0.567 0.636	0.706 0.770	0.851 0.904

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANDx is a family of AND-NOR circuits consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

HDL Syntax

Verilog ..... ANDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ANDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	AND2	AND4	AND6
A	1.1	1.0	2.0
B	1.1	1.0	2.0
C	1.0	1.0	2.0
D	1.1	1.1	2.1
E	1.1	1.1	2.0
F	1.1	1.1	2.0
G	1.0	1.0	2.0
H	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AND2	4.2	3.827	9.3
AND4	4.2	4.227	10.6
AND6	8.5	8.456	21.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

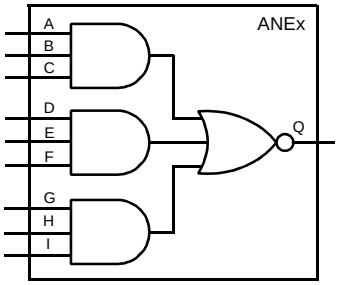
AND2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.326 0.357	0.463 0.501	0.638 0.674	0.850 0.878	1.016 1.034
AND4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.335 0.374	0.488 0.542	0.654 0.709	0.797 0.846	0.959 0.996
AND6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.275 0.306	0.429 0.503	0.587 0.649	0.725 0.785	0.865 0.933

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANEx is a family of AND-NOR circuits consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

HDL Syntax

Verilog ..... ANEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ANEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ANE2	ANE4	ANE6
A	1.1	1.0	2.0
B	1.1	1.0	2.0
C	1.0	1.0	2.0
D	1.1	1.1	2.1
E	1.1	1.1	2.0
F	1.1	1.1	2.0
G	1.1	1.1	2.0
H	1.1	1.1	2.0
I	1.0	1.1	2.1

AMI350LXSC 0.35 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANE2	4.5	4.052	9.8
ANE4	4.8	4.452	11.2
ANE6	9.2	8.904	22.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

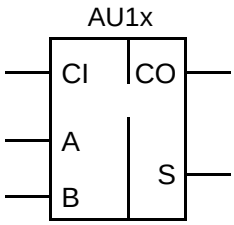
ANE2	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.326 0.362	0.462 0.496	0.636 0.665	0.849 0.870	1.015 1.031
ANE4	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.338 0.379	0.492 0.558	0.658 0.725	0.799 0.858	0.958 1.000
ANE6	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.284 0.320	0.441 0.490	0.592 0.652	0.727 0.790	0.876 0.927

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AU1x is a family of combinational one-bit full adders.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

HDL Syntax

Verilog ..... AU1x *inst_name* (CO, S, A, B, CI);

VHDL..... *inst_name*: AU1x port map (CO, S, A, B, CI);

Pin Loading

Pin Name	Equivalent Loads	
	AU11	AU12
A	4.9	10.3
B	4.9	10.0
CI	3.8	7.6

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AU11	4.5	3.476	9.4
AU12	10.0	7.096	20.7

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

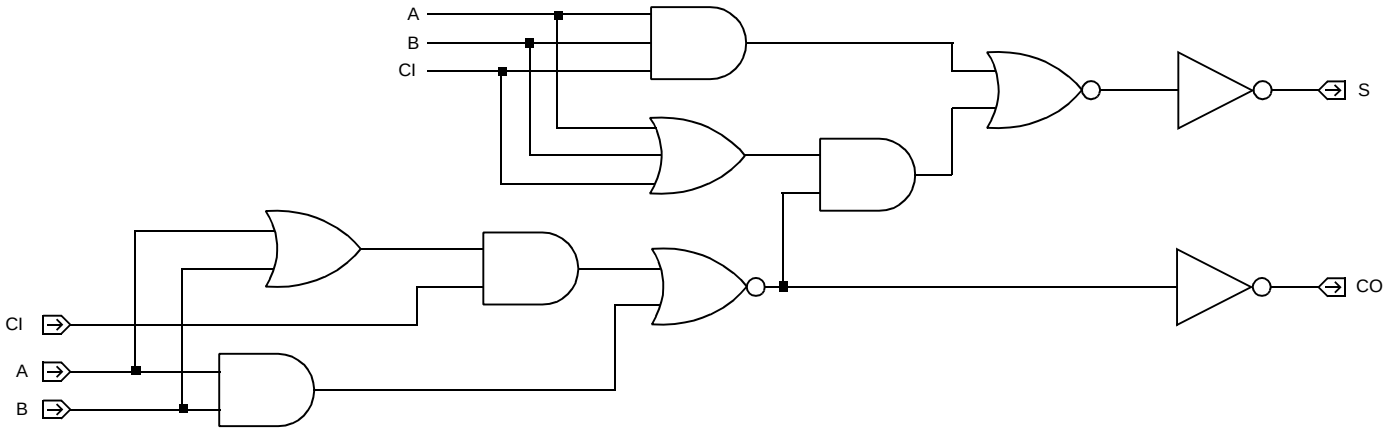
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
AU11	From: A To: S	t_{PLH} t_{PHL}	0.314 0.635	0.463 0.798	0.643 0.983	0.854 1.191	1.016 1.347
	From: B To: S	t_{PLH} t_{PHL}	0.296 0.704	0.438 0.875	0.605 1.061	0.811 1.267	0.986 1.420
	From: CI To: S	t_{PLH} t_{PHL}	0.275 0.712	0.417 0.883	0.596 1.068	0.813 1.271	0.983 1.422
	From: A To: CO	t_{PLH} t_{PHL}	0.299 0.400	0.447 0.584	0.630 0.781	0.849 0.997	1.020 1.156
	From: B To: CO	t_{PLH} t_{PHL}	0.326 0.415	0.465 0.596	0.640 0.788	0.853 0.997	1.021 1.151
	From: CI To: CO	t_{PLH} t_{PHL}	0.328 0.341	0.466 0.514	0.643 0.704	0.859 0.917	1.029 1.081
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
AU12	From: A To: S	t_{PLH} t_{PHL}	0.291 0.512	0.463 0.708	0.630 0.882	0.767 1.022	0.915 1.177
	From: B To: S	t_{PLH} t_{PHL}	0.263 0.566	0.418 0.760	0.583 0.944	0.722 1.091	0.878 1.250
	From: CI To: S	t_{PLH} t_{PHL}	0.234 0.556	0.395 0.744	0.565 0.934	0.707 1.091	0.866 1.263
	From: A To: CO	t_{PLH} t_{PHL}	0.206 0.314	0.357 0.527	0.522 0.709	0.663 0.849	0.823 0.995
	From: B To: CO	t_{PLH} t_{PHL}	0.206 0.331	0.360 0.537	0.526 0.721	0.667 0.865	0.827 1.019
	From: CI To: CO	t_{PLH} t_{PHL}	0.206 0.237	0.362 0.435	0.528 0.614	0.667 0.756	0.823 0.909

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

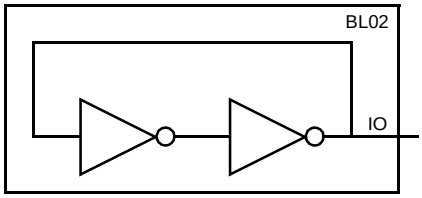


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

BL02 is a tristate bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	1.6

Equivalent Gates 1.7

HDL Syntax

Verilog ..... BL02 *inst_name* (IO);

VHDL..... *inst_name*: BL02 port map (IO);

Size And Power Characteristics

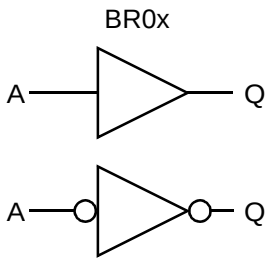
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.375	nA
EQL_{pd}	8.4	Eq-load

See page 2-13 for power equation.

Description

BR0x is a family of non-inverting bus receivers with a single output to be used as the output of tristate busses.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... BR0x *inst_name* (Q, A);

VHDL..... *inst_name*: BR0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	BR02	BR04	BR06
A	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
BR02	1.0	1.201	3.3
BR04	1.5	2.401	5.4
BR06	1.7	3.202	8.2

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

BR02	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.187 0.168	0.336 0.323	0.491 0.486	0.622 0.623	0.769 0.777
BR04	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.174 0.119	0.257 0.269	0.386 0.421	0.516 0.560	0.666 0.709
BR06	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.176 0.149	0.290 0.330	0.420 0.477	0.549 0.602	0.686 0.723

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

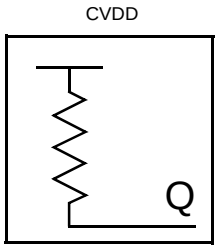
CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVDD *inst_name* (Q);

VHDL..... *inst_name*: CVDD port map (Q);



Description

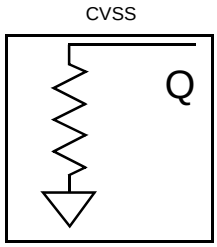
CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVSS *inst_name* (Q);

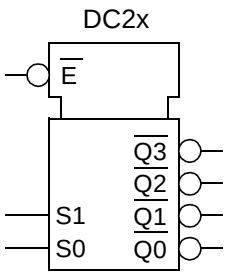
VHDL..... *inst_name*: CVSS port map (Q);



Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL..... *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.4	3.4
S1	3.4	3.4
EN	1.0	4.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC21	5.2	4.852	15.3
DC22	6.2	5.189	16.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

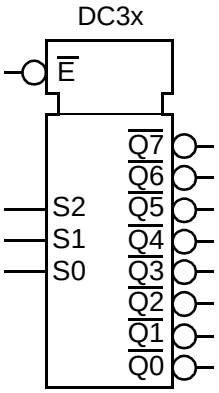
	Number of Equivalent Loads		1	2	4	5	7 (max)
DC21	From: Sx To: QN	t_{PLH} t_{PHL}	0.236 0.257	0.296 0.334	0.415 0.479	0.475 0.548	0.594 0.684
	From: EN To: QN	t_{PLH} t_{PHL}	0.331 0.321	0.391 0.398	0.509 0.542	0.567 0.612	0.681 0.748
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
DC22	From: Sx To: QN	t_{PLH} t_{PHL}	0.194 0.284	0.327 0.447	0.503 0.633	0.719 0.843	0.892 1.002
	From: EN To: QN	t_{PLH} t_{PHL}	0.218 0.349	0.350 0.507	0.525 0.681	0.743 0.890	0.917 1.060

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

DC3x is a family of three-to-eight line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

Core Logic

HDL Syntax

Verilog ..... DC3x *inst_name* (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

VHDL..... *inst_name* DC3x port map (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads	
	DC31	DC32
S0	5.9	6.1
S1	6.3	6.4
S2	5.7	5.7
EN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC31	11.5	10.313	37.0
DC32	15.8	11.852	53.5

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

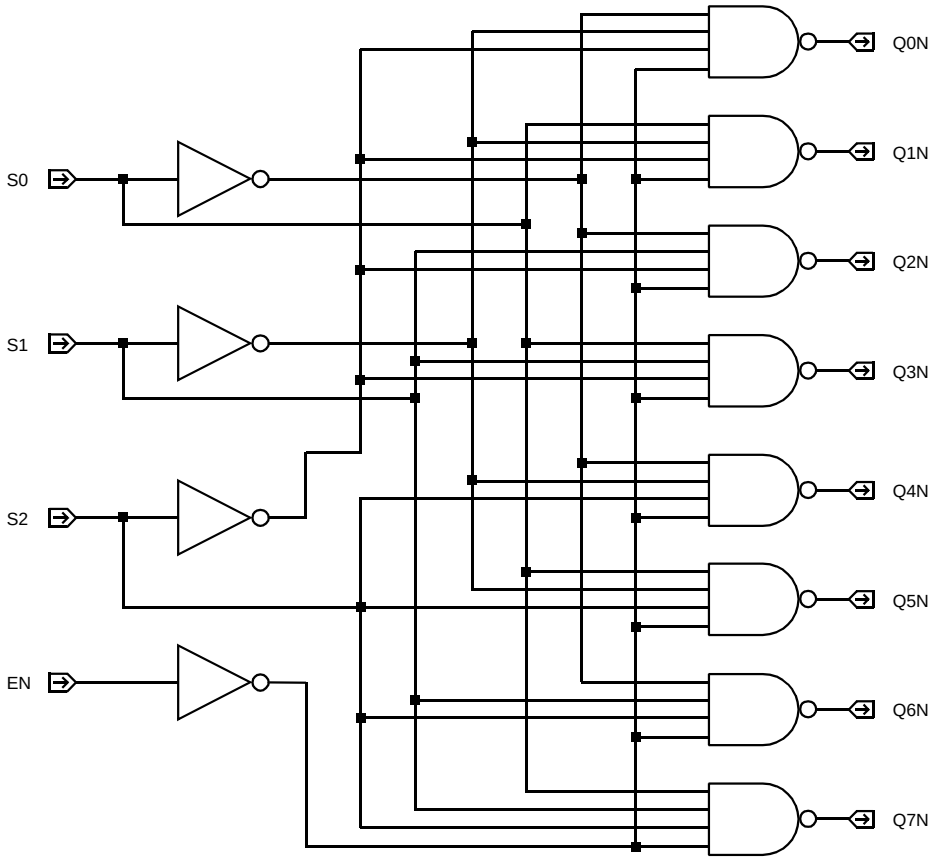
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	2	3	4	6 (max)
DC31	From: Sx To: QN	t_{PLH} t_{PHL}	0.303 0.344	0.375 0.439	0.444 0.529	0.512 0.615	0.645 0.776
	From: EN To: QN	t_{PLH} t_{PHL}	0.493 0.477	0.556 0.569	0.623 0.656	0.694 0.739	0.843 0.899
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
DC32	From: Sx To: QN	t_{PLH} t_{PHL}	0.217 0.313	0.351 0.493	0.516 0.694	0.725 0.921	0.903 1.090
	From: EN To: QN	t_{PLH} t_{PHL}	0.663 0.738	0.810 0.925	0.985 1.119	1.191 1.329	1.348 1.482

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

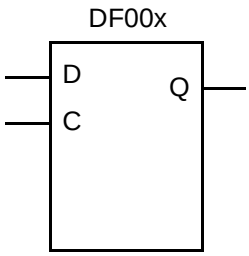
Logic Schematic



Description

DF00x is a family of static, master-slave D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q
H	↑	H
L	↑	L
X	L	NC

NC = No Change

HDL Syntax

Verilog ..... DF00x *inst_name* (Q, C, D);

VHDL..... *inst_name*: DF00x port map (Q, C, D);

Pin Loading

Pin Name	Equivalent Loads	
	DF001	DF002
D	1.1	1.1
C	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF001	3.8	2.851	7.8
DF002	3.8	3.251	9.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

DF001	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: C To: Q	t_{PLH} t_{PHL}	0.440 0.384	0.578 0.523	0.750 0.695	0.957 0.901	1.119 1.061
DF002	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: C To: Q	t_{PLH} t_{PHL}	0.418 0.378	0.579 0.561	0.743 0.733	0.879 0.872	1.029 1.022

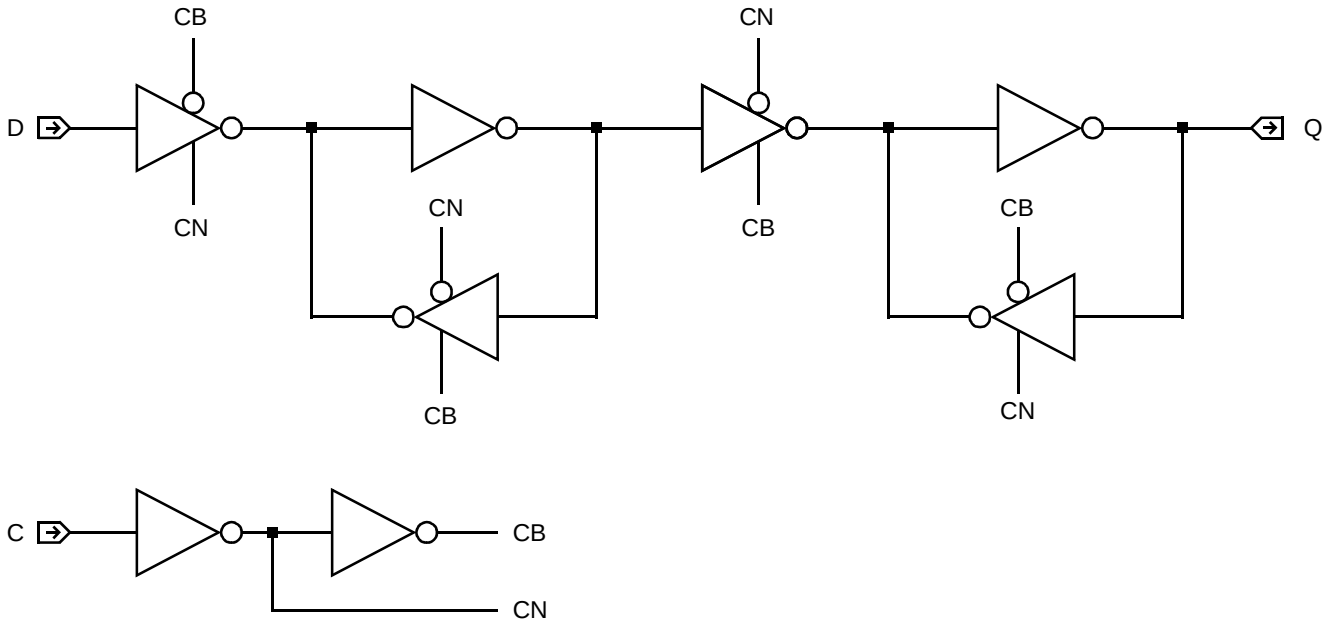
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell DF001	Cell DF002
Min C Width	High	t_w	0.449	0.414
Min C Width	Low	t_w	0.442	0.428
Min D Setup		t_{su}	0.258	0.261
Min D Hold		t_h	0.134	0.124

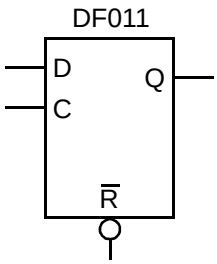
Logic Schematic



Description

DF011 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q
L	X	X	L
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.1
C	1.1
RN	1.1

Core Logic

Equivalent Gates 4.8

HDL Syntax

Verilog ..... DF011 *inst_name* (Q, C, D, RN);

VHDL..... *inst_name*: DF011 port map (Q, C, D, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.284	nA
EQL_{pd}	11.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.494 0.379	0.572 0.433	0.803 0.575	1.033 0.705	1.187 0.788
RN	Q	t_{PHL}	0.263	0.309	0.427	0.557	0.641

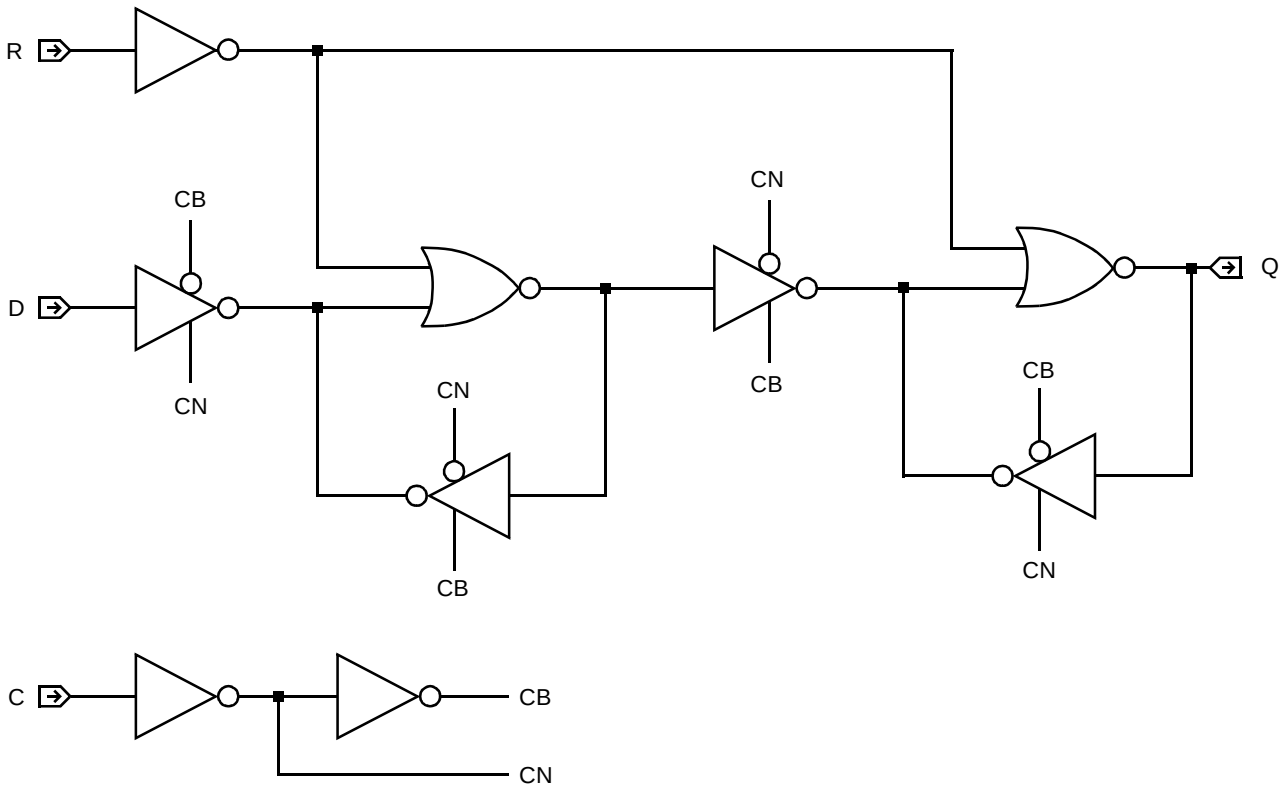
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.485
Min C Width	Low	t_w	0.448
Min RN Width	Low	t_w	0.467
Min D Setup		t_{su}	0.274
Min D Hold		t_h	0.125
Min RN Setup		t_{su}	0.246
Min RN Hold		t_h	0.286

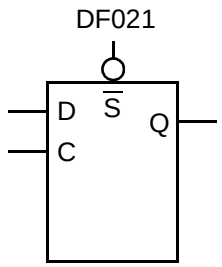
Logic Schematic



Description

DF021 is a static, master-slave D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q
L	X	X	H
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.1
C	1.1
SN	2.2

Equivalent Gates 4.5

HDL Syntax

Verilog.....DF021 *inst_name* (Q, C, D, SN);

VHDL..... *inst_name*: DF021 port map (Q, C, D, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.427	nA
EQL_{pd}	8.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.453 0.400	0.508 0.469	0.664 0.648	0.813 0.810	0.911 0.911
SN	Q	t_{PLH}	0.168	0.216	0.340	0.493	0.598

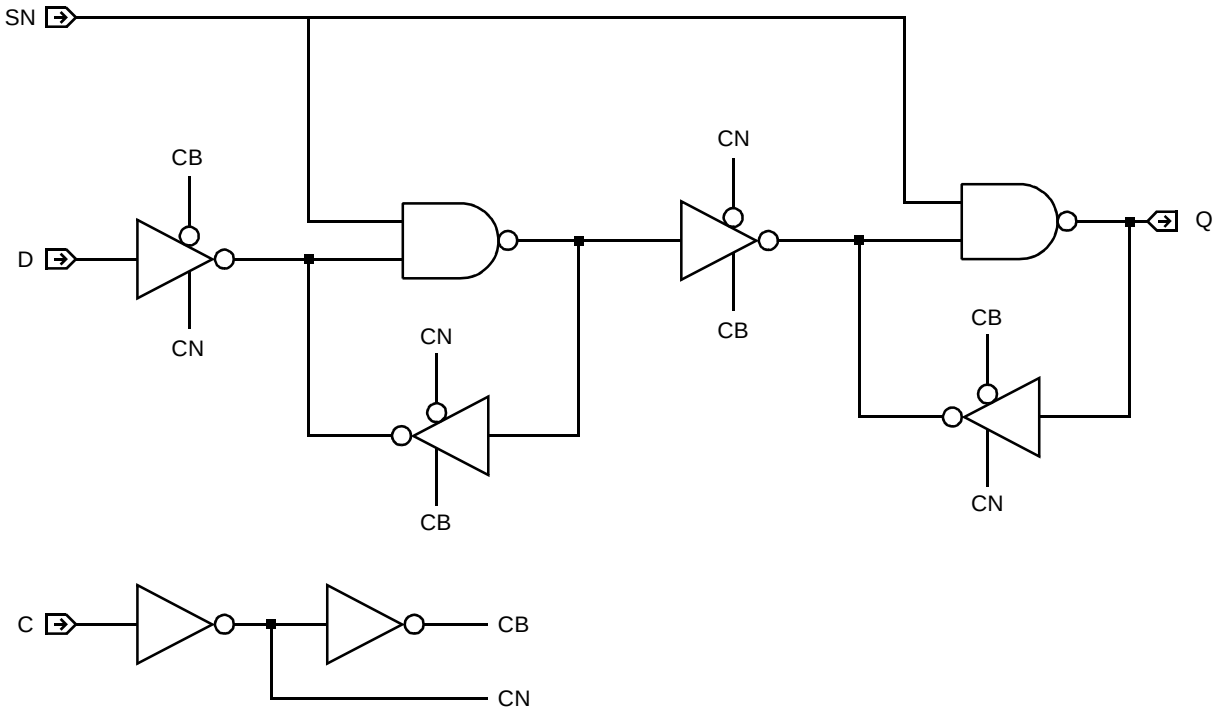
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.453
Min C Width	Low	t_w	0.451
Min SN Width	Low	t_w	0.675
Min D Setup		t_{su}	0.277
Min D Hold		t_h	0.125
Min SN Setup		t_{su}	0.125
Min SN Hold		t_h	0.410

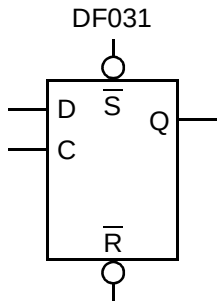
Logic Schematic



Description

DF031 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	L	↑	L
H	H	H	↑	H
H	H	X	L	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.2
RN	1.1

Equivalent Gates 5.5

HDL Syntax

Verilog ..... DF031 *inst_name* (Q, D, RN, SN);

VHDL..... *inst_name*: DF031 port map (Q, D, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.940	nA
EQL_{pd}	12.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.532 0.415	0.626 0.485	0.908 0.681	1.190 0.865	1.378 0.985
RN	Q	t_{PHL}	0.295	0.364	0.539	0.720	0.838
SN	Q	t_{PLH}	0.156	0.202	0.307	0.434	0.526

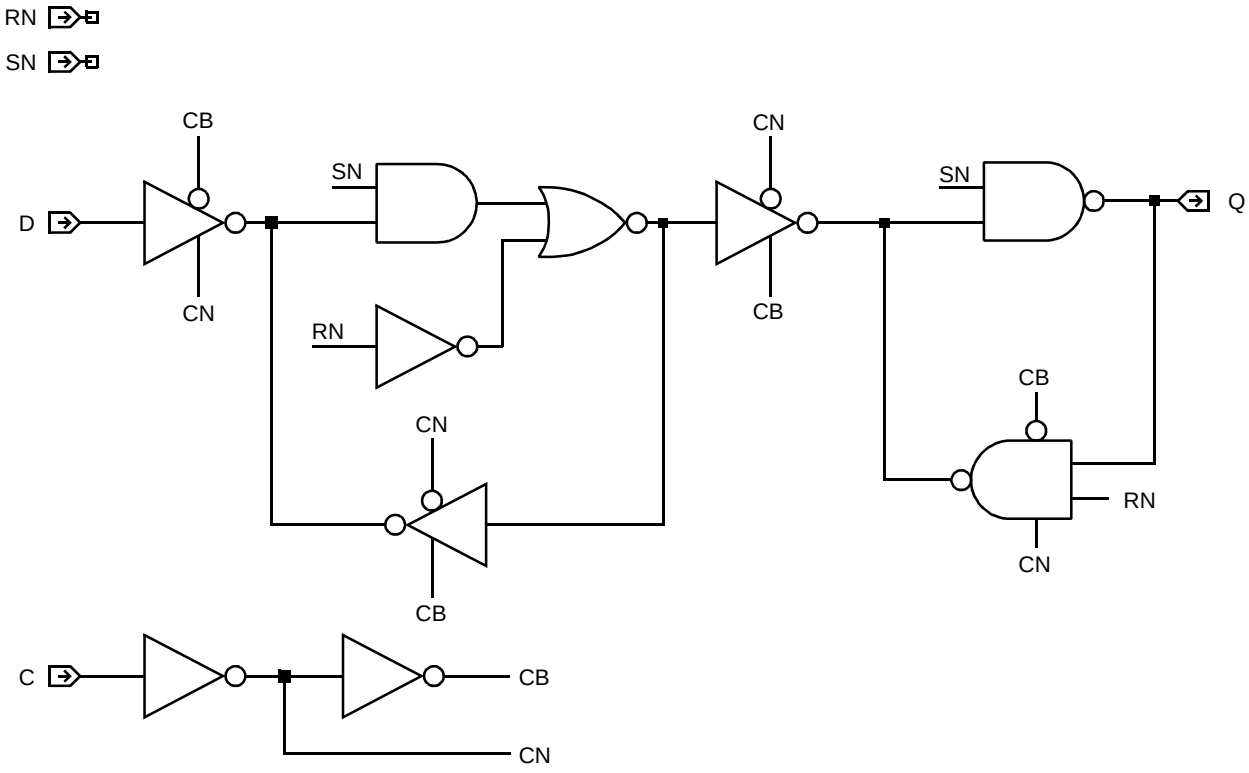
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.536
Min C Width	Low	t_w	0.469
Min RN Width	Low	t_w	0.477
Min SN Width	Low	t_w	0.638
Min D Setup		t_{su}	0.306
Min D Hold		t_h	0.129
Min RN Setup		t_{su}	0.280
Min RN Hold		t_h	0.284
Min SN Setup		t_{su}	0.149
Min SN Hold		t_h	0.409

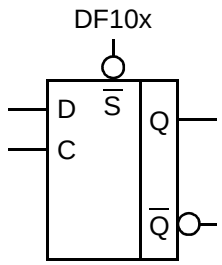
Logic Schematic



Description

DF10x is a family of static, master-slave D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF10x *inst_name* (Q, QN, C, D, SN);

VHDL.....*inst_name*: DF10x port map (Q, QN, C, D, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF101	DF102	DF104	DF106
D	1.1	1.0	1.1	1.0
C	1.1	1.0	1.1	1.1
SN	2.3	2.3	3.5	3.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
DF101	5.2	4.228	11.4
DF102	5.2	5.028	14.1
DF104	6.5	7.941	23.5
DF106	7.0	9.542	28.0

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF101	From: C To: Q	t_{PLH} t_{PHL}	0.462 0.421	0.597 0.582	0.772 0.765	0.987 0.972	1.158 1.128
	From: C To: QN	t_{PLH} t_{PHL}	0.532 0.594	0.657 0.721	0.827 0.889	1.042 1.098	1.216 1.265
	From: SN To: Q	t_{PLH}	0.538	0.671	0.849	1.072	1.250
	From: SN To: QN	t_{PHL}	0.242	0.379	0.547	0.749	0.906
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF102	From: C To: Q	t_{PLH} t_{PHL}	0.455 0.415	0.611 0.610	0.774 0.792	0.911 0.937	1.063 1.094
	From: C To: QN	t_{PLH} t_{PHL}	0.597 0.651	0.733 0.805	0.882 0.960	1.011 1.089	1.157 1.231
	From: SN To: Q	t_{PLH}	0.610	0.765	0.927	1.062	1.213
	From: SN To: QN	t_{PHL}	0.235	0.413	0.581	0.715	0.860
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DF104	From: C To: Q	t_{PLH} t_{PHL}	0.494 0.424	0.664 0.642	0.815 0.801	0.950 0.935	1.108 1.074
	From: C To: QN	t_{PLH} t_{PHL}	0.591 0.646	0.718 0.785	0.855 0.935	0.999 1.075	1.136 1.224
	From: SN To: Q	t_{PLH}	0.551	0.696	0.860	1.009	1.160
	From: SN To: QN	t_{PHL}	0.188	0.364	0.515	0.648	0.790
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF106	From: C To: Q	t_{PLH} t_{PHL}	0.520 0.438	0.673 0.672	0.815 0.846	0.944 0.990	1.072 1.131
	From: C To: QN	t_{PLH} t_{PHL}	0.648 0.703	0.796 0.865	0.934 1.020	1.055 1.154	1.176 1.290
	From: SN To: Q	t_{PLH}	0.615	0.800	0.969	1.116	1.258
	From: SN To: QN	t_{PHL}	0.215	0.396	0.538	0.668	0.802

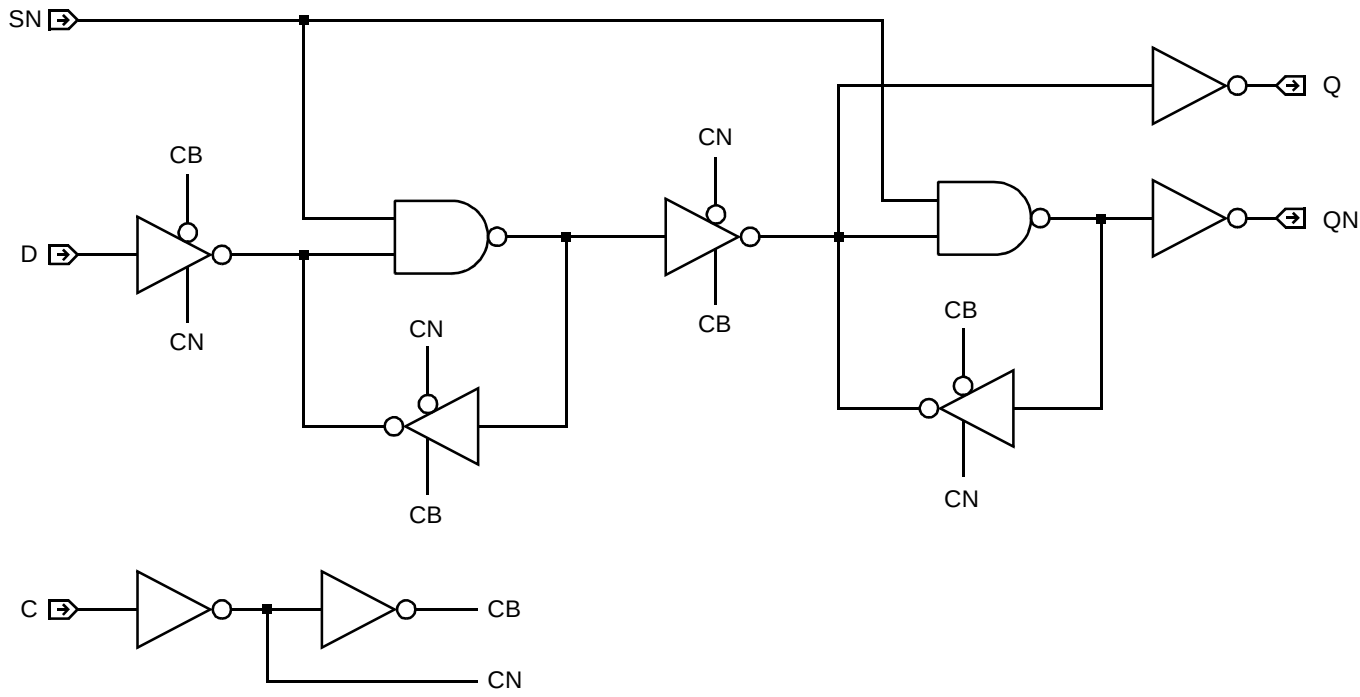
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF101	DF102	DF104	DF106
Min C Width	High	t_w	0.469	0.519	0.563	0.615
Min C Width	Low	t_w	0.457	0.454	0.542	0.522
Min SN Width		t_w	0.415	0.500	0.472	0.560
Min D Setup		t_{su}	0.279	0.284	0.325	0.310
Min D Hold		t_h	0.129	0.124	0.145	0.144
Min SN Setup		t_{su}	0.128	0.129	0.159	0.155
Min SN Hold		t_h	0.409	0.404	0.468	0.448

Logic Schematic

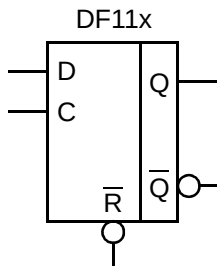


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DF11x is a family of static, master-slave D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF11x *inst_name* (Q, QN, C, D, RN);

VHDL.....inst_DF11x : DF11x port map (Q, QN, C, D, RN);

Pin Loading

Pin Name	Equivalent Loads			
	DF111	DF112	DF114	DF116
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
RN	1.0	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF111	5.5	4.084	13.8
DF112	5.8	4.885	16.9
DF114	7.0	7.526	26.2
DF116	8.0	9.126	31.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF111	From: C To: Q	t_{PLH} t_{PHL}	0.448 0.408	0.585 0.565	0.758 0.753	0.971 0.973	1.141 1.143
	From: C To: QN	t_{PLH} t_{PHL}	0.496 0.626	0.626 0.777	0.796 0.954	1.004 1.158	1.169 1.313
	From: RN To: Q	t_{PHL}	0.777	0.966	1.169	1.391	1.553
	From: RN To: QN	t_{PLH}	0.298	0.426	0.597	0.815	0.989
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF112	From: C To: Q	t_{PLH} t_{PHL}	0.439 0.417	0.605 0.619	0.773 0.804	0.914 0.950	1.069 1.107
	From: C To: QN	t_{PLH} t_{PHL}	0.555 0.709	0.692 0.869	0.851 1.037	0.990 1.178	1.151 1.334
	From: RN To: Q	t_{PHL}	0.874	1.118	1.310	1.453	1.600
	From: RN To: QN	t_{PLH}	0.307	0.448	0.610	0.752	0.914
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DF114	From: C To: Q	t_{PLH} t_{PHL}	0.518 0.400	0.667 0.620	0.827 0.796	0.972 0.934	1.126 1.062
	From: C To: QN	t_{PLH} t_{PHL}	0.531 0.697	0.678 0.886	0.817 1.030	0.944 1.158	1.081 1.295
	From: RN To: Q	t_{PHL}	0.776	1.008	1.198	1.357	1.515
	From: RN To: QN	t_{PLH}	0.304	0.454	0.601	0.729	0.881
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF116	From: C To: Q	t_{PLH} t_{PHL}	0.464 0.457	0.639 0.692	0.792 0.848	0.932 0.983	1.076 1.122
	From: C To: QN	t_{PLH} t_{PHL}	0.603 0.781	0.732 0.993	0.882 1.144	1.021 1.266	1.164 1.385
	From: RN To: Q	t_{PHL}	0.899	1.176	1.356	1.498	1.630
	From: RN To: QN	t_{PLH}	0.312	0.467	0.610	0.739	0.874

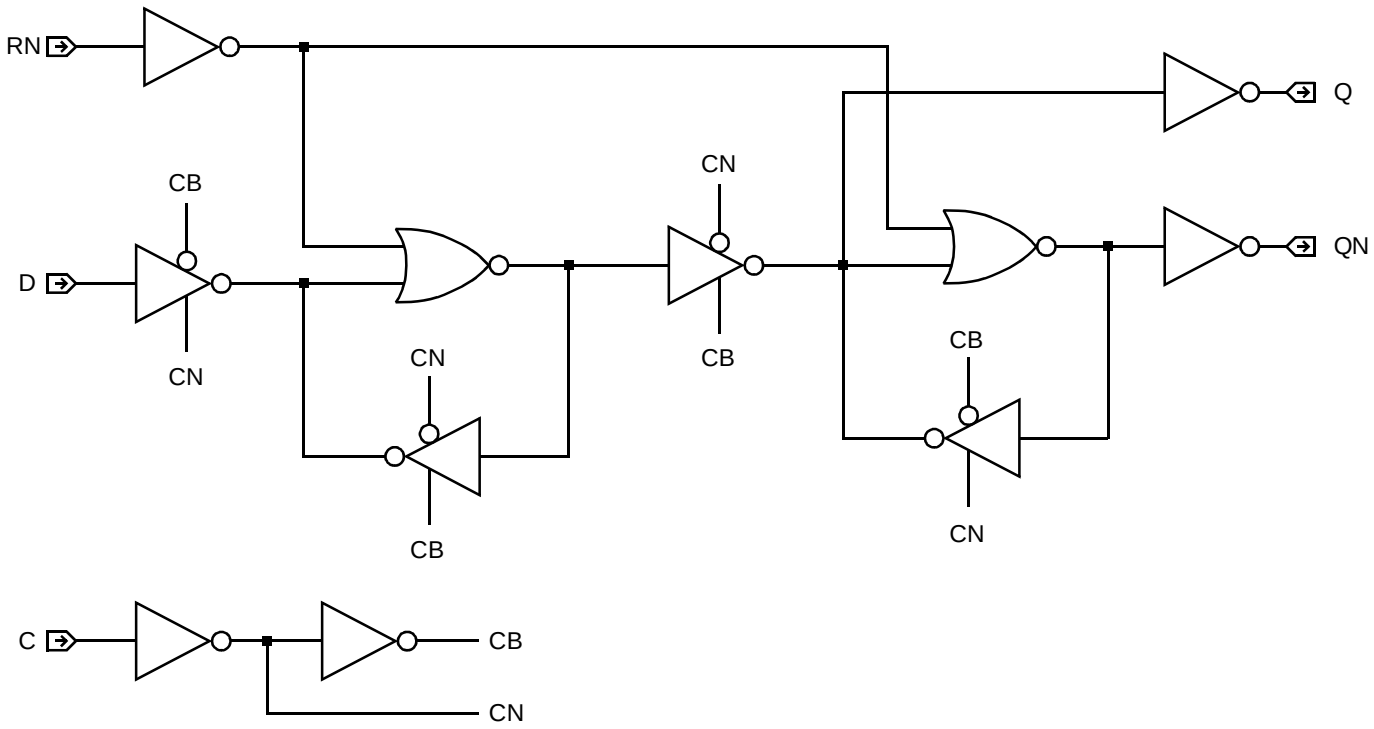
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF111	DF112	DF114	DF116
Min C Width	High	t_w	0.479	0.555	0.582	0.656
Min C Width	Low	t_w	0.424	0.436	0.499	0.499
Min RN Width		t_w	0.450	0.466	0.519	0.517
Min D Setup		t_{su}	0.263	0.270	0.305	0.305
Min D Hold		t_h	0.122	0.124	0.140	0.141
Min RN Setup		t_{su}	0.236	0.246	0.304	0.303
Min RN Hold		t_h	0.273	0.281	0.305	0.305

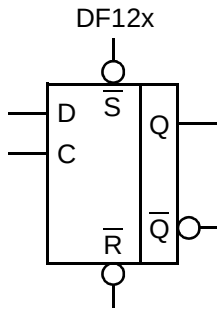
Logic Schematic



Description

DF12x is a family of static, master-slave D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DF12x *inst_name* (Q, QN, C, D, RN, SN);

VHDL..... *inst_name*: DF12x port map (Q, QN, C, D, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF121	DF122	DF124	DF126
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.2	2.2	2.2	2.2
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF121	6.2	4.741	15.0
DF122	6.2	5.541	17.5
DF124	7.5	7.942	25.0
DF126	8.5	9.543	30.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF121	From: C To: Q	t_{PLH} t_{PHL}	0.458 0.422	0.589 0.583	0.764 0.763	0.984 0.971	1.160 1.131
	From: C To: QN	t_{PLH} t_{PHL}	0.543 0.696	0.675 0.855	0.847 1.037	1.059 1.244	1.227 1.400
	From: SN To: Q	t_{PLH}	0.536	0.691	0.871	1.078	1.235
	From: SN To: QN	t_{PHL}	0.241	0.376	0.540	0.745	0.913
	From: RN To: Q	t_{PHL}	0.801	1.001	1.202	1.415	1.567
	From: RN To: QN	t_{PLH}	0.336	0.475	0.650	0.862	1.032
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF122	From: C To: Q	t_{PLH} t_{PHL}	0.450 0.418	0.609 0.618	0.774 0.801	0.913 0.947	1.066 1.103
	From: C To: QN	t_{PLH} t_{PHL}	0.615 0.771	0.757 0.959	0.908 1.130	1.035 1.265	1.179 1.410
	From: SN To: Q	t_{PLH}	0.603	0.768	0.930	1.062	1.207
	From: SN To: QN	t_{PHL}	0.229	0.402	0.570	0.706	0.854
	From: RN To: Q	t_{PHL}	0.874	1.102	1.301	1.454	1.615
	From: RN To: QN	t_{PLH}	0.336	0.492	0.660	0.801	0.958

	Number of Equivalent Loads		1	15	30	44	59 (max)
DF124	From: C To: Q	t_{PLH} t_{PHL}	0.777 0.659	0.934 0.822	1.079 0.978	1.206 1.117	1.338 1.262
	From: C To: QN	t_{PLH} t_{PHL}	0.519 0.577	0.657 0.757	0.796 0.915	0.926 1.048	1.067 1.184
	From: SN To: Q	t_{PLH}	0.306	0.456	0.605	0.737	0.877
	From: SN To: QN	t_{PHL}	0.677	0.847	1.005	1.143	1.285
	From: RN To: Q	t_{PHL}	0.462	0.627	0.785	0.920	1.064
	From: RN To: QN	t_{PLH}	0.904	1.022	1.169	1.314	1.477
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF126	From: C To: Q	t_{PLH} t_{PHL}	0.863 0.710	0.993 0.932	1.115 1.069	1.246 1.189	1.397 1.310
	From: C To: QN	t_{PLH} t_{PHL}	0.557 0.592	0.696 0.806	0.830 0.977	0.960 1.114	1.098 1.240
	From: SN To: Q	t_{PLH}	0.361	0.502	0.638	0.768	0.903
	From: SN To: QN	t_{PHL}	0.727	0.926	1.087	1.222	1.354
	From: RN To: Q	t_{PHL}	0.512	0.715	0.857	0.987	1.122
	From: RN To: QN	t_{PLH}	0.975	1.111	1.254	1.390	1.533

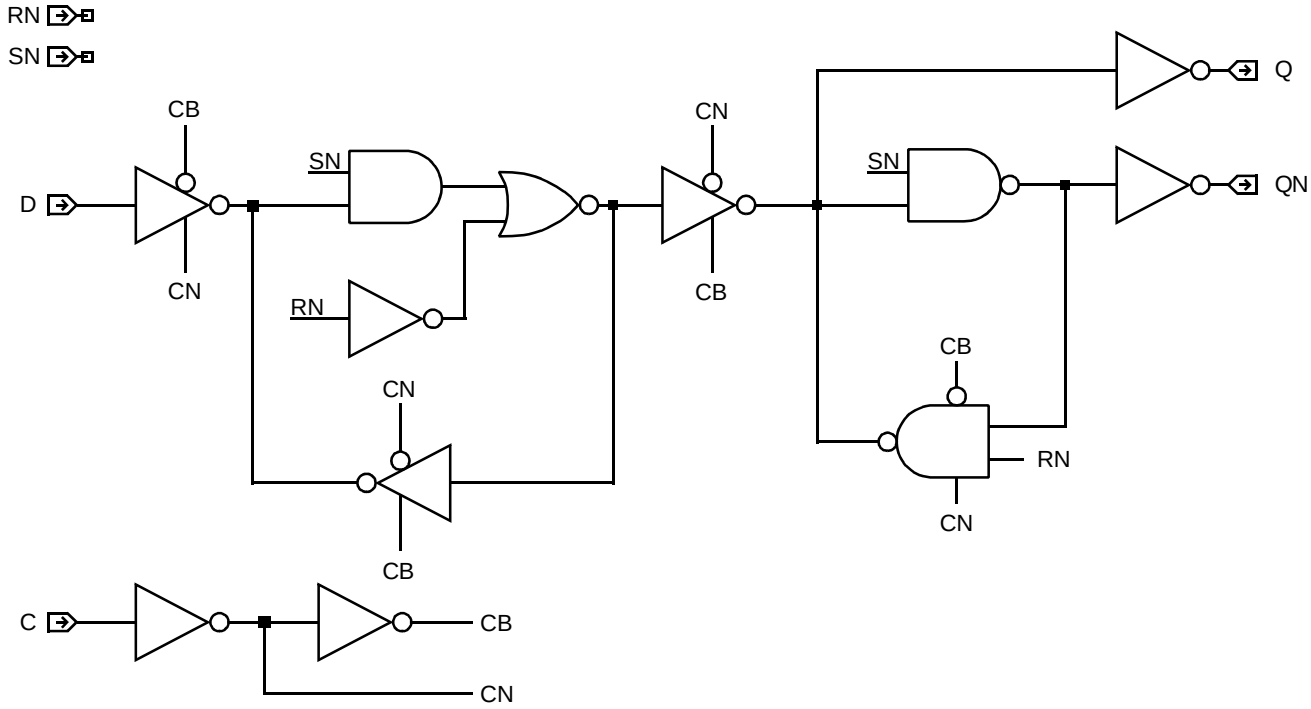
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF121	DF122	DF124	DF126
Min C Width	High	t_w	0.532	0.602	0.530	0.540
Min C Width	Low	t_w	0.461	0.465	0.463	0.465
Min RN Width	Low	t_w	0.463	0.467	0.472	0.467
Min SN Width	Low	t_w	0.418	0.497	0.421	0.429
Min D Setup		t_{su}	0.295	0.299	0.301	0.299
Min D Hold		t_h	0.130	0.130	0.126	0.129
Min RN Setup		t_{su}	0.271	0.276	0.278	0.277
Min RN Hold		t_h	0.282	0.282	0.280	0.281
Min SN Setup		t_{su}	0.147	0.149	0.149	0.149
Min SN Hold		t_h	0.406	0.407	0.405	0.407

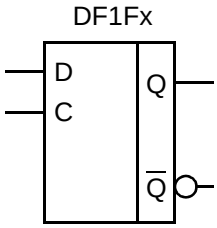
Logic Schematic



Description

DF1Fx is a family of static, master-slave D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
X	X	L	H
L	↑	L	H
H	↑	H	L
X	L	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF1Fx *inst_name* (Q, QN, C, D);

VHDL..... *inst_name*: DF1Fx port map (Q, QN, C, D)

Pin Loading

Pin Name	Equivalent Loads			
	DF1F1	DF1F2	DF1F4	DF1F6
D	1.1	1.0	1.0	1.0
C	1.1	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF1F1	4.8	3.652	11.1
DF1F2	4.8	4.452	12.9
DF1F4	5.5	6.852	20.0
DF1F6	6.0	8.853	26.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF1F1	From: C To: Q	t_{PLH} t_{PHL}	0.460 0.418	0.597 0.581	0.773 0.768	0.988 0.980	1.157 1.140
	From: C To: QN	t_{PLH} t_{PHL}	0.498 0.575	0.620 0.708	0.788 0.875	1.002 1.075	1.176 1.231
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF1F2	From: C To: Q	t_{PLH} t_{PHL}	0.437 0.408	0.596 0.609	0.764 0.792	0.906 0.936	1.064 1.090
	From: C To: QN	t_{PLH} t_{PHL}	0.529 0.578	0.671 0.734	0.824 0.894	0.954 1.027	1.101 1.175
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DF1F4	From: C To: Q	t_{PLH} t_{PHL}	0.634 0.603	0.770 0.789	0.919 0.936	1.057 1.068	1.206 1.210
	From: C To: QN	t_{PLH} t_{PHL}	0.445 0.506	0.583 0.674	0.732 0.825	0.872 0.956	1.023 1.089
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF1F6	From: C To: Q	t_{PLH} t_{PHL}	0.651 0.595	0.795 0.767	0.925 0.908	1.048 1.032	1.181 1.153
	From: C To: QN	t_{PLH} t_{PHL}	0.352 0.579	0.606 0.737	0.755 0.869	0.893 0.995	1.045 1.128

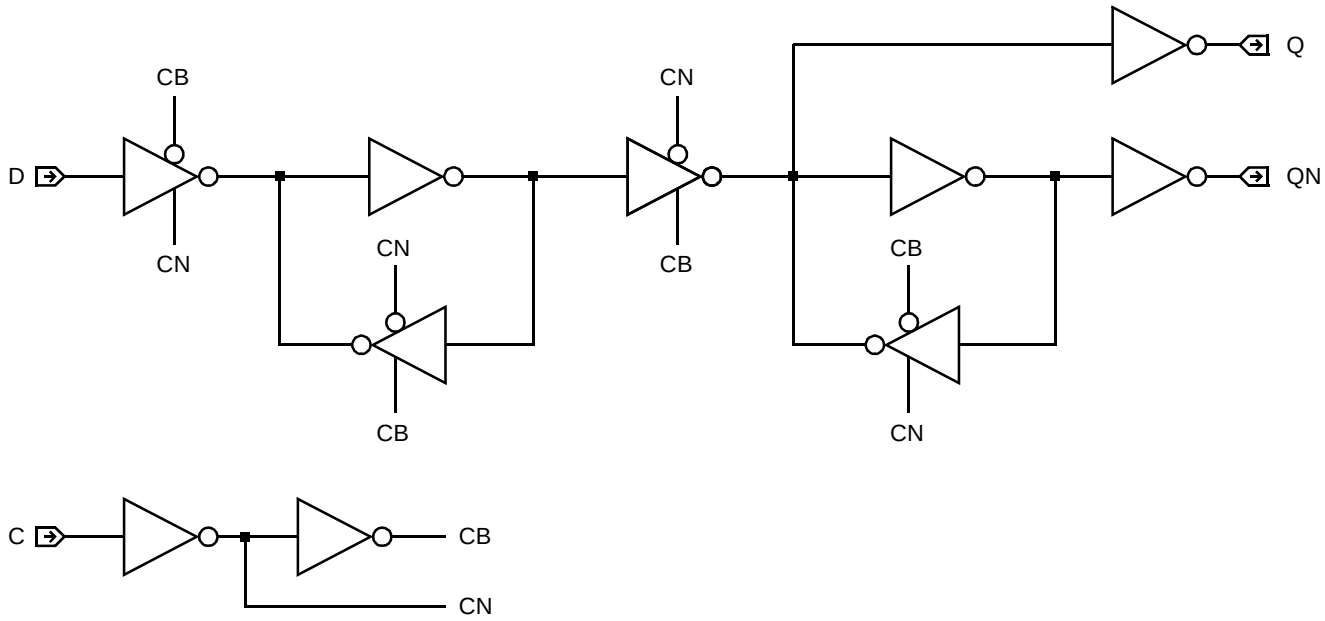
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell DF1F1	DF1F2	DF1F4	DF1F6
Min C Width	High	t_w	0.454	0.479	0.441	0.476
Min C Width	Low	t_w	0.442	0.418	0.422	0.425
Min D Setup		t_{su}	0.268	0.255	0.257	0.258
Min D Hold		t_h	0.128	0.124	0.123	0.124

Logic Schematic

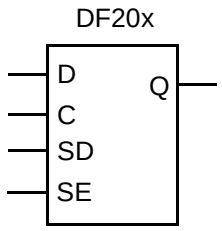


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DF20x is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q
↑	H	X	L	H
↑	L	X	L	L
↑	X	H	H	H
↑	X	L	H	L
L	X	X	X	NC

NC = No Change

HDL Syntax

Verilog ..... DF20x *inst_name* (Q, C, D, SD, SE);

VHDL..... *inst_name*: DF20x port map (Q, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads	
	DF201	DF202
C	1.0	1.0
D	1.0	1.0
SD	1.0	1.0
SE	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF201	5.0	3.876	11.5
DF202	5.0	4.068	12.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

DF201	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.425 0.375	0.562 0.519	0.734 0.691	0.942 0.891	1.104 1.045
DF202	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.421 0.379	0.569 0.545	0.730 0.721	0.867 0.869	1.021 1.036

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

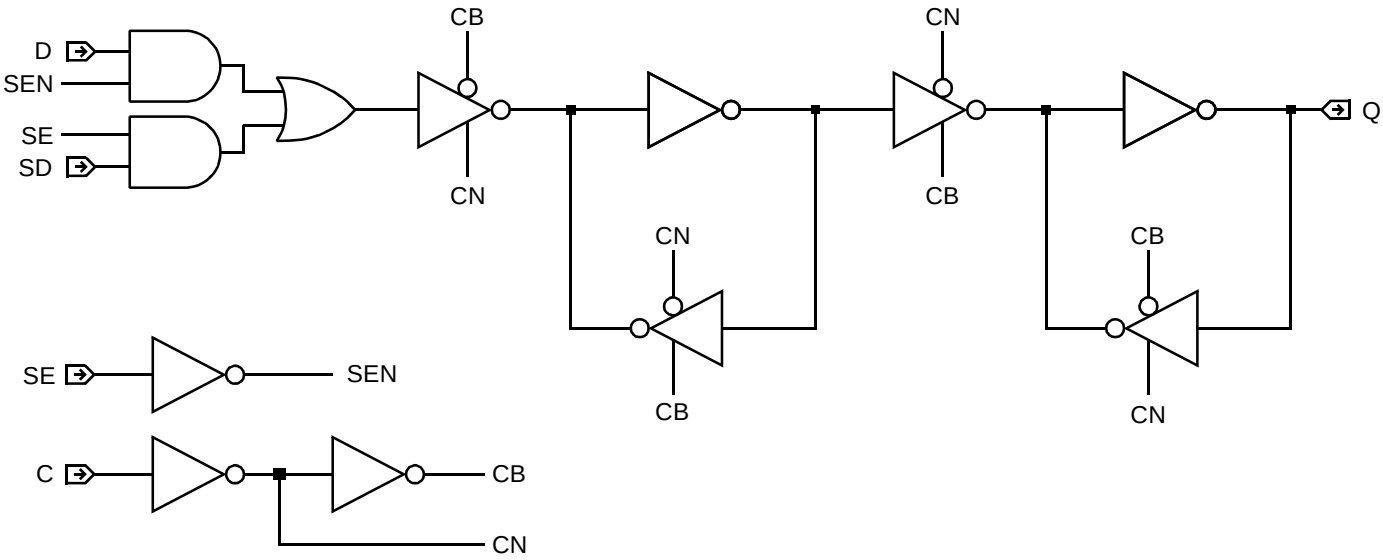
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DF201	**DF202**
Min C Width	High	t_w	0.426	0.419
Min C Width	Low	t_w	0.601	0.549
Min D Setup		t_{su}	0.481	0.461
Min D Hold		t_h	0.128	0.126
Min SD Setup		t_{su}	0.481	0.461
Min SD Hold		t_h	0.128	0.126
Min SE Setup		t_{su}	0.581	0.562
Min SE Hold		t_h	0.128	0.126

AMI350LXSC 0.35 micron CMOS Standard Cell

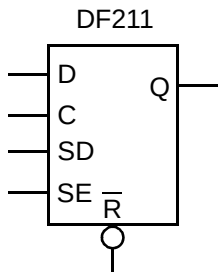
Logic Schematic



Description

DF211 is a static, master-slave, multiplexed scan D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q
↑	H	H	X	L	H
↑	L	H	X	L	L
↑	X	H	H	H	H
↑	X	H	L	H	L
X	X	L	X	X	L
L	X	H	X	X	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.0
D	1.0
RN	1.1
SD	1.0
SE	2.2

Core Logic

Equivalent Gates 6.0

HDL Syntax

Verilog ..... DF211 *inst_name* (Q, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF211 port map (Q, C, D, RN, SD, SE);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.373	nA
EQL_{pd}	14.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.491 0.391	0.574 0.446	0.806 0.588	1.028 0.714	1.172 0.793
RN	Q	t_{PHL}	0.266	0.313	0.433	0.558	0.639

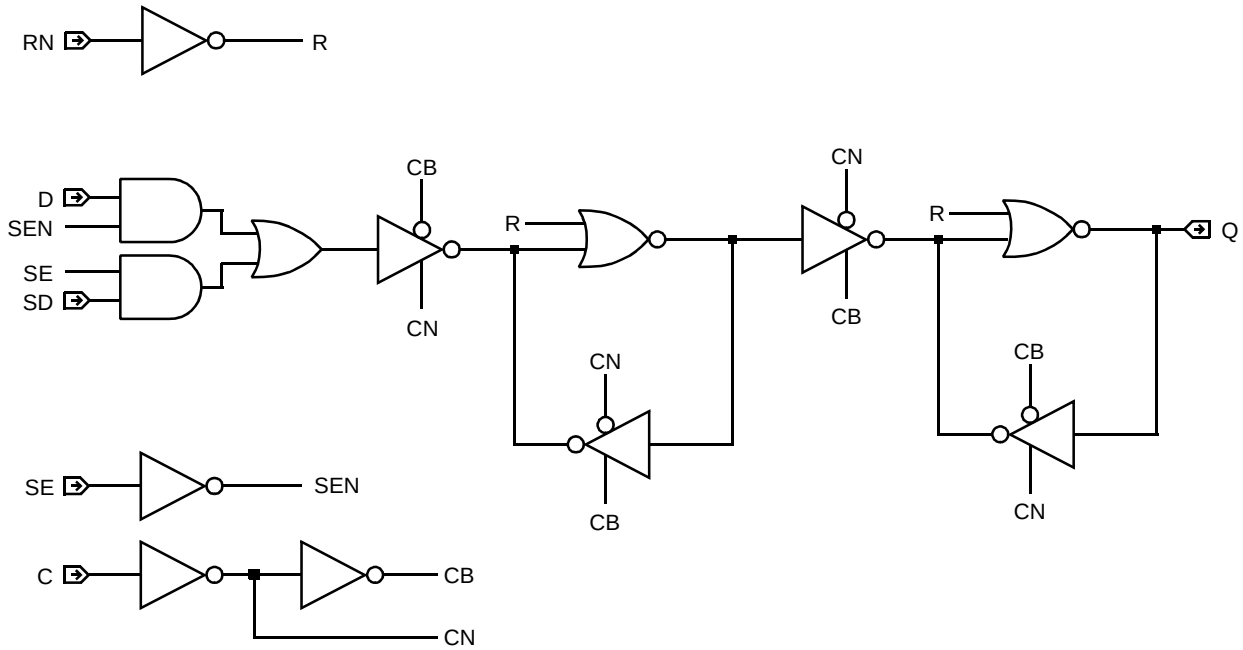
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.487
Min C Width	Low	t_w	0.563
Min RN Width	Low	t_w	0.472
Min D Setup		t_{su}	0.462
Min D Hold		t_h	0.127
Min SD Setup		t_{su}	0.462
Min SD Hold		t_h	0.127
Min SE Setup		t_{su}	0.562
Min SE Hold		t_h	0.127
Min RN Setup		t_{su}	0.248
Min RN Hold		t_h	0.295

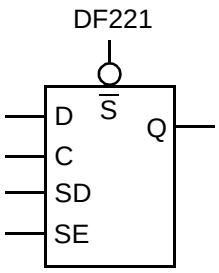
Logic Schematic



Description

DF221 is a static, master-slave, multiplexed scan D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q
↑	H	X	L	H	H
↑	L	X	L	H	L
↑	X	H	H	H	H
↑	X	L	H	H	L
X	X	X	X	L	H
L	X	X	X	H	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.0
D	1.0
SD	1.0
SE	2.2
SN	2.2

Equivalent Gates 5.5

HDL Syntax

Verilog ..... DF221 *inst_name* (Q, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF221 port map (Q, C, D, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.244	nA
EQL_{pd}	11.5	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.448 0.407	0.503 0.473	0.659 0.653	0.808 0.819	0.905 0.925
SN	Q	t_{PLH}	0.171	0.218	0.341	0.494	0.601

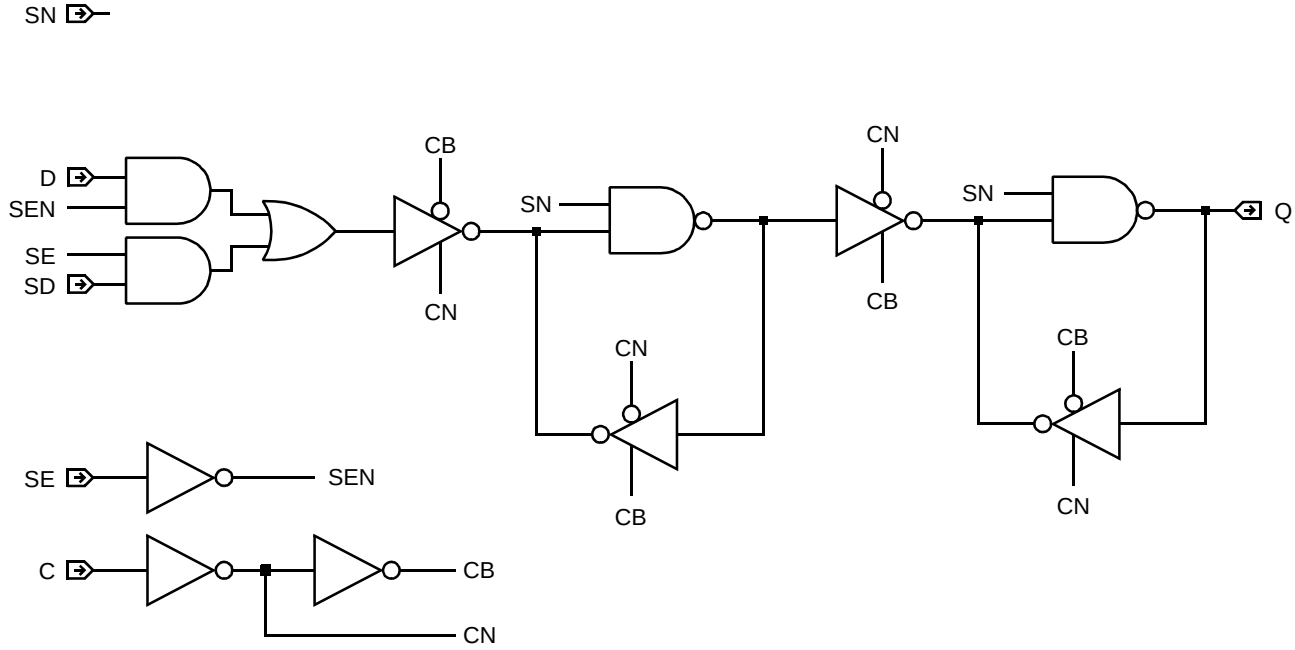
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.448
Min C Width	Low	t_w	0.583
Min SN Width	Low	t_w	0.400
Min D Setup		t_{su}	0.482
Min D Hold		t_h	0.127
Min SD Setup		t_{su}	0.482
Min SD Hold		t_h	0.127
Min SE Setup		t_{su}	0.583
Min SE Hold		t_h	0.127
Min SN Setup		t_{su}	0.127
Min SN Hold		t_h	0.414

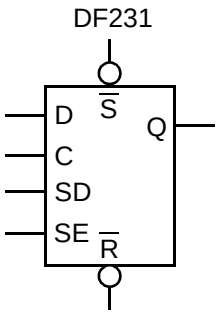
Logic Schematic



Description

DF231 is a static, master-slave, multiplexed scan D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q
↑	H	H	X	L	H	H
↑	L	H	X	L	H	L
↑	X	H	H	H	H	H
↑	X	H	L	H	H	L
X	X	L	X	X	H	L
X	X	H	X	X	L	H
X	X	L	X	X	L	IL
L	X	H	X	X	H	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	1.0
D	1.0
RN	1.0
SD	1.0
SE	2.2
SN	2.2

Equivalent Gates 6.8

HDL Syntax

Verilog ..... DF231 *inst_name* (Q, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF231 port map (Q, C, D, RN, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.757	nA
EQL_{pd}	15.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.533 0.411	0.632 0.476	0.915 0.668	1.187 0.860	1.365 0.988
RN	Q	t_{PHL}	0.278	0.343	0.525	0.709	0.831
SN	Q	t_{PLH}	0.144	0.191	0.307	0.432	0.517

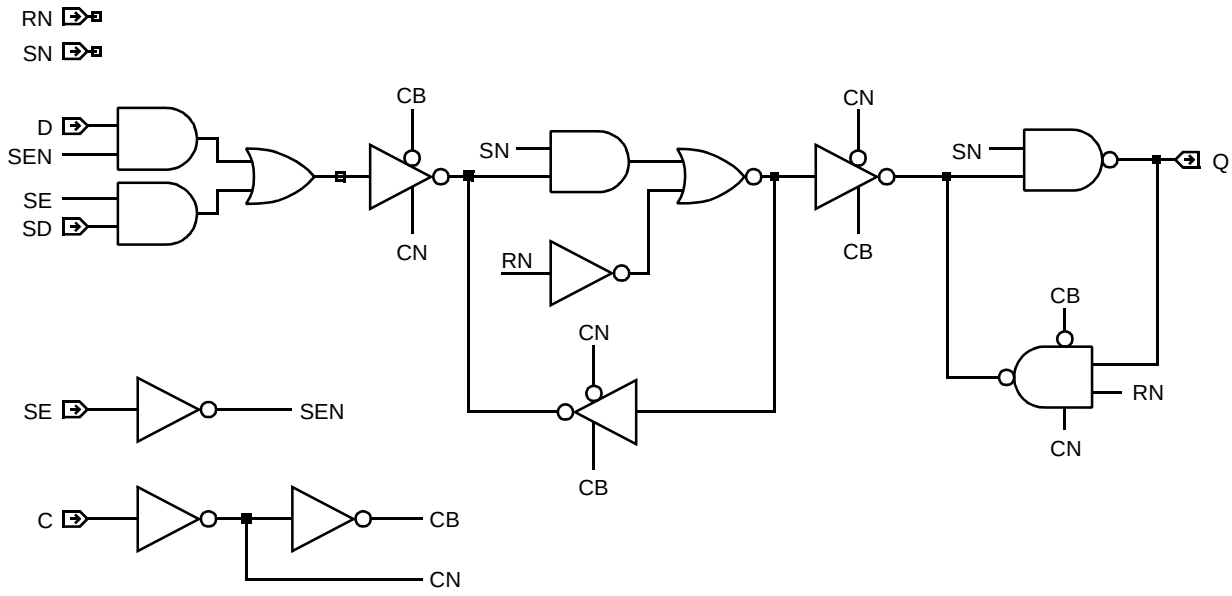
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.527
Min C Width	Low	t_w	0.605
Min RN Width	Low	t_w	0.492
Min SN Width	Low	t_w	0.381
Min D Setup		t_{su}	0.498
Min D Hold		t_h	0.129
Min SD Setup		t_{su}	0.498
Min SD Hold		t_h	0.129
Min SE Setup		t_{su}	0.598
Min SE Hold		t_h	0.129
Min RN Setup		t_{su}	0.287
Min RN Hold		t_h	0.299
Min SN Setup		t_{su}	0.156
Min SN Hold		t_h	0.420

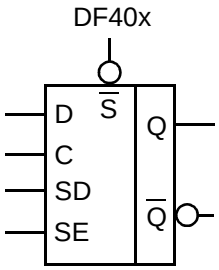
Logic Schematic



Description

DF40x is a family of static, master-slave, multiplexed scan D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF40x *inst_name* (Q, QN, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF40x port map (Q, QN, C, D, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF401	DF402	DF404	DF406
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SN	2.2	2.2	3.3	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF401	6.2	5.045	14.5
DF402	6.2	5.845	17.1
DF404	7.8	8.758	25.5
DF406	8.5	10.359	31.1

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF401	From: C To: Q	t_{PLH} t_{PHL}	0.454 0.415	0.595 0.575	0.771 0.757	0.982 0.965	1.147 1.124
	From: C To: QN	t_{PLH} t_{PHL}	0.522 0.583	0.652 0.732	0.823 0.899	1.035 1.091	1.203 1.244
	From: SN To: Q	t_{PLH}	0.533	0.680	0.858	1.070	1.234
	From: SN To: QN	t_{PHL}	0.229	0.369	0.542	0.750	0.911
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF402	From: C To: Q	t_{PLH} t_{PHL}	0.455 0.428	0.610 0.629	0.776 0.804	0.917 0.952	1.083 1.123
	From: C To: QN	t_{PLH} t_{PHL}	0.596 0.650	0.729 0.808	0.881 0.963	1.011 1.090	1.157 1.231
	From: SN To: Q	t_{PLH}	0.603	0.768	0.936	1.075	1.240
	From: S To: QN	t_{PHL}	0.234	0.408	0.577	0.714	0.863
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DF404	From: C To: Q	t_{PLH} t_{PHL}	0.458 0.399	0.629 0.613	0.781 0.784	0.912 0.928	1.049 1.067
	From: C To: QN	t_{PLH} t_{PHL}	0.558 0.636	0.698 0.789	0.845 0.942	0.982 1.074	1.129 1.213
	From: SN To: Q	t_{PLH}	0.527	0.701	0.858	0.998	1.147
	From: SN To: QN	t_{PHL}	0.197	0.363	0.509	0.645	0.792
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF406	From: C To: Q	t_{PLH} t_{PHL}	0.503 0.455	0.675 0.680	0.821 0.851	0.948 0.995	1.074 1.136
	From: C To: QN	t_{PLH} t_{PHL}	0.651 0.704	0.785 0.875	0.923 1.022	1.053 1.145	1.187 1.269
	From: SN To: Q	t_{PLH}	0.635	0.800	0.950	1.085	1.221
	From: SN To: QN	t_{PHL}	0.231	0.409	0.553	0.682	0.813

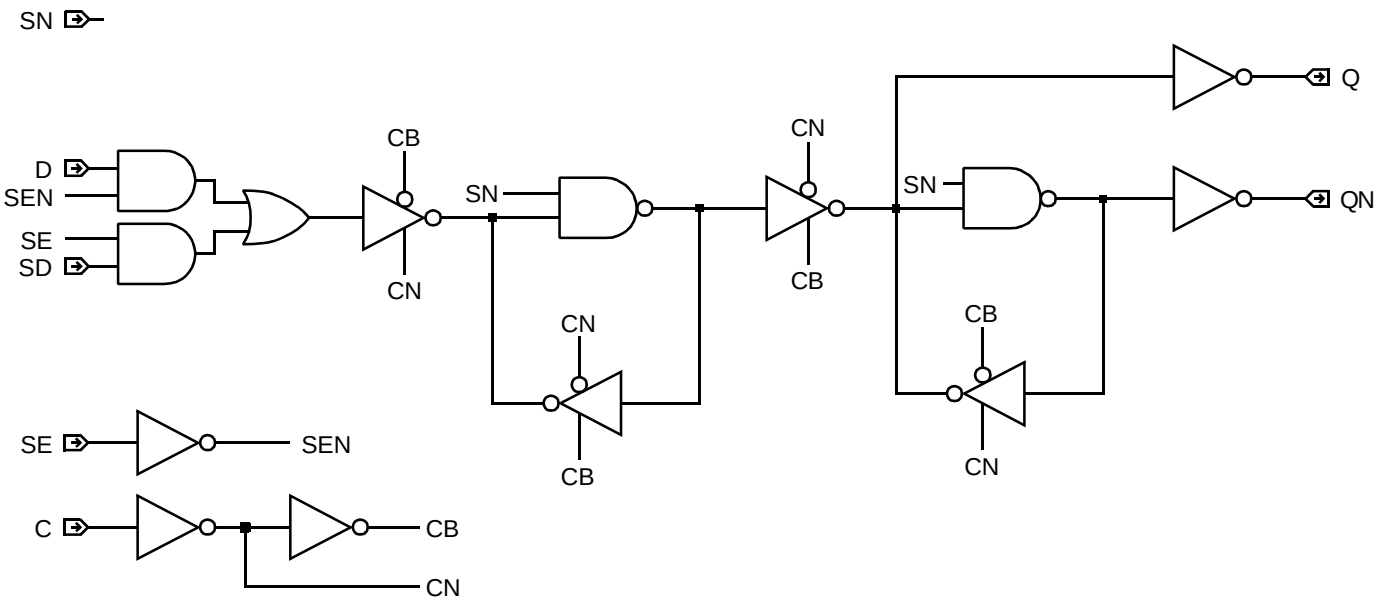
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF401	DF402	DF404	DF406
Min C Width	High	t_w	0.458	0.519	0.543	0.610
Min C Width	Low	t_w	0.584	0.582	0.663	0.671
Min SN Width	Low	t_w	0.410	0.502	0.458	0.553
Min D Setup		t_{su}	0.483	0.481	0.525	0.529
Min D Hold		t_h	0.127	0.127	0.141	0.142
Min SD Setup		t_{su}	0.483	0.481	0.525	0.529
Min SD Hold		t_h	0.127	0.127	0.141	0.142
Min SE Setup		t_{su}	0.583	0.581	0.626	0.630
Min SE Hold		t_h	0.127	0.127	0.141	0.142
Min SN Setup		t_{su}	0.127	0.127	0.160	0.160
Min SN Hold		t_h	0.414	0.414	0.454	0.459

Logic Schematic

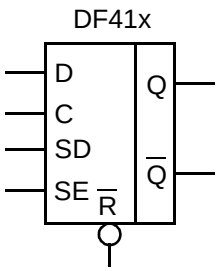


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DF41x is a family of static, master-slave, multiplexed scan D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF41x *inst_name* (Q, QN, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF41x port map (Q, QN, C, D, RN, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF411	DF412	DF414	DF416
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF411	6.8	4.901	17.2
DF412	6.8	5.701	20.0
DF414	8.5	8.343	29.7
DF416	9.2	9.943	35.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF411	From: C To: Q	t_{PLH} t_{PHL}	0.448 0.424	0.587 0.584	0.765 0.767	0.980 0.975	1.158 1.132
	From: C To: QN	t_{PLH} t_{PHL}	0.501 0.639	0.619 0.804	0.786 0.978	1.004 1.168	1.183 1.331
	From: RN To: Q	t_{PHL}	0.766	0.962	1.162	1.375	1.555
	From: RN To: QN	t_{PLH}	0.299	0.435	0.610	0.822	0.994
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF412	From: C To: Q	t_{PLH} t_{PHL}	0.448 0.426	0.601 0.628	0.766 0.811	0.908 0.955	1.068 1.112
	From: C To: QN	t_{PLH} t_{PHL}	0.558 0.708	0.687 0.894	0.843 1.057	0.987 1.190	1.159 1.346
	From: RN To: Q	t_{PHL}	0.870	1.117	1.308	1.448	1.591
	From: RN To: QN	t_{PLH}	0.302	0.448	0.610	0.751	0.912
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DF414	From: C To: Q	t_{PLH} t_{PHL}	0.497 0.410	0.629 0.649	0.781 0.827	0.922 0.969	1.057 1.108
	From: C To: QN	t_{PLH} t_{PHL}	0.537 0.685	0.657 0.890	0.801 1.053	0.943 1.182	1.095 1.306
	From: RN To: Q	t_{PHL}	0.813	1.033	1.215	1.372	1.534
	From: RN To: QN	t_{PLH}	0.324	0.457	0.615	0.764	0.924
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF416	From: C To: Q	t_{PLH} t_{PHL}	0.498 0.489	0.669 0.660	0.803 0.841	0.933 0.986	1.078 1.124
	From: C To: QN	t_{PLH} t_{PHL}	0.637 0.804	0.749 0.977	0.893 1.133	1.018 1.269	1.153 1.414
	From: RN To: Q	t_{PHL}	0.900	1.175	1.370	1.518	1.657
	From: RN To: QN	t_{PLH}	0.330	0.466	0.610	0.743	0.882

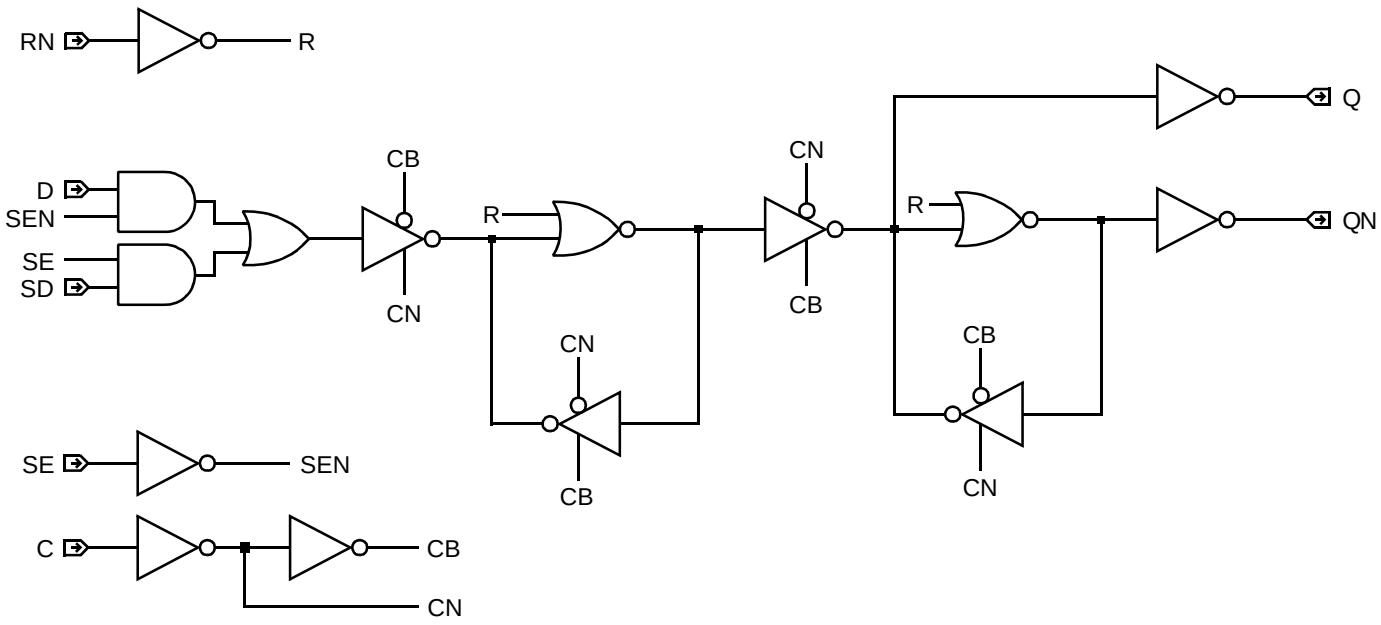
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell DF411	DF412	DF414	DF416
Min C Width	High	t_w	0.487	0.559	0.588	0.661
Min C Width	Low	t_w	0.562	0.558	0.643	0.641
Min RN Width	Low	t_w	0.474	0.476	0.536	0.537
Min D Setup		t_{su}	0.464	0.471	0.501	0.501
Min D Hold		t_h	0.127	0.127	0.142	0.142
Min SD Setup		t_{su}	0.464	0.471	0.501	0.501
Min SD Hold		t_h	0.127	0.127	0.142	0.142
Min SE Setup		t_{su}	0.564	0.571	0.601	0.601
Min SE Hold		t_h	0.127	0.127	0.142	0.142
Min RN Setup		t_{su}	0.247	0.248	0.312	0.313
Min RN Hold		t_h	0.296	0.296	0.321	0.321

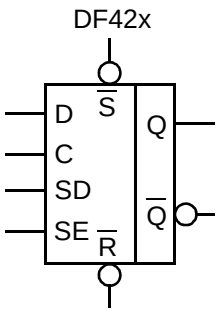
Logic Schematic



Description

DF42x is a family of static, master-slave, multiplexed scan D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

HDL Syntax

Verilog ..... DF421x *inst_name* (Q, QN, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF421x port map (Q, QN, C, D, RN, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF421	DF422	DF424	DF426
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.1	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SN	2.2	2.1	2.1	2.4

AMI350LXSC 0.35 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF421	7.5	8.274	18.5
DF422	7.5	6.358	21.5
DF424	8.8	8.759	28.6
DF426	9.8	10.360	34.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF421	From: C To: Q	t_{PLH} t_{PHL}	0.463 0.417	0.604 0.584	0.780 0.767	0.992 0.969	1.157 1.124
	From: C To: QN	t_{PLH} t_{PHL}	0.545 0.697	0.682 0.843	0.854 1.025	1.061 1.242	1.228 1.415
	From: RN To: Q	t_{PHL}	0.789	0.973	1.177	1.406	1.581
	From: RN To: QN	t_{PLH}	0.336	0.473	0.650	0.871	1.052
	From: SN To: Q	t_{PLH}	0.538	0.683	0.863	1.079	1.246
	From: SN To: QN	t_{PHL}	0.232	0.374	0.549	0.754	0.917
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF422	From: C To: Q	t_{PLH} t_{PHL}	0.461 0.430	0.609 0.640	0.778 0.819	0.925 0.957	1.092 1.112
	From: C To: QN	t_{PLH} t_{PHL}	0.621 0.784	0.758 0.975	0.909 1.146	1.039 1.279	1.188 1.422
	From: RN To: Q	t_{PHL}	0.901	1.132	1.329	1.481	1.650
	From: RN To: QN	t_{PLH}	0.340	0.494	0.661	0.803	0.967
	From: SN To: Q	t_{PLH}	0.615	0.777	0.946	1.082	1.229
	From: SN To: QN	t_{PHL}	0.235	0.404	0.573	0.709	0.862

	Number of Equivalent Loads		1	15	30	44	59 (max)
DF424	From: C To: Q	t_{PLH} t_{PHL}	0.826 0.677	0.935 0.865	1.081 1.020	1.215 1.152	1.367 1.285
	From: C To: QN	t_{PLH} t_{PHL}	0.515 0.597	0.658 0.775	0.813 0.923	0.955 1.055	1.106 1.198
	From: RN To: Q	t_{PHL}	0.470	0.646	0.790	0.928	1.075
	From: RN To: QN	t_{PLH}	0.904	1.054	1.200	1.330	1.469
	From: SN To: Q	t_{PLH}	0.311	0.455	0.603	0.742	0.891
	From: SN To: QN	t_{PHL}	0.688	0.853	1.001	1.137	1.296
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF426	From: C To: Q	t_{PLH} t_{PHL}	0.835 0.723	0.994 0.919	1.128 1.073	1.261 1.198	1.408 1.319
	From: C To: QN	t_{PLH} t_{PHL}	0.543 0.628	0.688 0.818	0.826 0.975	0.956 1.116	1.092 1.259
	From: RN To: Q	t_{PHL}	0.521	0.728	0.872	0.998	1.127
	From: RN To: QN	t_{PLH}	0.963	1.128	1.264	1.381	1.503
	From: SN To: Q	t_{PLH}	0.359	0.498	0.638	0.771	0.915
	From: SN To: QN	t_{PHL}	0.726	0.929	1.080	1.208	1.358

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

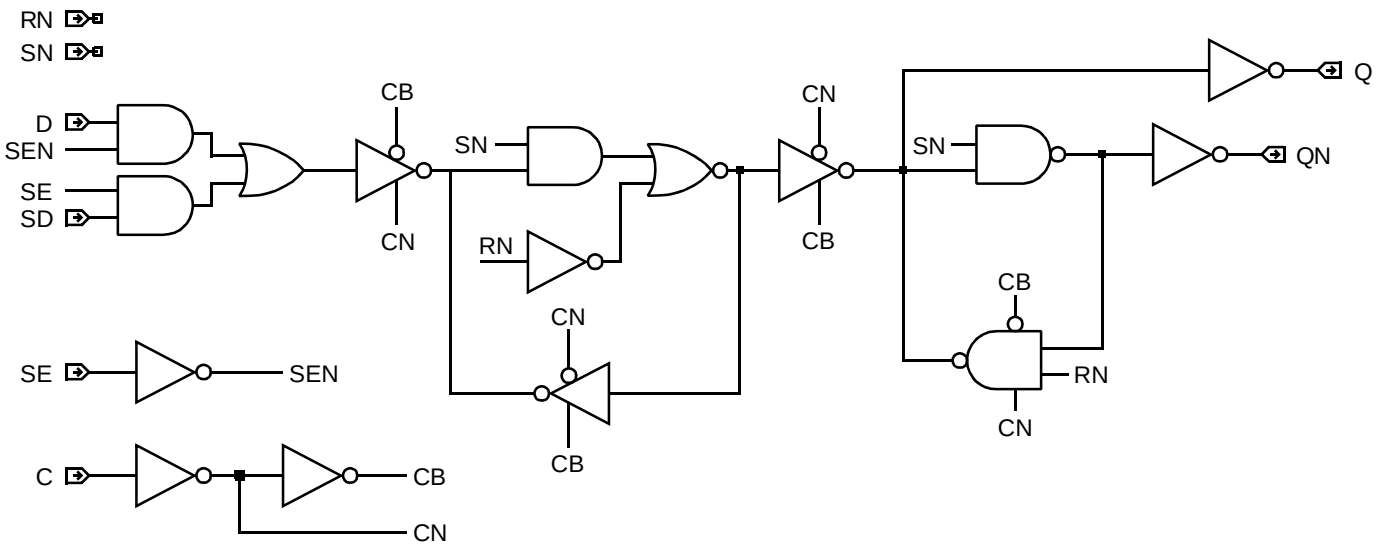
AMI350LXSC 0.35 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell DF421	DF422	DF424	DF426
Min C Width	High	t_w	0.530	0.609	0.538	0.547
Min C Width	Low	t_w	0.600	0.608	0.608	0.597
Min RN Width	Low	t_w	0.489	0.494	0.497	0.486
Min SN Width	Low	t_w	0.417	0.507	0.426	0.423
Min D Setup		t_{su}	0.495	0.500	0.499	0.488
Min D Hold		t_h	0.129	0.129	0.129	0.131
Min SD Setup		t_{su}	0.495	0.500	0.499	0.488
Min SD Hold		t_h	0.129	0.129	0.129	0.131
Min SE Setup		t_{su}	0.594	0.600	0.599	0.588
Min SE Hold		t_h	0.129	0.129	0.129	0.131
Min RN Setup		t_{su}	0.283	0.288	0.290	0.285
Min RN Hold		t_h	0.299	0.301	0.301	0.296
Min SN Setup		t_{su}	0.153	0.156	0.156	0.153
Min SN Hold		t_h	0.420	0.423	0.422	0.422

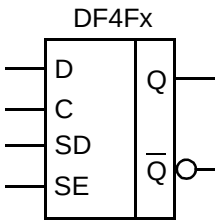
Logic Schematic



Description

DF4Fx is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF4Fx *inst_name* (Q, QN, C, D, SD, SE);

VHDL..... *inst_name*: DF4Fx port map (Q, QN, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF4F1	DF4F2	DF4F4	DF4F6
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF4F1	5.8	4.468	13.8
DF4F2	5.8	5.269	16.5
DF4F4	6.8	7.669	23.3
DF4F6	7.5	9.670	30.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF4F1	From: C To: Q	t_{PLH} t_{PHL}	0.442 0.411	0.584 0.574	0.760 0.756	0.970 0.961	1.139 1.114
	From: C To: QN	t_{PLH} t_{PHL}	0.481 0.547	0.609 0.682	0.778 0.848	0.988 1.046	1.158 1.210
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DF4F2	From: C To: Q	t_{PLH} t_{PHL}	0.449 0.423	0.612 0.625	0.775 0.805	0.912 0.948	1.066 1.105
	From: C To: QN	t_{PLH} t_{PHL}	0.547 0.612	0.692 0.762	0.845 0.915	0.973 1.042	1.156 1.184
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DF4F4	From: C To: Q	t_{PLH} t_{PHL}	0.655 0.599	0.793 0.782	0.937 0.953	1.070 1.079	1.214 1.196
	From: C To: QN	t_{PLH} t_{PHL}	0.456 0.512	0.598 0.681	0.745 0.840	0.878 0.964	1.023 1.098
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DF4F6	From: C To: Q	t_{PLH} t_{PHL}	0.654 0.610	0.798 0.758	0.932 0.901	1.054 1.028	1.186 1.156
	From: C To: QN	t_{PLH} t_{PHL}	0.478 0.543	0.615 0.733	0.751 0.870	0.884 0.995	1.029 1.132

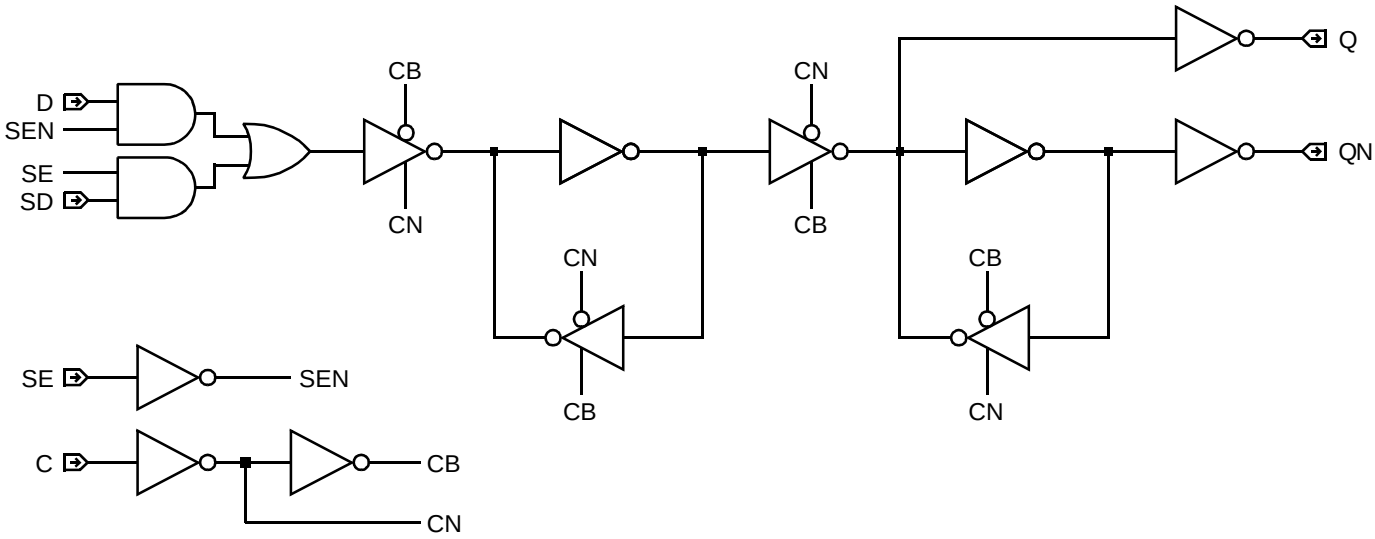
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF4F1	DF4F2	DF4F4	DF4F6
Min C Width	High	t_w	0.433	0.492	0.446	0.468
Min C Width	Low	t_w	0.544	0.544	0.553	0.549
Min D Setup		t_{su}	0.450	0.457	0.455	0.462
Min D Hold		t_h	0.124	0.127	0.125	0.126
Min SD Setup		t_{su}	0.450	0.457	0.455	0.462
Min SD Hold		t_h	0.124	0.127	0.125	0.126
Min SE Setup		t_{su}	0.551	0.559	0.554	0.562
Min SE Hold		t_h	0.124	0.127	0.125	0.126

Logic Schematic

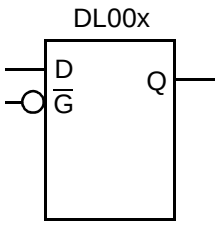


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DL00x is a family of transparent, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q
L	L	L
L	H	H
H	X	NC

NC = No Change

HDL Syntax

Verilog ..... DL00x *inst_name* (Q, D, GN);

VHDL..... *inst_name*: DL00x port map (Q, D, GN);

Pin Loading

Pin Name	Equivalent Loads	
	DL001	DL002
D	1.0	1.0
GN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL001	2.2	1.826	3.4
DL002	2.2	2.226	4.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL001	From: D To: Q	t_{PLH} t_{PHL}	0.252 0.288	0.391 0.433	0.567 0.607	0.778 0.810	0.944 0.966
	From: GN To: Q	t_{PLH} t_{PHL}	0.309 0.409	0.439 0.556	0.611 0.728	0.824 0.926	0.994 1.076
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DL002	From: D To: Q	t_{PLH} t_{PHL}	0.247 0.298	0.396 0.486	0.562 0.658	0.706 0.795	0.869 0.942
	From: GN To: Q	t_{PLH} t_{PHL}	0.303 0.408	0.454 0.597	0.618 0.770	0.759 0.908	0.917 1.055

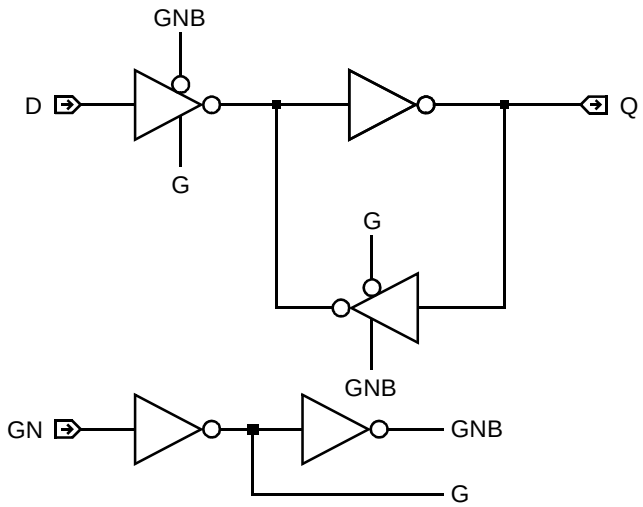
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DL001	DL002
Min GN Width	Low	t_w	0.409	0.409
Min D Setup		t_{su}	0.300	0.298
Min D Hold		t_h	0.102	0.102

Logic Schematic



Core Logic

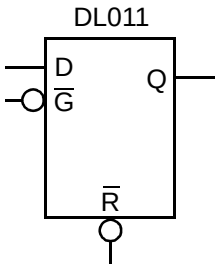
DL011

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DL011 is a transparent, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q
H	L	L	L
H	H	L	H
H	X	H	NC
L	X	X	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
RN	1.0

Equivalent Gates 3.0

HDL Syntax

Verilog ..... DL011 *inst_name* (Q, D, GN, RN);

VHDL..... *inst_name*: DL011 port map (Q, D, GN, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.242	nA
EQL_{pd}	5.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
D	Q	t_{PLH} t_{PHL}	0.313 0.309	0.390 0.365	0.621 0.507	0.852 0.632	1.007 0.709
GN	Q	t_{PLH} t_{PHL}	0.364 0.415	0.439 0.466	0.669 0.608	0.906 0.745	1.066 0.835
RN	Q	t_{PLH} t_{PHL}	0.261 0.198	0.337 0.245	0.565 0.377	0.794 0.503	0.947 0.585

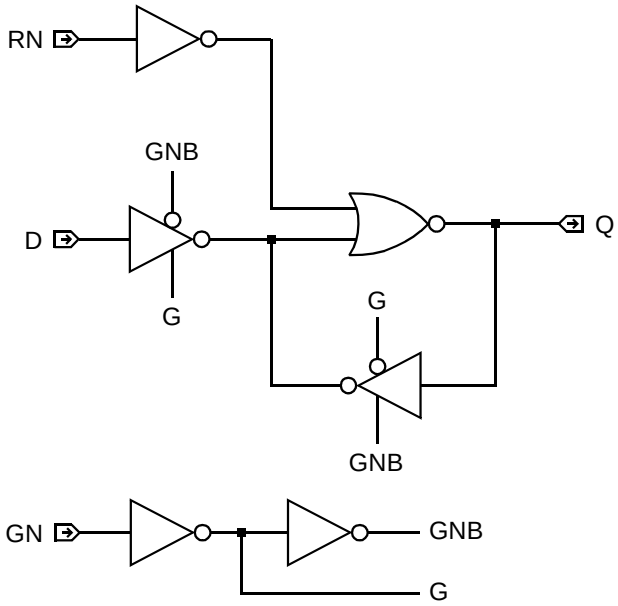
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.420
Min RN Width	Low	t_w	0.609
Min D Setup		t_{su}	0.315
Min D Hold		t_h	0.103
Min RN Setup		t_{su}	0.259
Min RN Hold		t_h	0.147

Logic Schematic



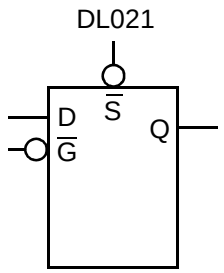
DL021

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DL021 is a transparent, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q
L	X	X	H
H	H	X	NC
H	L	L	L
H	L	H	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0

Equivalent Gates 2.7

HDL Syntax

Verilog ..... DL021 *inst_name* (Q, D, GN, SN);

VHDL..... *inst_name*: DL021 port map (Q, D, GN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.114	nA
EQL_{pd}	3.6	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
D	Q	t_{PLH} t_{PHL}	0.275 0.322	0.326 0.388	0.480 0.563	0.635 0.726	0.739 0.834
GN	Q	t_{PLH} t_{PHL}	0.326 0.437	0.379 0.504	0.535 0.683	0.687 0.844	0.787 0.947
SN	Q	t_{PLH} t_{PHL}	0.142 0.169	0.197 0.229	0.344 0.394	0.492 0.554	0.598 0.661

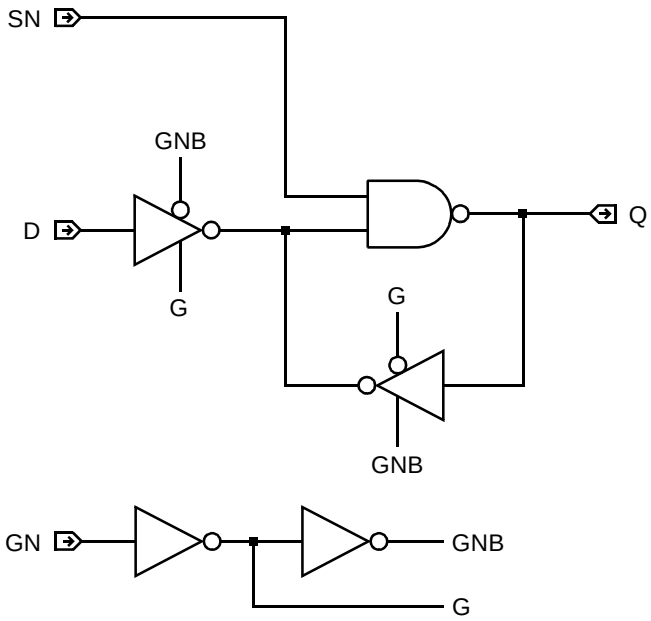
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.436
Min SN Width	Low	t_w	0.679
Min D Setup		t_{su}	0.320
Min D Hold		t_h	0.099
Min SN Setup		t_{su}	0.169
Min SN Hold		t_h	0.344

Logic Schematic

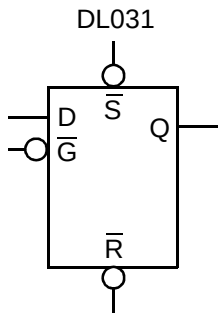


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DL031 is a transparent, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	X	H	NC
H	H	L	L	L
H	H	H	L	H

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0
RN	1.1

Equivalent Gates 3.2

HDL Syntax

Verilog ..... DL031 *inst_name* (Q, D, GN, RN, SN);

VHDL..... *inst_name*: DL031 port map (Q, D, GN, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.587	nA
EQL_{pd}	5.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
D	Q	t_{PLH} t_{PHL}	0.337 0.402	0.395 0.473	0.558 0.666	0.714 0.841	0.815 0.951
GN	Q	t_{PLH} t_{PHL}	0.390 0.544	0.443 0.609	0.603 0.791	0.762 0.963	0.869 1.075
SN	Q	t_{PLH} t_{PHL}	0.143 0.178	0.197 0.238	0.353 0.401	0.502 0.561	0.599 0.669
RN	Q	t_{PLH} t_{PHL}	0.358 0.334	0.417 0.398	0.578 0.578	0.728 0.747	0.824 0.857

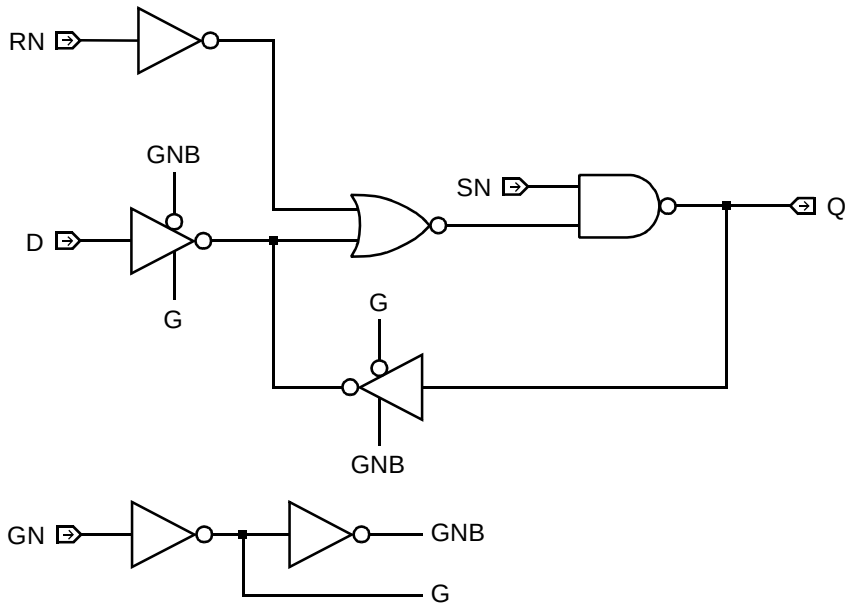
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.539
Min RN Width	Low	t_w	0.115
Min SN Width	Low	t_w	0.658
Min D Setup		t_{su}	0.412
Min D Hold		t_h	0.103
Min SN Setup		t_{su}	0.174
Min SN Hold		t_h	0.304
Min RN Setup		t_{su}	0.348
Min RN Hold		t_h	0.149

Logic Schematic

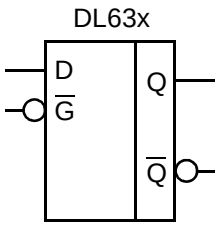


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

DL63x is a family of transparent, buffered D latches with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DL63x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL63x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL631	DL632	DL634	DL636
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL631	3.8	3.027	7.8
DL632	3.8	3.827	10.1
DL634	4.2	5.827	15.7
DL636	5.0	7.828	22.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL631	From: D To: Q	t_{PLH} t_{PHL}	0.417 0.441	0.537 0.575	0.708 0.739	0.930 0.935	1.112 1.086
	From: D To: QN	t_{PLH} t_{PHL}	0.366 0.372	0.500 0.511	0.673 0.681	0.885 0.884	1.051 1.041
	From: GN To: Q	t_{PLH} t_{PHL}	0.471 0.560	0.594 0.694	0.763 0.859	0.977 1.054	1.151 1.206
	From: GN To: QN	t_{PLH} t_{PHL}	0.489 0.425	0.608 0.562	0.777 0.732	0.998 0.935	1.179 1.094
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DL632	From: D To: Q	t_{PLH} t_{PHL}	0.439 0.464	0.583 0.614	0.740 0.772	0.875 0.905	1.028 1.054
	From: D To: QN	t_{PLH} t_{PHL}	0.345 0.356	0.489 0.521	0.655 0.691	0.801 0.834	0.968 0.992
	From: GN To: Q	t_{PLH} t_{PHL}	0.497 0.594	0.639 0.735	0.795 0.887	0.929 1.016	1.080 1.161
	From: GN To: QN	t_{PLH} t_{PHL}	0.470 0.411	0.611 0.588	0.770 0.754	0.909 0.887	1.066 1.030
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DL634	From: D To: Q	t_{PLH} t_{PHL}	0.488 0.544	0.622 0.711	0.767 0.855	0.904 0.988	1.051 1.128
	From: D To: QN	t_{PLH} t_{PHL}	0.369 0.355	0.511 0.515	0.658 0.662	0.794 0.798	0.939 0.943
	From: GN To: Q	t_{PLH} t_{PHL}	0.524 0.664	0.664 0.814	0.810 0.963	0.945 1.098	1.089 1.240
	From: GN To: QN	t_{PLH} t_{PHL}	0.494 0.391	0.613 0.567	0.760 0.719	0.912 0.851	1.056 0.987

	Number of Equivalent Loads		1	22	44	65	87 (max)
DL636	From: D To: Q	t_{PLH} t_{PHL}	0.483 0.541	0.605 0.688	0.747 0.837	0.883 0.966	1.023 1.088
	From: D To: QN	t_{PLH} t_{PHL}	0.416 0.414	0.559 0.570	0.681 0.696	0.807 0.828	0.954 0.976
	From: GN To: Q	t_{PLH} t_{PHL}	0.547 0.633	0.668 0.801	0.808 0.940	0.946 1.070	1.096 1.208
	From: GN To: QN	t_{PLH} t_{PHL}	0.514 0.421	0.657 0.600	0.797 0.755	0.929 0.885	1.063 1.014

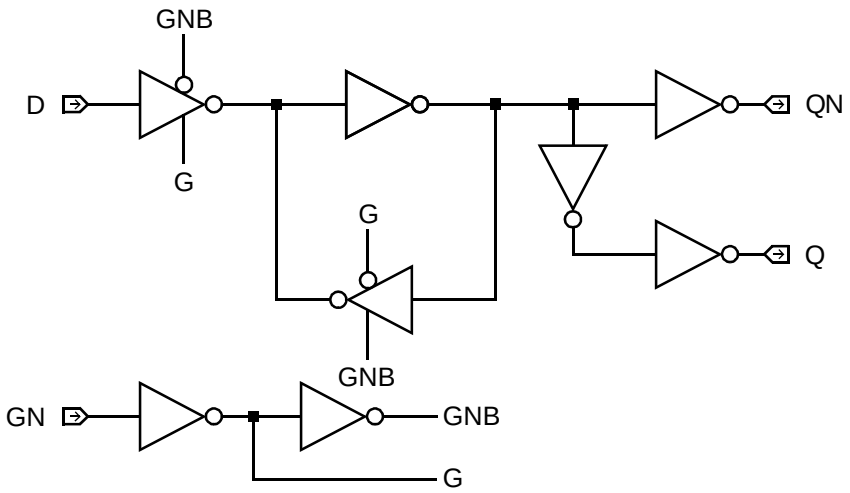
Delay will vary with input conditions. See page 2-Reference for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell DL631	DL632	DL634	DL636
Min GN Width	Low	t_w	0.399	0.413	0.445	0.476
Min D Setup		t_{su}	0.281	0.293	0.328	0.361
Min D Hold		t_h	0.103	0.102	0.102	0.102

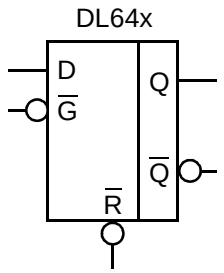
Logic Schematic



Description

DL64x is a family of transparent, buffered D latches with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

HDL Syntax

Verilog ..... DL64x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL64x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL641	DL642	DL644	DL646
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL641	3.8	3.099	7.8
DL642	3.8	3.899	10.4
DL644	5.2	7.044	20.4
DL646	6.0	8.645	26.0

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL641	From: D To: Q	t_{PLH} t_{PHL}	0.317 0.401	0.478 0.585	0.666 0.778	0.882 0.986	1.047 1.137
	From: D To: QN	t_{PLH} t_{PHL}	0.501 0.454	0.621 0.585	0.789 0.754	1.005 0.964	1.181 1.130
	From: GN To: Q	t_{PLH} t_{PHL}	0.384 0.523	0.533 0.697	0.716 0.891	0.934 1.108	1.103 1.269
	From: GN To: QN	t_{PLH} t_{PHL}	0.630 0.512	0.747 0.651	0.912 0.819	1.126 1.017	1.302 1.170
	From: RN To: Q	t_{PLH} t_{PHL}	0.344 0.301	0.500 0.460	0.685 0.634	0.898 0.840	1.061 1.009
	From: RN To: QN	t_{PLH} t_{PHL}	0.389 0.477	0.520 0.613	0.692 0.781	0.905 0.982	1.074 1.138
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DL642	From: D To: Q	t_{PLH} t_{PHL}	0.333 0.417	0.507 0.639	0.682 0.834	0.828 0.986	0.988 1.147
	From: D To: QN	t_{PLH} t_{PHL}	0.565 0.508	0.702 0.669	0.856 0.834	0.990 0.971	1.144 1.122
	From: GN To: Q	t_{PLH} t_{PHL}	0.391 0.547	0.558 0.767	0.731 0.956	0.875 1.102	1.036 1.256
	From: GN To: QN	t_{PLH} t_{PHL}	0.704 0.558	0.834 0.704	0.988 0.871	1.126 1.018	1.285 1.186
	From: RN To: Q	t_{PLH} t_{PHL}	0.345 0.277	0.532 0.463	0.703 0.642	0.841 0.787	0.991 0.945
	From: RN To: QN	t_{PLH} t_{PHL}	0.430 0.524	0.564 0.678	0.720 0.841	0.858 0.978	1.016 1.131

	Number of Equivalent Loads		1	15	30	44	59 (max)
DL644	From: D To: Q	t_{PLH} t_{PHL}	0.516 0.449	0.674 0.633	0.821 0.781	0.953 0.905	1.090 1.028
	From: D To: QN	t_{PLH} t_{PHL}	0.529 0.616	0.639 0.771	0.784 0.920	0.933 1.053	1.101 1.190
	From: GN To: Q	t_{PLH} t_{PHL}	0.578 0.555	0.706 0.722	0.858 0.881	1.006 1.019	1.170 1.162
	From: GN To: QN	t_{PLH} t_{PHL}	0.641 0.675	0.769 0.802	0.913 0.949	1.051 1.090	1.201 1.246
	From: RN To: Q	t_{PLH} t_{PHL}	0.446 0.358	0.598 0.529	0.750 0.671	0.888 0.805	1.032 0.951
	From: RN To: QN	t_{PLH} t_{PHL}	0.413 0.567	0.552 0.706	0.705 0.851	0.848 0.989	1.000 1.138
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
DL646	From: D To: Q	t_{PLH} t_{PHL}	0.537 0.481	0.638 0.614	0.738 0.715	0.822 0.797	0.907 0.877
	From: D To: QN	t_{PLH} t_{PHL}	0.586 0.652	0.661 0.773	0.752 0.883	0.846 0.967	0.954 1.043
	From: GN To: Q	t_{PLH} t_{PHL}	0.598 0.599	0.682 0.736	0.779 0.841	0.873 0.925	0.976 1.006
	From: GN To: QN	t_{PLH} t_{PHL}	0.698 0.721	0.777 0.853	0.871 0.943	0.965 1.016	1.072 1.089
	From: RN To: Q	t_{PLH} t_{PHL}	0.489 0.376	0.586 0.509	0.682 0.608	0.766 0.697	0.854 0.792
	From: RN To: QN	t_{PLH} t_{PHL}	0.491 0.627	0.581 0.711	0.674 0.810	0.760 0.907	0.852 1.015

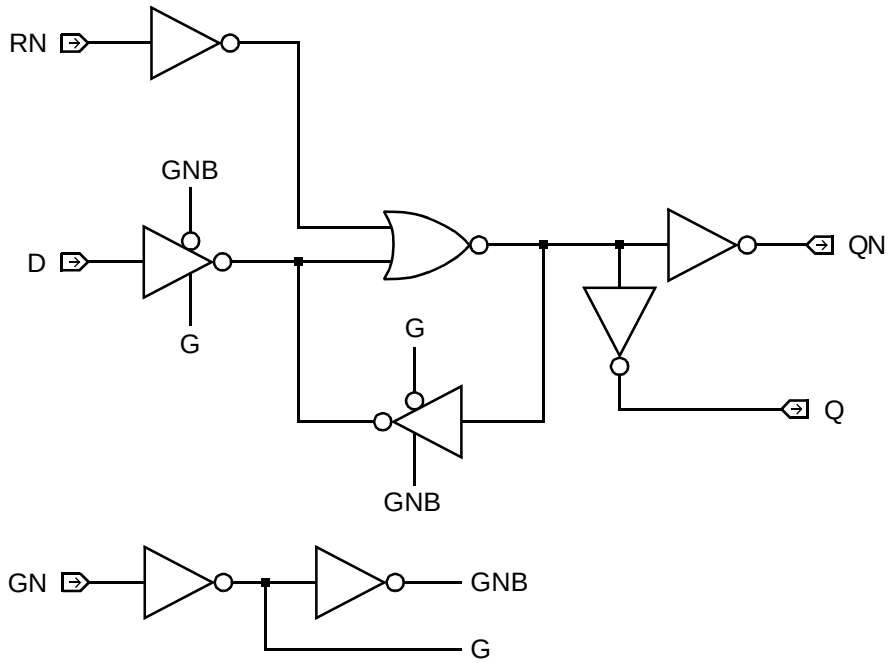
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL641	DL642	DL644	DL646
Min GN Width	Low	t_w	0.398	0.485	0.407	0.408
Min RN Width	Low	t_w	0.295	0.350	0.427	0.430
Min D Setup		t_{su}	0.398	0.485	0.299	0.300
Min D Hold		t_h	0.106	0.106	0.104	0.104
Min RN Setup		t_{su}	0.237	0.271	0.241	0.243
Min RN Hold		t_h	0.152	0.151	0.248	0.248

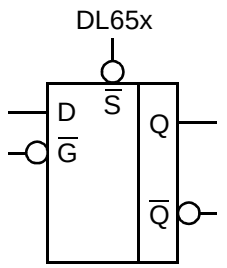
Logic Schematic



Description

DL65x is a family of transparent, buffered D latches with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

HDL Syntax

Verilog ..... DL65x *inst_name* (Q, QN, D, GN, SN);

VHDL..... *inst_name*: DL65x port map (Q, QN, D, GN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL651	DL652	DL654	DL656
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL651	4.0	3.315	8.0
DL652	4.0	4.115	10.5
DL654	5.0	6.916	18.7
DL656	5.8	8.517	24.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL651	From: D To: Q	t_{PLH} t_{PHL}	0.461 0.481	0.581 0.610	0.750 0.775	0.966 0.975	1.143 1.132
	From: D To: QN	t_{PLH} t_{PHL}	0.404 0.408	0.547 0.553	0.724 0.727	0.936 0.930	1.100 1.086
	From: GN To: Q	t_{PLH} t_{PHL}	0.507 0.599	0.642 0.726	0.812 0.891	1.017 1.093	1.177 1.253
	From: GN To: QN	t_{PLH} t_{PHL}	0.521 0.459	0.655 0.598	0.830 0.771	1.044 0.979	1.213 1.140
	From: SN To: Q	t_{PLH} t_{PHL}	0.324 0.329	0.452 0.454	0.621 0.615	0.830 0.816	0.996 0.977
	From: SN To: QN	t_{PLH} t_{PHL}	0.246 0.272	0.387 0.420	0.564 0.596	0.777 0.800	0.944 0.956
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DL652	From: D To: Q	t_{PLH} t_{PHL}	0.486 0.515	0.623 0.663	0.778 0.825	0.915 0.964	1.071 1.121
	From: D To: QN	t_{PLH} t_{PHL}	0.398 0.401	0.548 0.581	0.716 0.751	0.861 0.887	1.025 1.034
	From: GN To: Q	t_{PLH} t_{PHL}	0.540 0.643	0.674 0.790	0.829 0.941	0.964 1.068	1.119 1.208
	From: GN To: QN	t_{PLH} t_{PHL}	0.516 0.457	0.672 0.632	0.837 0.803	0.976 0.943	1.131 1.096
	From: SN To: Q	t_{PLH} t_{PHL}	0.350 0.356	0.486 0.511	0.645 0.669	0.785 0.802	0.946 0.948
	From: SN To: QN	t_{PLH} t_{PHL}	0.243 0.266	0.398 0.444	0.564 0.616	0.706 0.755	0.867 0.907

	Number of Equivalent Loads		1	15	30	44	59 (max)
DL654	From: D To: Q	t_{PLH} t_{PHL}	0.435 0.479	0.584 0.646	0.734 0.788	0.870 0.925	1.011 1.074
	From: D To: QN	t_{PLH} t_{PHL}	0.555 0.521	0.691 0.673	0.837 0.837	0.974 0.979	1.121 1.120
	From: GN To: Q	t_{PLH} t_{PHL}	0.498 0.586	0.635 0.736	0.779 0.891	0.913 1.034	1.058 1.187
	From: GN To: QN	t_{PLH} t_{PHL}	0.659 0.581	0.796 0.729	0.945 0.880	1.084 1.019	1.234 1.165
	From: SN To: Q	t_{PLH} t_{PHL}	0.312 0.311	0.456 0.490	0.606 0.647	0.746 0.785	0.889 0.926
	From: SN To: QN	t_{PLH} t_{PHL}	0.397 0.407	0.527 0.558	0.670 0.696	0.803 0.835	0.943 0.993
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DL656	From: D To: Q	t_{PLH} t_{PHL}	0.470 0.451	0.603 0.661	0.740 0.825	0.873 0.957	1.014 1.086
	From: D To: QN	t_{PLH} t_{PHL}	0.582 0.600	0.722 0.752	0.873 0.890	1.014 1.015	1.159 1.141
	From: GN To: Q	t_{PLH} t_{PHL}	0.520 0.596	0.644 0.799	0.783 0.949	0.921 1.075	1.071 1.196
	From: GN To: QN	t_{PLH} t_{PHL}	0.725 0.644	0.848 0.786	0.984 0.925	1.115 1.066	1.251 1.221
	From: SN To: Q	t_{PLH} t_{PHL}	0.338 0.324	0.469 0.491	0.609 0.650	0.746 0.793	0.891 0.936
	From: SN To: QN	t_{PLH} t_{PHL}	0.464 0.454	0.591 0.612	0.723 0.754	0.848 0.885	0.976 1.020

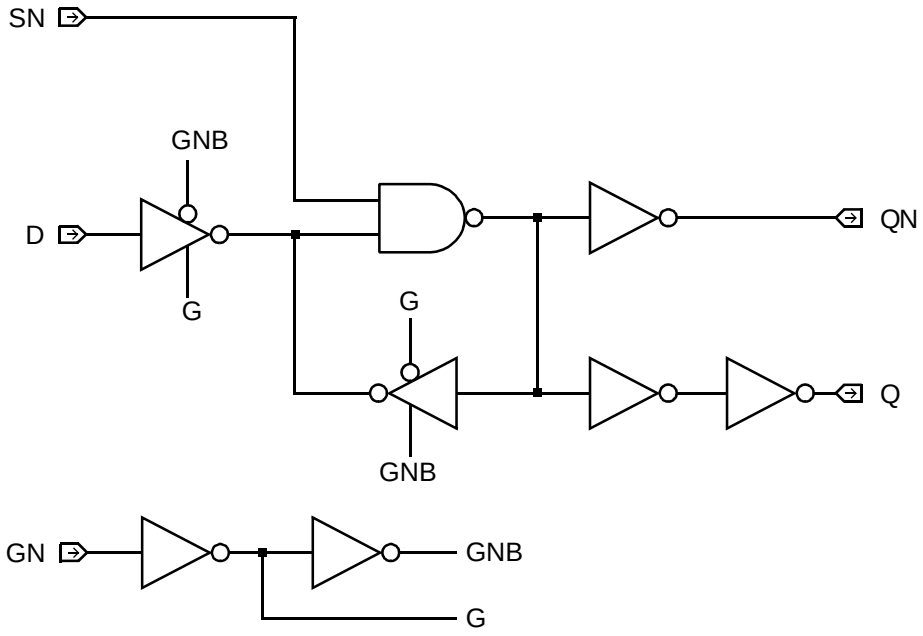
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL651	DL652	DL654	DL656
Min GN Width	Low	t_w	0.422	0.446	0.425	0.421
Min SN Width	Low	t_w	0.375	0.406	0.371	0.370
Min D Setup		t_{su}	0.306	0.329	0.304	0.303
Min D Hold		t_h	0.099	0.099	0.100	0.100
Min SN Setup		t_{su}	0.151	0.173	0.149	0.149
Min SN Hold		t_h	0.344	0.343	0.350	0.344

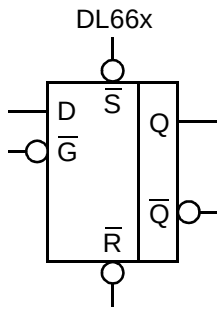
Logic Schematic



Description

DL66x is a family of transparent, buffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DL66x *inst_name* (Q, QN, D, GN, RN, SN);

VHDL..... *inst_name*: DL66x port map (Q, QN, D, GN, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL661	DL662	DL664	DL666
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	2.1	2.0
RN	1.1	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL661	4.2	3.787	9.8
DL662	4.2	4.588	12.3
DL664	6.5	8.117	24.5
DL666	7.2	9.718	30.1

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL661	From: D To: Q	t_{PLH} t_{PHL}	0.547 0.593	0.681 0.728	0.851 0.893	1.055 1.089	1.215 1.241
	From: D To: QN	t_{PLH} t_{PHL}	0.513 0.491	0.648 0.638	0.823 0.814	1.037 1.022	1.206 1.182
	From: GN To: Q	t_{PLH} t_{PHL}	0.602 0.721	0.732 0.841	0.901 1.005	1.110 1.213	1.275 1.381
	From: GN To: QN	t_{PLH} t_{PHL}	0.636 0.549	0.777 0.708	0.952 0.883	1.161 1.078	1.324 1.223
	From: SN To: Q	t_{PLH} t_{PHL}	0.349 0.352	0.471 0.478	0.639 0.643	0.853 0.846	1.026 1.007
	From: SN To: QN	t_{PLH} t_{PHL}	0.265 0.292	0.411 0.450	0.589 0.628	0.801 0.831	0.964 0.983
	From: R To: Q	t_{PLH} t_{PHL}	0.562 0.515	0.694 0.644	0.863 0.809	1.070 1.010	1.232 1.168
	From: RN To: QN	t_{PLH} t_{PHL}	0.434 0.519	0.567 0.671	0.741 0.836	0.957 1.034	1.128 1.202
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
DL662	From: D To: Q	t_{PLH} t_{PHL}	0.580 0.649	0.709 0.789	0.864 0.941	1.003 1.071	1.163 1.217
	From: D To: QN	t_{PLH} t_{PHL}	0.514 0.491	0.677 0.674	0.840 0.848	0.976 0.989	1.125 1.141
	From: GN To: Q	t_{PLH} t_{PHL}	0.648 0.774	0.766 0.911	0.913 1.064	1.048 1.195	1.206 1.344
	From: GN To: QN	t_{PLH} t_{PHL}	0.635 0.543	0.784 0.733	0.950 0.903	1.093 1.037	1.255 1.178
	From: SN To: Q	t_{PLH} t_{PHL}	0.381 0.376	0.506 0.528	0.669 0.690	0.814 0.826	0.976 0.979
	From: SN To: QN	t_{PLH} t_{PHL}	0.246 0.282	0.414 0.479	0.582 0.655	0.721 0.793	0.874 0.940
	From: RN To: Q	t_{PLH} t_{PHL}	0.611 0.560	0.732 0.701	0.879 0.853	1.012 0.982	1.167 1.128
	From: RN To: QN	t_{PLH} t_{PHL}	0.426 0.504	0.580 0.689	0.744 0.861	0.884 0.998	1.039 1.145

	Number of Equivalent Loads		1	15	30	44	59 (max)
DL664	From: D To: Q	t_{PLH} t_{PHL}	0.533 0.512	0.661 0.676	0.815 0.821	0.962 0.952	1.109 1.088
	From: D To: QN	t_{PLH} t_{PHL}	0.588 0.631	0.719 0.756	0.841 0.904	0.974 1.049	1.142 1.209
	From: GN To: Q	t_{PLH} t_{PHL}	0.590 0.625	0.726 0.799	0.864 0.945	0.996 1.066	1.143 1.186
	From: GN To: QN	t_{PLH} t_{PHL}	0.703 0.676	0.820 0.833	0.969 0.985	1.117 1.122	1.285 1.264
	From: SN To: Q	t_{PLH} t_{PHL}	0.256 0.332	0.410 0.480	0.554 0.620	0.678 0.761	0.825 0.921
	From: SN To: QN	t_{PLH} t_{PHL}	0.380 0.347	0.529 0.490	0.667 0.644	0.793 0.781	0.931 0.921
	From: RN To: Q	t_{PLH} t_{PHL}	0.436 0.377	0.589 0.556	0.738 0.709	0.870 0.838	1.008 0.967
	From: RN To: QN	t_{PLH} t_{PHL}	0.477 0.552	0.601 0.689	0.731 0.835	0.872 0.972	1.042 1.119
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
DL666	From: D To: Q	t_{PLH} t_{PHL}	0.548 0.540	0.677 0.701	0.817 0.835	0.952 0.968	1.094 1.112
	From: D To: QN	t_{PLH} t_{PHL}	0.627 0.675	0.742 0.841	0.889 0.978	1.039 1.095	1.203 1.208
	From: GN To: Q	t_{PLH} t_{PHL}	0.579 0.622	0.713 0.799	0.882 0.954	1.028 1.085	1.145 1.213
	From: GN To: QN	t_{PLH} t_{PHL}	0.752 0.734	0.894 0.879	1.031 1.018	1.156 1.146	1.285 1.278
	From: SN To: Q	t_{PLH} t_{PHL}	0.273 0.324	0.413 0.501	0.556 0.638	0.689 0.769	0.823 0.904
	From: SN To: QN	t_{PLH} t_{PHL}	0.442 0.404	0.574 0.558	0.710 0.699	0.835 0.825	0.963 0.952
	From: RN To: Q	t_{PLH} t_{PHL}	0.461 0.393	0.594 0.565	0.739 0.720	0.878 0.858	1.023 0.990
	From: RN To: QN	t_{PLH} t_{PHL}	0.502 0.600	0.654 0.736	0.789 0.881	0.914 1.016	1.041 1.154

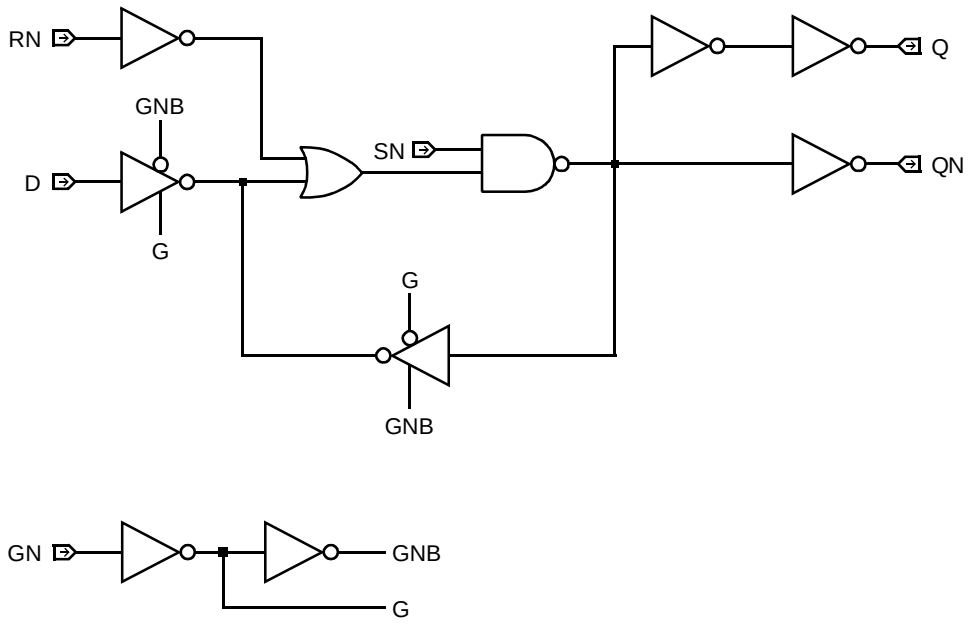
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL661	DL662	DL664	DL666
Min GN Width	Low	t_w	0.535	0.564	0.451	0.448
Min RN Width	Low	t_w	0.332	0.357	0.220	0.218
Min SN Width	Low	t_w	0.364	0.397	0.417	0.416
Min D Setup		t_{su}	0.407	0.436	0.335	0.335
Min D Hold		t_h	0.104	0.104	0.099	0.099
Min SN Setup		t_{su}	0.167	0.188	0.135	0.135
Min SN Hold		t_h	0.302	0.304	0.407	0.403
Min RN Setup		t_{su}	0.354	0.378	0.248	0.247
Min RN Hold		t_h	0.149	0.149	0.311	0.310

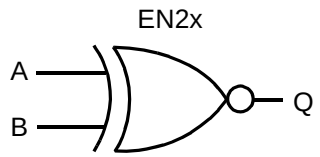
Logic Schematic



Description

EN2x is a family of 2-input gates which perform the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... EN2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EN2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EN21	EN22	EN23	EN24	EN26
A	2.0	4.2	3.9	3.9	3.9
B	2.1	4.2	4.0	3.9	3.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EN21	1.7	1.434	3.1
EN22	3.5	2.867	7.2
EN23	2.7	3.075	9.0
EN24	2.7	3.715	11.0
EN26	3.2	4.355	13.7

a. See page 2-13 for power equation.

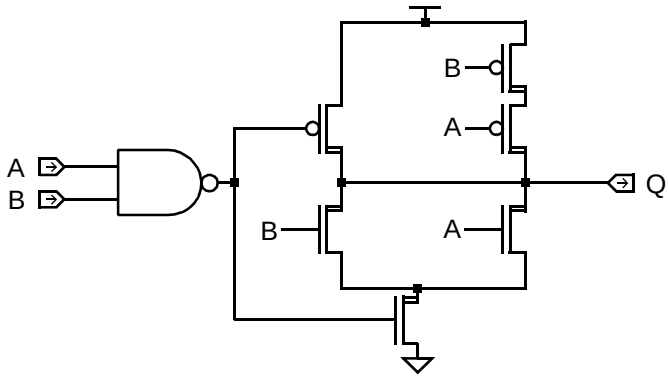
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

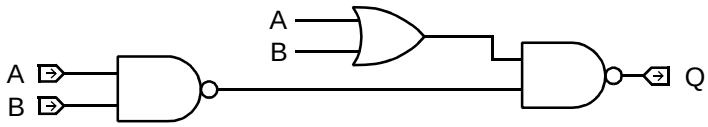
EN21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.220 0.169	0.264 0.239	0.393 0.414	0.522 0.595	0.608 0.738
EN22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.192 0.118	0.254 0.224	0.332 0.347	0.426 0.492	0.499 0.610
EN23	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.184 0.303	0.333 0.471	0.497 0.643	0.639 0.785	0.799 0.941
EN24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.211 0.321	0.369 0.509	0.525 0.670	0.661 0.810	0.799 0.955
EN26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.217 0.357	0.373 0.561	0.513 0.711	0.645 0.850	0.785 0.999

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



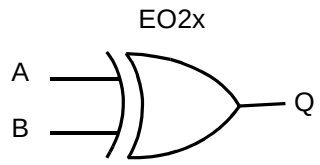
LOGICAL



Description

EO2x is a family of 2-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... EO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EO21	EO22	EO23	EO24	EO26
A	2.1	3.9	4.2	4.1	4.1
B	2.2	3.9	4.2	4.1	4.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO21	1.7	1.250	3.3
EO22	2.2	2.434	6.2
EO23	4.0	3.667	9.9
EO24	4.5	4.468	12.8
EO26	4.5	5.268	14.8

a. See page 2-13 for power equation.

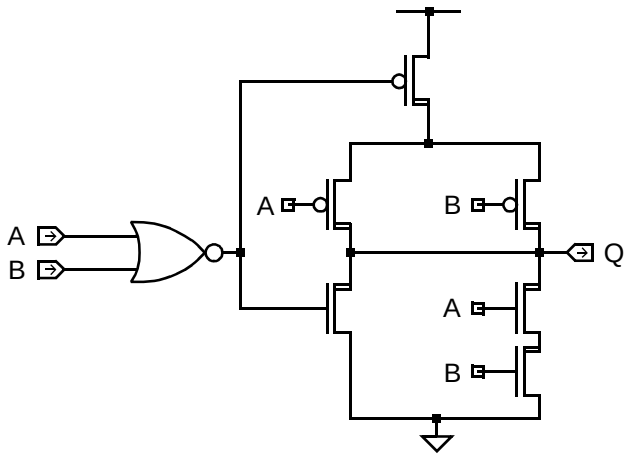
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

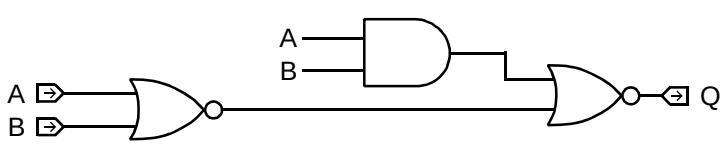
EO21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.265 0.190	0.341 0.267	0.567 0.475	0.792 0.678	0.942 0.811
EO22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.212 0.127	0.314 0.250	0.452 0.389	0.626 0.558	0.766 0.703
EO23	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.164 0.263	0.316 0.429	0.476 0.596	0.615 0.733	0.778 0.884
EO24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.178 0.288	0.322 0.447	0.472 0.601	0.609 0.738	0.753 0.879
EO26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.215 0.295	0.343 0.481	0.475 0.625	0.612 0.754	0.763 0.885

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



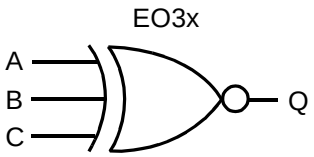
LOGICAL



Description

EO3x is a family of 3-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

HDL Syntax

Verilog ..... EO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: EO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	EO31	EO32	EO33	EO34	EO36
A	2.1	2.1	2.2	2.1	2.1
B	2.1	2.1	2.1	2.1	2.1
C	2.1	3.1	3.2	3.2	3.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO31	3.2	2.435	8.6
EO32	3.8	3.044	12.0
EO33	5.0	3.804	15.7
EO34	5.2	4.604	17.6
EO36	5.5	5.405	20.7

a. See page 2-13 for power equation.

AMI350LXSC 0.35 micron CMOS Standard Cell

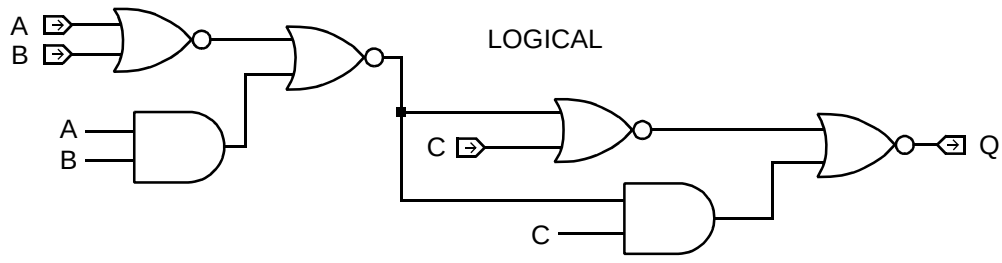
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

EO31	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.546 0.482	0.614 0.565	0.837 0.799	1.074 1.022	1.238 1.168
EO32	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.576 0.519	0.672 0.628	0.809 0.783	0.987 0.965	1.132 1.103
EO33	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.543 0.679	0.689 0.830	0.849 0.994	0.989 1.132	1.151 1.286
EO34	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.541 0.672	0.699 0.838	0.851 1.002	0.984 1.146	1.122 1.292
EO36	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.587 0.714	0.744 0.902	0.887 1.051	1.018 1.178	1.152 1.301

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

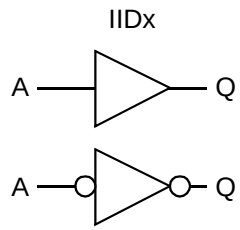
Logic Schematic



Description

IIDx is a family of non-inverting clock drivers with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... IIDx *inst_name* (Q, A);

VHDL..... *inst_name*: IIDx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads				
	IID1	IID2	IID3	IID4	IID6
A	1.0	1.0	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IID1	1.0	0.801	2.1
IID2	1.0	1.201	3.3
IID3	1.2	2.001	4.5
IID4	1.5	2.401	5.8
IID6	1.7	3.202	8.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

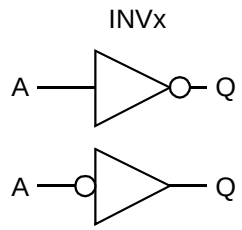
IID1	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.171 0.164	0.301 0.294	0.470 0.461	0.684 0.667	0.859 0.832
IID2	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.223 0.161	0.379 0.326	0.538 0.489	0.672 0.623	0.826 0.769
IID3	**Number of Equivalent Loads**		**1**	**11**	**22**	**34**	**45 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.128 0.119	0.261 0.263	0.405 0.408	0.563 0.563	0.711 0.706
IID4	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.135 0.125	0.284 0.278	0.425 0.425	0.558 0.557	0.708 0.695
IID6	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.136 0.165	0.290 0.323	0.432 0.454	0.565 0.590	0.709 0.735

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

INVx is a family of inverters which perform the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

HDL Syntax

Verilog ..... INVx *inst_name* (Q, A);

VHDL..... *inst_name*: INVx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads					
	INV1	INV2	INV3	INV4	INV5	INV6
A	1.0	1.9	2.9	4.0	4.9	5.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
INV1	0.8	0.401	0.5
INV2	1.0	0.801	0.9
INV3	1.0	1.201	1.1
INV4	1.2	1.601	1.4
INV5	1.2	2.001	1.7
INV6	1.5	3.047	1.9

a. See page 2-13 power equation

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

INV1	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.091 0.118	0.219 0.255	0.384 0.414	0.588 0.611	0.748 0.775
INV2	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.059 0.080	0.212 0.243	0.361 0.402	0.491 0.534	0.647 0.682
INV3	**Number of Equivalent Loads**		**1**	**11**	**22**	**34**	**45 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.049 0.065	0.186 0.223	0.320 0.361	0.466 0.497	0.602 0.614
INV4	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.040 0.082	0.201 0.215	0.342 0.375	0.470 0.512	0.607 0.638
INV5	**Number of Equivalent Loads**		**1**	**18**	**36**	**55**	**73 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.046 0.063	0.177 0.217	0.318 0.357	0.453 0.488	0.570 0.590
INV6	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.049 0.045	0.184 0.235	0.320 0.383	0.439 0.505	0.555 0.620

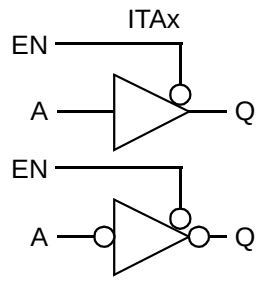
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ITAx is a family of non-inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

HDL Syntax

Verilog ..... ITAx *inst_name* (Q, A, EN);

VHDL..... *inst_name*: ITAx port map (Q, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITA1	ITA2	ITA4	ITA6
A	1.0	1.0	1.0	1.0
EN	1.6	2.1	3.3	4.5
Q	0.6	0.6	1.3	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITA1	1.5	1.217	3.4
ITA2	2.0	1.634	5.3
ITA4	2.7	2.466	9.7
ITA6	3.8	3.299	14.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	15	30	45	60 (max)
ITA1	From: A To: Q	t_{PLH} t_{PHL}	0.275 0.228	1.341 1.235	2.499 2.310	3.669 3.383	4.846 4.455
	From: EN To: Q	t_{ZH} t_{ZL}	0.076 0.181	1.262 1.160	2.415 2.226	3.545 3.304	4.687 4.389
	Number of Equivalent Loads		**1**	**26**	**52**	**77**	**103 (max)**
ITA2	From: A To: Q	t_{PLH} t_{PHL}	0.221 0.234	1.186 1.120	2.197 2.045	3.172 2.941	4.189 3.876
	From: EN To: Q	t_{ZH} t_{ZL}	0.148 0.122	1.143 1.034	2.065 1.963	3.011 2.855	4.091 3.782
	Number of Equivalent Loads		**1**	**48**	**96**	**143**	**191 (max)**
ITA4	From: A To: Q	t_{PLH} t_{PHL}	0.251 0.242	1.158 1.102	2.090 1.968	3.004 2.807	3.938 3.658
	From: EN To: Q	t_{ZH} t_{ZL}	0.113 0.124	1.062 0.998	1.938 1.854	2.825 2.693	3.784 3.558
	Number of Equivalent Loads		**1**	**70**	**139**	**208**	**278 (max)**
ITA6	From: A To: Q	t_{PLH} t_{PHL}	0.286 0.298	1.175 1.149	2.061 1.970	2.955 2.793	3.868 3.631
	From: EN To: Q	t_{ZH} t_{ZL}	0.052 0.147	1.042 1.001	1.905 1.823	2.763 2.646	3.641 3.487

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

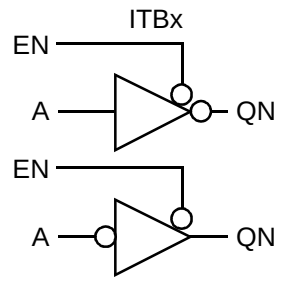
Delay (ns) From	To	Parameter	Cell ITA1	ITA2	ITA4	ITA6
EN	Q	t_{HZ} t_{LZ}	0.115 0.098	0.114 0.117	0.113 0.153	0.111 0.187

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ITBx is a family of inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITBx *inst_name* (QN, A, EN);

VHDL..... *inst_name*: ITBx port map (QN, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITB1	ITB2	ITB4	ITB6
A	1.0	2.0	4.2	6.3
EN	1.7	2.1	3.3	4.5
QN	0.6	0.6	1.3	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITB1	1.2	0.817	1.9
ITB2	1.5	1.233	2.7
ITB4	2.5	2.066	5.1
ITB6	3.5	2.899	7.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	15	30	45	60 (max)
ITB1	From: A To: QN	t_{PLH} t_{PHL}	0.160 0.173	1.250 1.180	2.407 2.253	3.568 3.322	4.742 4.392
	From: EN To: QN	t_{ZH} t_{ZL}	0.216 0.174	1.299 1.173	2.389 2.247	3.535 3.324	4.722 4.402
	Number of Equivalent Loads		**1**	**26**	**52**	**77**	**103 (max)**
ITB2	From: A To: QN	t_{PLH} t_{PHL}	0.105 0.122	1.092 1.050	2.088 1.966	3.052 2.850	4.070 3.785
	From: EN To: QN	t_{ZH} t_{ZL}	0.107 0.124	1.117 1.033	2.088 1.968	3.047 2.862	4.089 3.789
	Number of Equivalent Loads		**1**	**48**	**96**	**143**	**191 (max)**
ITB4	From: A To: QN	t_{PLH} t_{PHL}	0.080 0.093	1.022 0.967	1.937 1.823	2.838 2.658	3.775 3.512
	From: EN To: QN	t_{ZH} t_{ZL}	0.074 0.129	1.037 0.995	1.918 1.855	2.800 2.694	3.733 3.553
	Number of Equivalent Loads		**1**	**70**	**139**	**208**	**278 (max)**
ITB6	From: A To: QN	t_{PLH} t_{PHL}	0.075 0.120	0.965 0.952	1.854 1.748	2.748 2.567	3.662 3.425
	From: EN To: QN	t_{ZH} t_{ZL}	0.086 0.156	1.043 0.989	1.920 1.817	2.806 2.644	3.722 3.483

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ITB1	ITB2	ITB4	ITB6
EN	QN	t_{HZ} t_{LZ}	0.114 0.101	0.113 0.118	0.112 0.155	0.112 0.185

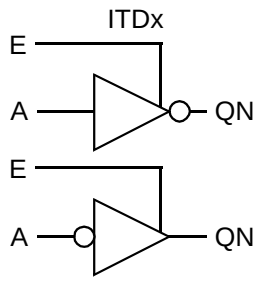
ITD1x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ITD1x is a family of inverting internal tristate buffers with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITDx *inst_name* (QN, A, E);

VHDL..... *inst_name*: ITDx port map (QN, A, E);

Pin Loading

Pin Name	Equivalent Loads			
	ITD1	ITD2	ITD4	ITD6
A	1.0	2.0	4.2	6.2
E	1.5	1.9	2.8	3.7
QN	0.5	0.6	1.4	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITD1	1.2	0.817	2.0
ITD2	1.5	1.233	3.0
ITD4	2.5	2.066	5.6
ITD6	3.5	2.899	8.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	15	30	45	60 (max)
ITD1	From: A To: QN	t_{PLH} t_{PHL}	0.164 0.168	1.250 1.187	2.400 2.238	3.567 3.296	4.748 4.379
	From: E To: QN	t_{ZH} t_{ZL}	0.191 0.228	1.264 1.247	2.426 2.254	3.592 3.311	4.759 4.379
	Number of Equivalent Loads		**1**	**26**	**52**	**77**	**103 (max)**
ITD2	From: A To: QN	t_{PLH} t_{PHL}	0.120 0.103	1.086 1.040	2.084 1.963	3.052 2.849	4.076 3.782
	From: E To: QN	t_{ZH} t_{ZL}	0.142 0.108	1.120 1.043	2.125 1.994	3.093 2.877	4.108 3.771
	Number of Equivalent Loads		**1**	**48**	**96**	**143**	**191 (max)**
ITD4	From: A To: QN	t_{PLH} t_{PHL}	0.098 0.092	1.021 0.962	1.951 1.811	2.858 2.642	3.780 3.496
	From: E To: QN	t_{ZH} t_{ZL}	0.135 0.096	1.074 1.040	1.998 1.842	2.902 2.653	3.830 3.539
	Number of Equivalent Loads		**1**	**70**	**139**	**208**	**278 (max)**
ITD6	From: A To: QN	t_{PLH} t_{PHL}	0.106 0.110	0.985 0.937	1.865 1.734	2.758 2.550	3.679 3.401
	From: E To: QN	t_{ZH} t_{ZL}	0.168 0.054	1.078 1.029	1.959 1.849	2.850 2.633	3.768 3.416

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

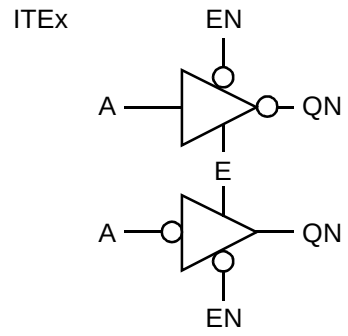
Delay (ns) From	To	Parameter	Cell ITD1	ITD2	ITD4	ITD6
E	QN	t_{HZ} t_{LZ}	0.126 0.045	0.162 0.045	0.241 0.044	0.313 0.043

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ITEx is a family of two-phase enable inverting internal tristate buffers.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

HDL Syntax

Verilog ..... ITEx *inst_name* (QN, A, E, EN);

VHDL..... *inst_name*: ITEx port map (QN, A, E, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITE1	ITE2	ITE4	ITE6
A	1.0	2.0	4.2	6.3
E	0.4	0.9	1.8	2.7
EN	0.6	1.1	2.3	3.5
QN	0.5	0.6	1.3	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITE1	1.0	0.417	0.9
ITE2	1.2	0.833	1.3
ITE4	2.2	1.666	2.7
ITE6	3.2	2.499	4.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ITE1	Number of Equivalent Loads		1	15	30	45	60 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.168 0.162	1.241 1.178	2.405 2.247	3.573 3.313	4.743 4.383
	From: EN To: QN	t_{ZH}	0.193	1.280	2.426	3.563	4.705
	From: E To: QN	t_{ZL}	0.235	1.200	2.223	3.262	4.291
ITE2	Number of Equivalent Loads		1	26	52	77	103 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.110 0.117	1.088 1.048	2.083 1.973	3.048 2.856	4.066 3.773
	From: EN To: QN	t_{ZH}	0.151	1.129	2.104	3.067	4.106
	From: E To: QN	t_{ZL}	0.161	1.079	1.975	2.845	3.760
ITE4	Number of Equivalent Loads		1	48	96	143	191 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.075 0.111	1.008 0.975	1.941 1.809	2.847 2.638	3.768 3.509
	From: EN To: QN	t_{ZH}	0.121	1.050	1.940	2.843	3.820
	From: E To: QN	t_{ZL}	0.108	1.056	1.889	2.693	3.519
ITE6	Number of Equivalent Loads		1	70	139	208	278 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.087 0.102	0.993 0.954	1.875 1.751	2.749 2.551	3.628 3.374
	From: EN To: QN	t_{ZH}	0.112	1.068	1.902	2.765	3.695
	From: E To: QN	t_{ZL}	0.084	0.999	1.818	2.618	3.422

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ITE1	ITE2	ITE4	ITE6
EN	QN	t_{HZ}	0.115	0.115	0.114	0.112
E	QN	t_{LZ}	0.046	0.047	0.045	0.044

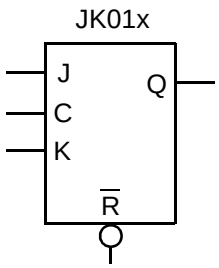
JK01x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

JK01x is a family of static, master-slave JK flip-flops. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)
L	X	X	X	L
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK01x *inst_name* (Q, C, J, K, RN);

VHDL..... *inst_name*: JK01x port map (Q, C, J, K, RN);

Pin Loading

Pin Name	Equivalent Loads	
	JK011	JK012
J	1.1	1.1
K	1.1	1.1
C	1.0	1.0
RN	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK011	6.2	4.661	17.9
JK012	6.5	5.077	20.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	2	5	8	10 (max)
JK011	From: C To: Q	t_{PLH} t_{PHL}	0.609 0.533	0.690 0.596	0.925 0.759	1.152 0.903	1.301 0.993
	From: RN To: Q	t_{PHL}	0.254	0.308	0.433	0.554	0.636
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
JK012	From: C To: Q	t_{PLH} t_{PHL}	0.570 0.512	0.680 0.611	0.824 0.723	1.003 0.850	1.146 0.945
	From: RN To: Q	t_{PHL}	0.234	0.315	0.405	0.505	0.580

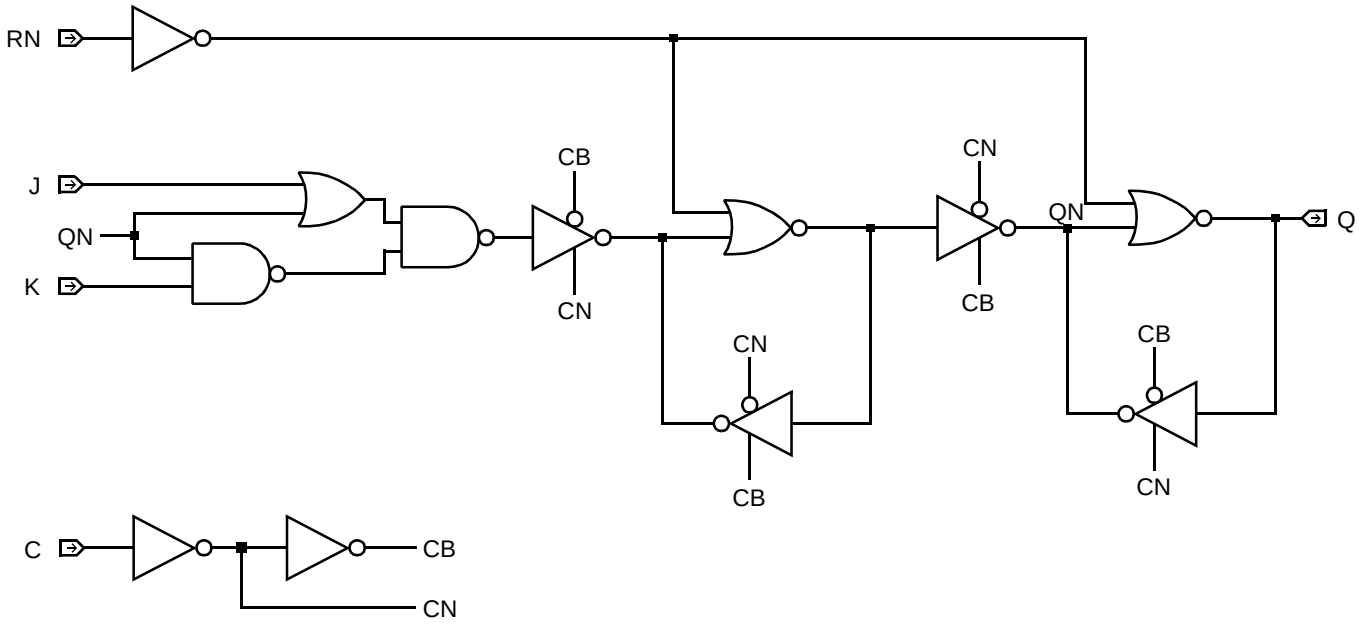
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK011	JK012
Min C Width	High	t_w	0.624	0.570
Min C Width	Low	t_w	0.500	0.503
Min RN Width	Low	t_w	0.468	0.494
Min J Setup		t_{su}	0.500	0.503
Min J Hold		t_h	0.137	0.137
Min K Setup		t_{su}	0.431	0.431
Min K Hold		t_h	0.137	0.137
Min RN Setup		t_{su}	0.248	0.268
Min RN Hold		t_h	0.302	0.301

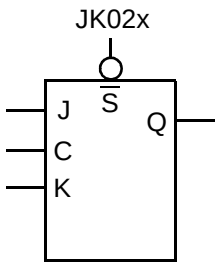
Logic Schematic



Description

JK02x is a family of static, master-slave JK flip-flops. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)
L	X	X	X	H
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK02x *inst_name* (Q, C, J, K, SN);

VHDL..... *inst_name*: JK02x port map (Q, C, J, K, SN);

Pin Loading

Pin Name	Equivalent Loads	
	JK021	JK022
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
SN	2.2	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK021	5.8	4.804	14.9
JK022	6.2	5.493	16.2

a. See page 2-13 for power equation.

Core Logic

AMI350LXSC 0.35 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	2	5	8	10 (max)
JK021	From: C To: Q	t_{PLH} t_{PHL}	0.549 0.536	0.609 0.604	0.770 0.799	0.919 0.989	1.014 1.115
	From: SN To: Q	t_{PLH}	0.164	0.215	0.339	0.484	0.584
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
JK022	From: C To: Q	t_{PLH} t_{PHL}	0.539 0.526	0.629 0.637	0.729 0.770	0.842 0.924	0.926 1.042
	From: SN To: Q	t_{PLH}	0.090	0.168	0.260	0.370	0.468

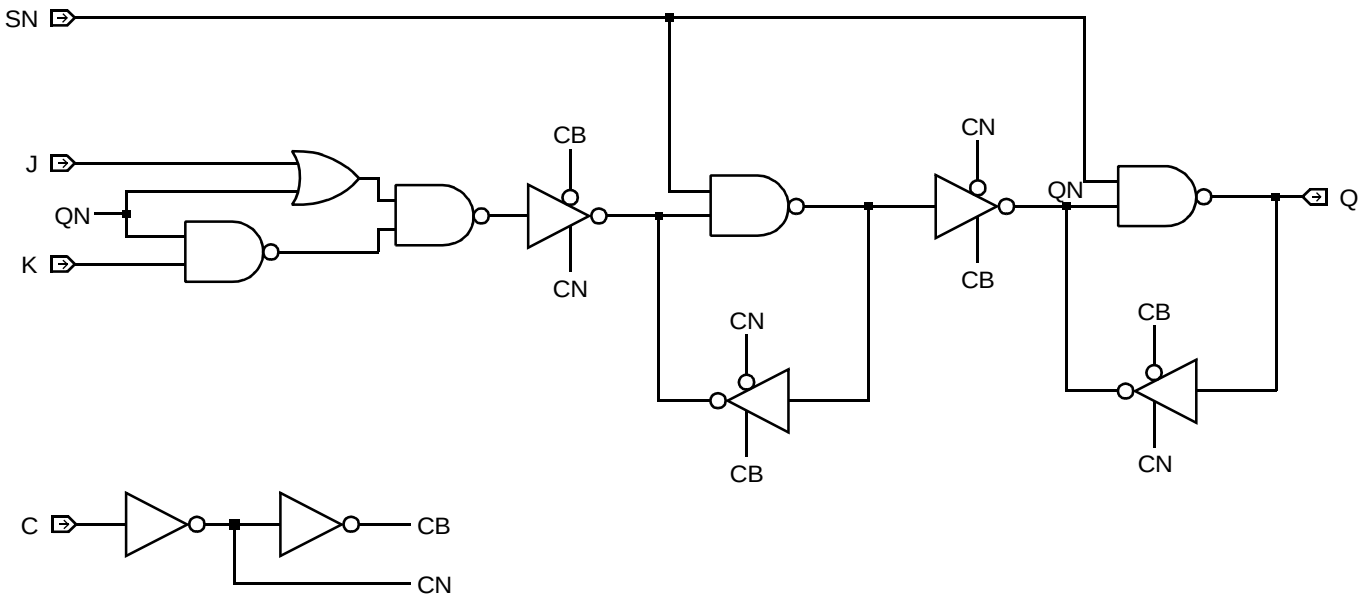
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK021	JK022
Min C Width	High	t_w	0.551	0.542
Min C Width	Low	t_w	0.482	0.476
Min SN Width	Low	t_w	0.861	0.825
Min J Setup		t_{su}	0.482	0.476
Min J Hold		t_h	0.127	0.131
Min K Setup		t_{su}	0.406	0.399
Min K Hold		t_h	0.127	0.131
Min SN Setup		t_{su}	0.125	0.124
Min SN Hold		t_h	0.418	0.419

Logic Schematic



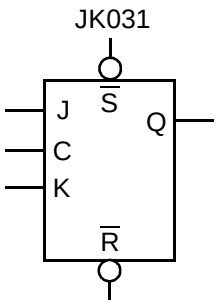
JK031

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

JK031 is a static, master-slave JK flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)
L	L	X	X	X	IL
L	H	X	X	X	L
H	L	X	X	X	H
H	H	L	L	↑	NC
H	H	L	H	↑	L
H	H	H	L	↑	H
H	H	H	H	↑	$\overline{Q(n)}$

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	1.0
SN	2.2
RN	1.1

Equivalent Gates 7.0

HDL Syntax

Verilog ..... JK031 *inst_name* (Q, C, J, K, RN, SN);

VHDL..... *inst_name*: JK031 port map (Q, C, J, K, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.373	nA
EQL_{pd}	19.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.646 0.559	0.751 0.633	1.036 0.842	1.299 1.042	1.468 1.172
RN	Q	t_{PHL}	0.299	0.369	0.550	0.725	0.839
SN	Q	t_{PLH}	0.133	0.185	0.313	0.439	0.522

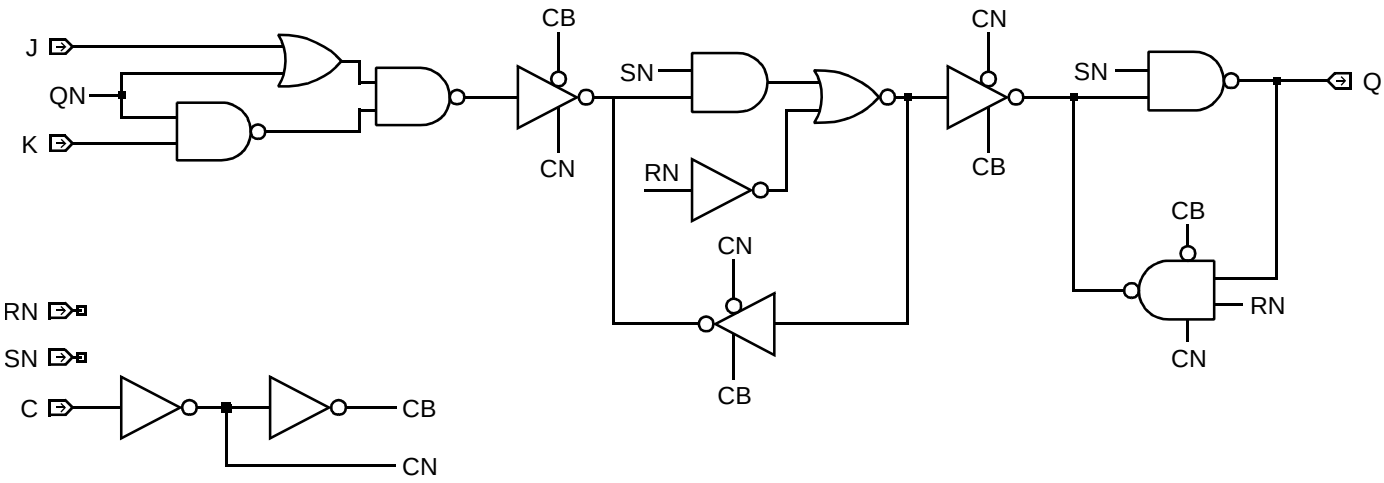
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.646
Min C Width	Low	t_w	0.507
Min RN Width	Low	t_w	0.494
Min SN Width	Low	t_w	0.812
Min J Setup		t_{su}	0.507
Min J Hold		t_h	0.135
Min K Setup		t_{su}	0.457
Min K Hold		t_h	0.135
Min RN Setup		t_{su}	0.285
Min RN Hold		t_h	0.296
Min SN Setup		t_{su}	0.150
Min SN Hold		t_h	0.421

Logic Schematic



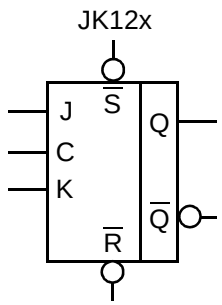
JK12x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

JK12x is a family of static, master-slave JK flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... JK12x *inst_name* (Q, QN, C, J, K, RN, SN);

VHDL..... *inst_name*: JK12x port map (Q, QN, C, J, K, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	JK121	JK122	JK124	JK126
J	1.0	1.0	1.0	1.0
K	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.2	2.2	2.2	2.2
RN	1.1	1.0	1.1	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK121	7.8	6.174	22.1
JK122	8.5	7.775	28.3
JK124	9.0	9.375	32.0
JK126	9.8	11.184	38.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
JK121	From: C To: Q	t_{PLH} t_{PHL}	0.560 0.544	0.711 0.720	0.892 0.920	1.105 1.147	1.268 1.318
	From: C To: QN	t_{PLH} t_{PHL}	0.652 0.785	0.790 0.937	0.963 1.118	1.170 1.330	1.333 1.492
	From: RN To: Q	t_{PHL}	1.086	1.328	1.553	1.777	1.933
	From: RN To: QN	t_{PLH}	0.346	0.485	0.660	0.871	1.036
	From: SN To: Q	t_{PLH}	0.708	0.868	1.059	1.282	1.453
	From: SN To: QN	t_{PHL}	0.228	0.366	0.537	0.741	0.901
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
JK122	From: C To: Q	t_{PLH} t_{PHL}	0.858 0.733	1.012 0.893	1.164 1.056	1.288 1.191	1.424 1.340
	From: C To: QN	t_{PLH} t_{PHL}	0.465 0.549	0.597 0.699	0.759 0.858	0.907 0.992	1.078 1.141
	From: RN To: Q	t_{PHL}	0.533	0.714	0.885	1.023	1.170
	From: RN To: QN	t_{PLH}	0.875	1.009	1.160	1.292	1.442
	From: SN To: Q	t_{PLH}	0.357	0.510	0.671	0.806	0.967
	From: SN To: QN	t_{PHL}	0.640	0.791	0.944	1.071	1.211

AMI350LXSC 0.35 micron CMOS Standard Cell

	Number of Equivalent Loads		1	15	30	44	59 (max)
JK124	From: C To: Q	t_{PLH} t_{PHL}	0.838 0.694	1.017 0.901	1.160 1.067	1.285 1.194	1.415 1.360
	From: C To: QN	t_{PLH} t_{PHL}	0.492 0.571	0.642 0.753	0.789 0.905	0.922 1.033	1.060 1.163
	From: RN To: Q	t_{PHL}	0.580	0.756	0.910	1.047	1.196
	From: RN To: QN	t_{PLH}	0.915	1.058	1.186	1.305	1.434
	From: SN To: Q	t_{PLH}	0.381	0.521	0.676	0.823	0.982
	From: SN To: QN	t_{PHL}	0.646	0.840	0.991	1.115	1.237
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
JK126	From: C To: Q	t_{PLH} t_{PHL}	0.959 0.855	1.123 1.051	1.268 1.176	1.397 1.318	1.526 1.472
	From: C To: QN	t_{PLH} t_{PHL}	0.554 0.644	0.709 0.854	0.854 1.009	0.981 1.136	1.107 1.258
	From: RN To: Q	t_{PHL}	0.635	0.843	1.010	1.143	1.266
	From: RN To: QN	t_{PLH}	0.734	0.901	1.037	1.159	1.283
	From: SN To: Q	t_{PLH}	0.414	0.587	0.734	0.859	0.986
	From: SN To: QN	t_{PHL}	0.583	0.789	0.938	1.067	1.200

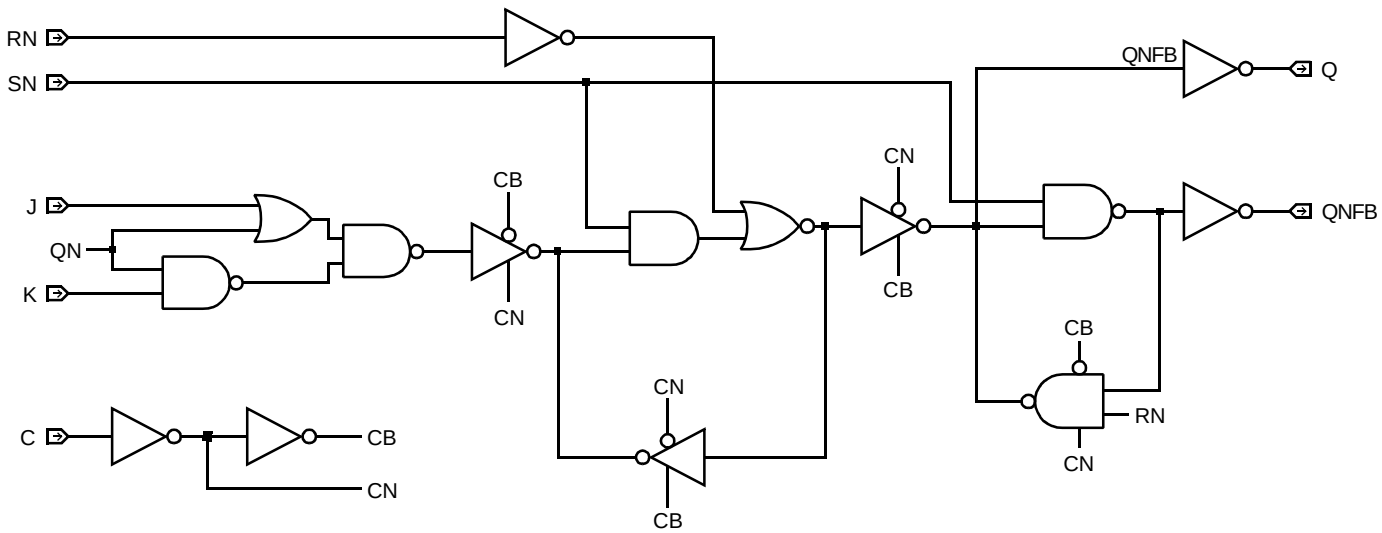
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			JK121	JK122	JK124	JK126
Min C Width	High	t_w	0.621	0.540	0.527	0.583
Min C Width	Low	t_w	0.510	0.508	0.508	0.508
Min RN Width	Low	t_w	0.496	0.498	0.496	0.496
Min SN Width	Low	t_w	0.563	0.419	0.407	0.348
Min J Setup		t_{su}	0.510	0.508	0.508	0.508
Min J Hold		t_h	0.129	0.130	0.129	0.133
Min K Setup		t_{su}	0.459	0.457	0.458	0.457
Min K Hold		t_h	0.129	0.130	0.129	0.133
Min RN Setup		t_{su}	0.287	0.288	0.287	0.286
Min RN Hold		t_h	0.289	0.290	0.290	0.293
Min SN Setup		t_{su}	0.151	0.150	0.150	0.150
Min SN Hold		t_h	0.416	0.417	0.417	0.426

Logic Schematic

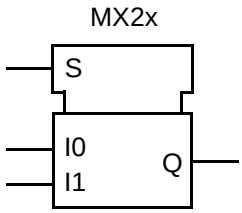


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

MX2x is a family of two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

HDL Syntax

Verilog ..... MX2x *inst_name* (Q, I0, I1, S);

VHDL..... *inst_name*: MX2x port map (Q, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MX21	MX22	MX24	MX26
I0	1.1	1.1	2.0	2.0
I1	1.0	1.0	2.0	2.0
S	1.6	1.6	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX21	2.0	1.410	4.2
MX22	2.0	1.810	5.4
MX24	3.0	4.067	10.7
MX26	3.2	4.867	13.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

MX21	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.252 0.272	0.387 0.424	0.562 0.594	0.777 0.796	0.946 0.961
	From: S To: Q	t_{PLH} t_{PHL}	0.359 0.384	0.496 0.532	0.669 0.710	0.879 0.919	1.043 1.079
MX22	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.253 0.275	0.413 0.470	0.573 0.645	0.709 0.784	0.867 0.932
	From: S To: Q	t_{PLH} t_{PHL}	0.356 0.390	0.508 0.573	0.673 0.748	0.814 0.890	0.972 1.044
MX24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.221 0.240	0.380 0.431	0.526 0.589	0.660 0.725	0.811 0.864
	From: S To: Q	t_{PLH} t_{PHL}	0.250 0.320	0.402 0.523	0.545 0.680	0.680 0.815	0.830 0.956
MX26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.268 0.293	0.418 0.486	0.556 0.643	0.685 0.781	0.819 0.915
	From: S To: Q	t_{PLH} t_{PHL}	0.286 0.361	0.444 0.560	0.573 0.716	0.708 0.856	0.857 0.993

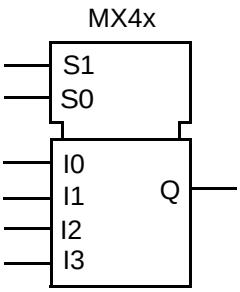
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

MX4x is a family of four-to-one digital multiplexers.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

HDL Syntax

Verilog ..... MX4x *inst_name* (Q, I0, I1, I2, I3, S0, S1);

VHDL..... *inst_name*: MX4x port map (Q, I0, I1, I2, I3, S0, S1);

Pin Loading

Pin Name	Equivalent Loads			
	MX41	MX42	MX44	MX46
I0	1.1	1.0	1.0	1.0
I1	1.0	1.1	1.0	1.0
I2	1.0	1.1	1.1	1.1
I3	1.1	1.1	1.0	1.0
S0	3.4	3.5	3.5	3.5
S1	3.4	2.2	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX41	4.2	2.868	11.7
MX42	5.2	5.332	16.6
MX44	6.0	6.821	21.4
MX46	6.2	7.621	24.1

a. See page 2-13 for power equation.

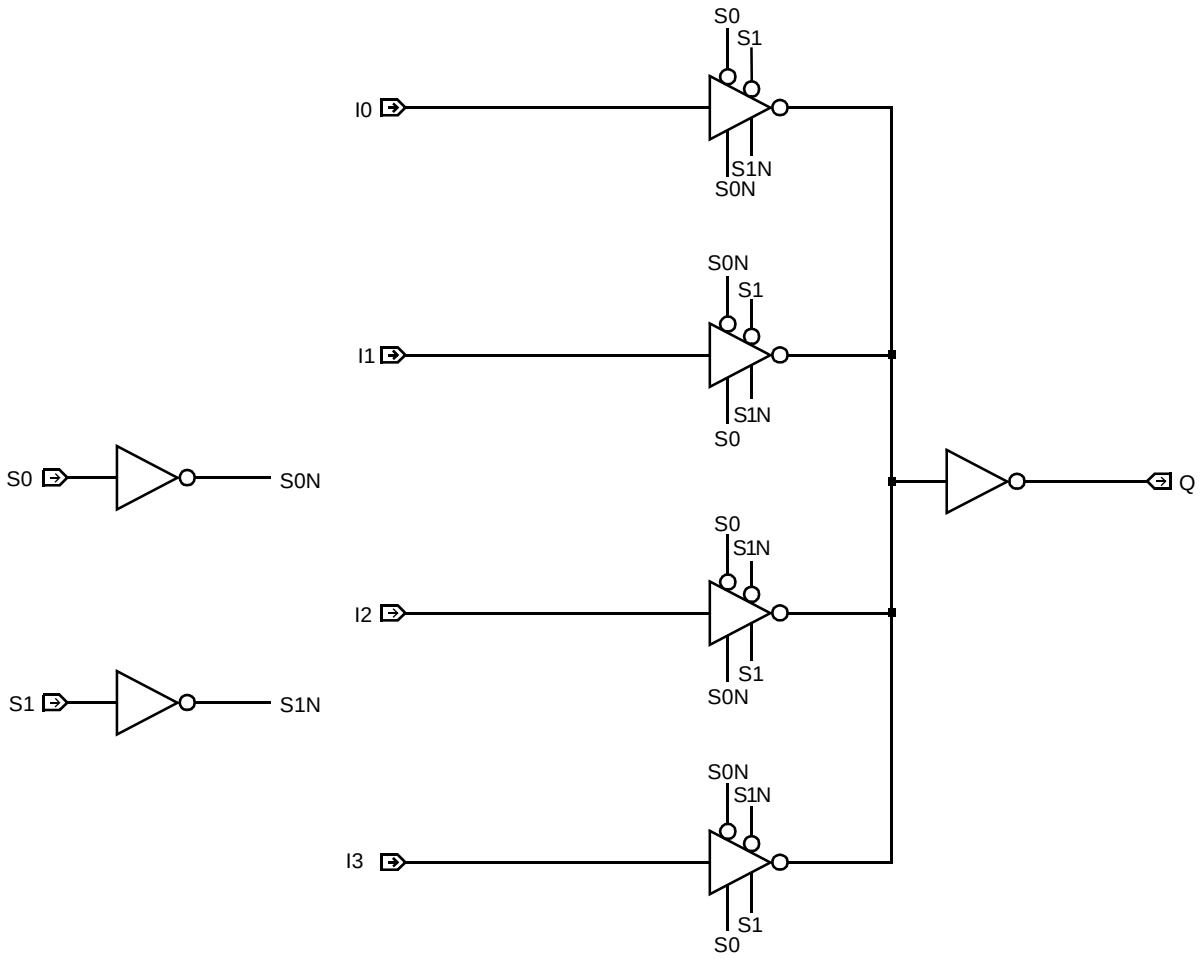
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

MX41	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.480 0.542	0.629 0.748	0.812 0.959	1.030 1.185	1.200 1.348
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.560 0.670	0.725 0.864	0.907 1.073	1.109 1.301	1.259 1.469
MX42	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.440 0.462	0.590 0.619	0.754 0.782	0.894 0.918	1.054 1.070
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.513 0.590	0.661 0.768	0.821 0.936	0.957 1.071	1.111 1.216
MX44	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.440 0.445	0.594 0.612	0.741 0.769	0.880 0.903	1.031 1.037
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.506 0.611	0.657 0.766	0.815 0.917	0.952 1.056	1.086 1.211
MX46	Number of Equivalent Loads		1	22	44	65	87 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.445 0.470	0.591 0.633	0.742 0.787	0.881 0.924	1.021 1.062
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.563 0.631	0.705 0.816	0.845 0.939	0.974 1.078	1.105 1.225

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

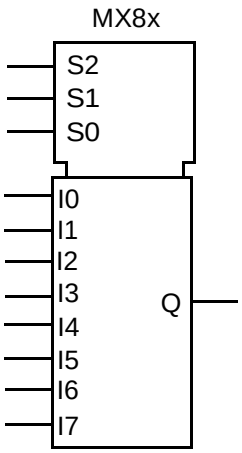
Logic Schematic



Description

MX8x is a family of eight-to-one digital multiplexers.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

HDL Syntax

Verilog ..... MX8x *inst_name* (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

VHDL..... *inst_name*: MX8x port map (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads			
	MX81	MX82	MX84	MX86
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.1
I2	1.1	1.1	1.1	1.1
I3	1.1	1.1	1.1	1.1
I4	1.0	1.0	1.0	1.0
I5	1.1	1.0	1.1	1.1
I6	1.0	1.0	1.0	1.0
I7	1.1	1.1	1.1	1.1
S0	5.9	6.0	6.0	6.0
S1	3.4	3.6	3.6	3.6
S2	2.2	2.3	3.3	3.3

AMI350LXSC 0.35 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX81	8.8	7.431	28.4
MX82	10.0	10.328	37.3
MX84	10.0	9.464	36.5
MX86	10.5	10.264	39.3

a. See page 2-13 for power equation.

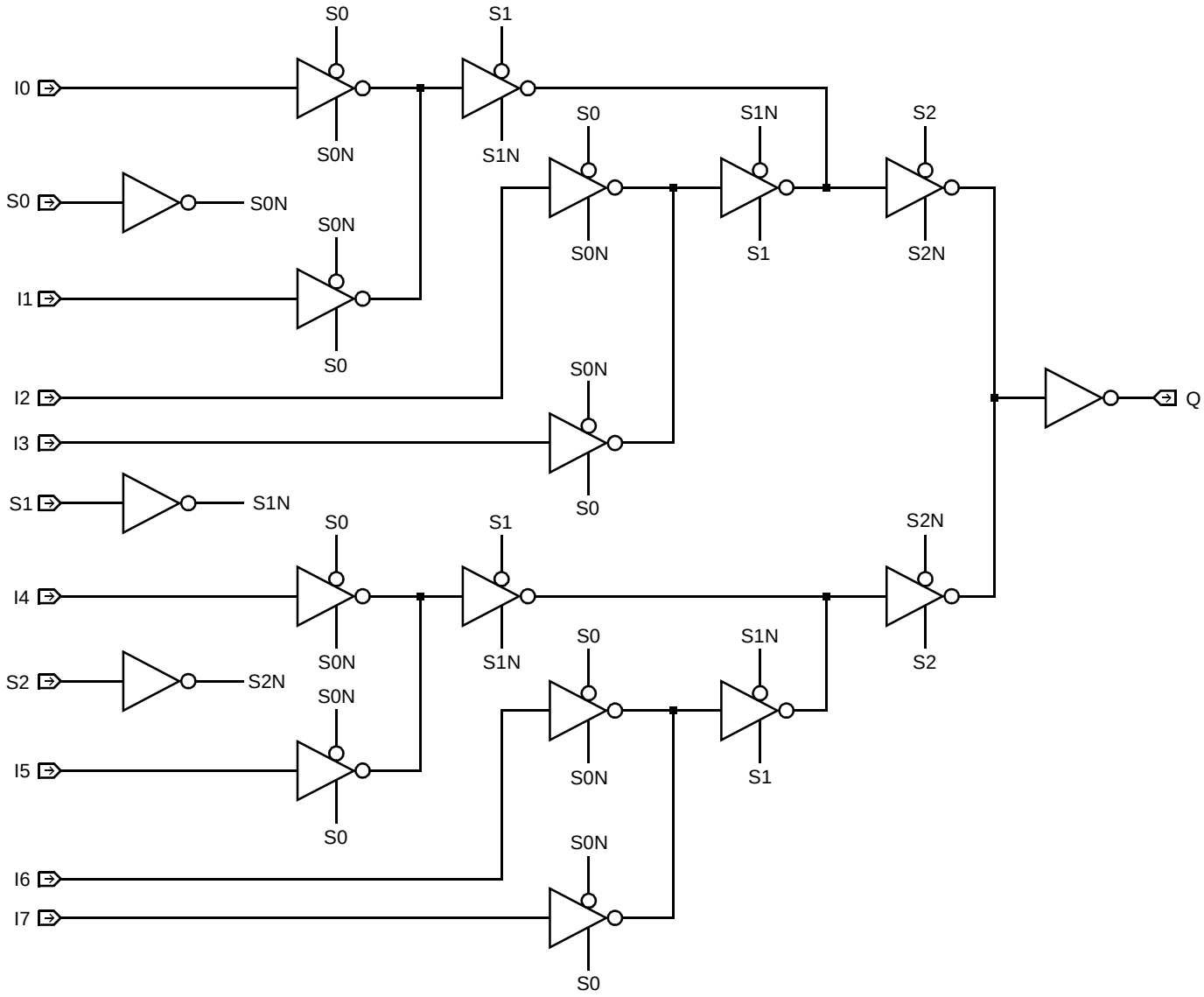
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
MX81	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.616 0.638	0.762 0.806	0.937 0.984	1.140 1.178	1.296 1.321
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.774 0.805	0.914 0.953	1.089 1.134	1.300 1.349	1.465 1.515
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
MX82	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.608 0.614	0.695 0.725	0.780 0.834	0.850 0.924	0.926 1.023
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.763 0.790	0.859 0.911	0.944 1.019	1.009 1.104	1.078 1.194
	Number of Equivalent Loads		**1**	**15**	**30**	**44**	**59 (max)**
MX84	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.630 0.632	0.806 0.849	0.964 1.002	1.089 1.122	1.207 1.238
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.816 0.806	0.979 0.970	1.119 1.135	1.237 1.285	1.355 1.442
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
MX86	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.661 0.677	0.817 0.896	0.970 1.058	1.106 1.189	1.242 1.309
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.850 0.771	1.003 1.043	1.147 1.228	1.279 1.362	1.413 1.475

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

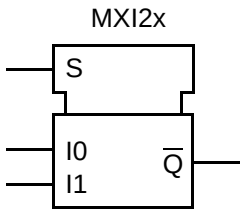


AMI350LXSC 0.35 micron CMOS Standard Cell

Description

MXI2x is a family of inverting two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

HDL Syntax

Verilog ..... MXI2x *inst_name* (QN, I0, I1, S);

VHDL..... *inst_name*: MXI2x port map (QN, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MXI21	MXI22	MXI24	MXI26
I0	1.1	1.1	1.1	1.1
I1	1.0	1.0	1.1	1.0
S	1.6	1.6	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MXI21	2.5	1.810	5.7
MXI22	2.5	2.210	7.0
MXI24	3.0	4.066	10.7
MXI26	4.0	5.555	15.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

MXI21	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.319 0.335	0.451 0.462	0.621 0.627	0.831 0.829	0.998 0.988
	From: S To: QN	t_{PLH} t_{PHL}	0.437 0.436	0.567 0.557	0.737 0.721	0.947 0.929	1.114 1.097
MXI22	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.312 0.328	0.457 0.493	0.618 0.657	0.757 0.792	0.914 0.940
	From: S To: QN	t_{PLH} t_{PHL}	0.432 0.438	0.565 0.590	0.729 0.751	0.877 0.886	1.051 1.036
MXI24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.281 0.337	0.436 0.520	0.587 0.679	0.723 0.816	0.866 0.955
	From: S To: QN	t_{PLH} t_{PHL}	0.388 0.393	0.551 0.569	0.691 0.724	0.825 0.859	0.972 0.995
MXI26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.285 0.313	0.439 0.484	0.576 0.630	0.707 0.759	0.848 0.887
	From: S To: QN	t_{PLH} t_{PHL}	0.375 0.353	0.532 0.505	0.670 0.654	0.804 0.797	0.951 0.946

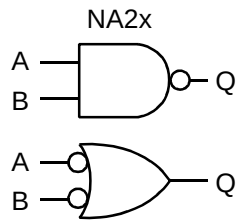
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA2x is a family of 2-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... NA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NA21	NA22	NA23	NA24	NA26
A	1.0	2.0	3.9	2.0	1.9
B	1.0	2.0	4.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA21	1.0	1.110	0.7
NA22	1.2	1.377	1.2
NA23	1.7	2.434	2.5
NA24	2.2	3.778	8.8
NA26	2.7	4.578	11.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.106 0.147	0.160 0.216	0.313 0.406	0.464 0.582	0.564 0.696
NA22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.072 0.101	0.153 0.200	0.244 0.321	0.354 0.466	0.444 0.581
NA23	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.050 0.073	0.151 0.175	0.260 0.273	0.350 0.354	0.449 0.444
NA24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.180 0.333	0.322 0.492	0.470 0.641	0.604 0.772	0.747 0.909
NA26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.203 0.230	0.348 0.408	0.490 0.555	0.621 0.685	0.756 0.822

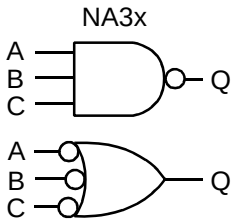
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA3x is a family of 3-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

HDL Syntax

Verilog ..... NA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NA31	NA32	NA33	NA34	NA36
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.1	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA31	1.2	0.913	1.1
NA32	1.7	1.826	2.0
NA33	2.5	3.026	6.2
NA34	2.7	4.226	9.6
NA36	3.0	5.027	12.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.138 0.179	0.202 0.255	0.320 0.396	0.377 0.466	0.488 0.608
NA32	**Number of Equivalent Loads**		**1**	**3**	**6**	**9**	**12 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.080 0.121	0.148 0.203	0.237 0.318	0.312 0.428	0.379 0.534
NA33	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.213 0.257	0.355 0.405	0.516 0.571	0.657 0.713	0.818 0.871
NA34	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.214 0.245	0.350 0.402	0.493 0.546	0.629 0.676	0.777 0.819
NA36	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.221 0.256	0.364 0.422	0.495 0.579	0.632 0.711	0.779 0.838

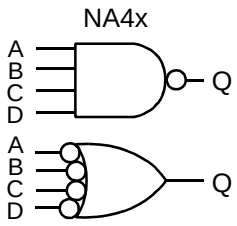
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA4x is a family of 4-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

HDL Syntax

Verilog ..... NA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NA41	NA42	NA43	NA44	NA46
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.1	2.1	2.1	2.1
D	1.0	2.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA41	1.5	1.089	1.4
NA42	2.0	2.178	2.5
NA43	2.7	3.379	6.8
NA44	3.0	4.579	10.1
NA46	3.2	5.379	12.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA41	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.165 0.203	0.229 0.291	0.289 0.374	0.349 0.454	0.482 0.618
NA42	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.106 0.138	0.140 0.186	0.229 0.316	0.316 0.437	0.378 0.516
NA43	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.229 0.274	0.365 0.424	0.529 0.589	0.676 0.732	0.846 0.894
NA44	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.219 0.264	0.360 0.421	0.508 0.571	0.643 0.706	0.785 0.846
NA46	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.243 0.301	0.380 0.450	0.511 0.597	0.647 0.733	0.800 0.875

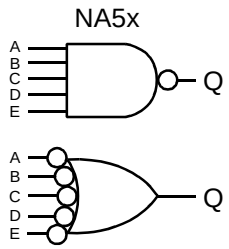
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA5x is a family of 5-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

HDL Syntax

Verilog ..... NA5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NA5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NA51	NA52	NA53	NA54	NA56
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.1	2.0	2.0
D	1.0	1.0	2.1	2.1	2.1
E	1.0	1.0	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA51	2.75	2.418	6.5
NA52	2.7	2.818	7.7
NA53	3.8	4.819	9.8
NA54	3.8	5.635	13.4
NA56	4.0	6.435	16.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA51	**Number of Equivalent Loads**		**1**	**1**	**2**	**4**	**5 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.233 0.312	0.233 0.312	0.277 0.370	0.365 0.472	0.408 0.516
NA52	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.268 0.361	0.331 0.450	0.409 0.545	0.504 0.650	0.579 0.726
NA53	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.227 0.363	0.324 0.513	0.429 0.634	0.519 0.725	0.620 0.819
NA54	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.212 0.294	0.359 0.477	0.507 0.638	0.640 0.775	0.781 0.914
NA56	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.223 0.326	0.364 0.529	0.504 0.683	0.637 0.820	0.775 0.961

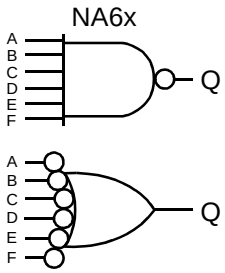
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA6x is a family of 6-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: NA6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads				
	NA61	NA62	NA63	NA64	NA66
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.0	2.0	2.0
D	1.0	2.0	2.0	2.0	2.0
E	1.0	2.0	2.1	2.1	2.1
F	1.0	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA61	3.0	2.642	6.8
NA62	3.8	5.283	12.0
NA63	4.0	5.684	13.1
NA64	4.0	6.084	14.2
NA66	4.2	6.884	16.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA61	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.284 0.369	0.418 0.511	0.590 0.685	0.801 0.890	0.968 1.049
NA62	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.213 0.288	0.360 0.445	0.522 0.614	0.660 0.757	0.817 0.918
NA63	Number of Equivalent Loads		1	11	22	34	45 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.213 0.296	0.351 0.468	0.496 0.623	0.652 0.779	0.793 0.913
NA64	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.222 0.312	0.372 0.512	0.512 0.637	0.648 0.780	0.800 0.929
NA66	Number of Equivalent Loads		1	22	44	65	87 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.241 0.346	0.376 0.552	0.510 0.710	0.643 0.845	0.788 0.975

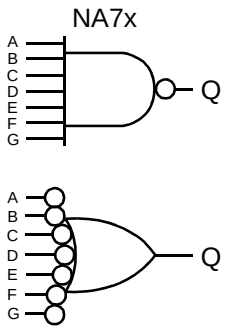
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA7x is a family of 7-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA7x *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: NA7x port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads				
	NA71	NA72	NA73	NA74	NA76
A	2.0	2.0	2.0	2.0	2.0
B	2.0	2.0	2.0	2.0	2.0
C	2.0	2.0	2.0	2.0	2.0
D	2.0	2.0	2.0	2.0	2.0
E	2.0	2.0	2.0	2.0	2.0
F	2.1	2.0	2.1	2.1	2.0
G	2.1	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA71	4.8	5.428	10.4
NA72	4.8	6.276	15.5
NA73	5.0	6.676	16.3
NA74	5.2	7.076	17.6
NA76	5.2	7.876	20.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA71	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.279 0.427	0.413 0.582	0.585 0.766	0.797 0.982	0.964 1.148
NA72	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.258 0.380	0.406 0.557	0.569 0.731	0.710 0.874	0.869 1.031
NA73	Number of Equivalent Loads		1	11	22	34	45 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.256 0.396	0.403 0.590	0.550 0.754	0.704 0.913	0.842 1.048
NA74	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.269 0.406	0.414 0.624	0.561 0.791	0.696 0.928	0.838 1.062
NA76	Number of Equivalent Loads		1	22	44	65	87 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.280 0.477	0.416 0.697	0.561 0.858	0.700 1.003	0.846 1.155

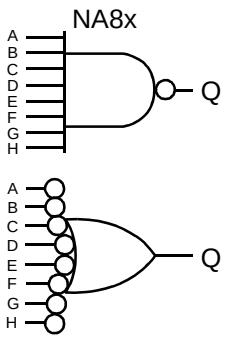
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NA8x is a family of 8-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA8x *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: NA8x port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads				
	NA81	NA82	NA83	NA84	NA86
A	1.1	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.0	2.0	2.0
D	1.0	2.0	2.0	2.0	2.0
E	1.1	2.1	2.1	2.1	2.1
F	1.0	2.1	2.1	2.1	2.1
G	1.0	2.0	2.0	2.0	2.0
H	1.0	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA81	3.8	2.995	7.2
NA82	5.2	6.725	16.4
NA83	5.5	7.125	17.2
NA84	5.5	7.525	18.4
NA86	5.8	8.325	21.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NA81	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.303 0.386	0.438 0.530	0.611 0.704	0.822 0.908	0.989 1.065
NA82	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.262 0.383	0.403 0.575	0.567 0.751	0.711 0.890	0.875 1.039
NA83	Number of Equivalent Loads		1	11	22	34	45 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.259 0.396	0.398 0.581	0.543 0.744	0.699 0.905	0.839 1.043
NA84	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.314 0.426	0.468 0.629	0.605 0.786	0.745 0.927	0.900 1.079
NA86	Number of Equivalent Loads		1	22	44	65	87 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.292 0.470	0.430 0.693	0.572 0.863	0.706 1.001	0.846 1.131

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

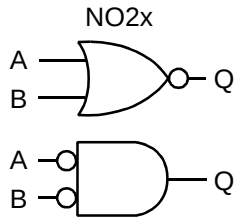
NO2x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NO2x is a family of 2-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

HDL Syntax

Verilog ..... NO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NO21	NO22	NO23	NO24	NO26
A	1.0	1.9	3.9	1.9	1.9
B	1.0	2.0	3.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO21	1.0	0.609	0.8
NO22	1.2	1.217	1.2
NO23	1.7	2.434	2.7
NO24	2.2	3.234	9.4
NO26	2.7	4.034	11.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NO21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.154 0.130	0.234 0.180	0.452 0.319	0.676 0.452	0.839 0.532
NO22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.099 0.105	0.221 0.180	0.370 0.263	0.556 0.365	0.711 0.448
NO23	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.062 0.073	0.190 0.157	0.330 0.246	0.449 0.320	0.583 0.402
NO24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.228 0.205	0.371 0.358	0.517 0.513	0.650 0.646	0.792 0.784
NO26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.243 0.306	0.396 0.445	0.525 0.559	0.653 0.694	0.797 0.835

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

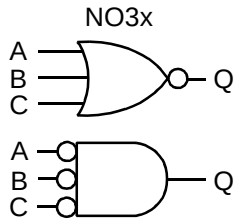
NO3x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NO3x is a family of 3-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

HDL Syntax

Verilog ..... NO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NO31	NO32	NO33	NO34	NO36
A	1.0	2.0	2.0	2.0	2.0
B	1.0	1.9	1.9	1.9	1.9
C	1.0	2.0	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO31	1.2	0.817	1.3
NO32	1.2	1.633	2.2
NO33	2.0	2.594	6.5
NO34	2.5	3.555	10.4
NO36	3.0	4.195	12.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.198 0.159	0.306 0.213	0.512 0.313	0.614 0.361	0.820 0.455
NO32	**Number of Equivalent Loads**		**1**	**3**	**6**	**9**	**12 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.123 0.107	0.222 0.175	0.367 0.258	0.511 0.328	0.655 0.391
NO33	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.277 0.249	0.414 0.407	0.571 0.574	0.712 0.717	0.879 0.877
NO34	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.291 0.232	0.432 0.381	0.579 0.529	0.712 0.662	0.850 0.803
NO36	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.291 0.257	0.425 0.416	0.587 0.561	0.726 0.695	0.845 0.834

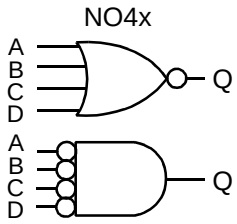
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NO4x is a family of 4-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... NO4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NO4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NO41	NO42	NO43	NO44	NO46
A	1.0	1.0	2.0	2.1	2.0
B	1.1	1.0	2.1	2.0	2.1
C	1.0	1.0	2.1	2.0	2.1
D	1.0	1.0	2.1	1.9	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO41	1.5	0.961	1.6
NO42	2.5	1.922	6.0
NO43	3.0	2.883	6.9
NO44	4.2	3.844	12.1
NO46	3.5	4.483	17.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NO41	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.213 0.173	0.337 0.235	0.460 0.291	0.585 0.346	0.844 0.461
NO42	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.302 0.299	0.434 0.438	0.607 0.608	0.819 0.810	0.987 0.966
NO43	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.285 0.383	0.435 0.538	0.596 0.702	0.733 0.840	0.887 0.994
NO44	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.328 0.255	0.430 0.408	0.568 0.553	0.701 0.690	0.846 0.841
NO46	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.328 0.255	0.475 0.402	0.603 0.543	0.734 0.681	0.876 0.831

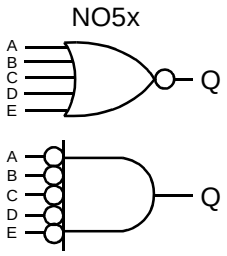
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

NO5x is a family of 5-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

HDL Syntax

Verilog ..... NO5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NO5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NO51	NO52	NO53	NO54	NO56
A	1.0	1.0	2.0	1.9	1.9
B	1.0	1.0	1.9	1.9	1.9
C	1.0	1.0	2.0	1.9	2.0
D	1.0	1.0	2.0	1.9	1.9
E	1.0	1.0	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
NO51	2.7	2.122	6.4
NO52	2.7	2.442	7.6
NO53	3.0	4.187	10.0
NO54	3.5	4.883	13.5
NO56	3.8	5.524	16.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

NO51	**Number of Equivalent Loads**		**1**	**1**	**2**	**4**	**5 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.300 0.307	0.300 0.307	0.346 0.355	0.432 0.439	0.474 0.477
NO52	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.303 0.307	0.369 0.382	0.449 0.468	0.545 0.565	0.619 0.638
NO53	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.267 0.293	0.367 0.414	0.475 0.529	0.567 0.622	0.670 0.724
NO54	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.239 0.272	0.391 0.419	0.535 0.567	0.672 0.704	0.821 0.849
NO56	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.283 0.263	0.416 0.443	0.552 0.589	0.686 0.721	0.831 0.858

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

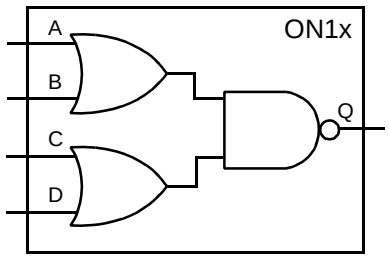
ON1x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON1x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON11	ON12	ON14	ON16
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	1.9
C	1.1	1.0	1.0	1.9
D	1.0	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON11	1.5	0.721	2.0
ON12	2.5	2.146	6.1
ON14	2.5	2.466	7.4
ON16	3.0	4.931	13.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON11	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.196 0.169	0.291 0.239	0.560 0.435	0.830 0.610	1.015 0.715
ON12	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.281 0.312	0.413 0.452	0.585 0.628	0.798 0.838	0.967 1.002
ON14	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.286 0.330	0.426 0.506	0.588 0.679	0.732 0.821	0.897 0.977
ON16	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.244 0.272	0.396 0.461	0.535 0.616	0.665 0.752	0.813 0.895

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

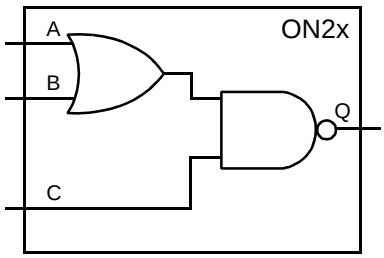
ON2X

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON2x is a family of OR-NAND circuits consisting of one 2-input OR and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

HDL Syntax

Verilog ..... ON2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: ON2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	ON21	ON22	ON24	ON26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON21	1.2	0.745	1.5
ON22	2.2	1.858	5.7
ON24	2.2	2.178	7.0
ON26	2.7	4.035	12.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.197 0.174	0.292 0.248	0.567 0.445	0.842 0.619	1.029 0.727
ON22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.299 0.313	0.422 0.458	0.587 0.632	0.798 0.836	0.970 0.994
ON24	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.289 0.322	0.424 0.496	0.584 0.669	0.727 0.811	0.895 0.966
ON26	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.255 0.269	0.393 0.452	0.541 0.611	0.675 0.747	0.814 0.898

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

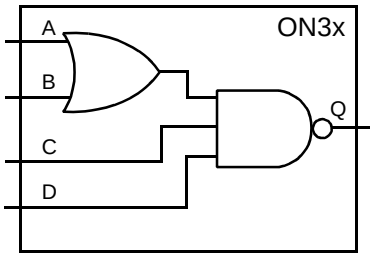
ON3x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON3x is a family of OR-NAND circuits consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON31	ON32	ON34	ON36
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	1.9
C	1.1	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON31	1.5	0.985	1.8
ON32	2.5	1.922	6.0
ON34	2.5	2.322	7.1
ON36	3.2	4.643	13.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.232 0.214	0.339 0.290	0.547 0.424	0.653 0.490	0.869 0.626
ON32	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.286 0.315	0.413 0.460	0.586 0.634	0.804 0.839	0.979 0.999
ON34	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.282 0.326	0.431 0.507	0.592 0.679	0.730 0.817	0.885 0.966
ON36	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.242 0.293	0.385 0.459	0.534 0.606	0.670 0.740	0.813 0.892

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

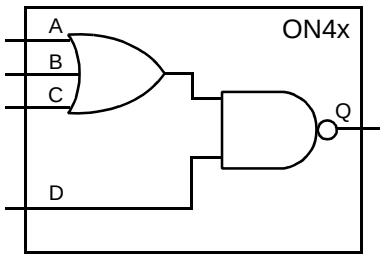
ON4x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON4x is a family of OR-NAND circuits consisting of one 3-input OR gate into and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON41	ON42	ON44	ON46
A	1.0	1.1	1.1	2.0
B	1.0	1.1	1.1	1.9
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON41	1.5	0.785	2.1
ON42	2.5	2.066	6.2
ON44	2.5	2.386	7.4
ON46	3.0	4.451	13.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.255 0.192	0.374 0.266	0.608 0.405	0.726 0.473	0.969 0.602
ON42	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.349 0.368	0.479 0.503	0.650 0.669	0.863 0.873	1.032 1.036
ON44	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.354 0.364	0.494 0.539	0.653 0.712	0.792 0.855	0.950 1.012
ON46	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.290 0.286	0.444 0.474	0.590 0.636	0.719 0.770	0.851 0.904

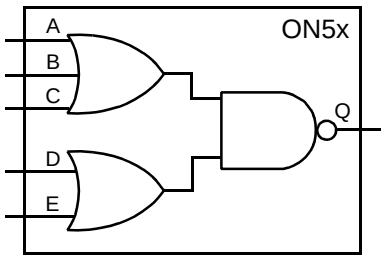
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON5x

Description

ON5x is a family of OR-NAND circuits consisting of one 3-input OR gate and one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON52	ON54	ON56
A	1.1	1.1	2.0
B	1.1	1.1	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON52	2.7	2.354	6.4
ON54	2.7	2.674	7.7
ON56	3.2	5.347	14.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON52	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.348 0.353	0.483 0.490	0.657 0.664	0.869 0.876	1.037 1.042
ON54	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.347 0.360	0.484 0.540	0.644 0.713	0.786 0.852	0.950 1.004
ON56	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.288 0.290	0.429 0.471	0.576 0.626	0.712 0.759	0.870 0.895

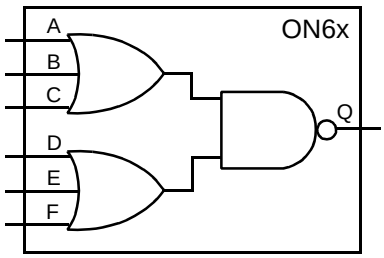
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON6x is a family of OR-NAND circuits consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON62	ON64	ON66
A	1.1	1.1	2.0
B	1.1	1.1	2.0
C	1.0	1.0	2.0
D	1.0	1.0	1.9
E	1.1	1.1	1.9
F	1.0	1.1	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON62	3.0	2.563	7.0
ON64	3.0	2.883	8.3
ON66	3.8	5.764	14.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON62	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.363 0.354	0.490 0.496	0.661 0.671	0.875 0.879	1.046 1.041
ON64	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.371 0.294	0.507 0.481	0.671 0.657	0.817 0.797	0.987 0.949
ON66	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.294 0.288	0.434 0.471	0.576 0.631	0.712 0.766	0.862 0.900

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

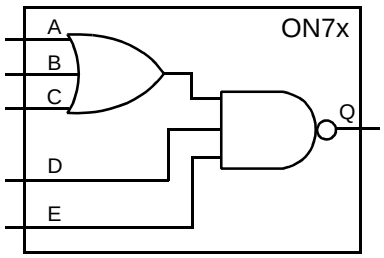
ON7x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON7x is a family of OR-NAND circuits consisting of one 3-input OR gate a two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

HDL Syntax

Verilog ..... ON7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON72	ON74	ON76
A	1.0	1.0	2.0
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON72	2.7	2.122	6.4
ON74	2.7	2.442	7.6
ON76	3.5	4.883	14.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON72	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.349 0.348	0.484 0.491	0.657 0.666	0.869 0.874	1.037 1.034
ON74	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.349 0.352	0.506 0.536	0.666 0.710	0.800 0.851	0.947 1.004
ON76	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.288 0.326	0.430 0.514	0.581 0.682	0.716 0.823	0.859 0.961

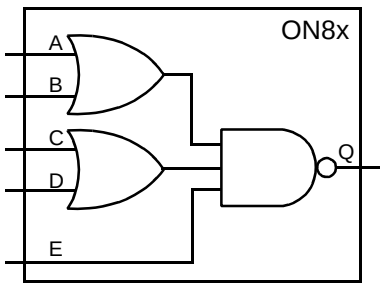
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON8x is a family of OR-NAND circuits consisting of two 2-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON82	ON84	ON86
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.1	1.0	2.0
D	1.0	1.0	1.9
E	1.0	1.1	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON82	3.5	2.675	8.2
ON84	3.5	2.995	9.5
ON86	3.8	5.988	16.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON82	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.308 0.373	0.446 0.540	0.626 0.727	0.844 0.935	1.016 1.090
ON84	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.327 0.400	0.468 0.598	0.628 0.785	0.769 0.934	0.929 1.095
ON86	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.270 0.335	0.420 0.539	0.564 0.696	0.693 0.836	0.826 0.992

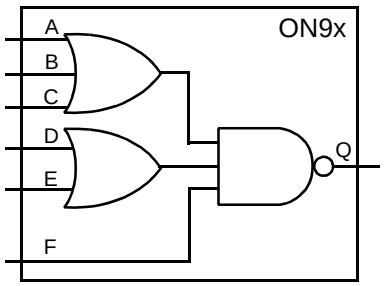
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ON9x is a family of OR-NAND circuits consisting of one 3-input OR gate, one 2-input OR gate, and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON92	ON94	ON96
A	1.0	1.0	2.0
B	1.1	1.0	2.0
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.9
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON92	3.8	2.883	8.7
ON94	3.8	3.203	9.9
ON96	4.2	6.404	17.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ON92	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.394 0.408	0.520 0.571	0.691 0.758	0.906 0.969	1.078 1.128
ON94	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.396 0.428	0.538 0.636	0.700 0.821	0.841 0.966	1.003 1.120
ON96	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.316 0.367	0.461 0.573	0.612 0.735	0.746 0.880	0.884 1.021

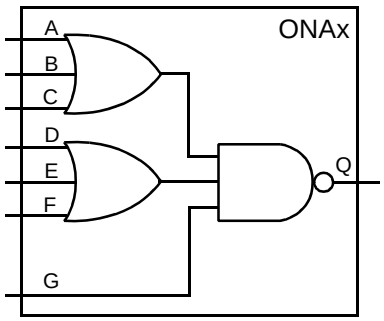
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONAx

Description

ONAx is a family of OR-NAND circuits consisting of two 3-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONAx port map (Q, A, B, C, D, E, F, G;)

Pin Loading

Pin Name	Equivalent Loads		
	ONA2	ONA4	ONA6
A	1.0	1.0	2.0
B	1.1	1.1	2.0
C	1.0	1.0	1.9
D	1.1	1.1	2.0
E	1.1	1.1	2.0
F	1.0	1.0	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONA2	4.0	3.091	9.2
ONA4	4.0	3.411	10.5
ONA6	4.8	6.821	18.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ONA2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.397 0.421	0.525 0.573	0.694 0.749	0.905 0.957	1.075 1.118
ONA4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.390 0.433	0.531 0.641	0.691 0.825	0.832 0.970	0.992 1.123
ONA6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.321 0.374	0.451 0.573	0.591 0.725	0.729 0.862	0.900 1.010

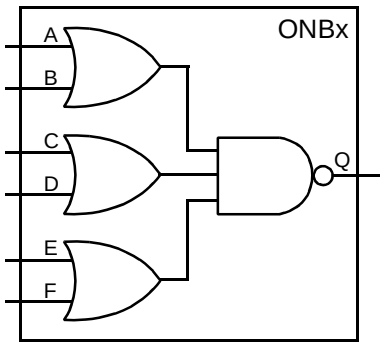
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONBx

Description

ONBx is a family of OR-NAND circuits consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ONBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ONBx port map (Q, A, B, C, D, E, F)

Pin Loading

Pin Name	Equivalent Loads		
	ONB2	ONB4	ONB6
A	1.1	1.1	2.0
B	1.0	1.0	1.9
C	1.1	1.1	2.0
D	1.0	1.0	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONB2	3.5	2.963	8.5
ONB4	3.5	3.283	9.8
ONB6	4.2	6.564	17.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ONB2	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.324 0.375	0.451 0.536	0.621 0.721	0.835 0.931	1.007 1.089
ONB4	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.326 0.394	0.466 0.600	0.625 0.783	0.764 0.926	0.922 1.078
ONB6	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.282 0.329	0.410 0.539	0.553 0.704	0.691 0.842	0.831 0.981

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

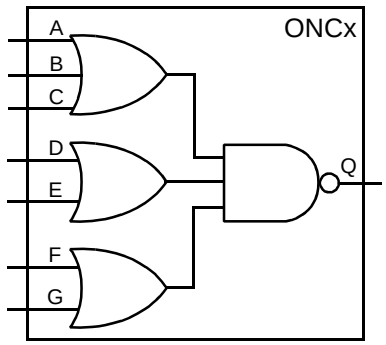
ONCx

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ONCx is a family of OR-NAND circuits consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ONC2	ONC4	ONC6
A	1.0	1.0	2.0
B	1.1	1.1	2.0
C	1.0	1.0	1.9
D	1.0	1.1	2.0
E	1.0	1.0	1.9
F	1.1	1.0	1.9
G	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONC2	4.0	3.171	9.0
ONC4	3.8	3.491	10.3
ONC6	4.8	6.981	18.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ONC2	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.394 0.406	0.520 0.568	0.691 0.754	0.905 0.966	1.077 1.126
ONC4	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.387 0.422	0.534 0.629	0.694 0.815	0.831 0.961	0.986 1.115
ONC6	Number of Equivalent Loads		1	15	30	44	59 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.321 0.353	0.457 0.561	0.602 0.728	0.739 0.870	0.886 1.018

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

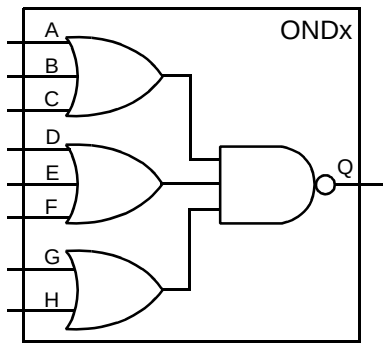
ONDx

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ONDx is a family of OR-NAND circuits consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

HDL Syntax

Verilog ..... ONDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ONDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	OND2	OND4	OND6
A	1.1	1.0	2.0
B	1.1	1.1	2.0
C	1.0	1.0	1.9
D	1.1	1.1	2.0
E	1.1	1.0	2.0
F	1.0	1.0	1.9
G	1.0	1.0	1.9
H	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OND2	4.2	3.379	9.5
OND4	4.2	3.700	10.7
OND6	4.8	7.397	19.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

OND2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.387 0.401	0.513 0.564	0.684 0.745	0.897 0.954	1.069 1.118
OND4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.389 0.423	0.540 0.632	0.701 0.816	0.837 0.958	0.990 1.109
OND6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.316 0.387	0.465 0.612	0.607 0.779	0.738 0.929	0.886 1.085

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

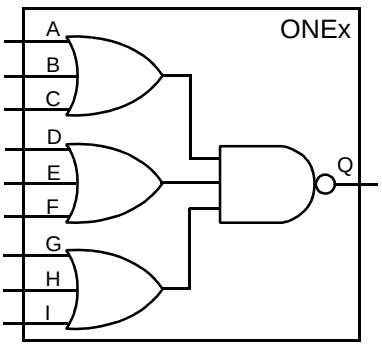
ONEx

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

ONEx is a family of OR-NAND circuits consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

HDL Syntax

Verilog ..... ONEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ONEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ONE2	ONE4	ONE6
A	1.0	1.0	2.0
B	1.0	1.1	2.0
C	1.0	1.0	1.9
D	1.1	1.1	2.0
E	1.1	1.1	2.0
F	1.0	1.0	1.9
G	1.1	1.1	2.0
H	1.1	1.1	2.0
I	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONE2	4.5	3.588	9.9
ONE4	4.5	3.908	11.2
ONE6	5.2	7.813	20.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ONE2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.397 0.406	0.530 0.568	0.701 0.752	0.909 0.961	1.074 1.118
ONE4	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.399 0.427	0.534 0.627	0.692 0.809	0.834 0.954	0.997 1.108
ONE6	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.356 0.349	0.472 0.563	0.610 0.731	0.742 0.874	0.883 1.018

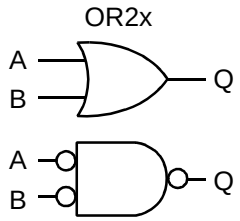
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

OR2x is a family of 2-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

HDL Syntax

Verilog ..... OR2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR21	OR22	OR24	OR26
A	1.0	1.0	2.0	2.0
B	1.0	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR21	1.2	0.929	2.3
OR22	1.5	1.249	3.3
OR24	2.0	2.498	6.2
OR26	2.2	3.234	8.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

OR21	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.177 0.221	0.310 0.364	0.483 0.538	0.697 0.744	0.868 0.904
OR22	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.165 0.238	0.317 0.419	0.480 0.594	0.618 0.734	0.772 0.887
OR24	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.152 0.194	0.294 0.383	0.440 0.541	0.576 0.677	0.722 0.814
OR26	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.172 0.257	0.313 0.450	0.450 0.591	0.582 0.727	0.721 0.864

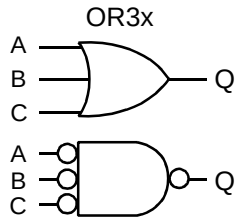
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

OR3x is a family of 3-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

HDL Syntax

Verilog ..... OR3x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR3x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR31	OR32	OR34	OR36
A	1.0	1.0	2.1	3.0
B	1.0	1.0	2.1	3.0
C	1.0	1.0	2.1	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR31	1.5	1.137	2.8
OR32	1.5	1.457	4.0
OR34	2.7	2.914	6.8
OR36	3.0	4.371	10.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

OR31	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.183 0.291	0.320 0.457	0.499 0.643	0.716 0.853	0.886 1.011
OR32	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.185 0.305	0.340 0.508	0.503 0.698	0.641 0.849	0.795 1.012
OR34	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.146 0.240	0.293 0.458	0.442 0.631	0.578 0.769	0.719 0.904
OR36	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.170 0.225	0.296 0.437	0.428 0.597	0.561 0.739	0.708 0.891

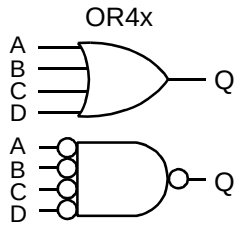
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

OR4x is a family of 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

HDL Syntax

Verilog ..... OR4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: OR4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	OR41	OR42	OR44	OR46
A	1.0	1.0	3.0	3.0
B	1.1	1.1	3.1	3.0
C	1.0	1.0	3.1	3.1
D	1.1	1.1	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR41	1.7	1.282	3.2
OR42	1.7	1.602	4.4
OR44	3.2	4.163	8.8
OR46	3.5	4.803	11.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

OR41	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.207 0.343	0.348 0.511	0.523 0.702	0.734 0.922	0.898 1.089
OR42	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.222 0.359	0.370 0.589	0.530 0.786	0.671 0.938	0.834 1.097
OR44	**Number of Equivalent Loads**		**1**	**15**	**30**	**44**	**59 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.167 0.214	0.305 0.433	0.432 0.606	0.571 0.755	0.725 0.905
OR46	**Number of Equivalent Loads**		**1**	**22**	**44**	**65**	**87 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.180 0.312	0.324 0.492	0.459 0.671	0.583 0.818	0.710 0.957

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORD

Description

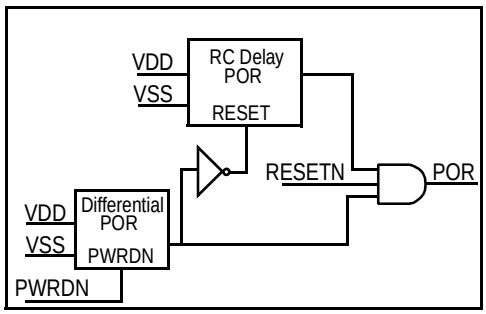
PORD is a high current, continous power monitoring power-on-reset circuit.

In this mode, the POR pulse is generated from a parallel combination of a self-latching RC delay circuit and a differential self biased circuit. The strengths of this circuit are in fast slew-rate power supply conditions and in continuous power monitoring. The POR signal will transition to a logic “Hi” in a specified delay time after the power supply has reached V_t. Once the power supply goes below the threshold voltage, V_t, the POR will transition to a logic “Low” and become active to prevent unknown states from occurring. There is a separate PWRDN input from the core that allows the user to put the PORD cell into low current mode during static IDDQ testing. If the PORD cell is put into low power mode, the continuous power supply monitoring function is disabled.

One drawback of this option is the high static IDD current of 400uA maximum, when the PWRDN port is driven to a “Low” state. This option is not for designs requiring a low power option without an external power down control from a known drive source. As shown in the Truth Table, PWRDN input does not effect the output of the POR cell if the power supply is static high or low. This circuit is characterized under the condition of fast power supply slew (100ns) and slow power supply slew of (100ms). The delay is measured relative to the power supply crossing the POR trip point, V_t = 1.65V. Operating specifications are given in Table 1. Figures 1 and 2 identify the dynamic parameters specified in Table 1.

Logic Symbol

PORD



Truth Table

LVDD	PWRDN	RESET	POROUT
$<V_t$	X	X	0
$>V_t$	X	0	1
$>V_t$	X	1	0

Pin Loading

	Load
RESET	1.8 eql
PWRDN	327.9 eql

HDL Syntax

Verilog ..... PORD *inst_name* (POROUT, PWRDN, RESET);

VHDL..... *inst_name*: PORD port map (POROUT, PWRDN, RESET);

Table 1: PORD Delay Specifications

Operating Conditions: 0-VDD Ramp rate, Minimum: 0.1us, Maximum: 100ms

Parameter	Parameter Description	Min	Max
t_{PSR}	Power Supply Ramp Time, 0-VDD	0.1us	
$t_{POR(Max)}$	POR Delay Time from V_T (Min VDD ramp rate)	0.075ms	0.150ms
$t_{POR(Min)}$	POR Delay Time from V_T (Max VDD ramp rate)	5ns	
t_{PSD}	Power Supply Cycle Down Time	0.1ms	
I_{SD}	Static Current Dissipation		400uA
t_{RDEL}	Delay from RESET (Active high) to POR (10pF Core Load		5ns

Parameter	Parameter Description	Min	Max
V_T	POR Teset Trigger Voltage	1.70 Volts	2.75 Volts

Figure 1: Continuous Monitoring PORD cell power up/down behavior waveform

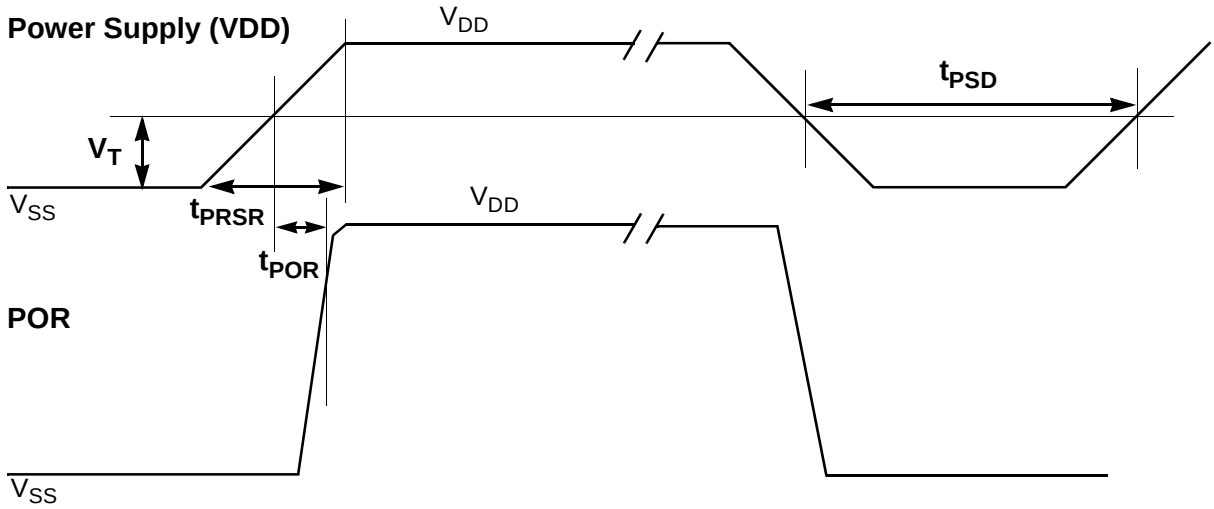
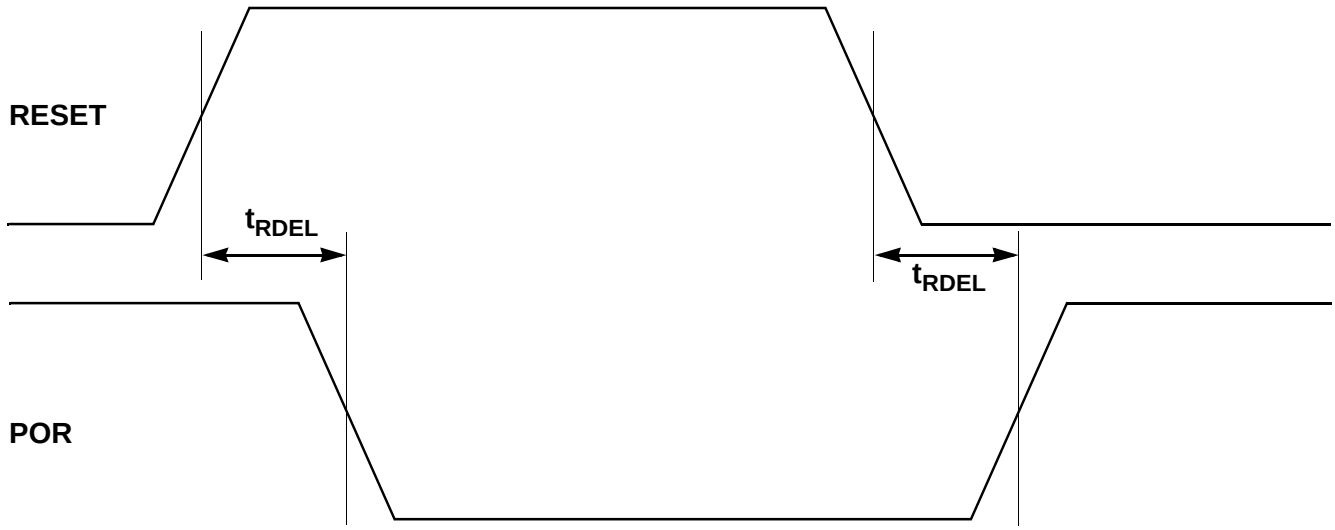


Figure 2: RESET to Software PORD delay waveform



Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	22	29 (max)
RESET	POROUT	t_{PLH}	0.208	0.288	0.376	0.472	0.550
RESET	POROUT	t_{PHL}	0.213	0.303	0.393	0.475	0.530

PORE

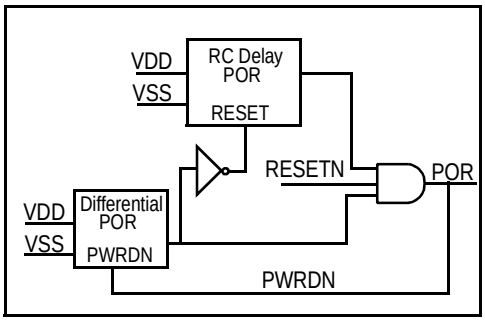
Description

PORE is a low power, non-continuous power monitoring power-on-reset circuit.

In this mode, the cell has the advantages of the RC Delay/ Differential POR and low power. A block diagram of this cell configuration is shown below. The one drawback is the self-latching feature, which requires the power supply to go below V_T and remain there for some minimum specified discharge time. The advantages are that it can handle both fast and slow power supply slew and uses low power after the POR is asserted. This circuit is characterized under the condition of fast power supply slew (0.1us) and slow power supply slew of (100ms). The delay is measured relative to V_T. Operating specifications are given in Table 1. Figures 1 and 2 identify the dynamic parameters specified in Table 1.

Logic Symbol

PORE



Truth Table

LVDD	PWRDN	RESET	POROUT
$<V_t$	X	X	0
$>V_t$	X	0	1
$>V_t$	X	1	0

Pin Loading

	Load
RESET	1.8 eql
PWRDN	328.4 eql

HDL Syntax

Verilog ..... PORE *inst_name* (POROUT, PWRDN, RESET);

VHDL..... *inst_name*: PORE port map (POROUT, PWRDN, RESET);

Table 1: PORE Delay Specifications

Operating Conditions: 0-VDD Ramp rate, Minimum: 0.1us, Maximum: 100ms

Parameter	Parameter Description	Min	Max
t_{PSR}	Power Supply Ramp Time, 0-VDD	0.1us	
$t_{POR(Max)}$	POR Delay Time from V_T (Min VDD ramp rate)	0.075ms	0.150ms
$t_{POR(Min)}$	POR Delay Time from V_T (Max VDD ramp rate)	5ns	
t_{PSD}	Power Supply Cycle Down Time	100ms	
I_{SD}	Static Current Dissipation		<1uA
t_{RDEL}	Delay from RESET (Active high) to POR		5ns
V_T	POR Trigger Voltage	1.70Volts	2.75 Volts

Figure 1: Continuous Monitoring PORE cell power up/down behavior waveform

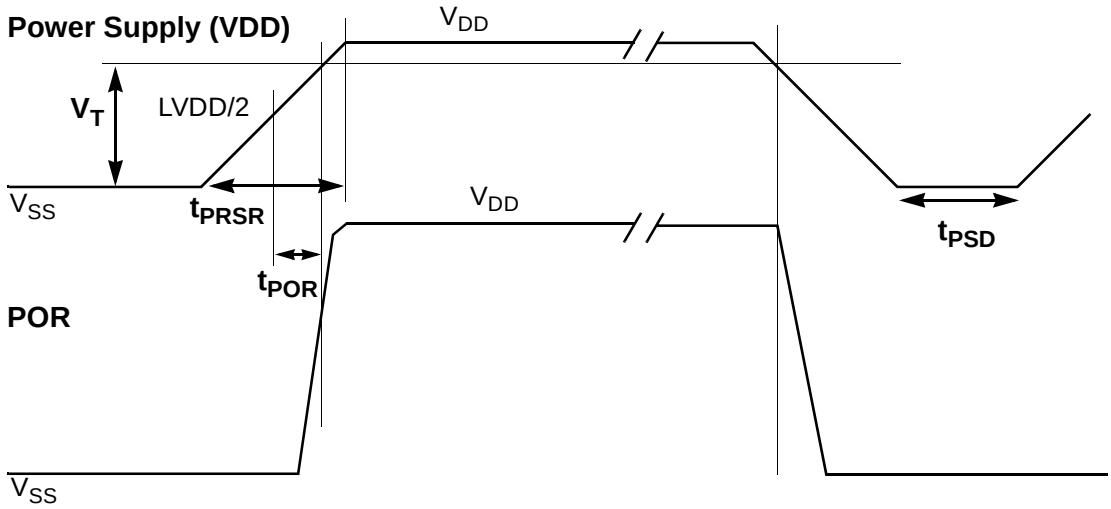
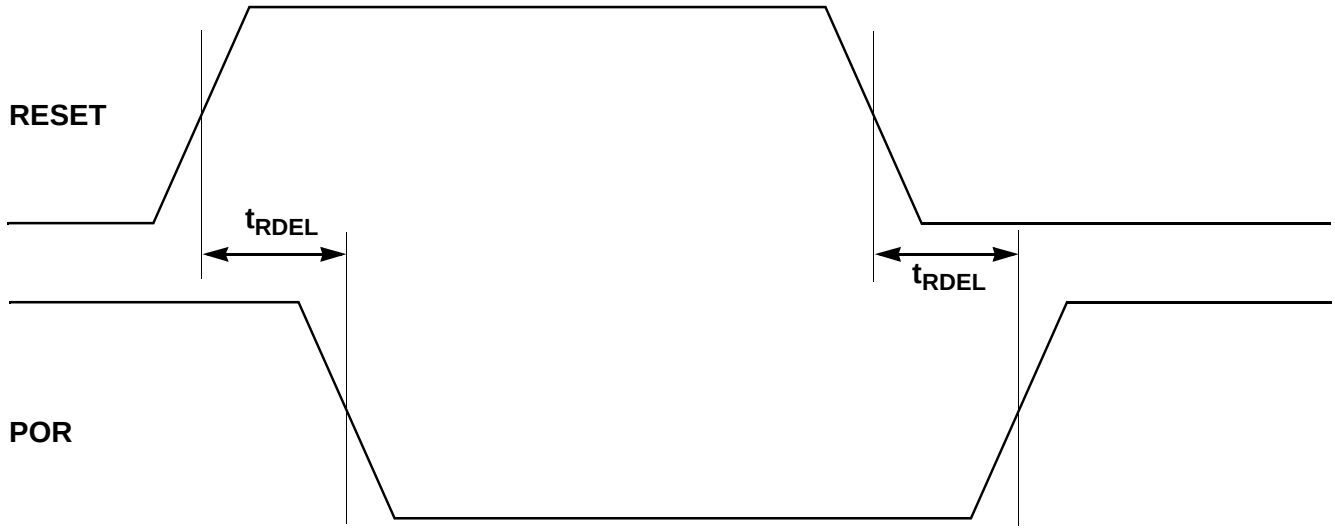


Figure 2: RESET to Software PORE delay waveform



Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	22	29 (max)
RESET	POROUT	t_{PLH}	0.214	0.292	0.380	0.475	0.554
RESET	POROUT	t_{PHL}	0.220	0.308	0.396	0.477	0.533

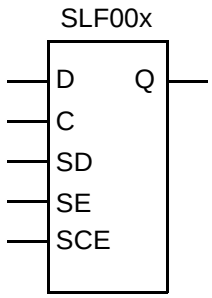
SLF00x

AMI350LXSC 0.35 micron CMOS Standard Cell

Description

SLF00x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low.

Logic Symbol



Truth Table

C	D	SD	SE	SCE	Q
↑	H	X	L	L	H
↑	L	X	L	L	L
↑	X	H	H	L	H
↑	X	L	H	L	L
L	X	X	X	L	NC
L	H	X	L	H	H
L	L	X	L	H	L
L	X	H	H	H	H
L	X	L	H	H	L
H	X	X	X	H	NC

NC = No Change

HDL Syntax

Verilog ..... SLF00x *inst_name* (Q, C, D, SCE, SD, SE);

VHDL..... *inst_name*: SLF00x port map (Q, C, D, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF001	SLF002	SLF004	SLF006
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SCE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF001	7.5	5.302	15.1
SLF002	8.0	6.110	18.4
SLF004	8.2	6.911	21.0
SLF006	8.5	7.711	23.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF001	From: C To: Q	t_{PLH} t_{PHL}	0.738 0.873	0.883 1.026	1.059 1.207	1.265 1.418	1.425 1.580
	From: D To: Q	t_{PLH} t_{PHL}	0.646 0.796	0.776 0.943	0.950 1.124	1.169 1.342	1.345 1.510
	From: SCE To: Q	t_{PLH} t_{PHL}	0.561 0.655	0.702 0.806	0.878 0.987	1.088 1.199	1.252 1.361
	From: SD To: Q	t_{PLH} t_{PHL}	0.660 0.809	0.783 0.975	0.956 1.155	1.180 1.354	1.362 1.501
	From: SE To: Q	t_{PLH} t_{PHL}	0.699 0.890	0.855 1.025	1.029 1.206	1.224 1.432	1.370 1.613
SLF002	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.701 0.852	0.844 1.015	0.998 1.179	1.129 1.313	1.277 1.461
	From: D To: Q	t_{PLH} t_{PHL}	0.649 0.758	0.799 0.928	0.952 1.097	1.080 1.236	1.220 1.389
	From: SCE To: Q	t_{PLH} t_{PHL}	0.502 0.618	0.659 0.790	0.825 0.961	0.965 1.101	1.122 1.254
	From: SD To: Q	t_{PLH} t_{PHL}	0.647 0.779	0.801 0.935	0.962 1.100	1.096 1.238	1.244 1.392
	From: SE To: Q	t_{PLH} t_{PHL}	0.698 0.869	0.834 1.045	0.988 1.207	1.122 1.334	1.275 1.471

AMI350LXSC 0.35 micron CMOS Standard Cell

	Number of Equivalent Loads		1	15	30	44	59 (max)
SLF004	From: C To: Q	t_{PLH} t_{PHL}	0.716 0.860	0.865 1.083	1.015 1.246	1.152 1.369	1.295 1.486
	From: D To: Q	t_{PLH} t_{PHL}	0.647 0.812	0.802 1.019	0.944 1.167	1.082 1.284	1.234 1.397
	From: SCE To: Q	t_{PLH} t_{PHL}	0.544 0.657	0.707 0.852	0.834 1.009	0.962 1.139	1.118 1.268
	From: SD To: Q	t_{PLH} t_{PHL}	0.651 0.773	0.821 0.984	0.960 1.134	1.093 1.268	1.241 1.414
	From: SE To: Q	t_{PLH} t_{PHL}	0.713 0.873	0.863 1.085	1.009 1.242	1.140 1.369	1.277 1.492
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
SLF006	From: C To: Q	t_{PLH} t_{PHL}	0.737 0.904	0.909 1.109	1.051 1.271	1.173 1.409	1.293 1.543
	From: D To: Q	t_{PLH} t_{PHL}	0.677 0.857	0.798 1.063	0.991 1.219	1.116 1.351	1.218 1.477
	From: SCE To: Q	t_{PLH} t_{PHL}	0.561 0.658	0.733 0.886	0.880 1.055	1.013 1.196	1.150 1.332
	From: SD To: Q	t_{PLH} t_{PHL}	0.692 0.830	0.851 1.048	1.000 1.209	1.128 1.342	1.251 1.470
	From: SE To: Q	t_{PLH} t_{PHL}	0.745 0.955	0.907 1.169	1.042 1.321	1.159 1.445	1.275 1.562

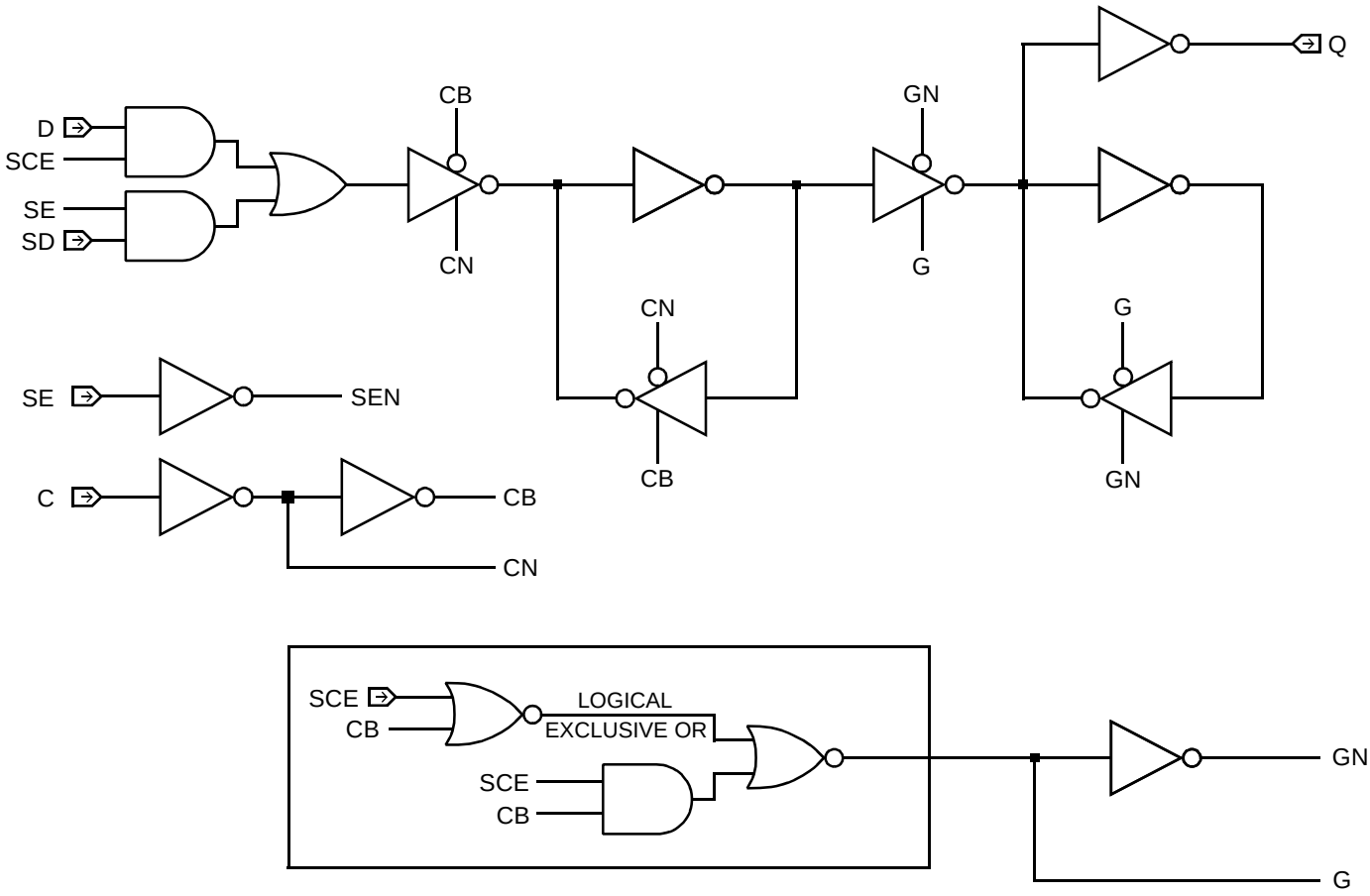
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF001	SLF002	SLF004	SLF006
Min C Width	High	t_w	0.781	0.781	0.825	0.875
Min C Width	Low	t_w	0.566	0.601	0.603	0.599
Min D Setup		t_{su}	0.474	0.511	0.502	0.509
Min D Hold		t_h	0.106	0.106	0.106	0.106
Min SD Setup		t_{su}	0.474	0.511	0.502	0.509
Min SD Hold		t_h	0.106	0.106	0.106	0.106
Min SE Setup		t_{su}	0.576	0.613	0.603	0.611
Min SE Hold		t_h	0.106	0.106	0.106	0.106
Min SCE Setup		t_{su}	0.603	0.603	0.647	0.696
Min SCE Hold		t_h	0.671	0.685	0.714	0.746

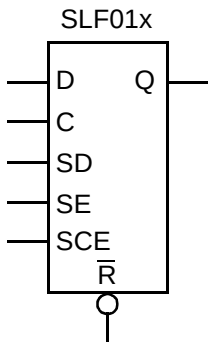
Logic Schematic



Description

SLF01x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. RESET is asynchronous and active low.

Logic Symbol



Truth Table

RN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF01x *inst_name* (Q, C, D, RN, SCE, SD, SE);

VHDL..... *inst_name*: SLF01x port map (Q, C, D, RN, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF011	SLF012	SLF014	SLF016
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.1
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SCE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF011	8.2	5.734	18.5
SLF012	9.0	6.543	22.0
SLF014	9.2	7.343	24.1
SLF016	9.0	8.527	27.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF011	From: C To: Q	t_{PLH} t_{PHL}	0.754 0.894	0.883 1.058	1.060 1.240	1.278 1.444	1.459 1.597
	From: D To: Q	t_{PLH} t_{PHL}	0.727 0.819	0.866 0.987	1.043 1.169	1.256 1.369	1.423 1.516
	From: RN To: Q	t_{PLH} t_{PHL}	0.558 0.740	0.694 0.942	0.871 1.138	1.087 1.341	1.258 1.484
	From: SCE To: Q	t_{PLH} t_{PHL}	0.563 0.663	0.701 0.830	0.877 1.011	1.093 1.210	1.263 1.357
	From: SD To: Q	t_{PLH} t_{PHL}	0.743 0.804	0.888 0.965	1.064 1.147	1.272 1.355	1.433 1.512
	From: SE To: Q	t_{PLH} t_{PHL}	0.782 0.914	0.934 1.076	1.110 1.259	1.312 1.465	1.465 1.618
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
SLF012	From: C To: Q	t_{PLH} t_{PHL}	0.763 0.879	0.912 1.028	1.067 1.192	1.196 1.334	1.339 1.495
	From: D To: Q	t_{PLH} t_{PHL}	0.758 0.804	0.899 0.971	1.054 1.135	1.187 1.269	1.337 1.416
	From: RN To: Q	t_{PLH} t_{PHL}	0.564 0.885	0.713 1.124	0.879 1.331	1.023 1.491	1.186 1.659
	From: SCE To: Q	t_{PLH} t_{PHL}	0.518 0.646	0.662 0.814	0.826 0.978	0.969 1.109	1.133 1.250
	From: SD To: Q	t_{PLH} t_{PHL}	0.766 0.800	0.914 0.973	1.069 1.136	1.199 1.266	1.345 1.407
	From: SE To: Q	t_{PLH} t_{PHL}	0.810 0.903	0.966 1.053	1.119 1.218	1.245 1.360	1.382 1.520

AMI350LXSC 0.35 micron CMOS Standard Cell

	Number of Equivalent Loads		1	15	30	44	59 (max)
SLF014	From: C To: Q	t_{PLH} t_{PHL}	0.778 0.891	0.955 1.088	1.100 1.252	1.219 1.389	1.334 1.526
	From: D To: Q	t_{PLH} t_{PHL}	0.738 0.832	0.888 1.046	1.046 1.194	1.189 1.308	1.335 1.417
	From: RN To: Q	t_{PLH} t_{PHL}	0.606 1.083	0.774 1.374	0.917 1.582	1.037 1.748	1.156 1.907
	From: SCE To: Q	t_{PLH} t_{PHL}	0.567 0.655	0.715 0.857	0.866 1.018	1.006 1.152	1.154 1.284
	From: SD To: Q	t_{PLH} t_{PHL}	0.786 0.809	0.911 1.013	1.057 1.183	1.201 1.321	1.363 1.455
	From: SE To: Q	t_{PLH} t_{PHL}	0.828 0.881	0.965 1.101	1.107 1.277	1.240 1.420	1.385 1.564
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
SLF016	From: C To: Q	t_{PLH} t_{PHL}	1.011 1.042	1.168 1.177	1.296 1.322	1.407 1.464	1.540 1.613
	From: D To: Q	t_{PLH} t_{PHL}	0.977 0.951	1.099 1.138	1.237 1.275	1.373 1.387	1.518 1.493
	From: RN To: Q	t_{PLH} t_{PHL}	0.803 0.383	0.921 0.549	1.062 0.697	1.203 0.830	1.355 0.972
	From: SCE To: Q	t_{PLH} t_{PHL}	0.830 0.795	0.961 0.976	1.068 1.119	1.194 1.239	1.363 1.355
	From: SD To: Q	t_{PLH} t_{PHL}	0.952 0.938	1.125 1.126	1.274 1.268	1.404 1.387	1.531 1.501
	From: SE To: Q	t_{PLH} t_{PHL}	1.032 1.021	1.159 1.183	1.303 1.334	1.444 1.471	1.594 1.611

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

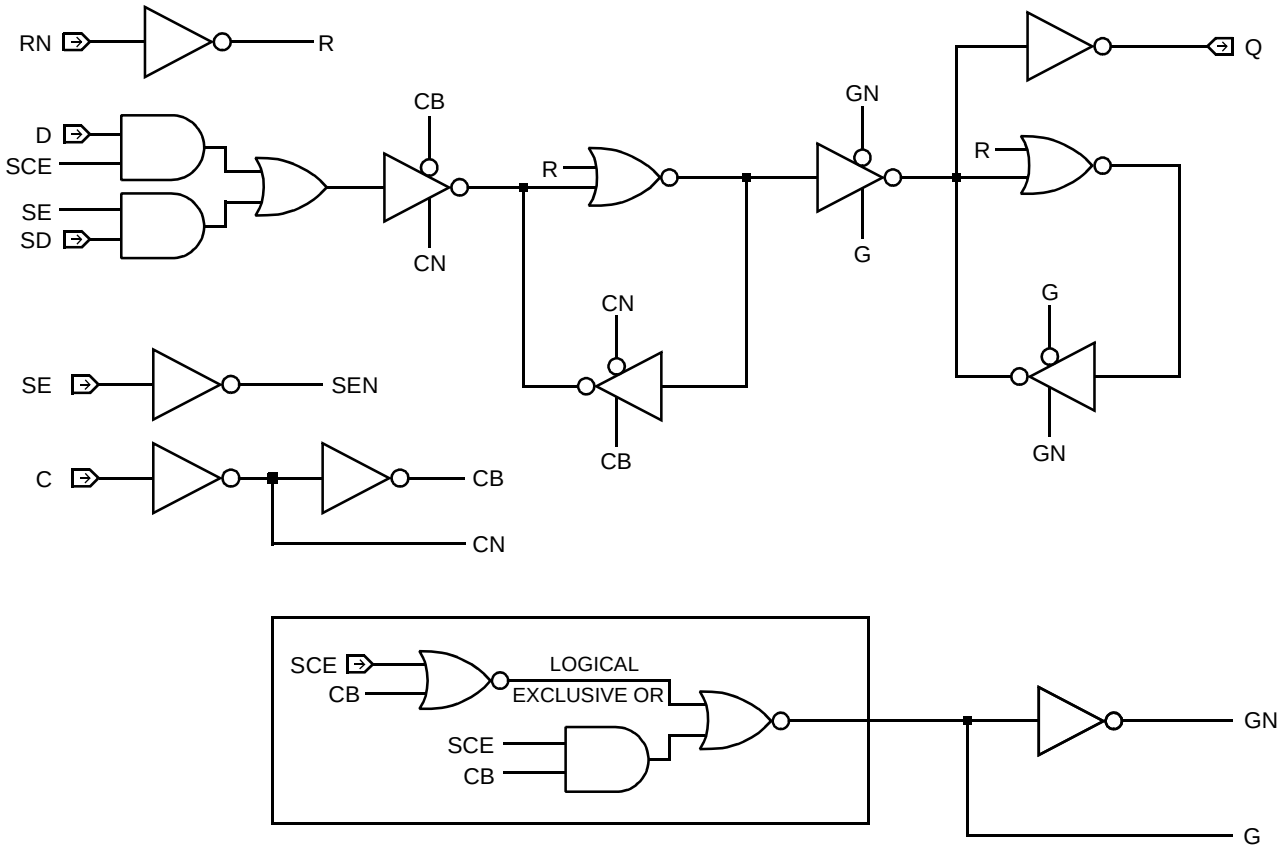
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF011	SLF012	SLF014	SLF016
Min C Width	High	t_w	0.798	0.808	0.855	0.823
Min C Width	Low	t_w	0.588	0.624	0.627	0.589
Min RN Width	Low	t_w	0.490	0.514	0.514	0.491
Min D Setup		t_{su}	0.487	0.534	0.526	0.487
Min D Hold		t_h	0.107	0.107	0.107	0.107
Min SD Setup		t_{su}	0.487	0.534	0.526	0.487
Min SD Hold		t_h	0.107	0.107	0.107	0.107
Min SE Setup		t_{su}	0.588	0.636	0.627	0.590
Min SE Hold		t_h	0.107	0.107	0.107	0.107
Min SCE Setup		t_{su}	0.620	0.630	0.676	0.644
Min SCE Hold		t_h	0.679	0.698	0.730	0.661
Min RN Setup		t_{su}	0.257	0.296	0.295	0.259
Min RN Hold		t_h	0.294	0.293	0.293	0.293

AMI350LXSC 0.35 micron CMOS Standard Cell

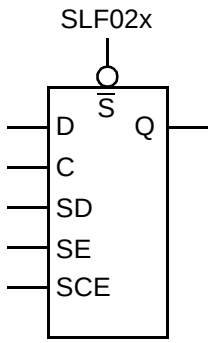
Logic Schematic



Description

SLF02x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET is asynchronous and active low.

Logic Symbol



Truth Table

SN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	H

NC = No Change

HDL Syntax

Verilog ..... SLF02x *inst_name* (Q, C, D, SCE, SD, SE, SN);

VHDL..... *inst_name*:SLF02x port map (Q, C, D, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF021	SLF022	SLF024	SLF026
C	1.0	1.0	1.0	1.0
D	1.1	1.1	1.1	1.1
SD	1.0	1.0	1.0	1.1
SE	2.2	2.2	2.2	2.2
SCE	2.1	2.1	2.1	2.1
SN	2.2	2.2	2.2	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF021	8.0	5.878	15.9
SLF022	8.8	6.687	19.2
SLF024	9.0	7.487	21.2
SLF026	8.8	8.671	24.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
SLF021	From: C To: Q	t_{PLH} t_{PHL}	0.743 0.923	0.872 1.072	1.047 1.256	1.268 1.474	1.445 1.642
	From: D To: Q	t_{PLH} t_{PHL}	0.679 0.853	0.808 1.018	0.982 1.201	1.202 1.404	1.379 1.556
	From: SCE To: Q	t_{PLH} t_{PHL}	0.593 0.667	0.747 0.822	0.922 1.005	1.119 1.216	1.267 1.377
	From: SD To: Q	t_{PLH} t_{PHL}	0.692 0.853	0.816 1.023	0.990 1.204	1.213 1.402	1.395 1.547
	From: SE To: Q	t_{PLH} t_{PHL}	0.730 0.934	0.843 1.096	1.014 1.279	1.244 1.486	1.438 1.641
	From: SN To: Q	t_{PLH} t_{PHL}	0.485 0.472	0.627 0.646	0.807 0.861	1.026 1.117	1.197 1.317
	Number of Equivalent Loads		**1**	**8**	**16**	**23**	**31 (max)**
SLF022	From: C To: Q	t_{PLH} t_{PHL}	0.712 0.914	0.862 1.106	1.016 1.263	1.143 1.381	1.285 1.504
	From: D To: Q	t_{PLH} t_{PHL}	0.682 0.841	0.833 1.015	0.986 1.178	1.114 1.308	1.254 1.449
	From: SCE To: Q	t_{PLH} t_{PHL}	0.570 0.638	0.717 0.801	0.871 0.965	1.000 1.100	1.143 1.247
	From: SD To: Q	t_{PLH} t_{PHL}	0.690 0.820	0.833 0.986	0.991 1.151	1.123 1.286	1.267 1.434
	From: SE To: Q	t_{PLH} t_{PHL}	0.733 0.926	0.887 1.093	1.040 1.257	1.166 1.391	1.303 1.538
	From: SN To: Q	t_{PLH} t_{PHL}	0.566 0.423	0.741 0.621	0.919 0.826	1.068 0.997	1.232 1.187

AMI350LXSC 0.35 micron CMOS Standard Cell

	Number of Equivalent Loads		1	15	30	44	59 (max)
SLF024	From: C To: Q	t_{PLH} t_{PHL}	0.731 0.937	0.887 1.129	1.033 1.283	1.161 1.408	1.292 1.527
	From: D To: Q	t_{PLH} t_{PHL}	0.682 0.867	0.851 1.077	0.998 1.232	1.125 1.355	1.253 1.475
	From: SCE To: Q	t_{PLH} t_{PHL}	0.563 0.664	0.722 0.837	0.885 1.004	1.029 1.152	1.178 1.307
	From: SD To: Q	t_{PLH} t_{PHL}	0.700 0.837	0.862 1.045	1.011 1.202	1.143 1.336	1.279 1.473
	From: SE To: Q	t_{PLH} t_{PHL}	0.720 0.930	0.880 1.126	1.033 1.287	1.169 1.430	1.314 1.566
	From: SN To: Q	t_{PLH} t_{PHL}	0.670 0.450	0.883 0.658	1.046 0.854	1.179 1.029	1.309 1.211
SLF026	Number of Equivalent Loads		1	22	44	65	87 (max)
	From: C To: Q	t_{PLH} t_{PHL}	0.905 1.069	1.047 1.205	1.185 1.354	1.310 1.490	1.436 1.622
	From: D To: Q	t_{PLH} t_{PHL}	0.845 0.978	0.999 1.128	1.137 1.279	1.256 1.421	1.369 1.569
	From: SCE To: Q	t_{PLH} t_{PHL}	0.751 0.819	0.890 0.986	1.030 1.132	1.159 1.262	1.291 1.391
	From: SD To: Q	t_{PLH} t_{PHL}	0.834 0.984	0.997 1.151	1.139 1.297	1.265 1.425	1.391 1.553
	From: SE To: Q	t_{PLH} t_{PHL}	0.911 1.094	1.041 1.222	1.171 1.368	1.297 1.509	1.431 1.657
	From: SN To: Q	t_{PLH} t_{PHL}	0.309 0.597	0.455 0.793	0.589 0.971	0.717 1.126	0.852 1.277

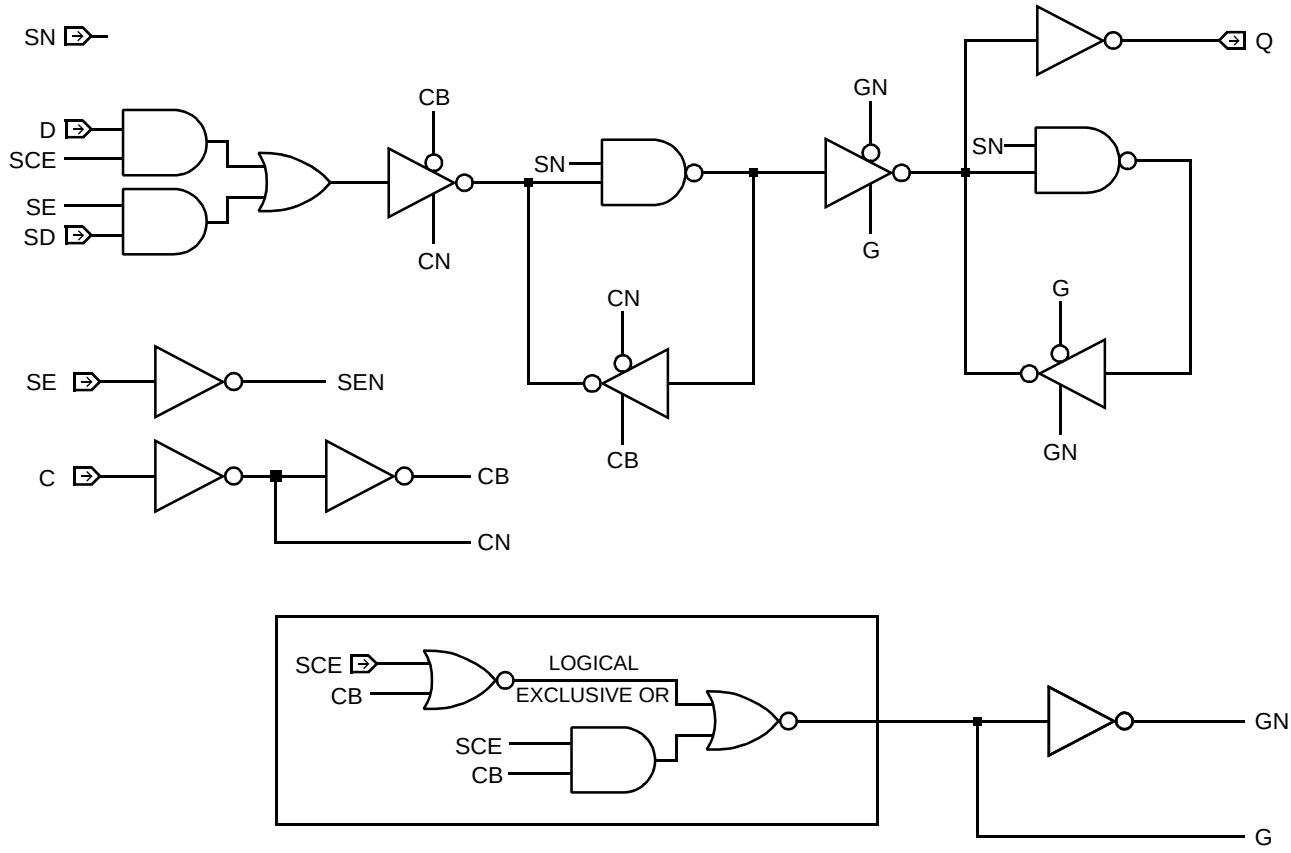
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF021	SLF022	SLF024	SLF026
Min C Width	High	t_w	0.811	0.818	0.868	0.835
Min C Width	Low	t_w	0.612	0.655	0.655	0.605
Min SN Width	Low	t_w	0.373	0.415	0.415	0.376
Min D Setup		t_{su}	0.509	0.553	0.553	0.501
Min D Hold		t_h	0.107	0.107	0.107	0.107
Min SD Setup		t_{su}	0.509	0.553	0.553	0.501
Min SD Hold		t_h	0.107	0.107	0.107	0.107
Min SE Setup		t_{su}	0.613	0.655	0.655	0.606
Min SE Hold		t_h	0.107	0.107	0.107	0.107
Min SCE Setup		t_{su}	0.635	0.640	0.690	0.657
Min SCE Hold		t_h	0.676	0.697	0.727	0.659
Min SN Setup		t_{su}	0.134	0.165	0.164	0.136
Min SN Hold		t_h	0.451	0.452	0.452	0.452

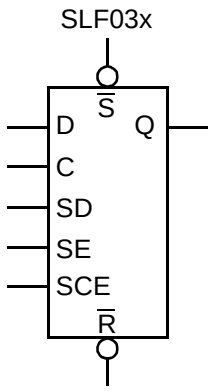
Logic Schematic



Description

SLF03x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET and RESET are asynchronous and active low.

Logic Symbol



Truth Table

RN	SN	C	D	SD	SE	SCE	Q
H	H	↑	H	X	L	L	H
H	H	↑	L	X	L	L	L
H	H	↑	X	H	H	L	H
H	H	↑	X	L	H	L	L
H	H	L	X	X	X	L	NC
H	H	L	H	X	L	H	H
H	H	L	L	X	L	H	L
H	H	L	X	H	H	H	H
H	H	L	X	L	H	H	L
H	H	H	X	X	X	H	NC
H	L	X	X	X	X	X	H
L	X	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF03x *inst_name* (Q, C, D, RN, SCE, SD, SE, SN);

VHDL..... *inst_name*: SLF03x port map (Q, C, D, RN, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF031	SLF032	SLF034	SLF036
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.2	2.2	2.2	2.2
SCE	2.1	2.1	2.1	2.1
SN	2.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF031	9.0	6.383	19.6
SLF032	9.5	7.199	22.9
SLF034	9.8	8.000	25.2
SLF036	10.2	8.800	28.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	8	16	23	31 (max)
SLF031	From: C To: Q	t_{PLH} t_{PHL}	0.791 0.933	1.124 1.263	1.475 1.603	1.770 1.888	2.100 2.204
	From: D To: Q	t_{PLH} t_{PHL}	0.790 0.860	1.092 1.185	1.433 1.527	1.730 1.814	2.068 2.134
	From: RN To: Q	t_{PLH} t_{PHL}	0.600 0.731	0.922 1.110	1.274 1.484	1.577 1.790	1.919 2.126
	From: SCE To: Q	t_{PLH} t_{PHL}	0.641 0.655	0.945 0.987	1.296 1.336	1.604 1.629	1.956 1.956
	From: SD To: Q	t_{PLH} t_{PHL}	0.786 0.843	1.114 1.192	1.465 1.540	1.762 1.827	2.096 2.141
	From: SE To: Q	t_{PLH} t_{PHL}	0.840 0.950	1.172 1.294	1.512 1.634	1.794 1.911	2.106 2.215
	From: SN To: Q	t_{PLH} t_{PHL}	0.473 0.477	0.790 0.875	1.151 1.297	1.466 1.655	1.825 2.054
SLF032	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: C To: Q	t_{PLH} t_{PHL}	0.824 0.927	0.974 1.115	1.129 1.275	1.258 1.397	1.401 1.524
	From: D To: Q	t_{PLH} t_{PHL}	0.814 0.848	0.941 1.017	1.096 1.181	1.236 1.315	1.398 1.461
	From: RN To: Q	t_{PLH} t_{PHL}	0.642 0.903	0.782 1.143	0.937 1.351	1.072 1.512	1.224 1.682
	From: SCE To: Q	t_{PLH} t_{PHL}	0.639 0.651	0.792 0.822	0.954 0.985	1.091 1.116	1.244 1.258
	From: SD To: Q	t_{PLH} t_{PHL}	0.828 0.829	0.960 0.993	1.115 1.158	1.253 1.294	1.411 1.444
	From: SE To: Q	t_{PLH} t_{PHL}	0.867 0.932	0.996 1.113	1.151 1.275	1.289 1.401	1.450 1.536
	From: SN To: Q	t_{PLH} t_{PHL}	0.574 0.455	0.759 0.657	0.932 0.862	1.070 1.030	1.219 1.216

	Number of Equivalent Loads		1	15	30	44	59 (max)
SLF034	From: C To: Q	t_{PLH} t_{PHL}	0.806 0.951	0.982 1.135	1.141 1.298	1.276 1.432	1.411 1.563
	From: D To: Q	t_{PLH} t_{PHL}	0.810 0.879	0.954 1.043	1.126 1.204	1.265 1.349	1.414 1.501
	From: RN To: Q	t_{PLH} t_{PHL}	0.659 1.061	0.818 1.324	0.969 1.549	1.102 1.741	1.240 1.934
	From: SCE To: Q	t_{PLH} t_{PHL}	0.673 0.680	0.828 0.874	0.974 1.028	1.105 1.160	1.243 1.295
	From: SD To: Q	t_{PLH} t_{PHL}	0.838 0.881	0.986 1.084	1.153 1.242	1.292 1.372	1.417 1.500
	From: SE To: Q	t_{PLH} t_{PHL}	0.897 0.947	1.024 1.149	1.168 1.332	1.302 1.488	1.446 1.643
	From: SN To: Q	t_{PLH} t_{PHL}	0.682 0.471	0.894 0.689	1.061 0.888	1.199 1.057	1.336 1.226
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
SLF036	From: C To: Q	t_{PLH} t_{PHL}	0.889 1.006	1.051 1.212	1.160 1.360	1.294 1.481	1.433 1.596
	From: D To: Q	t_{PLH} t_{PHL}	0.845 0.911	1.024 1.117	1.153 1.278	1.283 1.413	1.435 1.545
	From: RN To: Q	t_{PLH} t_{PHL}	0.692 1.299	0.845 1.626	0.988 1.841	1.116 2.012	1.244 2.172
	From: SCE To: Q	t_{PLH} t_{PHL}	0.700 0.738	0.852 0.919	1.001 1.065	1.135 1.210	1.269 1.372
	From: SD To: Q	t_{PLH} t_{PHL}	0.892 0.923	1.059 1.132	1.202 1.293	1.316 1.423	1.414 1.541
	From: SE To: Q	t_{PLH} t_{PHL}	0.918 0.992	1.082 1.236	1.224 1.385	1.350 1.508	1.475 1.628
	From: SN To: Q	t_{PLH} t_{PHL}	0.818 0.522	1.045 0.765	1.205 0.954	1.336 1.113	1.459 1.265

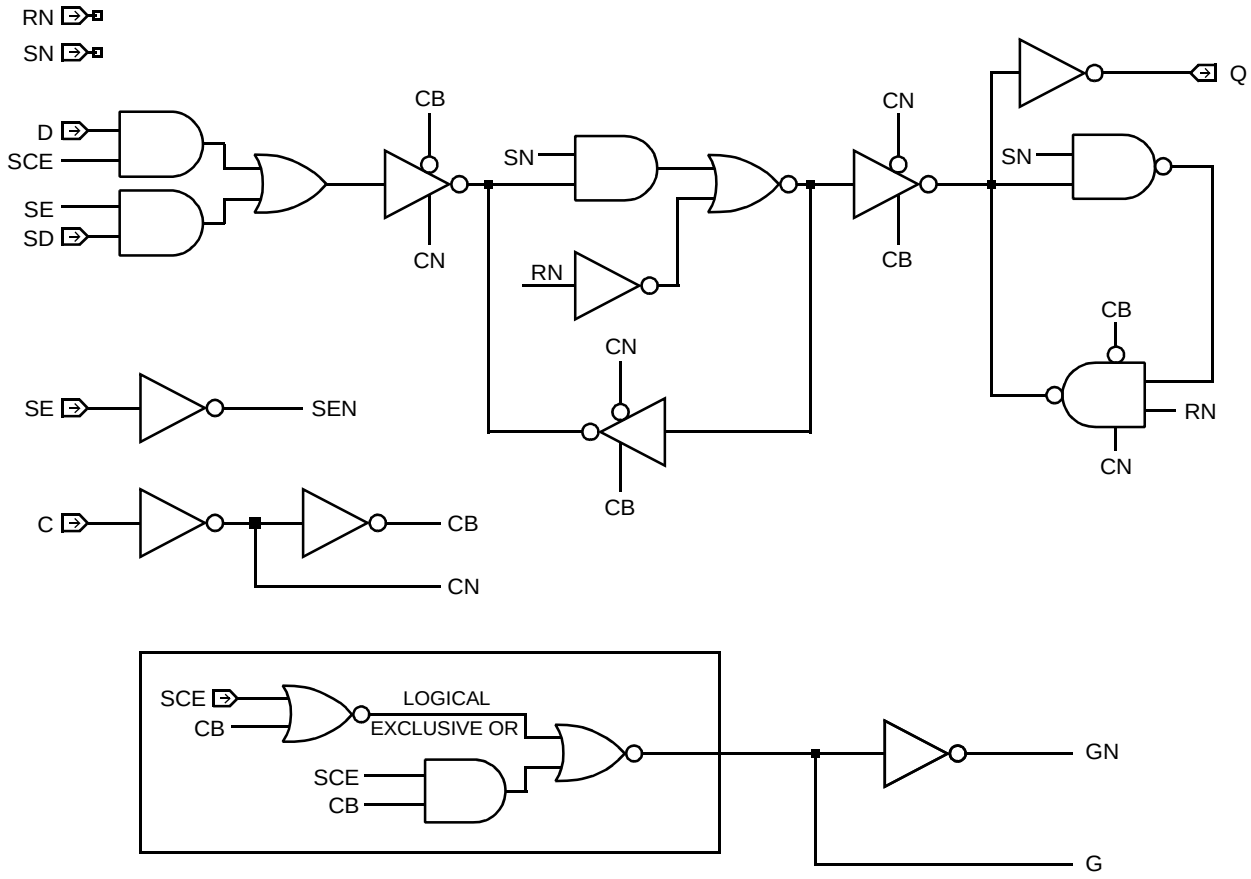
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF031	SLF032	SLF034	SLF036
Min C Width	High	t_w	0.824	0.833	0.881	0.927
Min C Width	Low	t_w	0.620	0.664	0.664	0.664
Min RN Width	Low	t_w	0.505	0.538	0.538	0.538
Min SN Width	Low	t_w	0.369	0.405	0.405	0.405
Min D Setup		t_{su}	0.518	0.563	0.563	0.563
Min D Hold		t_h	0.107	0.107	0.107	0.107
Min RN Setup		t_{su}	0.289	0.338	0.338	0.338
Min RN Hold		t_h	0.290	0.290	0.290	0.290
Min SCE Setup		t_{su}	0.661	0.679	0.729	0.775
Min SCE Hold		t_h	0.681	0.701	0.731	0.762
Min SD Setup		t_{su}	0.518	0.563	0.563	0.563
Min SD Hold		t_h	0.107	0.107	0.107	0.107
Min SE Setup		t_{su}	0.619	0.665	0.665	0.664
Min SE Hold		t_h	0.107	0.107	0.107	0.107
Min SN Setup		t_{su}	0.158	0.191	0.191	0.191
Min SN Hold		t_h	0.450	0.450	0.450	0.450

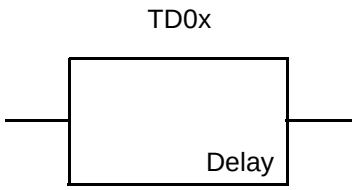
Logic Schematic



Description

TD0x is a family of non-inverting time delays.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... TD0x *inst_name* (Q, A);

VHDL..... *inst_name*: TD0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	TD01	TD02	TD06
A	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
TD01	3.8	4.051	16.9
TD02	5.5	4.276	22.9
TD06	13.7	11.049	63.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

TD01	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	1.085 1.076	1.199 1.233	1.348 1.381	1.486 1.499	1.651 1.627
TD02	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	2.220 2.213	2.333 2.383	2.482 2.526	2.621 2.636	2.786 2.751
TD06	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	6.374 6.520	6.399 6.663	6.494 6.700	6.644 6.718	6.903 6.732

Delay will vary with input conditions. See page 2-15 for interconnect estimates.