0.5 Micron CMOS Pad Library Datasheets
AMI500HXPS 3.3 Volt
Section 4
Revision 1.1

Input Drive Pieces

Name	Description	Page
IDCI3	Inverting, CMOS-level input buffer piece	4-5
IDCR0	Non-buffered, resistive analog interface input piece with ESD protection	4-6
IDCS3	Non-inverting, CMOS-level Schmitt trigger input buffer piece	4-7
IDCXx	Family of non-inverting, CMOS-level input buffer pieces	4-8
IDPX3	Non-inverting, PCI-level input buffer piece	4-9
IDQC0	Non-buffered, resistive crystal oscillator input receiver piece with ESD protection	4-10
IDQC3	Crystal oscillator input receiver pad piece with a non-inverting, CMOS-level input	4-11
IDQS3	Crystal oscillator input receiver pad piece	4-13
IDVS3	Non-inverting, LVTTL-level Schmitt input buffer piece	4-15
IDVX3	Non-inverting, LVTTL-level input buffer piece	4-16

Pull Pieces

PLD3	Active pull-down buffer piece	4-38
PLP3	programmable pull-up/pull-down buffer piece	4-39
PLU3	Active pull-up buffer piece	4-40

Output Drive Pieces

ODCHXE12	12 mA non-inverting, CMOS-level, tristate output piece with active low enable outputs	4-17
ODCHXX12	12 mA non-inverting, CMOS-level output piece	4-18
ODCSIPxx	Family of 4 to 12 mA, inverting, CMOS-level output pieces with P-channel open-drains (pull-up) and controlled slew rate outputs	4-19
ODCSXExx	Family of 4 to 12 mA, non-inverting, CMOS-level, tristate output pieces with active low enables and controlled slew rate outputs	4-21
ODCSXXxx	Family of 4 to 12 mA, non-inverting, CMOS-level, output pieces w/slew rate outputs	4-23
ODCXIPxx	Family of 1 to 12 mA, inverting, CMOS-level, output pieces w/P-channel, open-drains (pull-up)	4-25
ODCXXExx	Family of 1 to 12 mA, non-inverting, CMOS-level, tristate output w/active low enables	4-27
ODCXXXxx	Family of 1 to 12 mA, non-inverting, CMOS-level output pieces	4-29

Selection Guide

AMI500HXPS 0.5 micron CMOS Pad Library

Power Pad Cells

Name	Description	Page
PWRPAD	Generic power pad	4-41
GNDPAD	Generic ground pad	4-42

Special Pad Cells

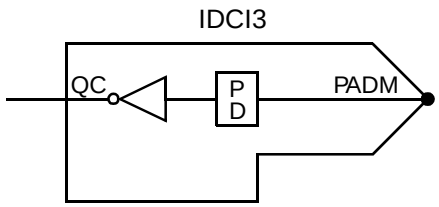
ODQFE01M	Fundamental mode, enabled crystal oscillator output for frequency range of 32 kHz - 1 MHz	4-31
ODQFE20M	Fundamental mode, enabled crystal oscillator output for frequency range of 1 MHz - 20 MHz	4-33
ODQTE60M	Third-overtone mode, enabled crystal oscillator output for frequency range of 20 - 60 MHz	4-35
ODQXXX00	Non-buffered, resistive analog crystal oscillator output pad piece with ESD protection	4-37
SHFTOUT	Mixed voltage single output for level-shifting from a 2.5 V core to a 3.3 V pad.	4-43
SHFTOUTT	Mixed voltage dual output for level-shifting from a 2.5 V core to a 3.3Vpad.	4-44

DATASHEETS

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	16.522	nA
EQL_{pd}	12.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.724 0.945	0.867 1.102	1.009 1.258	1.133 1.378	1.267 1.486

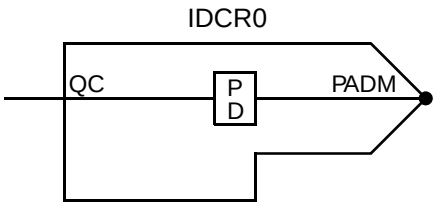
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.265	nA
EQL_{pd}	2.1	Eq-load

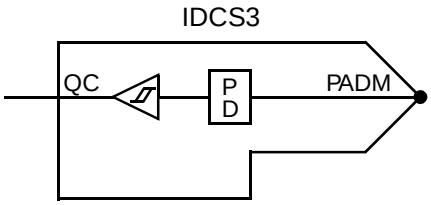
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCS3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.963	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.499 1.079	1.634 1.245	1.806 1.390	1.973 1.524	2.165 1.680

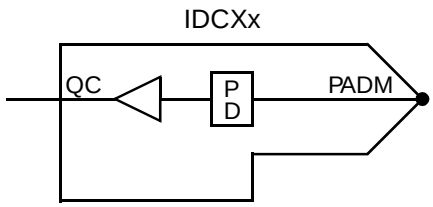
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	0.0	15.832	10.4
IDCX6	0.0	18.757	18.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

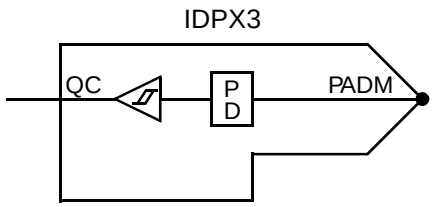
	Number of Equivalent Loads		1	11	22	32	43 (max)
IDCX3	From: PADM To: QC	t_{PLH} t_{PHL}	0.883 0.654	1.055 0.834	1.195 0.977	1.305 1.080	1.417 1.169
	Number of Equivalent Loads		**1**	**11**	**22**	**32**	**43 (max)**
IDCX6	From: PADM To: QC	t_{PLH} t_{PHL}	0.774 0.632	0.825 0.710	0.897 0.793	0.971 0.869	1.060 0.951

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load
	IDPX3
PADM (pF)	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	0.0	15.774	12.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
IDPX3	From: PADM	t_{PLH}	0.795	0.948	1.106	1.227	1.331
	To: QC	t_{PHL}	0.893	1.068	1.230	1.370	1.517

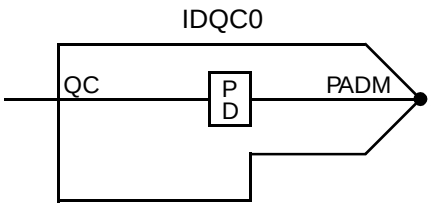
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);
VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.265	nA
EQL_{pd}	2.1	Eq-load

See page 2-13 for power equation.

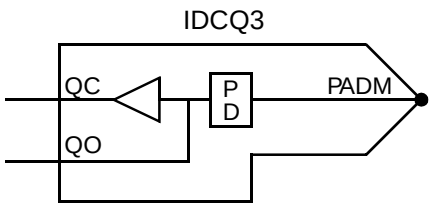
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

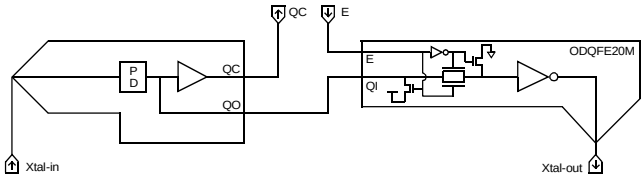
Description

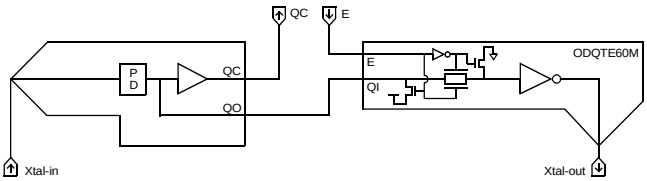
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.90 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.832	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.904 0.685	1.070 0.833	1.204 0.965	1.319 1.084	1.447 1.216
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

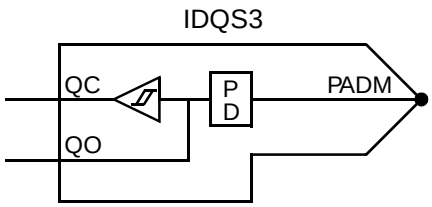
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

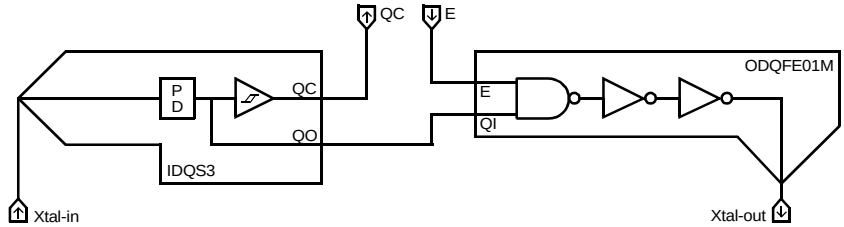
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load	
PADM	4.90	pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.963	nA
EQL_{pd}	18.0	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.533 1.093	1.648 1.299	1.806 1.451	1.966 1.568	2.154 1.683
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes:

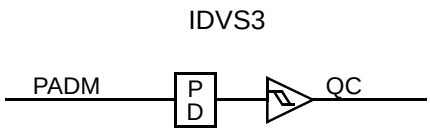
The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

3.3

Description

IDVS3 is a non-inverting, LVTTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM(pF)	4.90

HDL Syntax

Verilog ..... IDVS3 *inst_name*(QC, PADM);

VHDL..... *inst_name*: IDVS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.750	nA
EQL_{pd}	16.5	eql

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

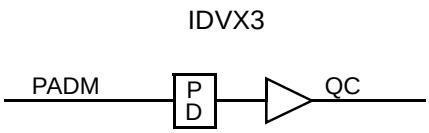
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.096 1.154	1.281 1.313	1.419 1.526	1.529 1.693	1.641 1.816

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDVX3 is a non-inverting, LVTTL-level input buffer piece

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM(pF)	4.90

HDL Syntax

Verilog ..... IDVX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDVX3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.630	nA
EQL_{pd}	10.4	eql

Propagation Delays

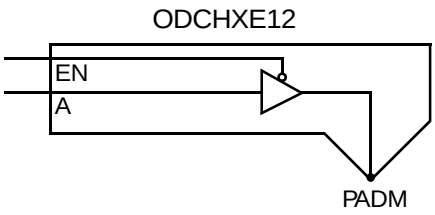
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.721 0.651	0.858 0.833	1.011 0.971	1.143 1.078	1.279 1.185

Description

ODCHXE12 is a high performance, 12 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.90 pF

HDL Syntax

Verilog ..... ODCHXE12 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE12 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	59.501	nA
EQL_{pd}	263.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.648 1.555	2.715 2.355	4.234 3.494	7.290 5.783	10.369 8.089
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.119 1.245 1.389 1.526	2.437 2.343	3.986 3.501	7.081 5.804	10.105 8.096

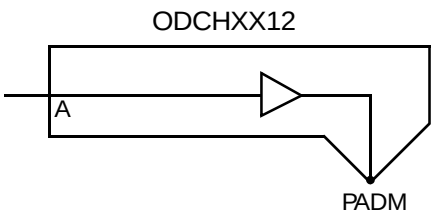
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODCHXX12 is a high performance, 12 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog ..... ODCHXX12 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXX12 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.517	nA
EQL_{pd}	216.6	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

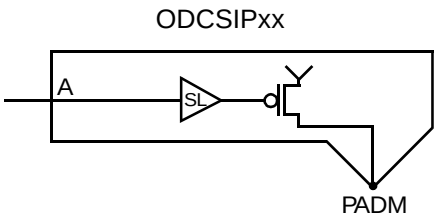
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.954	2.018	3.535	6.591	9.669
		t_{PHL}	1.072	1.863	2.988	5.279	7.606

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCSIPxx is a family of 4 to 12 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSIP04	ODCSIP08	ODCSIP12
A (eq-load)	4.1	4.1	4.1
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	56.824	198.7
ODCSIP08	8	56.824	211.8
ODCSIP12	12	56.824	219.2

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	3.833	9.167	16.769	31.979	47.208
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.510	5.198	9.015	16.743	24.433
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.218	4.390	7.451	13.567	19.728

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

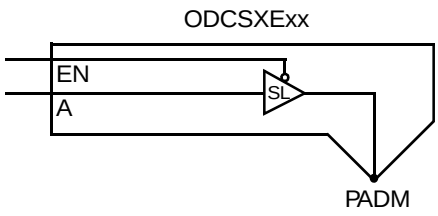
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns)		Parameter	Cell		
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**
A	PADM	t_{HZ}	0.899	1.107	1.226

Description

ODCSXExx is a family of 4 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSXE04	ODCSXE08	ODCSXE12
A (eq-load)	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	58.395	227.1
ODCSXE08	8	58.395	247.8
ODCSXE12	12	58.395	262.0

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	4.541 4.178	9.915 8.978	17.616 15.756	32.583 29.374	46.954 43.118
	From: EN To: PADM	t_{ZH} t_{ZL}	3.991 3.890	9.466 8.649	17.172 15.503	32.072 29.198	46.531 42.818
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	2.870 2.997	5.547 5.405	9.427 8.852	17.170 15.769	24.828 22.705
	From: EN To: PADM	t_{ZH} t_{ZL}	2.810 2.687	5.512 5.151	9.383 8.634	17.099 15.552	24.783 22.500
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	2.987 2.640	5.147 4.287	8.208 6.577	14.337 11.150	20.488 15.778
	From: EN To: PADM	t_{ZH} t_{ZL}	2.626 2.354	4.787 4.012	7.854 6.301	13.985 10.869	20.128 15.510

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

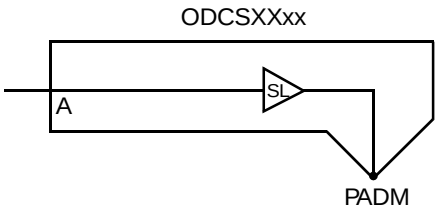
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12
EN	PADM	t_{HZ} t_{LZ}	0.957 1.176	1.166 1.332	1.284 1.465

Description

ODCSXXxx is a family of 4 to 12 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSXX04	ODCSXX08	ODCSXX12
A (eq-load)	9.3	9.3	9.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	54.738	206.8
ODCSXX08	8	54.738	227.5
ODCSXX12	12	54.738	241.7

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

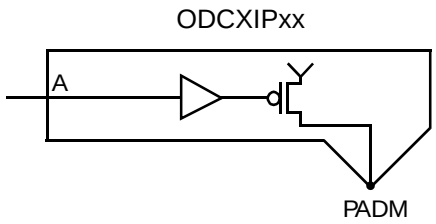
ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	3.265	8.669	16.296	31.000	45.222
	To: PADM	t_{PHL}	3.164	7.909	14.798	28.504	42.071
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	2.116	4.746	8.610	16.334	23.985
	To: PADM	t_{PHL}	2.083	4.439	7.906	14.879	21.763
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.911	4.029	7.069	13.194	19.359
	To: PADM	t_{PHL}	1.709	3.296	5.623	10.242	14.786

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCXIPxx is a family of 1 to 12 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
A (eq-load)	2.8	2.8	2.8	3.9	3.9
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	46.245	158.6
ODCXIP02	2	46.764	163.4
ODCXIP04	4	47.309	172.7
ODCXIP08	8	48.374	188.7
ODCXIP12	12	49.438	198.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXIP01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{ZH}	6.676	9.841	12.971	17.584	25.097

AMI500HXPS 0.5 micron CMOS Pad Library

ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	3.684	8.992	12.789	16.590	24.205
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.426	5.089	8.873	16.445	24.040
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.700	3.077	5.021	8.875	12.703
ODCXIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.626	2.770	4.315	7.366	12.703

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

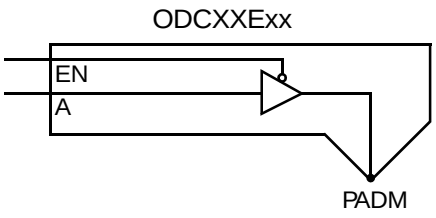
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**	**ODCXIP12**
APADM		t_{HZ}	1.125	0.999	1.198	1.410	1.420

Description

ODCXXExx is a family of 1 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
A (eq-load)	5.6	7.9	7.9	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	47.619	164.6
ODCXXE02	2	49.110	174.0
ODCXXE04	4	49.110	185.5
ODCXXE08	8	55.615	232.0
ODCXXE12	12	55.615	246.7

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	6.577 6.416	9.663 9.178	12.752 11.922	17.366 16.004	24.985 22.847
	From: EN To: PADM	t_{ZH} t_{ZL}	6.795 6.366	9.880 9.202	12.963 11.918	17.578 15.946	25.240 22.855
ODCXXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	3.512 3.377	8.880 8.217	12.693 11.666	16.496 15.086	24.080 21.848
	From: EN To: PADM	t_{ZH} t_{ZL}	3.689 3.615	9.158 8.288	12.993 11.722	16.790 15.153	24.305 21.955
ODCXXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.466 2.415	5.059 4.824	8.797 8.221	16.425 15.040	23.969 21.900
	From: EN To: PADM	t_{ZH} t_{ZL}	2.434 2.401	5.105 4.791	8.901 8.248	16.481 15.130	24.062 21.902
ODCXXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.493 2.118	3.871 3.334	5.795 5.071	9.636 8.542	13.493 12.011
	From: EN To: PADM	t_{ZH} t_{ZL}	2.133 1.904	3.503 3.128	5.414 4.864	9.250 8.331	13.121 11.799
ODCXXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.459 1.929	3.604 2.779	5.146 3.953	8.192 6.260	11.278 8.542
	From: EN To: PADM	t_{ZH} t_{ZL}	2.165 1.782	3.260 2.655	4.729 3.836	7.759 6.142	10.916 8.435

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

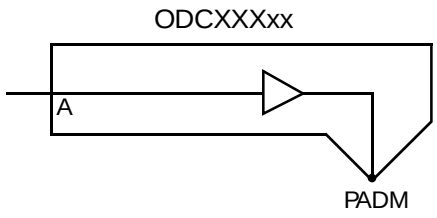
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
EN	PADM	t_{HZ} t_{LZ}	1.630 0.514	1.378 0.457	1.852 0.612	1.256 1.262	1.419 1.460

Description

ODCXXXxx is a family of 1 to 12 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12
A (eq-load)	4.3	4.3	6.2	8.3	8.2

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	46.179	159.3
ODCXXX02	2	46.179	164.8
ODCXXX04	4	47.216	176.3
ODCXXX08	8	48.303	198.8
ODCXXX12	12	48.303	213.5

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

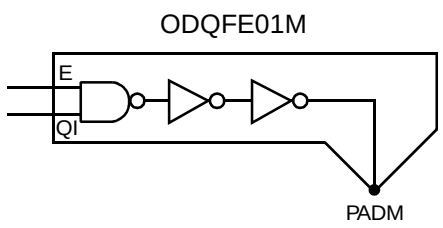
ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	6.354 5.866	9.415 8.738	12.470 11.544	17.059 15.647	24.747 22.285
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.605 3.268	8.894 8.023	12.704 11.425	16.516 14.840	24.114 21.701
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.069 2.090	4.720 4.463	8.531 7.905	16.129 14.753	23.682 21.525
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.280 1.514	2.880 2.751	4.868 4.515	8.645 8.003	12.548 11.434
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To PADM	t_{PLH} t_{PHL}	1.547 1.445	2.592 2.273	4.071 3.345	7.056 5.453	10.066 7.572

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

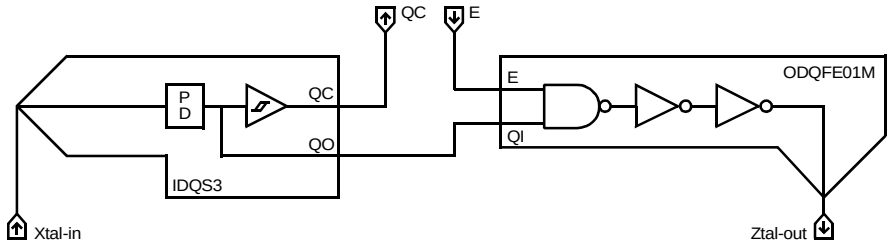
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	4.0 eql
QI	3.2 eql

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.039	nA
EQL_{pd}	161.5	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	6.965 7.304	10.095 10.028	13.178 12.752	17.745 16.847	25.248 23.697
QI	PADM	t_{PLH} t_{PHL}	7.002 7.549	10.066 10.288	13.130 13.027	17.726 17.129	25.398 23.947

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

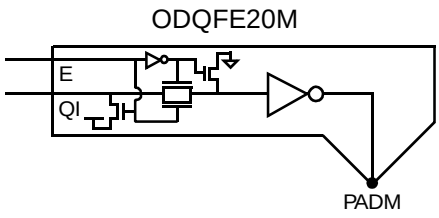
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

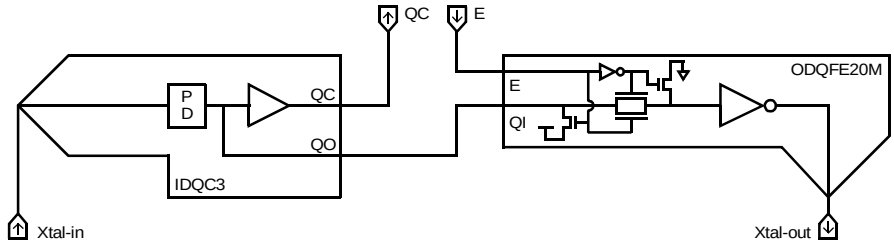
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	46.401	nA
EQL_{pd}	175.2	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	4.655 3.246	10.034 8.030	13.867 11.452	17.675 14.871	25.222 21.692
QI	PADM	t_{PLH} t_{PHL}	3.328 3.165	8.644 8.082	12.442 11.480	16.241 14.856	23.840 21.725

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

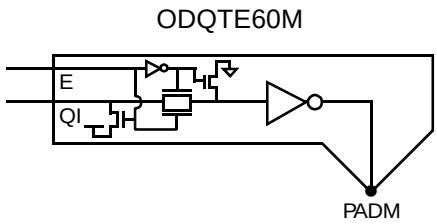
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

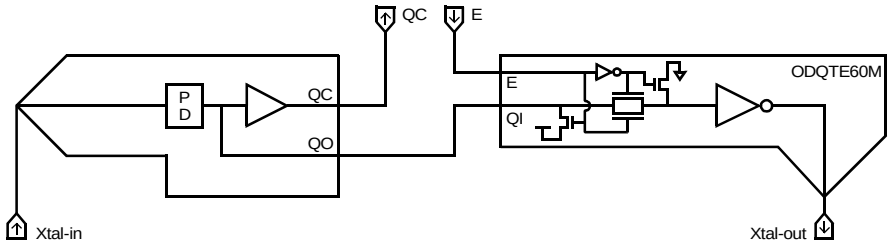
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	46.401	nA
EQL_{pd}	186.8	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	3.677 2.101	6.364 4.494	10.165 7.907	17.744 14.734	25.321 21.568
QI	PADM	t_{PLH} t_{PHL}	2.022 2.178	4.722 4.568	8.536 7.967	16.100 14.802	23.615 21.609

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

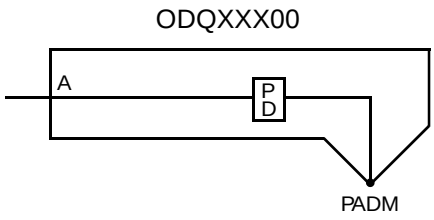
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.4 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

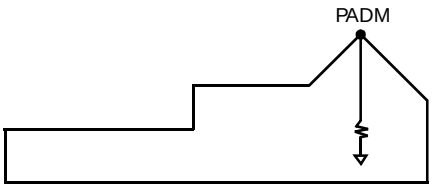
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	45.048	nA
EQL_{pd}	148.8	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLD3  	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

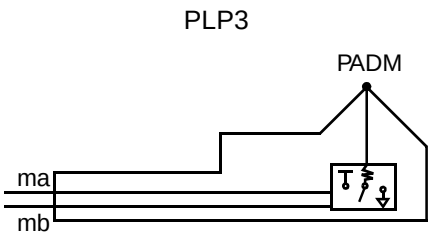
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.883	nA
EQL_{pd}	149.6	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.1 eql
MB	1.8 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.883	nA
EQL_{pd}	146.6	Eq-load

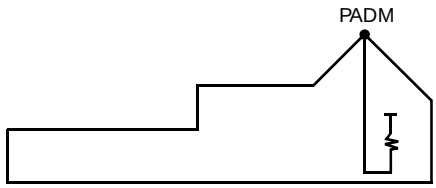
See page 2-13 for power equation.

PLU3

AMI500HXPS 0.5 micron CMOS Pad Library

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3  	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

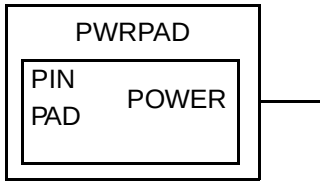
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.892	nA
EQL_{pd}	149.5	Eq-load

See page 2-13 for power equation.

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

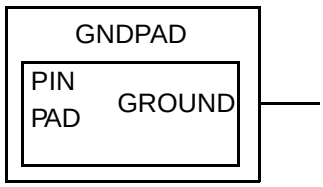
- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

GNDPAD

AMI500HXPS 0.5 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
          port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

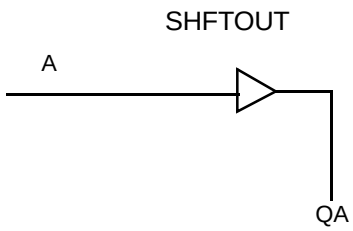
where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	4.1

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	12.309	nA
EQL_{pd}	8.3	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.28 0.21	0.33 0.23	0.40 0.27	0.48 0.31	0.54 0.34

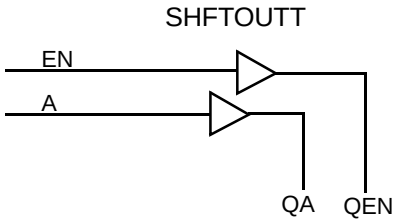
SHFTOUTT

AMI500HXPS 0.5 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	3.0
EN(eql)	3.2

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.217	nA
EQL_{pd}	10.6	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	6	8 (max)
A	QA	t_{PLH} t_{PHL}	0.34 0.24	0.38 0.26	0.46 0.31	0.54 0.35	0.63 0.40
EN	QEN	t_{PLH} t_{PHL}	0.35 0.24	0.39 0.27	0.48 0.32	0.56 0.36	0.65 0.40