0.5 Micron CMOS Pad Library Datasheets
AMI500HXPS 5.0 Volt
Section 4
Revision 1.1

Input Drive Pieces

Pull Pieces

Output Drive Pieces

Selection Guide

AMI500HXPS 0.5 micron CMOS Pad Library

Power Pad Cells

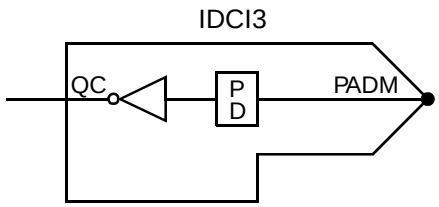
Special Pad Cells

DATASHEETS

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	16.522	nA
EQL_{pd}	12.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.602 0.795	0.728 0.918	0.811 1.029	0.873 1.129	0.931 1.241

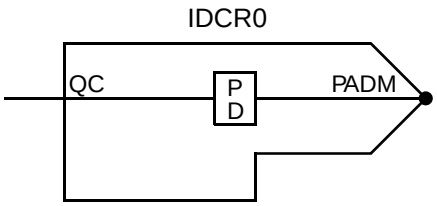
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.265	nA
EQL_{pd}	2.1	Eq-load

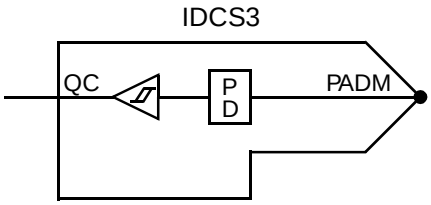
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCS3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.963	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.547 0.969	1.699 1.162	1.774 1.305	1.823 1.407	1.867 1.503

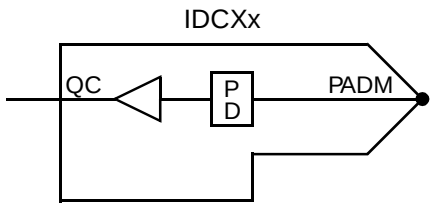
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	0.0	15.832	10.4
IDCX6	0.0	18.757	18.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

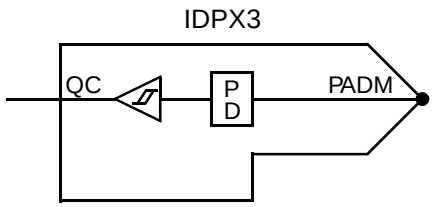
	Number of Equivalent Loads		1	11	22	32	43 (max)
IDCX3	From: PADM To: QC	t_{PLH} t_{PHL}	0.788 0.524	0.871 0.695	0.972 0.833	1.068 0.941	1.177 1.051
	Number of Equivalent Loads		**1**	**11**	**22**	**32**	**43 (max)**
IDCX6	From: PADM To: QC	t_{PLH} t_{PHL}	0.683 0.565	0.732 0.653	0.787 0.715	0.838 0.770	0.895 0.830

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load
	IDPX3
PADM (pF)	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	0.0	15.774	12.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
IDPX3	From: PADM	t_{PLH}	0.627	0.793	0.916	1.011	1.105
	To: QC	t_{PHL}	0.702	0.852	0.964	1.050	1.135

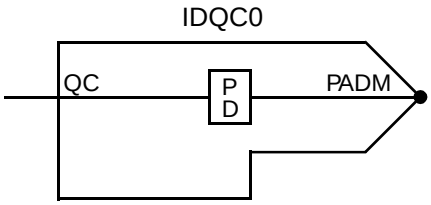
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);
VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.265	nA
EQL_{pd}	2.1	Eq-load

See page 2-13 for power equation.

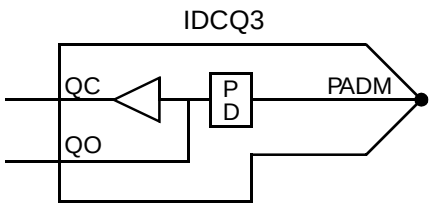
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

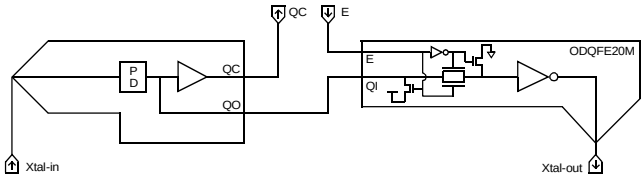
Description

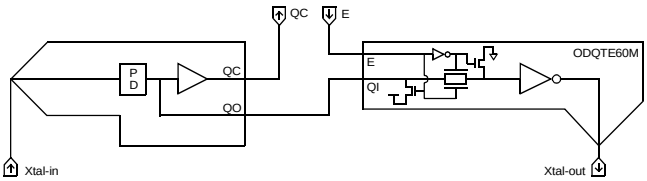
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.90 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.832	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

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Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.813 0.563	0.880 0.723	0.970 0.846	1.060 0.944	1.165 1.043
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

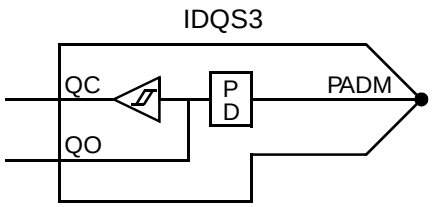
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

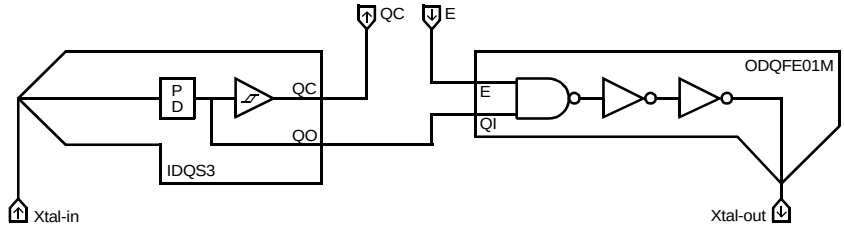
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load	
PADM	4.90	pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.963	nA
EQL_{pd}	18.0	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.551 1.018	1.616 1.159	1.705 1.278	1.796 1.372	1.902 1.465
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

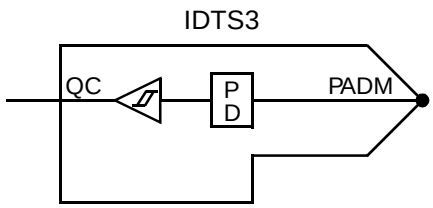
Design Notes:

The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

Description

IDTS3 is a non-inverting, TTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDTS3 inst_IDTS3 (QC, PADM);
VHDL..... inst_IDTS3 : IDTS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.451	nA
EQL_{pd}	15.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.962 1.640	1.062 1.829	1.166 2.014	1.256 2.171	1.354 2.336

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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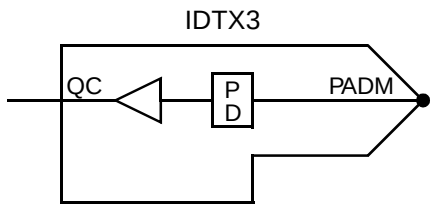
Description

IDTXx is a family of non-inverting, TTL-level, input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDTXx *inst_name (*QC, PADM);
VHDL..... *inst_name*: IDTXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDTX3	IDTX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDTX3	0.0	15.349	10.4
IDTX6	0.0	17.792	18.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

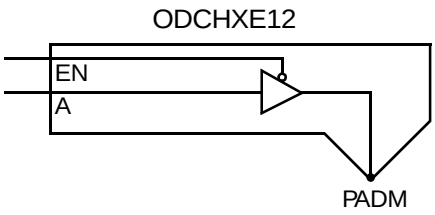
IDTX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t_{PLH}	0.573	0.718	0.823	0.917	1.026
	To: QC	t_{PHL}	0.662	0.860	0.986	1.078	1.166
IDTX6	Number of Equivalent Loads		1	21	42	62	83 (max)
	From: PADM	t_{PLH}	0.495	0.661	0.770	0.857	0.938
	To: QC	t_{PHL}	0.634	0.818	0.937	1.037	1.135

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCHXE12 is a high performance, 12 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.73 pF

HDL Syntax

Verilog ..... ODCHXE12 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE12 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	59.501	nA
EQL_{pd}	259.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.064 0.064 0.000 0.000	 0.000 0.000	 0.000 0.000	 0.000 0.000	 0.000 0.000

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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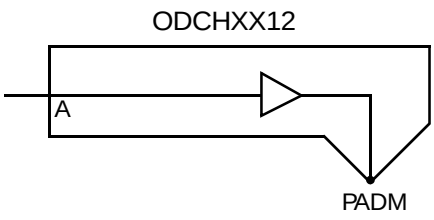
Description

ODCHXX12 is a high performance, 12 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog ..... ODCHXX12 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXX12 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.517	nA
EQL_{pd}	216.6	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

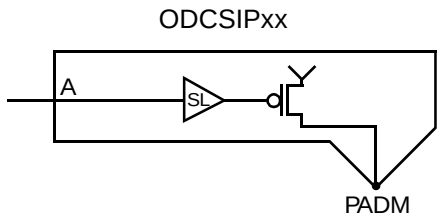
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.708	1.513	2.653	4.924	7.191
		t_{PHL}	0.778	1.470	2.462	4.437	6.395

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCSIPxx is a family of 4 to 12 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSIP04	ODCSIP08	ODCSIP12
A (eq-load)	4.1	4.1	4.1
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	56.824	198.7
ODCSIP08	8	56.824	211.8
ODCSIP12	12	56.824	219.2

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.444	6.591	12.223	23.247	34.434
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.759	3.800	6.642	12.269	17.930
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.754	3.265	5.450	9.928	14.494

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

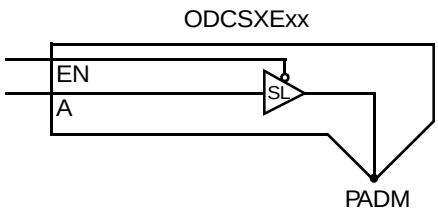
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Cell		
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**
A	PADM	t_{HZ}	0.787	1.011	1.142

Description

ODCSXExx is a family of 4 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSXE04	ODCSXE08	ODCSXE12
A (eq-load)	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	58.395	227.1
ODCSXE08	8	58.395	247.8
ODCSXE12	12	58.395	262.0

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	3.318 3.299	7.321 7.414	12.855 13.262	23.637 24.910	34.209 36.522
	From: EN To: PADM	t_{ZH} t_{ZL}	2.930 3.219	6.879 7.240	12.497 12.976	23.365 24.602	33.841 36.372
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	2.407 2.326	4.389 4.417	7.216 7.399	12.864 13.359	18.508 19.326
	From: EN To: PADM	t_{ZH} t_{ZL}	2.076 1.987	4.072 4.176	6.920 7.184	12.574 13.120	18.193 19.106
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	2.234 2.150	3.820 3.534	6.078 5.497	10.577 9.439	15.065 13.398
	From: EN To: PADM	t_{ZH} t_{ZL}	1.797 1.970	3.489 3.189	5.763 5.152	10.225 9.117	14.746 13.047

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

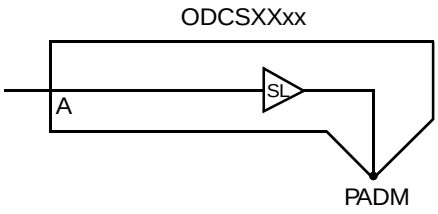
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12
EN	PADM	t_{HZ} t_{LZ}	0.825 0.914	1.051 1.082	1.180 1.229

Description

ODCSXXxx is a family of 4 to 12 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSXX04	ODCSXX08	ODCSXX12
A (eq-load)	9.3	9.3	9.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	54.738	206.8
ODCSXX08	8	54.738	227.5
ODCSXX12	12	54.738	241.7

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

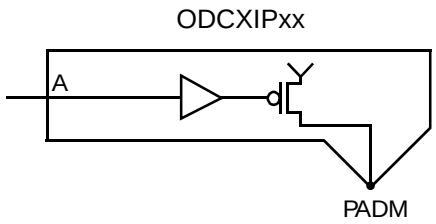
ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.506 2.731	6.388 6.772	11.894 12.584	22.615 24.242	32.966 35.895
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.593 1.719	3.544 3.789	6.341 6.755	11.947 12.699	17.564 18.653
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.536 1.364	3.071 2.770	5.272 4.739	9.728 8.654	14.250 12.610

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCXIPxx is a family of 1 to 12 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
A (eq-load)	2.8	2.8	2.8	3.9	3.9
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	46.245	158.6
ODCXIP02	2	46.764	163.4
ODCXIP04	4	47.309	172.7
ODCXIP08	8	48.374	188.7
ODCXIP12	12	49.438	198.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXIP01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{ZH}	4.792	7.018	9.250	12.605	18.208

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ODCXIP02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{ZH}	2.752	6.634	9.391	12.160	17.751
ODCXIP04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.748	3.690	6.473	12.023	17.547
ODCXIP08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.278	2.311	3.747	6.575	9.372
ODCXIP12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZH}	1.198	2.058	3.236	5.500	9.372

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

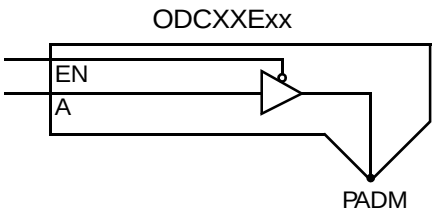
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
APADM		t_{HZ}	0.963	0.874	1.089	1.382	1.444

Description

ODCXXExx is a family of 1 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
A (eq-load)	5.6	7.9	7.9	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	37.149	20.1
ODCXXE02	2	49.110	174.0
ODCXXE04	4	49.110	185.5
ODCXXE08	8	55.615	232.0
ODCXXE12	12	55.615	246.7

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	4.754 5.210	7.026 7.471	9.282 9.760	12.637 13.249	18.169 19.186
	From: EN To: PADM	t_{ZH} t_{ZL}	4.938 5.224	7.236 7.550	9.504 9.877	12.857 13.370	18.356 19.207
ODCXXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.556 2.779	6.441 6.861	9.221 9.776	12.000 12.690	17.551 18.518
	From: EN To: PADM	t_{ZH} t_{ZL}	2.705 2.818	6.646 6.827	9.466 9.727	12.254 12.645	17.726 18.519
ODCXXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.720 1.831	3.690 3.880	6.474 6.813	12.017 12.656	17.551 18.463
	From: EN To: PADM	t_{ZH} t_{ZL}	1.830 1.836	3.832 3.908	6.658 6.839	12.212 12.672	17.689 18.487
ODCXXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.934 1.654	2.913 2.698	4.306 4.186	7.124 7.159	9.966 10.143
	From: EN To: PADM	t_{ZH} t_{ZL}	1.597 1.463	2.584 2.530	3.991 4.012	6.812 6.982	9.638 9.985
ODCXXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.990 1.614	2.778 2.335	3.898 3.300	6.147 5.248	8.404 7.255
	From: EN To: PADM	t_{ZH} t_{ZL}	1.473 1.344	2.323 2.092	3.477 3.115	5.731 5.102	7.963 7.049

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

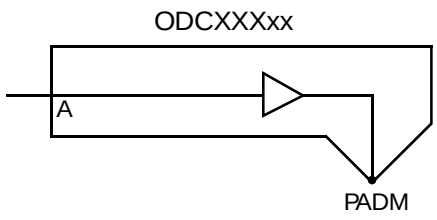
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
EN	PADM	t_{HZ} t_{LZ}	1.368 0.447	1.181 0.413	1.633 0.580	1.241 1.098	1.435 1.330

Description

ODCXXXxx is a family of 1 to 12 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12
A (eq-load)	4.3	3.7	5.0	6.5	8.2

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	46.179	159.3
ODCXXX02	2	46.179	161.9
ODCXXX04	4	47.216	170.4
ODCXXX08	8	48.303	187.0
ODCXXX12	12	48.303	213.5

a. See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

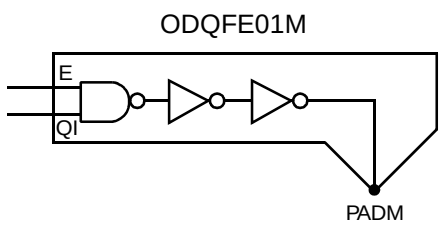
ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.601 4.928	6.825 7.268	9.054 9.587	12.403 13.053	17.995 18.884
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.549 2.872	6.430 6.940	9.236 9.849	12.030 12.761	17.535 18.593
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.499 1.733	3.429 3.753	6.207 6.651	11.764 12.471	17.283 18.312
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.174 1.283	2.191 2.304	3.627 3.773	6.459 6.754	9.255 9.724
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To PADM	t_{PLH} t_{PHL}	1.144 1.217	1.952 1.848	3.054 2.728	5.188 4.520	7.356 6.275

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

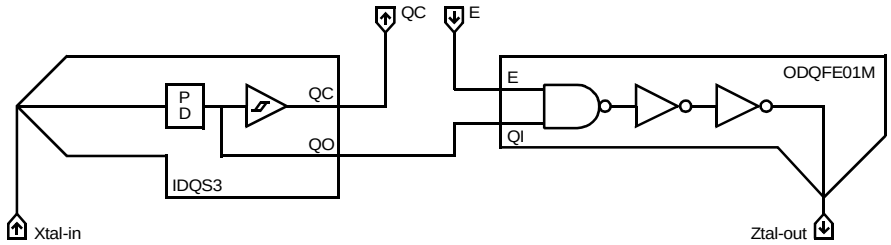
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	3.5 eql
QI	3.1 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.039	nA
EQL_{pd}	159.7	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	4.951 5.899	7.170 8.211	9.398 10.520	12.753 14.003	18.369 19.875
QI	PADM	t_{PLH} t_{PHL}	5.082 5.981	7.299 8.314	9.499 10.652	12.819 14.155	18.472 19.967

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

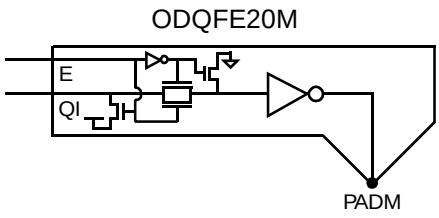
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

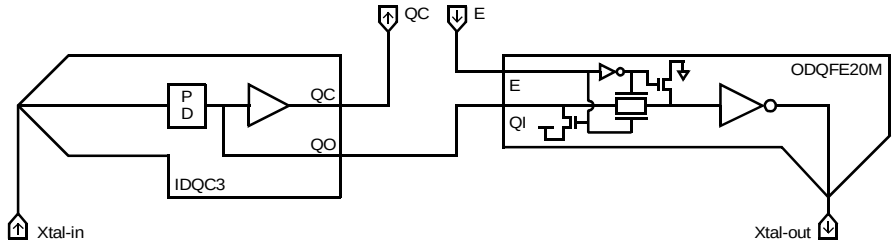
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	5.3 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	46.401	nA
EQL_{pd}	170.8	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	3.458 2.637	7.343 6.711	10.118 9.613	12.894 12.520	18.450 18.369
QI	PADM	t_{PLH} t_{PHL}	2.414 2.714	6.330 6.786	9.106 9.687	11.871 12.593	17.379 18.421

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

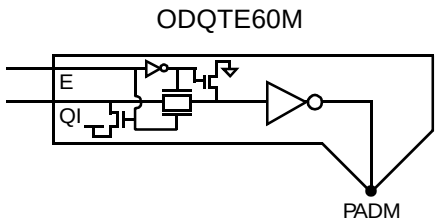
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

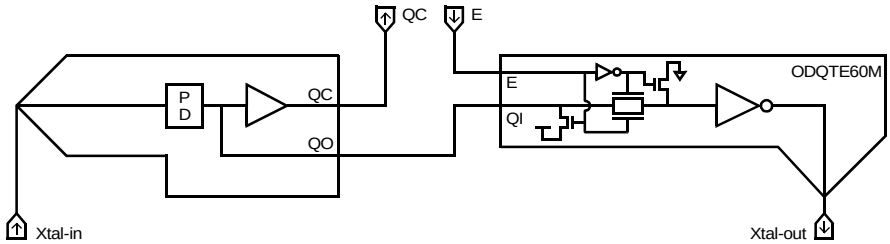
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	5.3 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	46.401	nA
EQL_{pd}	179.5	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	2.700 1.704	4.705 3.707	7.491 6.597	13.007 12.423	18.563 18.284
QI	PADM	t_{PLH} t_{PHL}	1.445 1.721	3.486 3.803	6.272 6.701	11.759 12.493	17.310 18.343

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

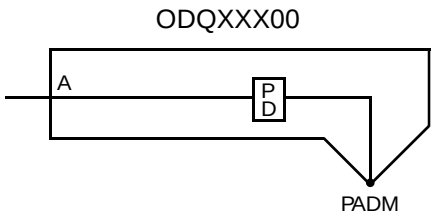
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.4 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	45.048	nA
EQL_{pd}	148.8	Eq-load

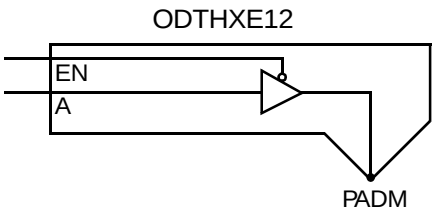
See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTHXE12 is a high performance, 12 mA, non-inverting, LVTTL-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.90 pF

HDL Syntax

Verilog ..... ODTHXE12 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTHXE12 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	59.501	nA
EQL_{pd}	263.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

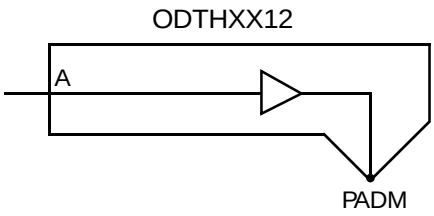
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.964 1.582	1.380 2.500	1.981 4.055	3.194 7.250	4.416 10.395
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.929 0.941 0.788 1.446	1.221 2.493	1.822 4.062	3.028 7.252	4.249 10.412

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODTHXX12 is a high performance,12 mA, non-inverting, LVTTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog ..... ODTHXX12 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTHXX12 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.517	nA
EQL_{pd}	216.6	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.516 1.042	0.942 2.158	1.551 3.727	2.761 6.876	3.958 10.068

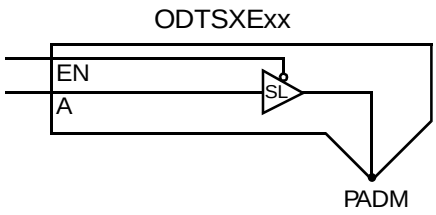
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTSXExx is a family of 4 to 12 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODTSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODTSXE**04**	ODTSXE**08**	ODTSXE**12**
A (eq-load)	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXE**04**	4	58.395	227.1
ODTSXE**08**	8	58.395	247.8
ODTSXE**12**	12	58.395	262.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODTSXE**04**	From: A To: PADM	t_{PLH} t_{PHL}	2.457 4.724	4.509 10.910	7.440 19.331	13.424 35.806	19.517 52.288
	From: EN To: PADM	t_{ZH} t_{ZL}	1.998 4.854	4.103 10.798	7.098 19.063	13.098 35.664	19.116 52.049
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE**08**	From: A To: PADM	t_{PLH} t_{PHL}	1.916 3.141	3.002 6.486	4.516 10.986	7.552 19.692	10.621 28.228
	From: EN To: PADM	t_{ZH} t_{ZL}	1.536 2.736	2.648 6.203	4.162 10.776	7.169 19.452	10.260 27.996
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE**12**	From: A To: PADM	t_{PLH} t_{PHL}	1.805 2.486	2.692 4.675	3.932 7.838	6.345 13.877	8.783 19.412
	From: EN To: PADM	t_{ZH} t_{ZL}	1.557 2.222	2.371 4.530	3.555 7.657	5.975 13.584	8.436 19.264

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

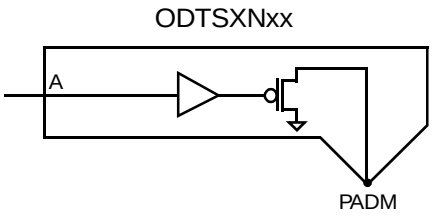
Delay (ns) From	To	Parameter	Cell ODTSXE**04**	ODTSXE**08**	ODTSXE**12**
EN	PADM	t_{HZ} t_{LZ}	0.825 0.914	1.051 1.082	1.180 1.229

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTSXNxx is a family of 4 to 12 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODTSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODTSXN**04**	ODTSXN**08**	ODTSXN**12**
A (eq-load)	8.1	8.1	8.1
PADM (pF)	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXN**04**	4	51.481	175.6
ODTSXN**08**	8	51.481	183.2
ODTSXN**12**	12	51.481	190.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODTSXN**04**	From: A To: PADM	t_{ZL}	3.612	9.523	17.805	34.107	50.214

ODTSXN**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.405	5.407	9.648	18.110	26.559
ODTSXN**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.643	3.809	6.700	12.319	17.893

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

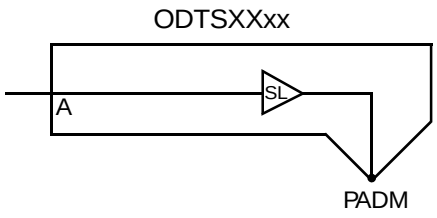
Delay (ns) From	To	Parameter	Cell		
			ODTSXN**04**	ODTSXN**08**	ODTSXN**12**
A	PADM	t_{LZ}	0.844	0.959	1.066

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTSXXxx is a family of 4 to 12 mA, non-inverting, LVTTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODTSXXxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODTSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODTSXX**04**	ODTSXX**08**	ODTSXX**12**
A (eq-load)	9.3	9.3	9.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXX**04**	4	54.738	206.8
ODTSXX**08**	8	54.738	227.5
ODTSXX**12**	12	54.738	241.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

ODTSXX**04**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.492 4.032	3.555 10.055	6.574 18.434	12.599 34.926	18.563 51.255
ODTSXX**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	0.999 2.503	2.088 5.772	3.633 10.191	6.677 18.790	9.684 27.319
ODTSXX**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.272 1.919	1.890 4.130	3.054 7.163	5.506 12.984	7.890 18.615

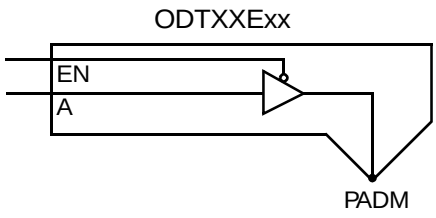
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTXXExx is a family of 1 to 12 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODTXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODTXXE**01**	ODTXXE**02**	ODTXXE**04**	ODTXXE**08**	ODTXXE**12**
A (eq-load)	5.6	7.9	7.9	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXE**01**	1	47.619	164.6
ODTXXE**02**	2	49.110	174.0
ODTXXE**04**	4	49.110	185.5
ODTXXE**08**	8	55.615	232.0
ODTXXE**12**	12	55.615	246.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

ODTXXE**01**	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.789 7.761	4.059 11.472	5.298 15.187	7.111 20.761	10.049 30.058
	From: EN To: PADM	t_{ZH} t_{ZL}	2.999 7.677	4.191 11.437	5.361 15.188	7.137 20.775	10.233 29.981
ODTXXE**02**	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.645 4.089	3.723 10.608	5.200 15.261	6.697 19.906	9.752 29.173
	From: EN To: PADM	t_{ZH} t_{ZL}	1.856 4.167	3.933 10.660	5.438 15.300	6.947 19.943	9.941 29.241
ODTXXE**04**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.250 2.526	2.308 5.789	3.798 10.432	6.791 19.716	9.799 29.008
	From: EN To: PADM	t_{ZH} t_{ZL}	1.383 2.505	2.492 5.769	3.986 10.412	6.951 19.717	9.981 29.053
ODTXXE**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.502 2.055	2.116 3.704	2.932 6.099	4.469 10.920	5.937 15.732
	From: EN To: PADM	t_{ZH} t_{ZL}	1.191 1.706	1.780 3.470	2.570 5.893	4.102 10.699	5.606 15.531
ODTXXE**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.589 1.860	2.082 2.961	2.742 4.567	3.985 7.764	5.166 10.900
	From: EN To: PADM	t_{ZH} t_{ZL}	1.304 1.652	1.794 2.804	2.406 4.379	3.620 7.542	4.858 10.747

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

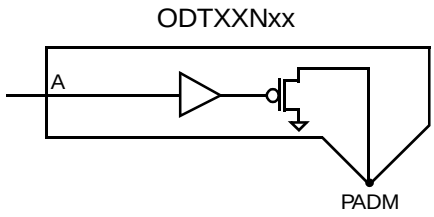
Delay (ns) From	To	Parameter	Cell				
			ODTXXE**01**	ODTXXE**02**	ODTXXE**04**	ODTXXE**08**	ODTXXE**12**
EN	PADM	t_{HZ} t_{LZ}	1.368 0.447	1.181 0.413	1.633 0.580	1.241 1.098	1.435 1.330

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTXXNxx is a family of 1 to 12 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODTXXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTXXN**01**	ODTXXN**02**	ODTXXN**04**	ODTXXN**08**	ODTXXN**12**
A (eq-load)	4.3	4.3	4.3	8.3	8.3
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXN**01**	1	46.168	153.0
ODTXXN**02**	2	46.168	154.9
ODTXXN**04**	4	46.168	158.9
ODTXXN**08**	8	48.292	167.4
ODTXXN**12**	12	48.292	174.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

ODTXXN**01**	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{ZL}	6.683	10.064	13.445	18.487	26.806

ODTXXN**02**	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZL}	3.507	9.368	13.551	17.739	26.133
ODTXXN**04**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.027	4.975	9.162	17.540	25.919
ODTXXN**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.208	2.732	4.882	9.165	13.443
ODTXXN**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.034	2.067	3.512	6.354	9.160

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

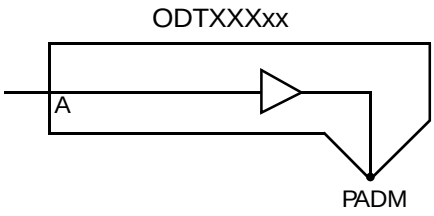
Delay (ns) From	To	Parameter	Cell				
			ODTXXN**01**	ODTXXN**02**	ODTXXN**04**	ODTXXN**08**	ODTXXN**12**
A	PADM	t_{LZ}	0.246	0.337	0.516	0.568	0.784

AMI500HXPS 0.5 micron CMOS Pad Library

Description

ODTXXXxx is a family of 1 to 12 mA, non-inverting, LVTTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODTXXXxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODTXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTXXX**01**	ODTXXX**02**	ODTXXX**04**	ODTXXX**08**	ODTXXX**12**
A (eq-load)	4.3	4.3	6.2	8.3	8.2

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXX**01**	1	46.179	159.3
ODTXXX**02**	2	46.179	164.8
ODTXXX**04**	4	47.216	176.3
ODTXXX**08**	8	48.303	198.8
ODTXXX**12**	12	48.303	213.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXX**01**	From: A	t_{PLH}	2.614	3.815	5.001	6.790	9.853
	To: PADM	t_{PHL}	7.546	11.250	14.965	20.542	29.823

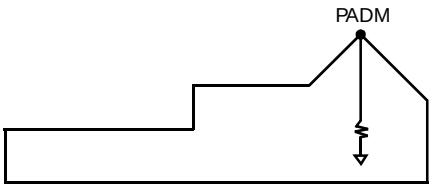
ODTXXX**02**	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.632 4.198	3.729 10.680	5.212 15.322	6.705 19.970	9.737 29.279
ODTXXX**04**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.065 2.388	2.116 5.610	3.608 10.252	6.605 19.555	9.596 28.823
ODTXXX**08**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.855 1.641	1.461 3.316	2.243 5.720	3.761 10.532	5.288 15.340
ODTXXX**12**	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.905 1.354	1.365 2.381	1.970 3.836	3.136 6.683	4.277 9.473

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLD3  	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);
VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

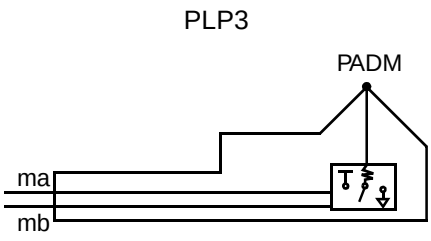
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.883	nA
EQL_{pd}	149.6	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.1 eql
MB	1.8 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

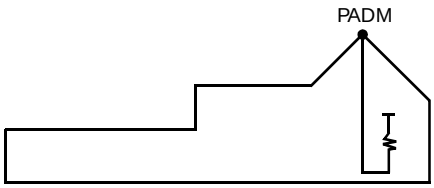
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.883	nA
EQL_{pd}	146.6	Eq-load

See page 2-13 for power equation.

AMI500HXPS 0.5 micron CMOS Pad Library

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3  	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

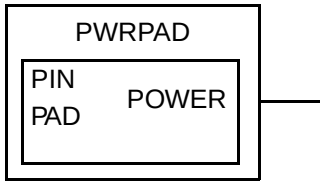
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.892	nA
EQL_{pd}	149.5	Eq-load

See page 2-13 for power equation.

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

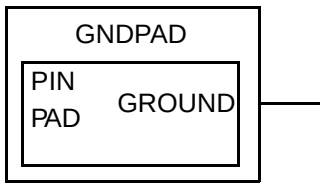
- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

GNDPAD

AMI500HXPS 0.5 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
          port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

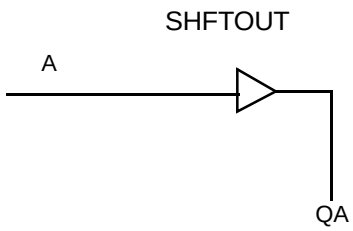
where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 3.3V core to a 5.0V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	4.1

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	12.309	nA
EQL_{pd}	8.3	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.274 0.252	0.309 0.289	0.352 0.345	0.407 0.418	0.450 0.472

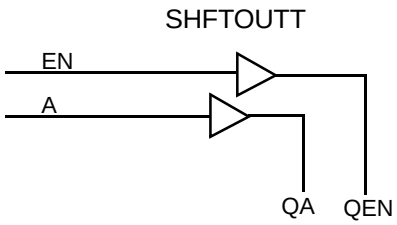
SHFTOUTT

AMI500HXPS 0.5 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 3.3V core to a 5.0V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	3.0
EN(eql)	3.2

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.217	nA
EQL_{pd}	10.6	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	6	8 (max)
A	QA	t_{PLH} t_{PHL}	0.292 0.290	0.321 0.331	0.374 0.411	0.427 0.489	0.484 0.567
EN	QEN	t_{PLH} t_{PHL}	0.294 0.303	0.327 0.345	0.390 0.423	0.448 0.497	0.503 0.568