0.5 Micron CMOS Core Library
Standard Cell Datasheets
AMI500SXSC 5.0 Volt
Section 3
Revision 1.1

Simple Gates

Complex Gates

Core Selection Guide

AMI500SXSC 0.5 micron CMOS Standard Cell

Complex Gates (cont)

Inverting Drivers

Internal 3-State Drivers

Clock Drivers

Muxes and Decoders

Sequential Logic

Sequential Logic (cont)

Power Cells

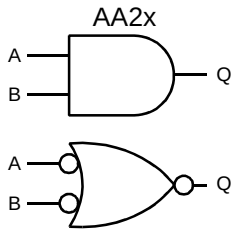
Special Core Cells

DATASHEETS

Description

AA2x is a family of 2-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... AA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: AA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	AA21	AA22	AA24	AA26
A	1.0	1.0	1.9	1.9
B	1.0	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA21	1.3	1.936	2.8
AA22	1.6	2.606	4.0
AA24	2.9	5.144	7.7
AA26	3.7	6.522	10.7

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

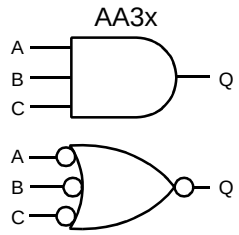
AA21	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.228 0.229	0.297 0.321	0.395 0.445	0.520 0.599	0.611 0.710
AA22	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.243 0.254	0.337 0.366	0.414 0.459	0.485 0.550	0.564 0.662
AA24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.218 0.220	0.297 0.327	0.370 0.425	0.439 0.517	0.506 0.607
AA26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.270 0.277	0.356 0.373	0.435 0.469	0.503 0.557	0.566 0.636

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA3x is a family of 3-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

HDL Syntax

Verilog ..... AA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AA31	AA32	AA34	AA36
A	1.0	1.0	2.0	2.9
B	1.0	1.0	1.9	2.9
C	1.0	1.0	1.9	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA31	1.8	2.360	3.5
AA32	2.1	3.029	4.6
AA34	4.2	6.112	10.3
AA36	5.5	9.047	14.6

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

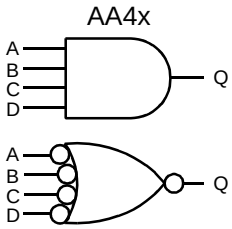
AA31	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.258 0.260	0.330 0.351	0.431 0.482	0.557 0.647	0.644 0.764
AA32	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.298 0.289	0.394 0.413	0.469 0.517	0.543 0.612	0.638 0.720
AA34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.309 0.242	0.372 0.350	0.444 0.473	0.503 0.569	0.557 0.644
AA36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.261 0.251	0.358 0.357	0.436 0.444	0.506 0.531	0.573 0.614

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA4x is a family of 4-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

HDL Syntax

Verilog ..... AA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AA41	AA42	AA44	AA46
A	1.0	1.0	2.9	2.9
B	1.0	1.0	2.9	2.9
C	1.0	1.0	2.9	2.9
D	1.0	1.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQLpd (Eq-load)
AA41	2.1	2.697	3.9
AA42	2.4	3.367	5.0
AA44	5.5	8.672	13.6
AA46	6.1	10.033	16.5

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

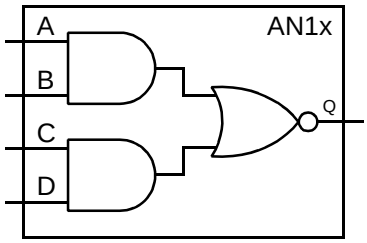
AA41	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.283 0.289	0.359 0.383	0.466 0.517	0.596 0.684	0.684 0.799
AA42	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.323 0.322	0.419 0.447	0.506 0.550	0.591 0.643	0.690 0.748
AA44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.283 0.238	0.357 0.351	0.432 0.453	0.511 0.544	0.583 0.630
AA46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.298 0.272	0.401 0.383	0.485 0.484	0.556 0.576	0.617 0.657

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN1x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

HDL Syntax

Verilog ..... AN1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN11	AN12	AN14	AN16
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN11	1.8	1.428	3.0
AN12	2.9	4.342	7.2
AN14	3.7	5.062	9.1
AN16	6.3	10.040	18.1

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

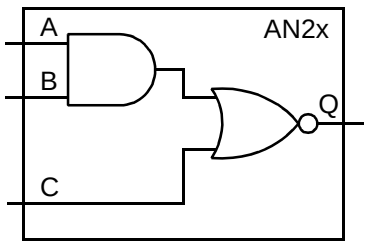
AN11	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.211 0.197	0.274 0.259	0.391 0.372	0.571 0.530	0.703 0.631
AN12	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.324 0.379	0.390 0.462	0.484 0.584	0.608 0.746	0.699 0.866
AN14	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.354 0.402	0.444 0.533	0.521 0.633	0.593 0.720	0.674 0.816
AN16	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.316 0.374	0.397 0.466	0.465 0.556	0.533 0.658	0.604 0.768

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN2x is a family of AND-NOR circuits consisting of one 2-input AND gate and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

HDL Syntax

Verilog ..... AN2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AN2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AN21	AN22	AN24	AN26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN21	1.6	1.196	2.5
AN22	2.6	3.847	6.7
AN24	3.4	4.569	8.7
AN26	5.5	8.369	16.7

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

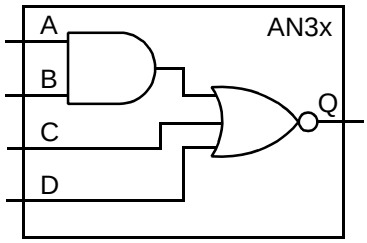
AN21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.140 0.214	0.198 0.279	0.311 0.399	0.469 0.575	0.569 0.697
AN22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.328 0.383	0.397 0.474	0.493 0.600	0.614 0.756	0.702 0.869
AN24	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.352 0.415	0.440 0.531	0.516 0.631	0.587 0.725	0.667 0.832
AN26	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.319 0.375	0.383 0.477	0.456 0.573	0.534 0.661	0.614 0.747

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN3x is a family of AND-NOR circuits consisting of one 2-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... AN3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN31	AN32	AN34	AN36
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN31	1.8	1.594	3.0
AN32	2.9	3.766	7.2
AN34	3.7	4.499	9.3
AN36	6.3	8.899	18.4

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

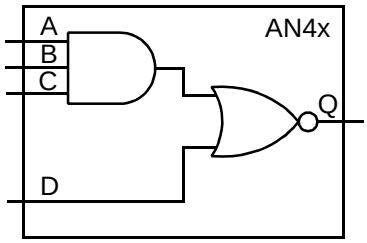
AN31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.175 0.255	0.244 0.335	0.371 0.488	0.436 0.564	0.576 0.715
AN32	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.310 0.395	0.376 0.481	0.470 0.602	0.593 0.757	0.684 0.869
AN34	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.331 0.432	0.423 0.561	0.498 0.664	0.567 0.757	0.644 0.861
AN36	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.318 0.376	0.386 0.493	0.449 0.594	0.515 0.684	0.584 0.767

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN4x is a family of AND-NOR circuits consisting of one 3-input AND gate, and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

HDL Syntax

Verilog ..... AN4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN41	AN42	AN44	AN46
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN41	1.8	1.311	3.1
AN42	2.9	4.256	7.4
AN44	4.0	4.996	9.5
AN46	6.1	9.202	18.1

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

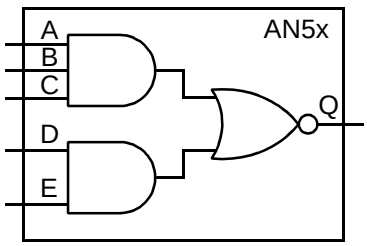
AN41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.171 0.259	0.233 0.334	0.350 0.475	0.406 0.546	0.514 0.691
AN42	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.361 0.423	0.431 0.517	0.526 0.643	0.644 0.798	0.728 0.909
AN44	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.390 0.456	0.482 0.574	0.558 0.673	0.628 0.762	0.706 0.864
AN46	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.358 0.427	0.426 0.520	0.503 0.617	0.576 0.711	0.643 0.803

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN5x is a family of AND-NOR circuits consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN52	AN54	AN56
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN52	3.2	4.753	7.9
AN54	3.7	5.459	9.3
AN56	7.4	10.933	20.3

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

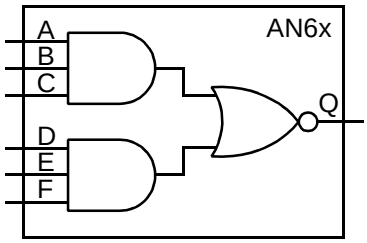
AN52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.354 0.440	0.414 0.525	0.509 0.643	0.640 0.792	0.739 0.901
AN54	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.390 0.449	0.471 0.571	0.549 0.673	0.625 0.767	0.716 0.874
AN56	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.355 0.435	0.418 0.511	0.495 0.595	0.575 0.691	0.655 0.797

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN6x is a family of AND-NOR circuits consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN62	AN64	AN66
A	1.0	1.0	1.9
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN62	3.4	5.162	8.3
AN64	4.5	5.871	9.9
AN66	7.9	11.760	21.4

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

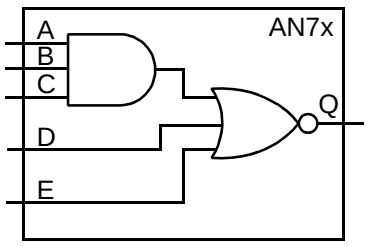
AN62	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.360 0.440	0.426 0.530	0.517 0.652	0.631 0.803	0.713 0.911
AN64	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.386 0.447	0.477 0.566	0.553 0.667	0.623 0.761	0.701 0.868
AN66	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.351 0.424	0.435 0.532	0.511 0.627	0.578 0.712	0.639 0.792

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN7x is a family of AND-NOR circuits consisting of one 3-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN72	AN74	AN76
A	1.0	1.0	1.9
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN72	3.2	4.298	7.8
AN74	3.7	5.008	9.6
AN76	7.1	9.990	20.2

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

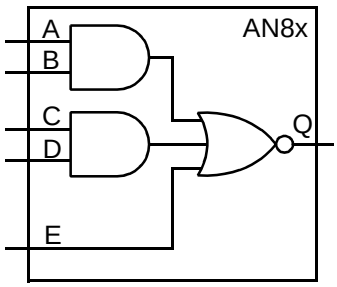
AN72	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.360 0.419	0.427 0.508	0.520 0.631	0.639 0.786	0.726 0.898
AN74	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.385 0.450	0.477 0.570	0.552 0.668	0.620 0.758	0.696 0.859
AN76	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.354 0.425	0.434 0.538	0.509 0.632	0.575 0.714	0.637 0.791

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN8x is a family of AND-NOR circuits consisting of two 2-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN82	AN84	AN86
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN82	4.0	5.472	9.6
AN84	4.5	6.160	11.4
AN86	7.9	12.294	22.7

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

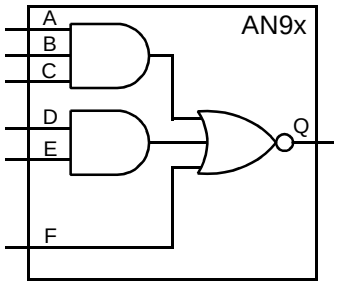
AN82	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.360 0.429	0.428 0.515	0.526 0.634	0.653 0.789	0.746 0.903
AN84	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.394 0.444	0.490 0.568	0.568 0.671	0.640 0.764	0.719 0.868
AN86	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.379 0.403	0.469 0.507	0.546 0.607	0.616 0.700	0.681 0.789

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN9x is a family of AND-NOR circuits consisting of one 3-input AND gate, one 2-input AND gate, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN92	AN94	AN96
A	1.0	1.0	1.9
B	1.0	1.0	2.0
C	1.0	1.0	1.9
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN92	4.2	5.882	10.2
AN94	4.7	6.564	11.6
AN96	9.0	13.189	24.2

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

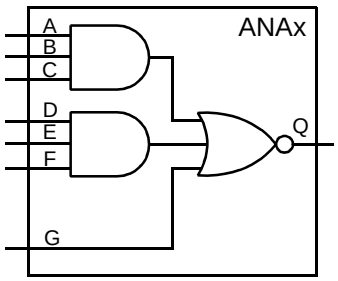
AN92	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.397 0.465	0.466 0.555	0.565 0.681	0.691 0.842	0.783 0.958
AN94	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.428 0.492	0.526 0.617	0.607 0.716	0.681 0.810	0.765 0.922
AN96	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.444 0.491	0.526 0.607	0.614 0.715	0.700 0.812	0.785 0.906

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANAx is a family of AND-NOR circuits consisting of two 3-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANAx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANA2	ANA4	ANA6
A	1.0	1.0	2.0
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANA2	4.5	6.292	10.9
ANA4	5.0	6.976	11.9
ANA6	9.8	14.068	25.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

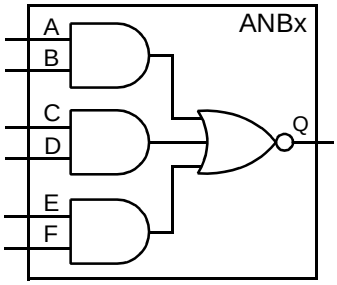
ANA2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.405 0.463	0.474 0.554	0.568 0.677	0.685 0.831	0.769 0.941
ANA4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.415 0.479	0.516 0.606	0.597 0.706	0.669 0.795	0.750 0.894
ANA6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.399 0.449	0.513 0.561	0.598 0.667	0.660 0.757	0.712 0.836

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANBx is a family of AND-NOR circuits consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... ANBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ANBx port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ANB2	ANB4	ANB6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	1.9
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANB2	4.0	5.962	10.1
ANB4	5.0	6.666	11.8
ANB6	9.0	13.355	24.6

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

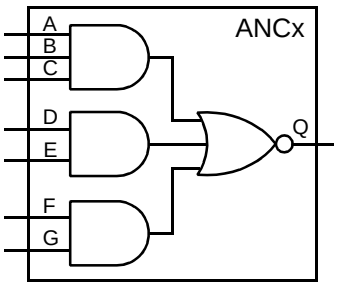
ANB2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.358 0.413	0.426 0.503	0.522 0.630	0.646 0.790	0.737 0.907
ANB4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.397 0.441	0.490 0.558	0.568 0.659	0.640 0.753	0.722 0.861
ANB6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.362 0.409	0.466 0.526	0.548 0.626	0.619 0.708	0.683 0.779

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANCx is a family of AND-NOR circuits consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANC2	ANC4	ANC6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANC2	4.2	6.372	10.7
ANC4	5.0	7.085	12.2
ANC6	9.8	14.233	25.6

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

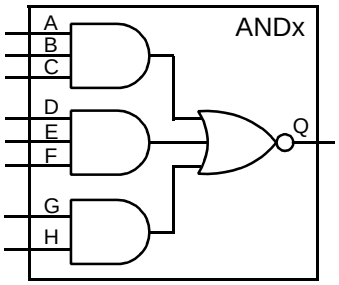
ANC2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.396 0.461	0.465 0.552	0.561 0.677	0.683 0.836	0.772 0.951
ANC4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.422 0.477	0.511 0.599	0.591 0.700	0.667 0.790	0.755 0.892
ANC6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.391 0.456	0.496 0.561	0.571 0.662	0.639 0.753	0.704 0.836

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANDx is a family of AND-NOR circuits consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

HDL Syntax

Verilog ..... ANDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ANDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	AND2	AND4	AND6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	2.0
F	1.0	1.0	1.9
G	1.0	1.0	2.0
H	1.0	1.0	2.0

AMI500SXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AND2	5.0	6.802	11.2
AND4	5.0	7.480	12.8
AND6	10.8	15.128	27.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

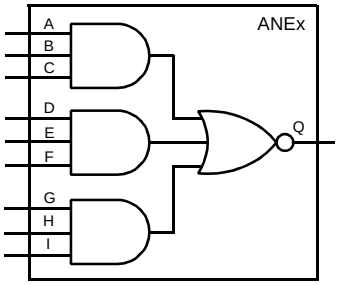
AND2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.396 0.460	0.471 0.558	0.570 0.686	0.690 0.840	0.775 0.948
AND4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.454 0.488	0.557 0.614	0.640 0.714	0.714 0.804	0.796 0.903
AND6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.392 0.481	0.483 0.571	0.569 0.665	0.648 0.764	0.722 0.856

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANEx is a family of AND-NOR circuits consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

HDL Syntax

Verilog ..... ANEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ANEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ANE2	ANE4	ANE6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	2.0
F	1.0	1.0	1.9
G	1.0	1.0	2.0
H	1.0	1.0	2.0
I	1.0	1.0	2.0

AMI500SXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANE2	5.3	7.216	12.1
ANE4	5.8	7.918	13.8
ANE6	11.6	16.011	29.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

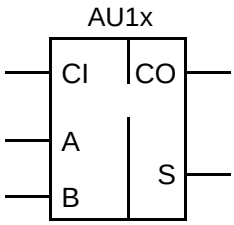
ANE2	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.394 0.471	0.460 0.557	0.557 0.677	0.683 0.830	0.777 0.941
ANE4	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.434 0.494	0.528 0.626	0.607 0.728	0.679 0.817	0.760 0.915
ANE6	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.343 0.450	0.460 0.568	0.577 0.670	0.650 0.761	0.705 0.848

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AU1x is a family of combinational one-bit full adders.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

HDL Syntax

Verilog ..... AU1x *inst_name* (CO, S, A, B, CI);

VHDL..... *inst_name*: AU1x port map (CO, S, A, B, CI);

Pin Loading

Pin Name	Equivalent Loads	
	AU11	AU12
A	4.7	9.8
B	4.6	9.9
CI	3.6	7.5

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AU11	5.0	6.329	12.8
AU12	13.2	13.050	27.4

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

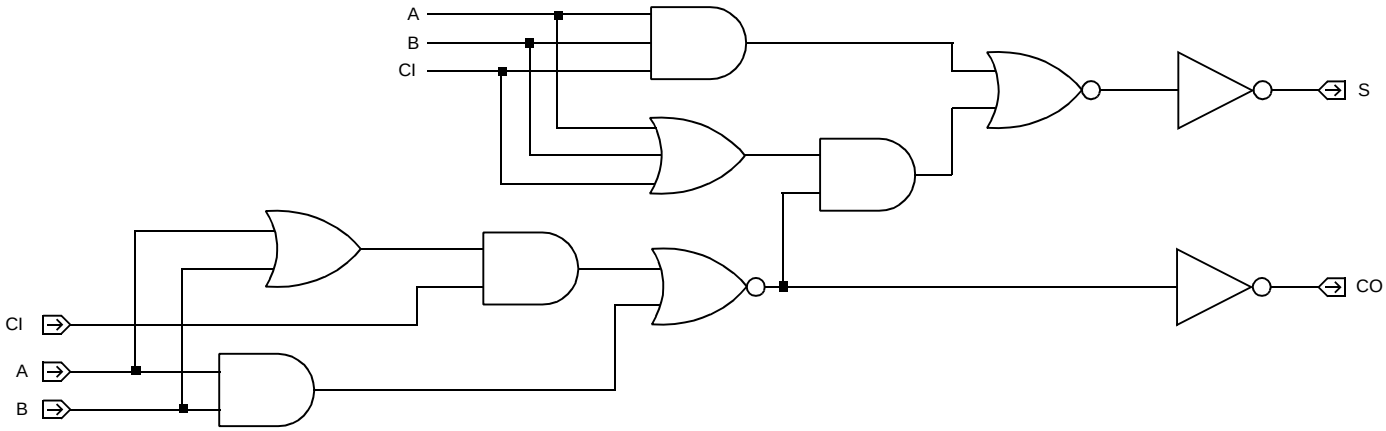
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
AU11	From: A To: S	t_{PLH} t_{PHL}	0.435 0.780	0.515 0.875	0.611 1.003	0.721 1.161	0.797 1.274
	From: B To: S	t_{PLH} t_{PHL}	0.388 0.871	0.460 0.974	0.554 1.106	0.668 1.264	0.748 1.375
	From: CI To: S	t_{PLH} t_{PHL}	0.360 0.872	0.440 0.978	0.541 1.108	0.659 1.260	0.742 1.365
	From: A To: CO	t_{PLH} t_{PHL}	0.382 0.488	0.464 0.602	0.572 0.747	0.702 0.920	0.794 1.040
	From: B To: CO	t_{PLH} t_{PHL}	0.393 0.507	0.475 0.617	0.582 0.757	0.712 0.926	0.803 1.042
	From: CI To: CO	t_{PLH} t_{PHL}	0.394 0.395	0.472 0.505	0.574 0.649	0.699 0.814	0.788 0.934
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
AU12	From: A To: S	t_{PLH} t_{PHL}	0.448 0.680	0.562 0.819	0.642 0.933	0.709 1.036	0.781 1.151
	From: B To: S	t_{PLH} t_{PHL}	0.386 0.742	0.489 0.894	0.571 1.008	0.645 1.109	0.727 1.219
	From: CI To: S	t_{PLH} t_{PHL}	0.349 0.748	0.454 0.894	0.539 1.004	0.616 1.102	0.703 1.208
	From: A To: CO	t_{PLH} t_{PHL}	0.278 0.421	0.373 0.577	0.460 0.698	0.542 0.806	0.636 0.926
	From: B To: CO	t_{PLH} t_{PHL}	0.287 0.416	0.384 0.574	0.466 0.700	0.541 0.812	0.627 0.935
	From: CI To: CO	t_{PLH} t_{PHL}	0.293 0.324	0.389 0.472	0.468 0.589	0.540 0.694	0.622 0.811

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



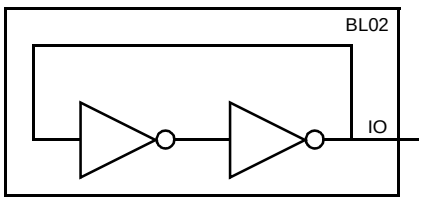
BL02

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

BL02 is a tristate bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	3.4

Equivalent Gates 2.4

HDL Syntax

Verilog ..... BL02 *inst_name* (IO);

VHDL..... *inst_name*: BL02 port map (IO);

Size And Power Characteristics

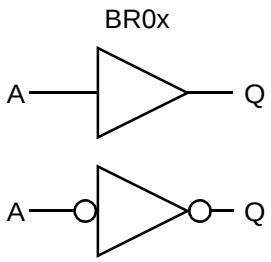
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.993	nA
EQL_{pd}	4.7	Eq-load

See page 2-13 for power equation.

Description

BR0x is a family of non-inverting bus receivers with a single output to be used as the output of tristate busses.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... BR0x *inst_name* (Q, A);

VHDL..... *inst_name*: BR0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	BR02	BR04	BR06
A	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
BR02	1.3	2.126	3.7
BR04	2.4	4.178	6.6
BR06	2.6	5.552	9.8

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

BR02	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.213 0.205	0.308 0.323	0.375 0.413	0.436 0.496	0.510 0.597
BR04	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.211 0.191	0.258 0.290	0.301 0.379	0.364 0.463	0.447 0.543
BR06	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.179 0.245	0.279 0.350	0.368 0.429	0.434 0.506	0.481 0.581

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

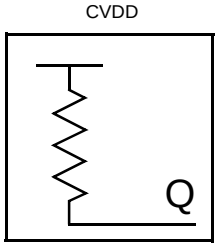
CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates 1.1

HDL Syntax

Verilog ..... CVDD *inst_name* (Q);

VHDL..... *inst_name*: CVDD port map (Q);



Description

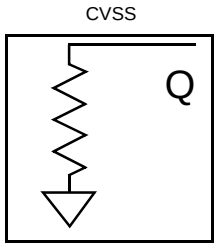
CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVSS *inst_name* (Q);

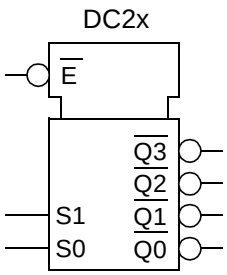
VHDL..... *inst_name*: CVSS port map (Q);



Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL..... *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.1	3.6
S1	3.1	3.6
EN	1.0	4.6

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC21	6.1	8.616	17.5
DC22	7.4	9.257	19.9

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

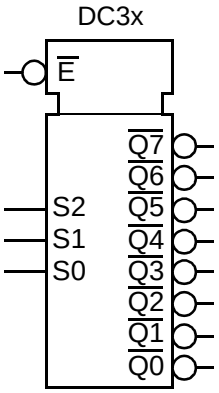
	Number of Equivalent Loads		1	2	4	5	7 (max)
DC21	From: Sx To: QN	t_{PLH} t_{PHL}	0.264 0.287	0.311 0.350	0.396 0.475	0.437 0.537	0.514 0.660
	From: EN To: QN	t_{PLH} t_{PHL}	0.401 0.389	0.444 0.456	0.523 0.579	0.561 0.637	0.636 0.749
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
DC22	From: Sx To: QN	t_{PLH} t_{PHL}	0.228 0.335	0.299 0.441	0.393 0.580	0.509 0.747	0.591 0.865
	From: EN To: QN	t_{PLH} t_{PHL}	0.257 0.419	0.330 0.522	0.428 0.657	0.550 0.819	0.638 0.934

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

DC3x is a family of three-to-eight line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC3x *inst_name* (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

VHDL..... *inst_name* DC3x port map (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads	
	DC31	DC32
S0	5.4	5.7
S1	5.6	5.7
S2	5.4	5.3
EN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC31	12.7	18.457	41.8
DC32	17.1	21.546	59.9

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

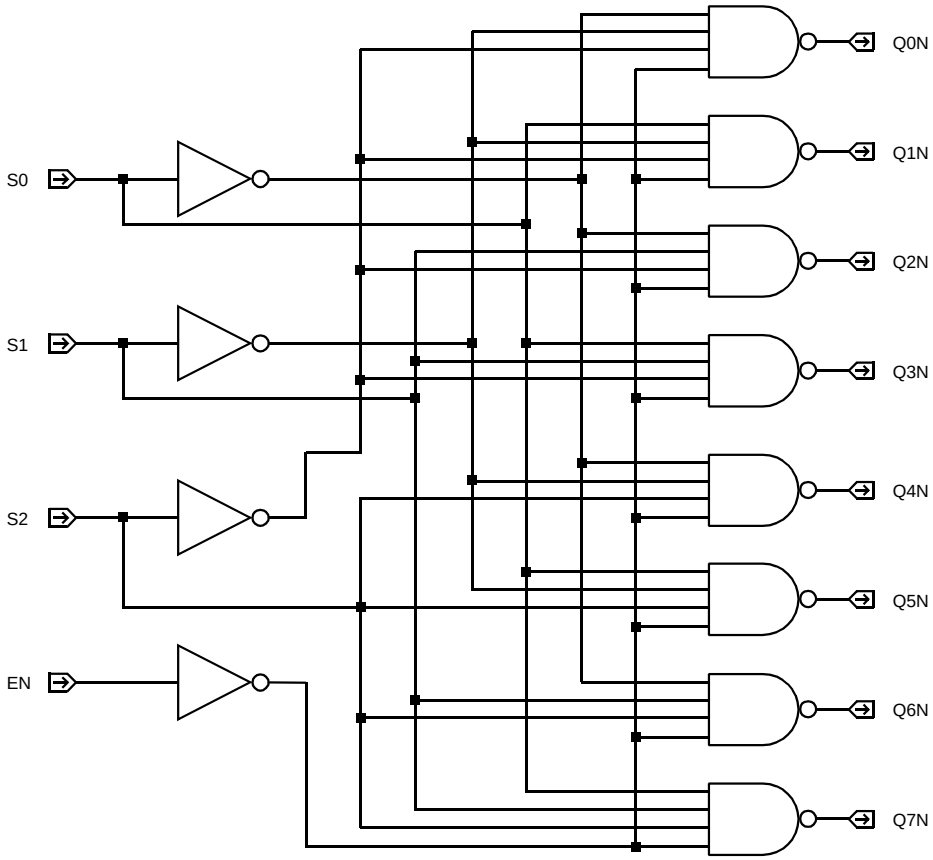
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	3	4	6 (max)
DC31	From: Sx To: QN	t_{PLH} t_{PHL}	0.341 0.377	0.390 0.452	0.439 0.527	0.490 0.602	0.591 0.754
	From: EN To: QN	t_{PLH} t_{PHL}	0.609 0.559	0.656 0.627	0.702 0.700	0.749 0.776	0.842 0.934
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
DC32	From: Sx To: QN	t_{PLH} t_{PHL}	0.239 0.368	0.309 0.479	0.403 0.629	0.519 0.813	0.602 0.944
	From: EN To: QN	t_{PLH} t_{PHL}	0.827 0.924	0.892 1.026	0.984 1.168	1.101 1.349	1.187 1.479

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

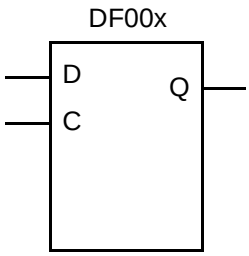
Logic Schematic



Description

DF00x is a family of static, master-slave D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q
H	↑	H
L	↑	L
X	L	NC

NC = No Change

HDL Syntax

Verilog ..... DF00x *inst_name* (Q, C, D);

VHDL..... *inst_name*: DF00x port map (Q, C, D);

Pin Loading

Pin Name	Equivalent Loads	
	DF001	DF002
D	1.0	1.0
C	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF001	4.2	5.191	9.3
DF002	4.5	5.860	10.0

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF001	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.545 0.460	0.605 0.553	0.695 0.676	0.815 0.829	0.905 0.938
DF002	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.533 0.466	0.626 0.587	0.704 0.691	0.774 0.788	0.853 0.899

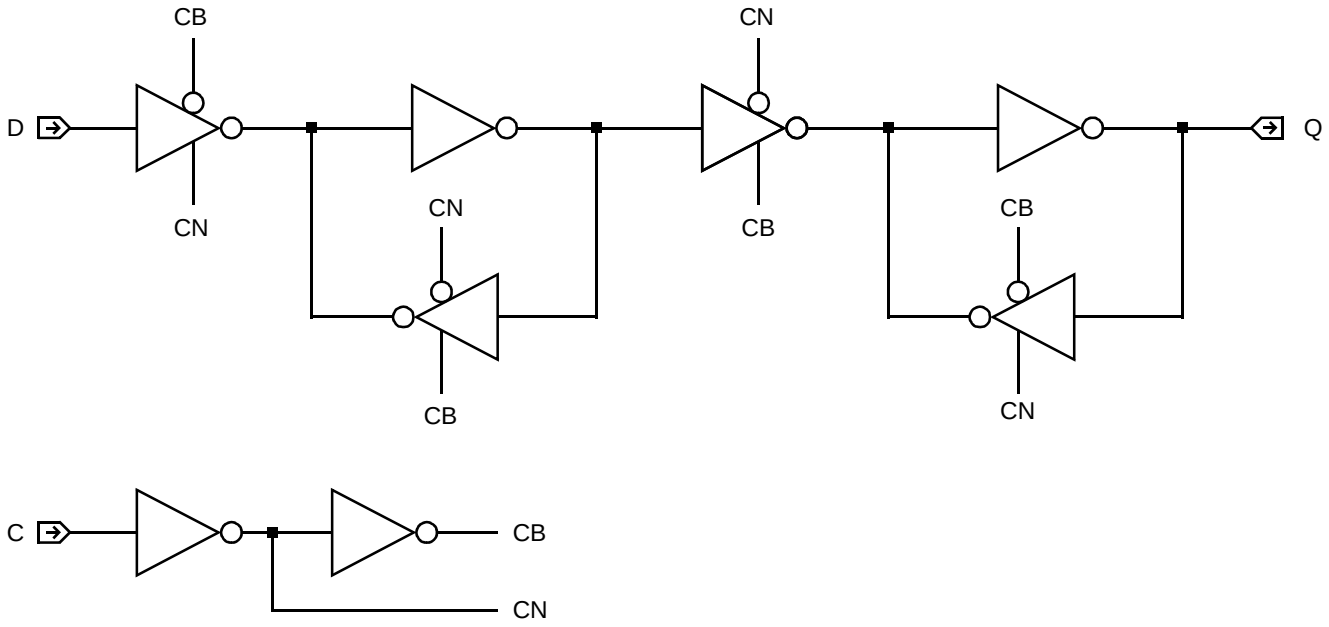
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF001	Cell DF002
Min C Width	High	t_w	0.545	0.535
Min C Width	Low	t_w	0.569	0.545
Min D Setup		t_{su}	0.347	0.342
Min D Hold		t_h	0.167	0.161

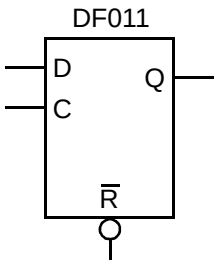
Logic Schematic



Description

DF011 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q
L	X	X	L
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.0
RN	1.1

Equivalent Gates 5.3

HDL Syntax

Verilog ..... DF011 *inst_name* (Q, C, D, RN);

VHDL..... *inst_name*: DF011 port map (Q, C, D, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.058	nA
EQL_{pd}	13.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.608 0.469	0.661 0.517	0.769 0.604	0.930 0.725	1.037 0.802
RN	Q	t_{PHL}	0.312	0.358	0.432	0.549	0.623

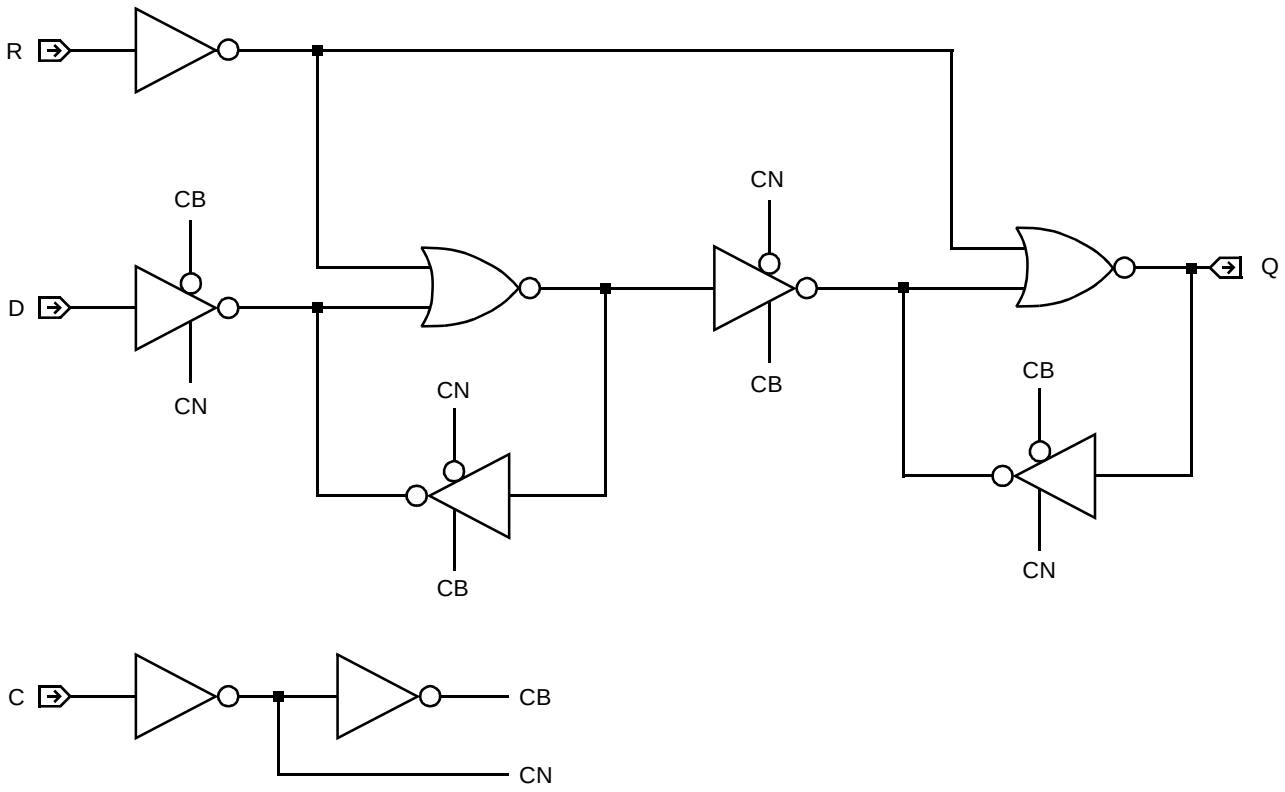
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.607
Min C Width	Low	t_w	0.593
Min RN Width	Low	t_w	0.566
Min D Setup		t_{su}	0.360
Min D Hold		t_h	0.162
Min RN Setup		t_{su}	0.322
Min RN Hold		t_h	0.334

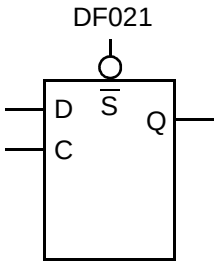
Logic Schematic



Description

DF021 is a static, master-slave D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q
L	X	X	H
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.1

Equivalent Gates 4.7

HDL Syntax

Verilog.....DF021 *inst_name* (Q, C, D, SN);

VHDL..... *inst_name*: DF021 port map (Q, C, D, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.112	nA
EQL_{pd}	10.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.574 0.494	0.615 0.556	0.687 0.664	0.785 0.808	0.846 0.897
SN	Q	t_{PLH}	0.130	0.169	0.261	0.356	0.423

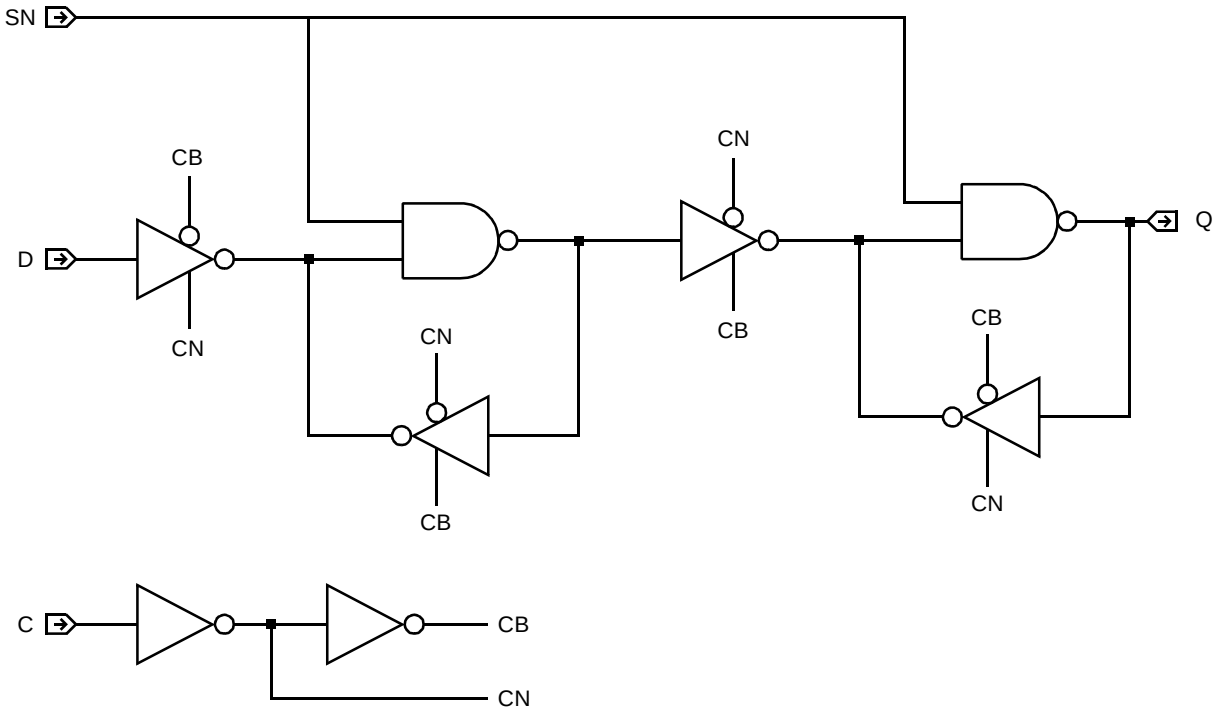
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.573
Min C Width	Low	t_w	0.582
Min SN Width	Low	t_w	0.712
Min D Setup		t_{su}	0.367
Min D Hold		t_h	0.164
Min SN Setup		t_{su}	0.168
Min SN Hold		t_h	0.576

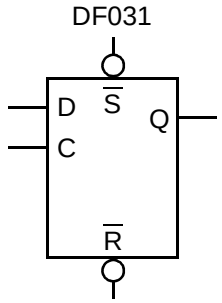
Logic Schematic



Description

DF031 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	L	↑	L
H	H	H	↑	H
H	H	X	L	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.1
RN	1.0

Equivalent Gates 6.1

HDL Syntax

Verilog ..... DF031 *inst_name* (Q, D, RN, SN);

VHDL..... *inst_name*: DF031 port map (Q, D, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.148	nA
EQL_{pd}	14.3	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.639 0.518	0.699 0.575	0.827 0.695	1.028 0.882	1.165 1.011
RN	Q	t_{PHL}	0.360	0.426	0.540	0.699	0.811
SN	Q	t_{PLH}	0.128	0.165	0.239	0.336	0.385

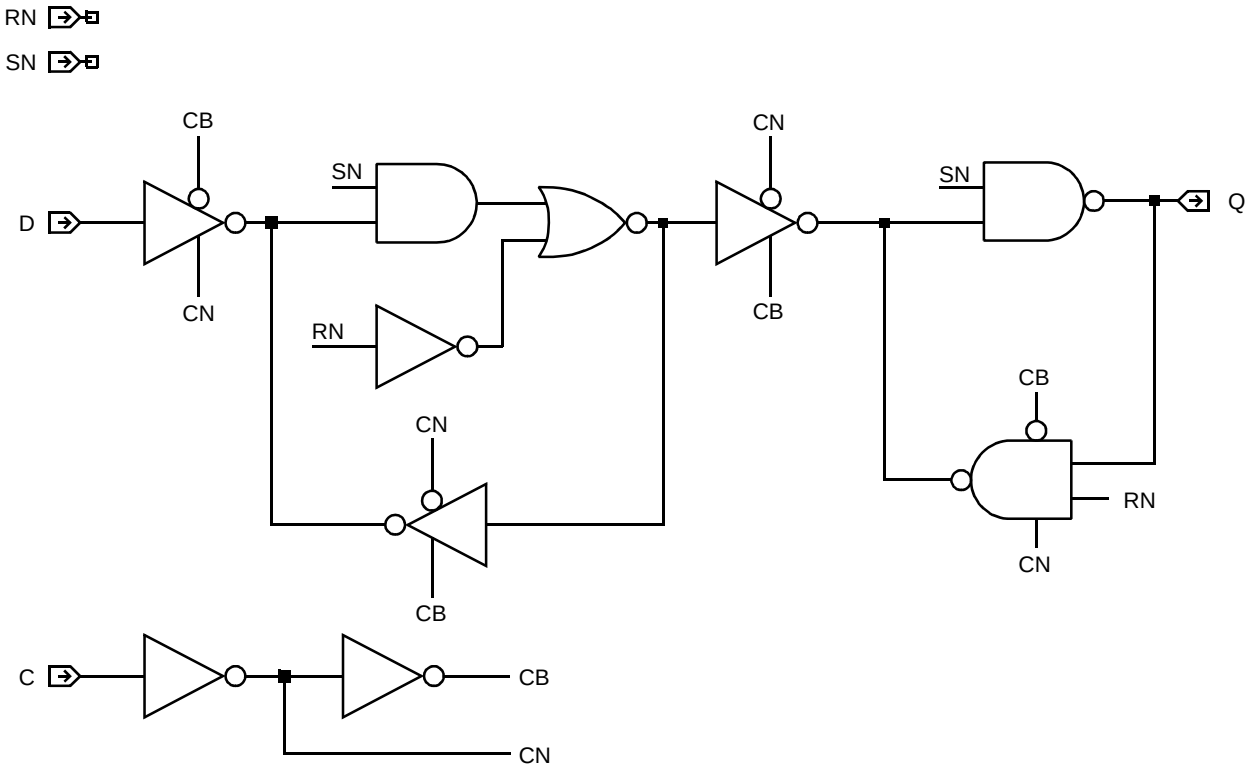
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.643
Min C Width	Low	t_w	0.609
Min RN Width	Low	t_w	0.604
Min SN Width	Low	t_w	0.671
Min D Setup		t_{su}	0.405
Min D Hold		t_h	0.164
Min RN Setup		t_{su}	0.363
Min RN Hold		t_h	0.335
Min SN Setup		t_{su}	0.207
Min SN Hold		t_h	0.545

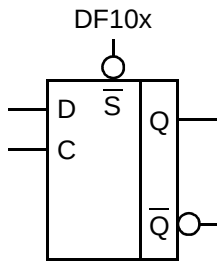
Logic Schematic



Description

DF10x is a family of static, master-slave D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF10x *inst_name* (Q, QN, C, D, SN);

VHDL.....*inst_name*: DF10x port map (Q, QN, C, D, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF101	DF102	DF104	DF106
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
DF101	5.8	7.537	13.5
DF102	6.1	8.864	15.5
DF104	8.7	13.907	26.3
DF106	9.8	16.650	32.1

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF101	From: C To: Q	t_{PLH} t_{PHL}	0.594 0.528	0.665 0.633	0.762 0.768	0.885 0.932	0.974 1.050
	From: C To: QN	t_{PLH} t_{PHL}	0.678 0.793	0.727 0.886	0.813 1.000	0.939 1.131	1.040 1.220
	From: SN To: Q	t_{PLH}	0.733	0.810	0.911	1.034	1.121
	From: SN To: QN	t_{PHL}	0.280	0.376	0.501	0.653	0.762
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF102	From: C To: Q	t_{PLH} t_{PHL}	0.600 0.527	0.696 0.678	0.773 0.797	0.843 0.902	0.921 1.019
	From: C To: QN	t_{PLH} t_{PHL}	0.777 0.886	0.856 0.979	0.919 1.059	0.977 1.135	1.041 1.221
	From: SN To: Q	t_{PLH}	0.845	0.950	1.024	1.087	1.155
	From: SN To: QN	t_{PHL}	0.303	0.423	0.524	0.618	0.729
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF104	From: C To: Q	t_{PLH} t_{PHL}	0.663 0.533	0.766 0.690	0.836 0.812	0.901 0.913	0.968 1.001
	From: C To: QN	t_{PLH} t_{PHL}	0.792 0.899	0.843 1.018	0.896 1.107	0.955 1.181	1.024 1.247
	From: SN To: Q	t_{PLH}	0.807	0.902	0.980	1.048	1.111
	From: SN To: QN	t_{PHL}	0.259	0.386	0.487	0.575	0.653
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF106	From: C To: Q	t_{PLH} t_{PHL}	0.699 0.596	0.810 0.766	0.885 0.885	0.945 0.980	0.994 1.058
	From: C To: QN	t_{PLH} t_{PHL}	0.926 1.030	0.980 1.120	1.033 1.209	1.095 1.290	1.163 1.362
	From: SN To: Q	t_{PLH}	0.975	1.064	1.126	1.185	1.241
	From: SN To: QN	t_{PHL}	0.306	0.429	0.532	0.619	0.692

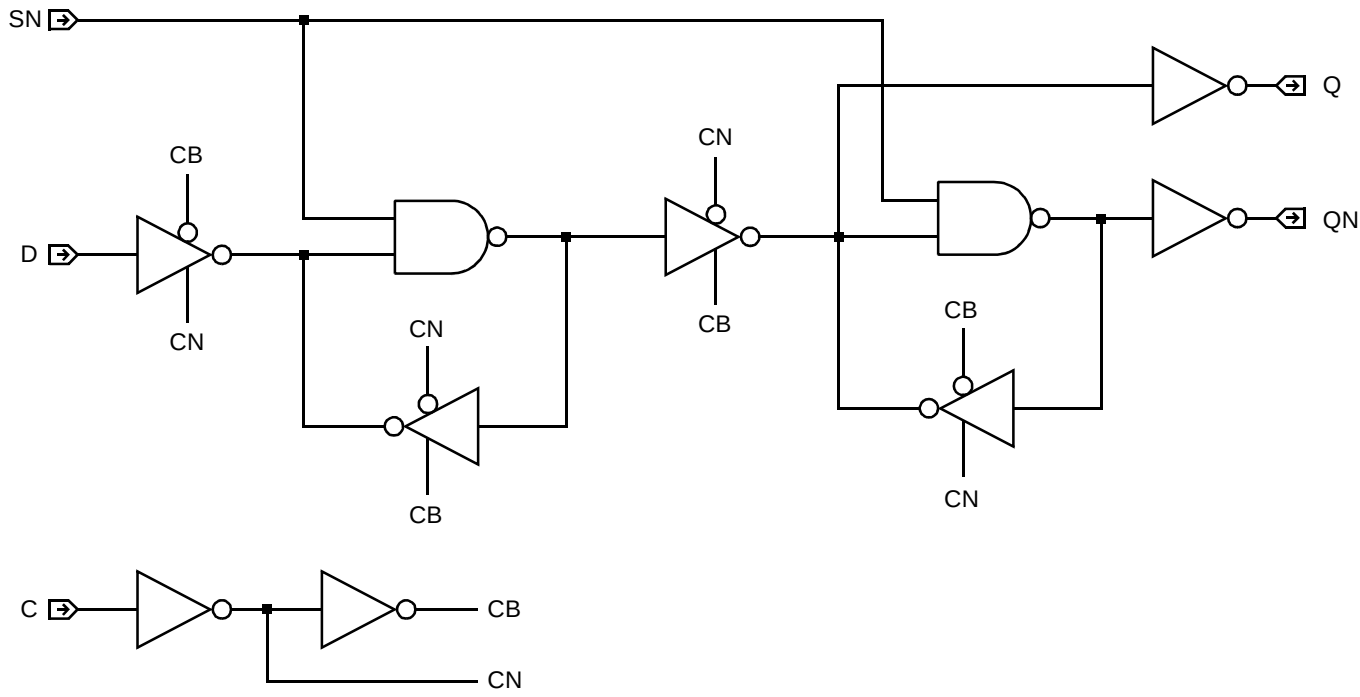
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF101	DF102	DF104	DF106
Min C Width	High	t_w	0.628	0.707	0.770	0.868
Min C Width	Low	t_w	0.585	0.576	0.672	0.667
Min SN Width		t_w	0.589	0.732	0.694	0.845
Min D Setup		t_{su}	0.370	0.361	0.405	0.406
Min D Hold		t_h	0.164	0.164	0.196	0.195
Min SN Setup		t_{su}	0.173	0.167	0.214	0.214
Min SN Hold		t_h	0.560	0.555	0.600	0.599

Logic Schematic

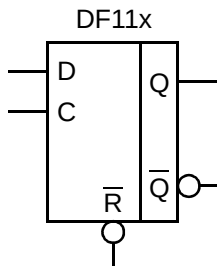


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DF11x is a family of static, master-slave D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF11x *inst_name* (Q, QN, C, D, RN);

VHDL.....inst_DF11x : DF11x port map (Q, QN, C, D, RN);

Pin Loading

Pin Name	Equivalent Loads			
	DF111	DF112	DF114	DF116
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF111	6.3	7.479	16.3
DF112	6.6	8.800	18.9
DF114	9.0	13.419	30.5
DF116	10.3	16.173	36.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF111	From: C To: Q	t_{PLH} t_{PHL}	0.567 0.510	0.636 0.616	0.733 0.755	0.857 0.923	0.946 1.041
	From: C To: QN	t_{PLH} t_{PHL}	0.638 0.824	0.683 0.920	0.763 1.044	0.884 1.192	0.982 1.296
	From: RN To: Q	t_{PHL}	0.933	1.047	1.192	1.365	1.485
	From: RN To: QN	t_{PLH}	0.381	0.453	0.547	0.662	0.746
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF112	From: C To: Q	t_{PLH} t_{PHL}	0.615 0.537	0.714 0.685	0.794 0.795	0.867 0.898	0.948 1.021
	From: C To: QN	t_{PLH} t_{PHL}	0.725 1.003	0.790 1.124	0.858 1.213	0.929 1.292	1.016 1.376
	From: RN To: Q	t_{PHL}	1.066	1.214	1.330	1.433	1.547
	From: RN To: QN	t_{PLH}	0.391	0.467	0.540	0.609	0.689
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF114	From: C To: Q	t_{PLH} t_{PHL}	0.647 0.531	0.741 0.683	0.808 0.804	0.866 0.909	0.928 1.006
	From: C To: QN	t_{PLH} t_{PHL}	0.746 0.953	0.788 1.086	0.849 1.182	0.920 1.270	0.998 1.354
	From: RN To: Q	t_{PHL}	1.127	1.278	1.379	1.465	1.546
	From: RN To: QN	t_{PLH}	0.435	0.493	0.565	0.639	0.716
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF116	From: C To: Q	t_{PLH} t_{PHL}	0.689 0.604	0.800 0.773	0.878 0.891	0.938 0.985	0.987 1.062
	From: C To: QN	t_{PLH} t_{PHL}	0.863 1.090	0.905 1.227	0.966 1.330	1.033 1.412	1.101 1.478
	From: RN To: Q	t_{PHL}	1.290	1.447	1.557	1.644	1.716
	From: RN To: QN	t_{PLH}	0.466	0.535	0.604	0.671	0.739

AMI500SXSC 0.5 micron CMOS Standard Cell

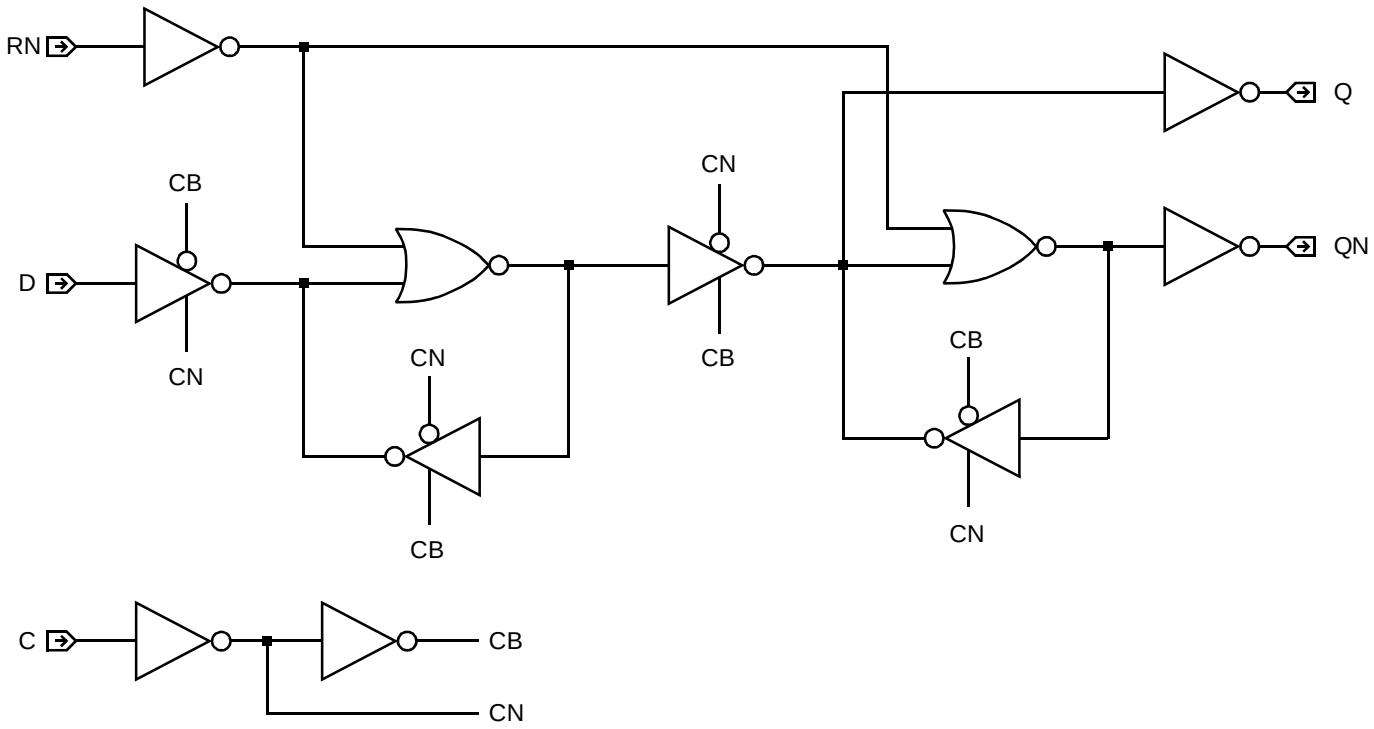
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF111	DF112	DF114	DF116
Min C Width	High	t_w	0.635	0.785	0.801	0.918
Min C Width	Low	t_w	0.568	0.589	0.660	0.660
Min RN Width		t_w	0.569	0.570	0.651	0.650
Min D Setup		t_{su}	0.367	0.360	0.408	0.408
Min D Hold		t_h	0.162	0.167	0.185	0.185
Min RN Setup		t_{su}	0.319	0.325	0.401	0.401
Min RN Hold		t_h	0.329	0.343	0.365	0.365

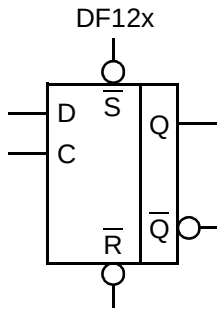
Logic Schematic



Description

DF12x is a family of static, master-slave D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DF12x *inst_name* (Q, QN, C, D, RN, SN);

VHDL..... *inst_name*: DF12x port map (Q, QN, C, D, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF121	DF122	DF124	DF126
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	2.1	2.1
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF121	7.1	8.572	17.8
DF122	7.6	9.943	20.7
DF124	9.5	14.068	29.6
DF126	10.8	16.820	35.5

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF121	From: C To: Q	t_{PLH} t_{PHL}	0.586 0.523	0.657 0.624	0.753 0.756	0.870 0.915	0.954 1.027
	From: C To: QN	t_{PLH} t_{PHL}	0.687 0.919	0.739 1.017	0.824 1.146	0.944 1.304	1.037 1.417
	From: SN To: Q	t_{PLH}	0.715	0.790	0.890	1.010	1.096
	From: SN To: QN	t_{PHL}	0.278	0.375	0.501	0.652	0.761
	From: RN To: Q	t_{PHL}	0.968	1.075	1.217	1.392	1.516
	From: RN To: QN	t_{PLH}	0.433	0.497	0.593	0.713	0.800
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF122	From: C To: Q	t_{PLH} t_{PHL}	0.605 0.537	0.707 0.671	0.789 0.791	0.863 0.905	0.945 1.036
	From: C To: QN	t_{PLH} t_{PHL}	0.819 1.075	0.896 1.184	0.962 1.280	1.022 1.371	1.090 1.476
	From: SN To: Q	t_{PLH}	0.865	0.956	1.029	1.095	1.171
	From: SN To: QN	t_{PHL}	0.297	0.422	0.519	0.610	0.712
	From: RN To: Q	t_{PHL}	1.134	1.292	1.404	1.499	1.602
	From: RN To: QN	t_{PLH}	0.460	0.555	0.634	0.707	0.789

	Number of Equivalent Loads		1	10	20	30	40 (max)
DF124	From: C To: Q	t_{PLH} t_{PHL}	1.096 0.913	1.176 1.033	1.243 1.132	1.301 1.219	1.355 1.299
	From: C To: QN	t_{PLH} t_{PHL}	0.682 0.814	0.771 0.912	0.842 1.018	0.902 1.122	0.955 1.221
	From: SN To: Q	t_{PLH}	0.438	0.517	0.589	0.652	0.719
	From: SN To: QN	t_{PHL}	0.968	1.110	1.205	1.276	1.335
	From: RN To: Q	t_{PHL}	0.670	0.782	0.885	0.967	1.056
	From: RN To: QN	t_{PLH}	1.178	1.215	1.275	1.350	1.436
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF126	From: C To: Q	t_{PLH} t_{PHL}	1.182 0.984	1.257 1.144	1.319 1.242	1.373 1.317	1.419 1.377
	From: C To: QN	t_{PLH} t_{PHL}	0.782 0.925	0.852 1.059	0.921 1.153	0.986 1.232	1.046 1.302
	From: SN To: Q	t_{PLH}	0.513	0.586	0.655	0.723	0.791
	From: SN To: QN	t_{PHL}	1.051	1.202	1.314	1.406	1.486
	From: RN To: Q	t_{PHL}	0.758	0.874	0.981	1.078	1.163
	From: RN To: QN	t_{PLH}	1.277	1.312	1.375	1.454	1.539

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

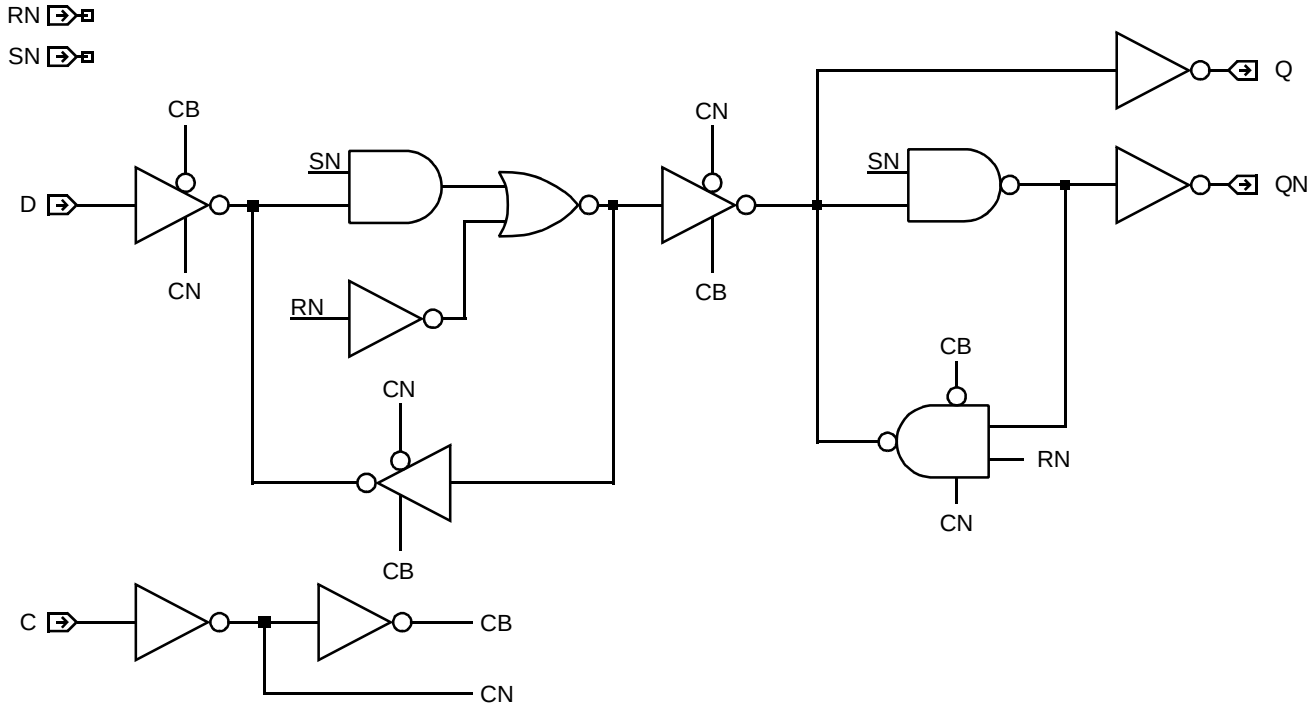
AMI500SXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF121	DF122	DF124	DF126
Min C Width	High	t_w	0.709	0.835	0.702	0.710
Min C Width	Low	t_w	0.611	0.611	0.606	0.609
Min RN Width	Low	t_w	0.605	0.605	0.597	0.604
Min SN Width	Low	t_w	0.589	0.732	0.595	0.600
Min D Setup		t_{su}	0.407	0.407	0.404	0.406
Min D Hold		t_h	0.166	0.166	0.165	0.166
Min RN Setup		t_{su}	0.356	0.356	0.359	0.358
Min RN Hold		t_h	0.336	0.336	0.334	0.335
Min SN Setup		t_{su}	0.208	0.208	0.207	0.207
Min SN Hold		t_h	0.546	0.546	0.542	0.545

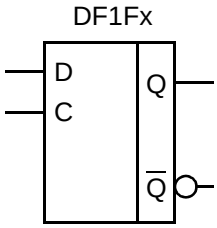
Logic Schematic



Description

DF1Fx is a family of static, master-slave D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
X	X	L	H
L	↑	L	H
H	↑	H	L
X	L	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF1Fx *inst_name* (Q, QN, C, D);

VHDL..... *inst_name*: DF1Fx port map (Q, QN, C, D)

Pin Loading

Pin Name	Equivalent Loads			
	DF1F1	DF1F2	DF1F4	DF1F6
D	1.0	1.0	1.0	1.0
C	1.1	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF1F1	5.3	6.619	12.8
DF1F2	5.8	7.962	15.3
DF1F4	7.4	12.073	23.2
DF1F6	9.0	15.492	30.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF1F1	From: C To: Q	t_{PLH} t_{PHL}	0.611 0.549	0.686 0.661	0.783 0.798	0.900 0.957	0.981 1.066
	From: C To: QN	t_{PLH} t_{PHL}	0.640 0.786	0.698 0.876	0.782 0.994	0.894 1.138	0.977 1.241
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF1F2	From: C To: Q	t_{PLH} t_{PHL}	0.636 0.565	0.733 0.722	0.815 0.837	0.892 0.936	0.980 1.044
	From: C To: QN	t_{PLH} t_{PHL}	0.750 0.866	0.809 0.969	0.874 1.064	0.941 1.155	1.024 1.262
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF1F4	From: C To: Q	t_{PLH} t_{PHL}	0.917 0.854	1.005 0.950	1.070 1.045	1.124 1.136	1.170 1.224
	From: C To: QN	t_{PLH} t_{PHL}	0.588 0.702	0.678 0.831	0.750 0.937	0.811 1.034	0.868 1.126
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF1F6	From: C To: Q	t_{PLH} t_{PHL}	0.923 0.865	1.012 0.959	1.067 1.043	1.108 1.119	1.141 1.185
	From: C To: QN	t_{PLH} t_{PHL}	0.661 0.776	0.724 0.871	0.783 0.966	0.856 1.054	0.941 1.133

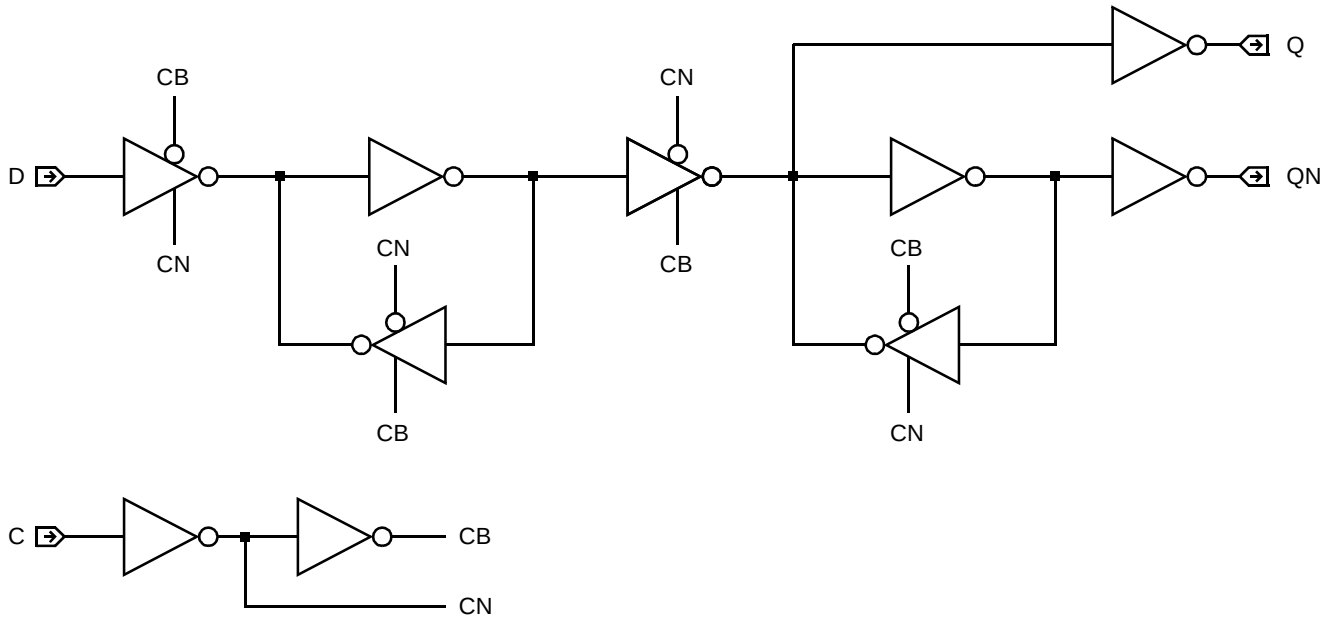
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF1F1	DF1F2	DF1F4	DF1F6
Min C Width	High	t_w	0.629	0.724	0.590	0.625
Min C Width	Low	t_w	0.549	0.563	0.533	0.530
Min D Setup		t_{su}	0.342	0.351	0.333	0.329
Min D Hold		t_h	0.169	0.168	0.162	0.160

Logic Schematic

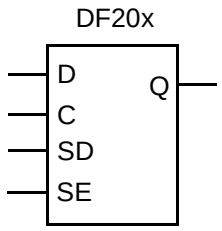


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DF20x is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q
↑	H	X	L	H
↑	L	X	L	L
↑	X	H	H	H
↑	X	L	H	L
L	X	X	X	NC

NC = No Change

HDL Syntax

Verilog ..... DF20x *inst_name* (Q, C, D, SD, SE);

VHDL..... *inst_name*: DF20x port map (Q, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads	
	DF201	DF202
C	1.0	1.0
D	1.0	1.0
SD	1.0	1.0
SE	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF201	5.5	7.079	13.8
DF202	5.8	7.393	13.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF201	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.599 0.527	0.669 0.622	0.761 0.752	0.871 0.916	0.948 1.033
DF202	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.546 0.478	0.628 0.615	0.699 0.720	0.766 0.811	0.841 0.912

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

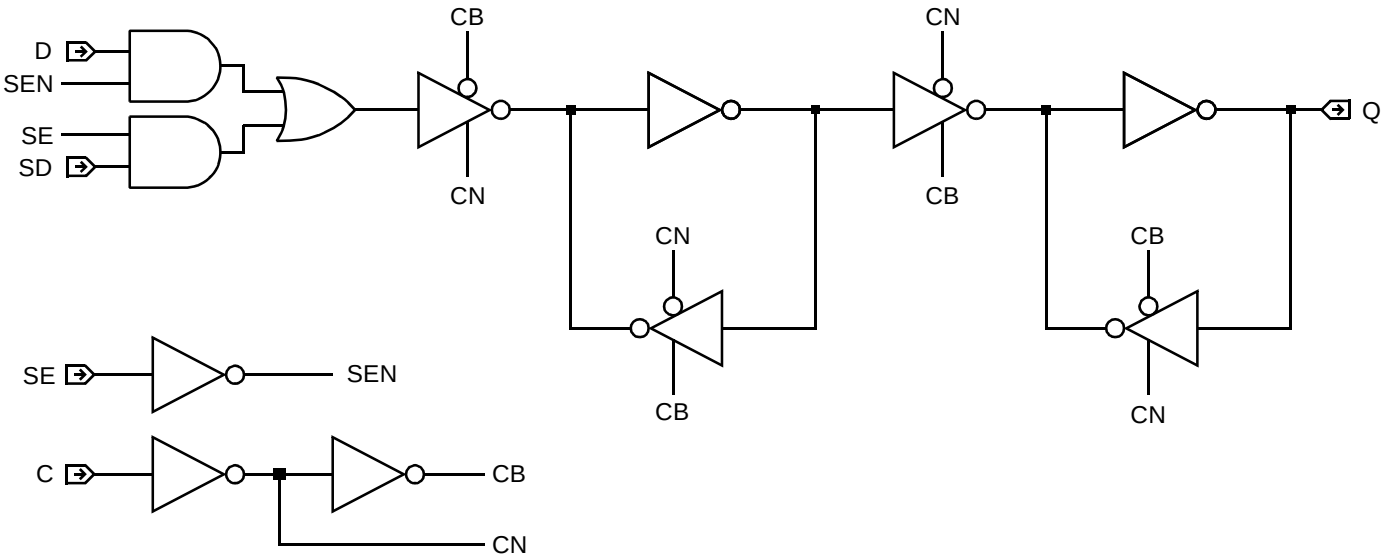
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DF201	**DF202**
Min C Width	High	t_w	0.595	0.543
Min C Width	Low	t_w	0.870	0.682
Min D Setup		t_{su}	0.708	0.571
Min D Hold		t_h	0.190	0.166
Min SD Setup		t_{su}	0.708	0.571
Min SD Hold		t_h	0.190	0.166
Min SE Setup		t_{su}	0.872	0.709
Min SE Hold		t_h	0.190	0.166

AMI500SXSC 0.5 micron CMOS Standard Cell

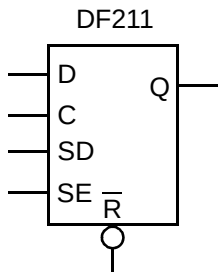
Logic Schematic



Description

DF211 is a static, master-slave, multiplexed scan D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q
↑	H	H	X	L	H
↑	L	H	X	L	L
↑	X	H	H	H	H
↑	X	H	L	H	L
X	X	L	X	X	L
L	X	H	X	X	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.1
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates 6.9

HDL Syntax

Verilog ..... DF211 *inst_name* (Q, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF211 port map (Q, C, D, RN, SD, SE);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.624	nA
EQL_{pd}	17.6	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.612 0.479	0.661 0.527	0.765 0.616	0.927 0.739	1.038 0.817
RN	Q	t_{PHL}	0.329	0.379	0.458	0.572	0.653

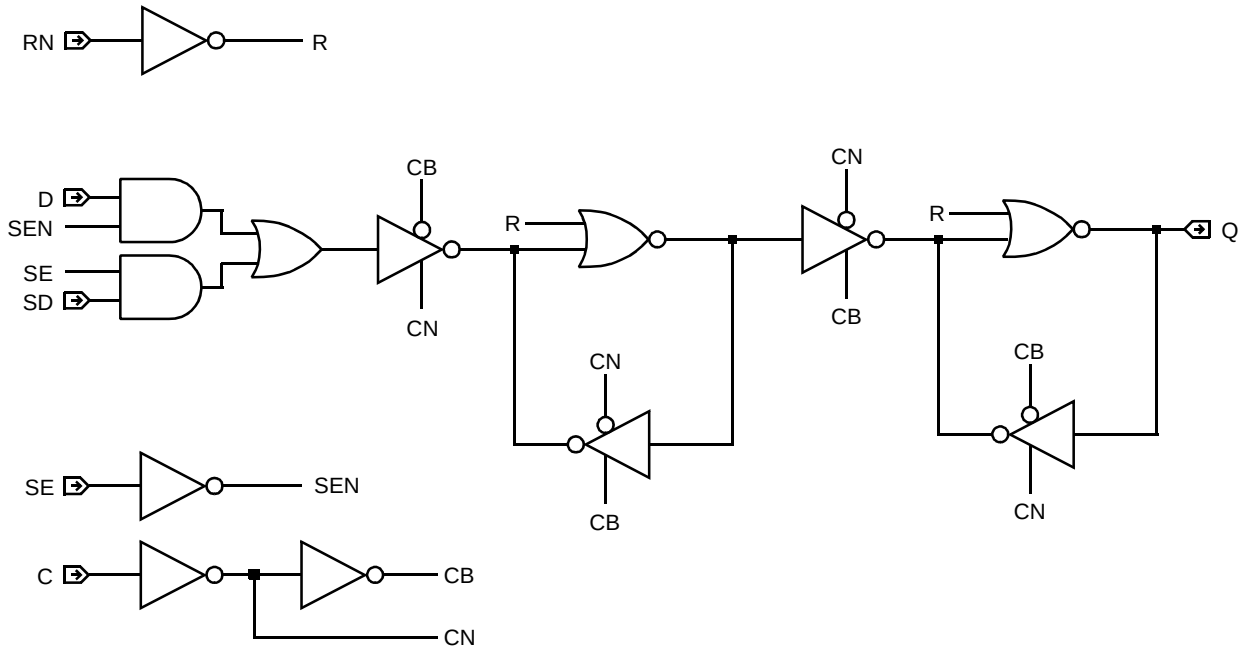
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.613
Min C Width	Low	t_w	0.737
Min RN Width	Low	t_w	0.581
Min D Setup		t_{su}	0.634
Min D Hold		t_h	0.170
Min SD Setup		t_{su}	0.634
Min SD Hold		t_h	0.170
Min SE Setup		t_{su}	0.745
Min SE Hold		t_h	0.170
Min RN Setup		t_{su}	0.325
Min RN Hold		t_h	0.347

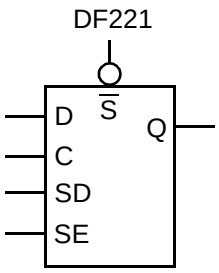
Logic Schematic



Description

DF221 is a static, master-slave, multiplexed scan D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q
↑	H	X	L	H	H
↑	L	X	L	H	L
↑	X	H	H	H	H
↑	X	L	H	H	L
X	X	X	X	L	H
L	X	X	X	H	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.1
D	1.0
SD	1.0
SE	2.0
SN	2.1

Equivalent Gates 6.3

HDL Syntax

Verilog ..... DF221 *inst_name* (Q, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF221 port map (Q, C, D, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.690	nA
EQL_{pd}	14.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.561 0.502	0.595 0.557	0.669 0.672	0.793 0.848	0.881 0.968
SN	Q	t_{PLH}	0.131	0.170	0.244	0.343	0.408

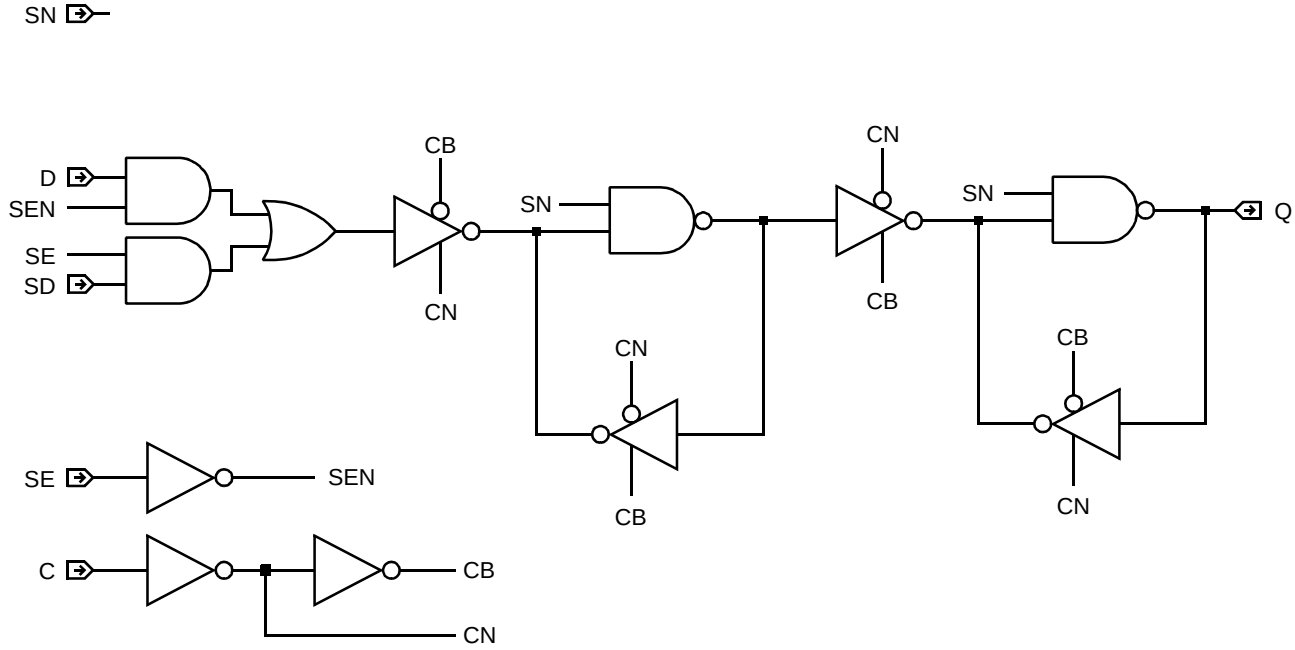
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.560
Min C Width	Low	t_w	0.790
Min SN Width	Low	t_w	0.501
Min D Setup		t_{su}	0.672
Min D Hold		t_h	0.168
Min SD Setup		t_{su}	0.672
Min SD Hold		t_h	0.168
Min SE Setup		t_{su}	0.809
Min SE Hold		t_h	0.168
Min SN Setup		t_{su}	0.173
Min SN Hold		t_h	0.553

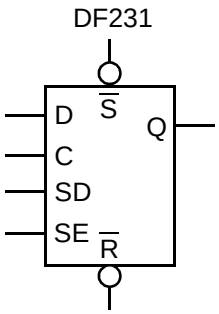
Logic Schematic



Description

DF231 is a static, master-slave, multiplexed scan D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q
↑	H	H	X	L	H	H
↑	L	H	X	L	H	L
↑	X	H	H	H	H	H
↑	X	H	L	H	H	L
X	X	L	X	X	H	L
X	X	H	X	X	L	H
X	X	L	X	X	L	IL
L	X	H	X	X	H	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	1.0
D	1.0
RN	1.0
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates 7.6

HDL Syntax

Verilog ..... DF231 *inst_name* (Q, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF231 port map (Q, C, D, RN, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.691	nA
EQL_{pd}	18.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.644 0.518	0.708 0.578	0.838 0.698	1.035 0.878	1.167 0.997
RN	Q	t_{PHL}	0.359	0.418	0.533	0.703	0.812
SN	Q	t_{PLH}	0.130	0.166	0.235	0.329	0.373

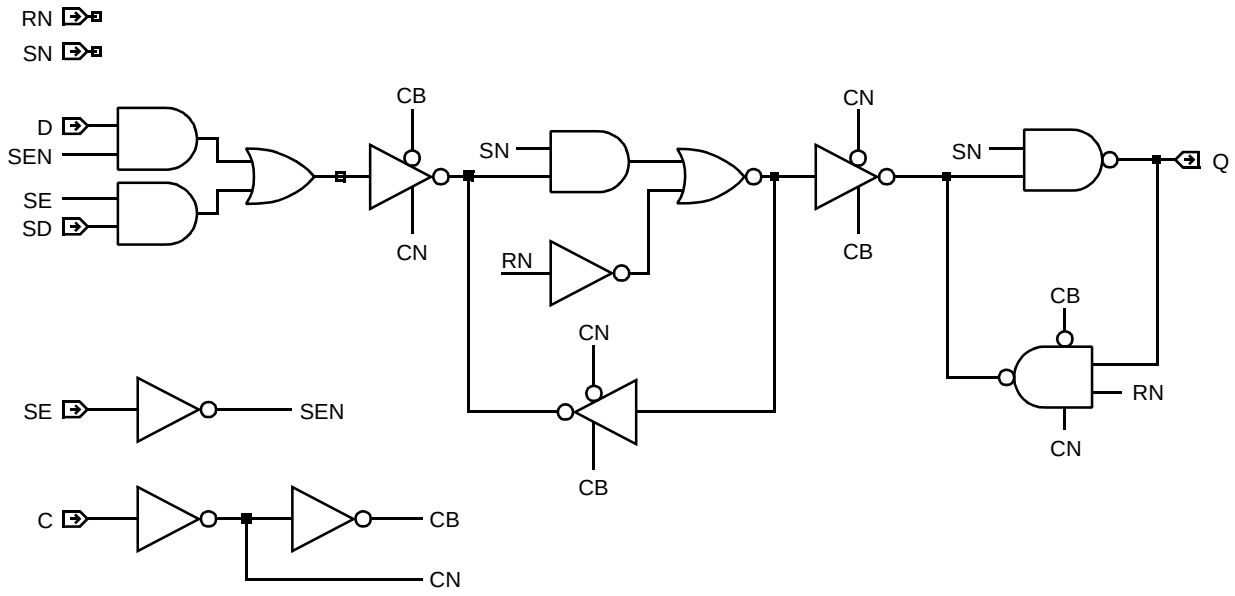
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.644
Min C Width	Low	t_w	0.769
Min RN Width	Low	t_w	0.615
Min SN Width	Low	t_w	0.503
Min D Setup		t_{su}	0.650
Min D Hold		t_h	0.170
Min SD Setup		t_{su}	0.650
Min SD Hold		t_h	0.170
Min SE Setup		t_{su}	0.778
Min SE Hold		t_h	0.170
Min RN Setup		t_{su}	0.368
Min RN Hold		t_h	0.353
Min SN Setup		t_{su}	0.214
Min SN Hold		t_h	0.559

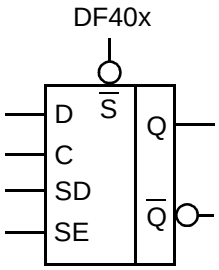
Logic Schematic



Description

DF40x is a family of static, master-slave, multiplexed scan D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF40x *inst_name* (Q, QN, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF40x port map (Q, QN, C, D, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF401	DF402	DF404	DF406
C	1.1	1.1	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SN	2.1	2.1	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF401	6.8	9.078	17.5
DF402	7.6	10.420	20.2
DF404	10.0	15.440	30.5
DF406	11.3	18.195	36.5

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF401	From: C To: Q	t_{PLH} t_{PHL}	0.600 0.523	0.675 0.632	0.776 0.773	0.901 0.939	0.995 1.053
	From: C To: QN	t_{PLH} t_{PHL}	0.665 0.809	0.733 0.889	0.823 1.009	0.936 1.165	1.021 1.289
	From: SN To: Q	t_{PLH}	0.736	0.822	0.925	1.043	1.124
	From: SN To: QN	t_{PHL}	0.289	0.386	0.517	0.675	0.788
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF402	From: C To: Q	t_{PLH} t_{PHL}	0.606 0.549	0.705 0.703	0.787 0.828	0.862 0.941	0.946 1.076
	From: C To: QN	t_{PLH} t_{PHL}	0.812 0.930	0.879 1.036	0.938 1.129	0.993 1.218	1.057 1.322
	From: SN To: Q	t_{PLH}	0.848	0.955	1.037	1.109	1.196
	From: S To: QN	t_{PHL}	0.321	0.448	0.559	0.661	0.775
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF404	From: C To: Q	t_{PLH} t_{PHL}	0.656 0.557	0.757 0.701	0.837 0.822	0.907 0.923	0.977 1.007
	From: C To: QN	t_{PLH} t_{PHL}	0.791 0.926	0.828 1.003	0.892 1.087	0.972 1.180	1.069 1.312
	From: SN To: Q	t_{PLH}	0.782	0.902	0.984	1.052	1.117
	From: SN To: QN	t_{PHL}	0.288	0.397	0.496	0.594	0.681
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF406	From: C To: Q	t_{PLH} t_{PHL}	0.704 0.613	0.817 0.764	0.893 0.907	0.956 0.998	1.010 1.095
	From: C To: QN	t_{PLH} t_{PHL}	0.957 1.046	0.992 1.148	1.050 1.241	1.112 1.321	1.186 1.387
	From: SN To: Q	t_{PLH}	0.976	1.058	1.145	1.211	1.277
	From: SN To: QN	t_{PHL}	0.315	0.441	0.546	0.636	0.719

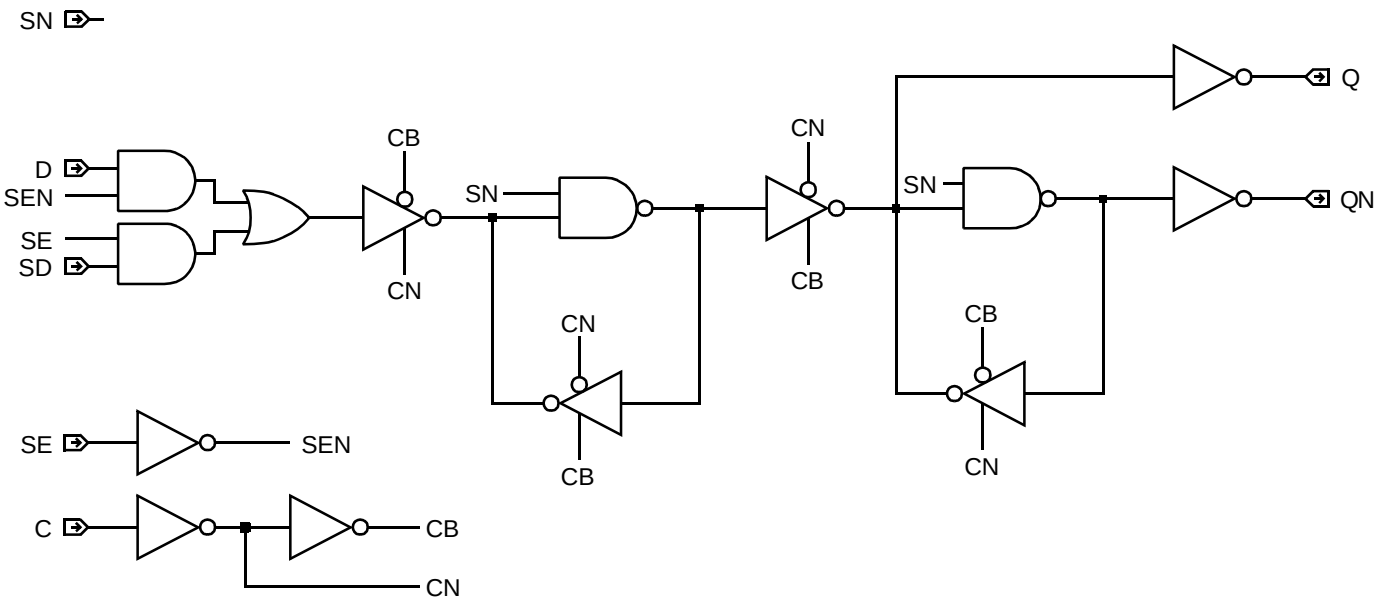
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF401	DF402	DF404	DF406
Min C Width	High	t_w	0.640	0.738	0.772	0.871
Min C Width	Low	t_w	0.765	0.786	0.855	0.857
Min SN Width	Low	t_w	0.587	0.744	0.697	0.857
Min D Setup		t_{su}	0.647	0.648	0.680	0.680
Min D Hold		t_h	0.166	0.167	0.190	0.190
Min SD Setup		t_{su}	0.647	0.648	0.680	0.680
Min SD Hold		t_h	0.166	0.167	0.190	0.190
Min SE Setup		t_{su}	0.774	0.774	0.806	0.806
Min SE Hold		t_h	0.166	0.167	0.190	0.190
Min SN Setup		t_{su}	0.176	0.179	0.225	0.225
Min SN Hold		t_h	0.559	0.558	0.613	0.604

Logic Schematic

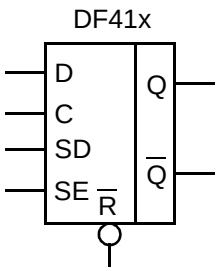


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DF41x is a family of static, master-slave, multiplexed scan D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF41x *inst_name* (Q, QN, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF41x port map (Q, QN, C, D, RN, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF411	DF412	DF414	DF416
C	1.1	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.1	1.0	1.0	1.0
SD	1.1	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF411	7.6	9.011	20.5
DF412	7.9	10.342	22.9
DF414	10.6	14.965	34.6
DF416	11.9	17.721	40.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF411	From: C To: Q	t_{PLH} t_{PHL}	0.597 0.497	0.673 0.607	0.772 0.743	0.890 0.904	0.975 1.031
	From: C To: QN	t_{PLH} t_{PHL}	0.643 0.849	0.708 0.944	0.800 1.068	0.919 1.216	1.005 1.321
	From: RN To: Q	t_{PHL}	0.936	1.047	1.190	1.361	1.488
	From: RN To: QN	t_{PLH}	0.402	0.471	0.568	0.693	0.792
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF412	From: C To: Q	t_{PLH} t_{PHL}	0.604 0.549	0.710 0.707	0.792 0.826	0.866 0.930	0.947 1.044
	From: C To: QN	t_{PLH} t_{PHL}	0.756 0.970	0.834 1.077	0.903 1.172	0.968 1.263	1.043 1.369
	From: RN To: Q	t_{PHL}	1.094	1.256	1.368	1.462	1.562
	From: RN To: QN	t_{PLH}	0.401	0.489	0.567	0.634	0.715
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF414	From: C To: Q	t_{PLH} t_{PHL}	0.651 0.544	0.749 0.705	0.830 0.821	0.898 0.920	0.974 1.013
	From: C To: QN	t_{PLH} t_{PHL}	0.754 0.921	0.818 1.097	0.882 1.203	0.937 1.289	0.992 1.368
	From: RN To: Q	t_{PHL}	1.115	1.262	1.377	1.474	1.562
	From: RN To: QN	t_{PLH}	0.433	0.513	0.589	0.652	0.713
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF416	From: C To: Q	t_{PLH} t_{PHL}	0.700 0.636	0.809 0.764	0.876 0.880	0.940 0.992	0.999 1.092
	From: C To: QN	t_{PLH} t_{PHL}	0.897 1.123	0.964 1.224	1.016 1.327	1.060 1.423	1.098 1.510
	From: RN To: Q	t_{PHL}	1.291	1.473	1.580	1.660	1.723
	From: RN To: QN	t_{PLH}	0.471	0.555	0.609	0.676	0.747

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

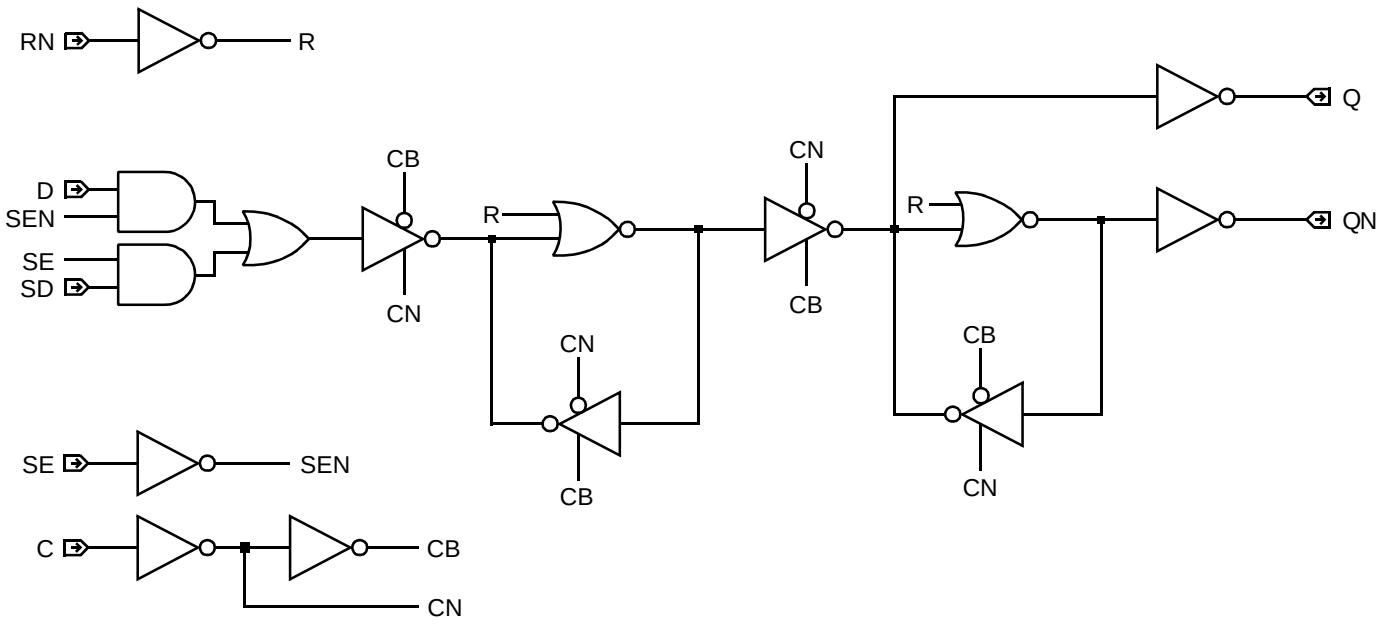
AMI500SXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF411	DF412	DF414	DF416
Min C Width	High	t_w	0.657	0.762	0.810	0.927
Min C Width	Low	t_w	0.742	0.731	0.827	0.827
Min RN Width	Low	t_w	0.583	0.576	0.662	0.662
Min D Setup		t_{su}	0.614	0.615	0.658	0.658
Min D Hold		t_h	0.167	0.171	0.189	0.189
Min SD Setup		t_{su}	0.614	0.615	0.658	0.658
Min SD Hold		t_h	0.167	0.171	0.189	0.189
Min SE Setup		t_{su}	0.748	0.743	0.787	0.787
Min SE Hold		t_h	0.167	0.171	0.189	0.189
Min RN Setup		t_{su}	0.325	0.318	0.421	0.421
Min RN Hold		t_h	0.348	0.350	0.380	0.380

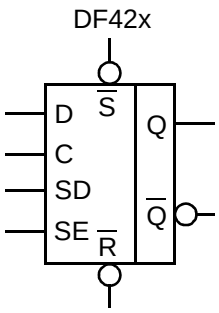
Logic Schematic



Description

DF42x is a family of static, master-slave, multiplexed scan D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

HDL Syntax

Verilog ..... DF421x *inst_name* (Q, QN, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF421x port map (Q, QN, C, D, RN, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF421	DF422	DF424	DF426
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SN	2.1	2.1	2.1	2.1

AMI500SXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF421	8.7	10.119	22.0
DF422	9.2	11.488	24.8
DF424	11.1	15.617	33.8
DF426	12.4	18.369	39.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF421	From: C To: Q	t_{PLH} t_{PHL}	0.603 0.533	0.674 0.636	0.777 0.771	0.911 0.936	1.010 1.052
	From: C To: QN	t_{PLH} t_{PHL}	0.709 0.921	0.785 1.018	0.878 1.149	0.985 1.313	1.065 1.436
	From: RN To: Q	t_{PHL}	1.004	1.124	1.268	1.439	1.562
	From: RN To: QN	t_{PLH}	0.456	0.528	0.628	0.751	0.849
	From: SN To: Q	t_{PLH}	0.735	0.823	0.929	1.050	1.148
	From: SN To: QN	t_{PHL}	0.288	0.382	0.511	0.671	0.788
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF422	From: C To: Q	t_{PLH} t_{PHL}	0.631 0.557	0.743 0.715	0.841 0.843	0.934 0.956	1.039 1.082
	From: C To: QN	t_{PLH} t_{PHL}	0.840 1.081	0.917 1.207	0.988 1.301	1.053 1.382	1.128 1.480
	From: RN To: Q	t_{PHL}	1.178	1.349	1.474	1.581	1.712
	From: RN To: QN	t_{PLH}	0.497	0.600	0.680	0.751	0.842
	From: SN To: Q	t_{PLH}	0.857	0.975	1.076	1.172	1.281
	From: SN To: QN	t_{PHL}	0.309	0.432	0.535	0.626	0.734

	Number of Equivalent Loads		1	10	20	30	40 (max)
DF424	From: C To: Q	t_{PLH} t_{PHL}	1.107 0.930	1.160 1.042	1.228 1.136	1.299 1.233	1.374 1.327
	From: C To: QN	t_{PLH} t_{PHL}	0.701 0.831	0.757 0.957	0.825 1.043	0.902 1.122	0.982 1.245
	From: RN To: Q	t_{PHL}	0.677	0.814	0.932	1.033	1.120
	From: RN To: QN	t_{PLH}	1.202	1.280	1.336	1.382	1.444
	From: SN To: Q	t_{PLH}	0.445	0.525	0.592	0.660	0.741
	From: SN To: QN	t_{PHL}	0.986	1.084	1.182	1.271	1.352
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF426	From: C To: Q	t_{PLH} t_{PHL}	1.175 1.024	1.255 1.133	1.313 1.235	1.365 1.328	1.426 1.435
	From: C To: QN	t_{PLH} t_{PHL}	0.786 0.942	0.878 1.064	0.947 1.156	1.003 1.237	1.065 1.317
	From: RN To: Q	t_{PHL}	0.762	0.870	0.978	1.077	1.166
	From: RN To: QN	t_{PLH}	1.276	1.346	1.410	1.465	1.525
	From: SN To: Q	t_{PLH}	0.511	0.585	0.654	0.718	0.790
	From: SN To: QN	t_{PHL}	1.084	1.198	1.299	1.389	1.468

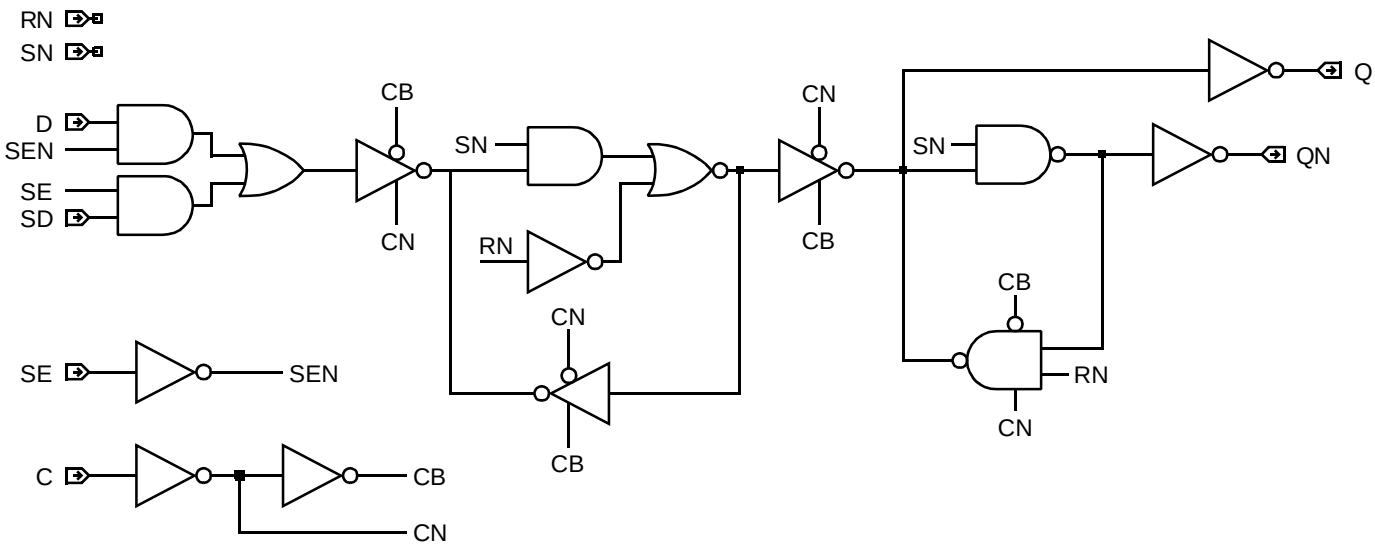
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF421	DF422	DF424	DF426
Min C Width	High	t_w	0.707	0.831	0.711	0.714
Min C Width	Low	t_w	0.767	0.778	0.770	0.775
Min RN Width	Low	t_w	0.629	0.649	0.610	0.617
Min SN Width	Low	t_w	0.591	0.731	0.593	0.598
Min D Setup		t_{su}	0.651	0.653	0.650	0.652
Min D Hold		t_h	0.170	0.170	0.171	0.170
Min SD Setup		t_{su}	0.651	0.653	0.650	0.652
Min SD Hold		t_h	0.170	0.170	0.171	0.170
Min SE Setup		t_{su}	0.776	0.777	0.778	0.779
Min SE Hold		t_h	0.170	0.170	0.171	0.170
Min RN Setup		t_{su}	0.366	0.374	0.366	0.363
Min RN Hold		t_h	0.352	0.352	0.353	0.353
Min SN Setup		t_{su}	0.217	0.217	0.214	0.216
Min SN Hold		t_h	0.557	0.560	0.559	0.560

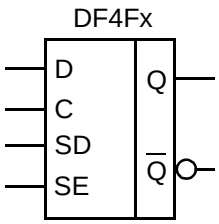
Logic Schematic



Description

DF4Fx is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF4Fx *inst_name* (Q, QN, C, D, SD, SE);

VHDL..... *inst_name*: DF4Fx port map (Q, QN, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF4F1	DF4F2	DF4F4	DF4F6
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF4F1	6.2	8.153	16.6
DF4F2	7.1	9.491	18.9
DF4F4	9.0	13.616	27.6
DF4F6	10.3	17.026	34.5

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF4F1	From: C To: Q	t_{PLH} t_{PHL}	0.584 0.522	0.655 0.636	0.751 0.775	0.870 0.933	0.957 1.040
	From: C To: QN	t_{PLH} t_{PHL}	0.620 0.746	0.677 0.830	0.761 0.945	0.874 1.090	0.959 1.195
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF4F2	From: C To: Q	t_{PLH} t_{PHL}	0.602 0.539	0.702 0.686	0.786 0.805	0.862 0.912	0.946 1.036
	From: C To: QN	t_{PLH} t_{PHL}	0.731 0.822	0.796 0.934	0.861 1.026	0.927 1.110	1.007 1.211
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF4F4	From: C To: Q	t_{PLH} t_{PHL}	0.953 0.891	1.031 1.008	1.092 1.093	1.144 1.171	1.230 1.258
	From: C To: QN	t_{PLH} t_{PHL}	0.616 0.722	0.685 0.830	0.755 0.940	0.827 1.040	0.908 1.111
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF4F6	From: C To: Q	t_{PLH} t_{PHL}	0.973 0.898	1.017 1.000	1.079 1.085	1.149 1.153	1.218 1.209
	From: C To: QN	t_{PLH} t_{PHL}	0.676 0.829	0.765 0.936	0.829 1.017	0.882 1.098	0.928 1.181

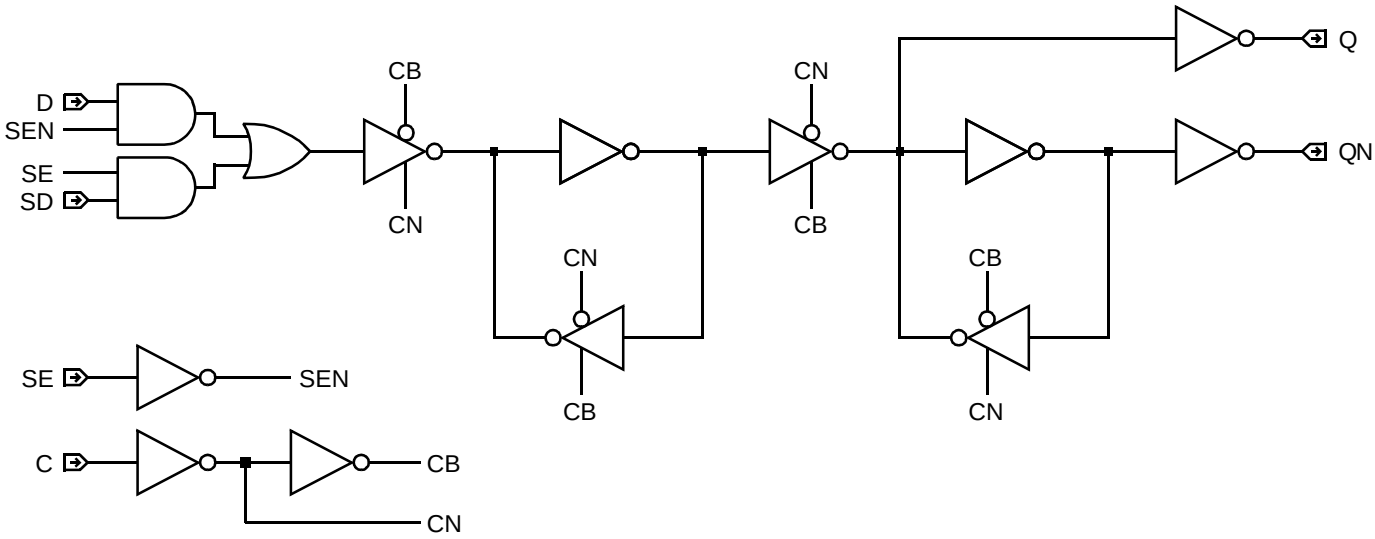
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF4F1	DF4F2	DF4F4	DF4F6
Min C Width	High	t_w	0.590	0.680	0.614	0.655
Min C Width	Low	t_w	0.709	0.710	0.708	0.706
Min D Setup		t_{su}	0.596	0.596	0.595	0.593
Min D Hold		t_h	0.168	0.169	0.168	0.168
Min SD Setup		t_{su}	0.596	0.596	0.595	0.593
Min SD Hold		t_h	0.168	0.169	0.168	0.168
Min SE Setup		t_{su}	0.722	0.722	0.723	0.721
Min SE Hold		t_h	0.168	0.169	0.168	0.168

Logic Schematic

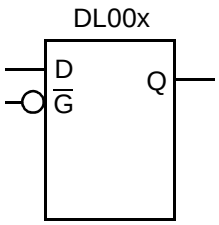


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DL00x is a family of transparent, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q
L	L	L
L	H	H
H	X	NC

NC = No Change

HDL Syntax

Verilog ..... DL00x *inst_name* (Q, D, GN);

VHDL..... *inst_name*: DL00x port map (Q, D, GN);

Pin Loading

Pin Name	Equivalent Loads	
	DL001	DL002
D	1.0	1.0
GN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL001	2.6	3.324	3.9
DL002	2.9	3.993	5.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL001	From: D To: Q	t_{PLH} t_{PHL}	0.301 0.353	0.370 0.448	0.466 0.573	0.588 0.723	0.678 0.829
	From: GN To: Q	t_{PLH} t_{PHL}	0.360 0.501	0.424 0.588	0.519 0.709	0.641 0.860	0.732 0.969
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL002	From: D To: Q	t_{PLH} t_{PHL}	0.322 0.377	0.404 0.510	0.482 0.609	0.557 0.700	0.646 0.807
	From: GN To: Q	t_{PLH} t_{PHL}	0.383 0.514	0.478 0.638	0.553 0.744	0.620 0.843	0.694 0.956

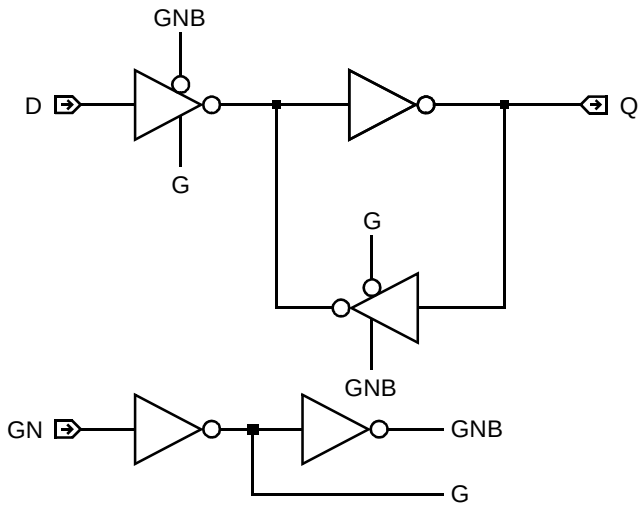
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL001	Cell DL002
Min GN Width	Low	t_w	0.504	0.512
Min D Setup		t_{su}	0.350	0.371
Min D Hold		t_h	0.138	0.138

Logic Schematic



Core Logic

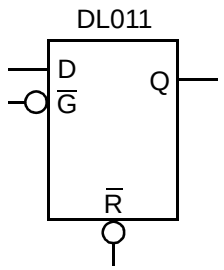
DL011

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DL011 is a transparent, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q
H	L	L	L
H	H	L	H
H	X	H	NC
L	X	X	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
RN	1.0

Equivalent Gates 3.4

HDL Syntax

Verilog ..... DL011 *inst_name* (Q, D, GN, RN);

VHDL..... *inst_name*: DL011 port map (Q, D, GN, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.112	nA
EQL_{pd}	6.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.351 0.371	0.404 0.419	0.514 0.506	0.684 0.626	0.800 0.701
GN	Q	t_{PLH} t_{PHL}	0.420 0.511	0.472 0.552	0.578 0.638	0.739 0.770	0.848 0.860
RN	Q	t_{PLH} t_{PHL}	0.292 0.264	0.347 0.307	0.456 0.389	0.615 0.506	0.719 0.582

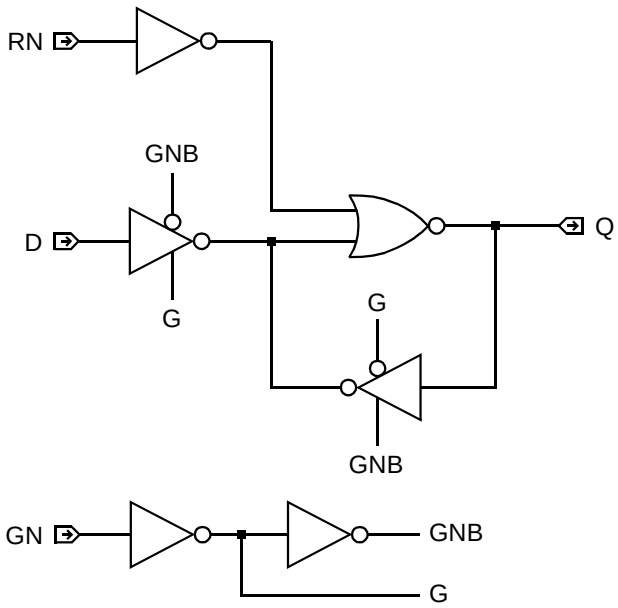
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.518
Min RN Width	Low	t_w	0.663
Min D Setup		t_{su}	0.367
Min D Hold		t_h	0.140
Min RN Setup		t_{su}	0.290
Min RN Hold		t_h	0.214

Logic Schematic



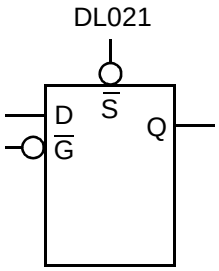
DL021

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DL021 is a transparent, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q
L	X	X	H
H	H	X	NC
H	L	L	L
H	L	H	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0

Equivalent Gates 2.9

HDL Syntax

Verilog ..... DL021 *inst_name* (Q, D, GN, SN);

VHDL..... *inst_name*: DL021 port map (Q, D, GN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.784	nA
EQL_{pd}	4.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.322 0.384	0.362 0.445	0.442 0.554	0.560 0.702	0.639 0.794
GN	Q	t_{PLH} t_{PHL}	0.398 0.540	0.435 0.603	0.508 0.710	0.613 0.850	0.682 0.936
SN	Q	t_{PLH} t_{PHL}	0.132 0.186	0.173 0.238	0.248 0.332	0.353 0.472	0.420 0.573

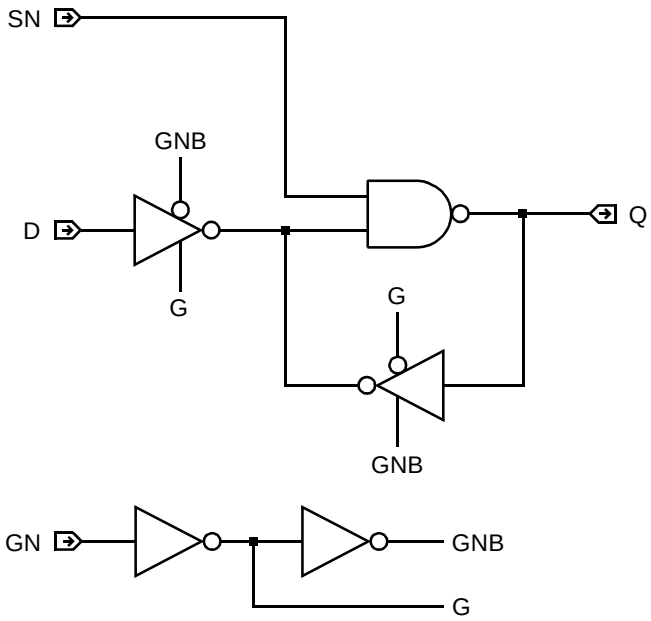
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.533
Min SN Width	Low	t_w	0.710
Min D Setup		t_{su}	0.385
Min D Hold		t_h	0.134
Min SN Setup		t_{su}	0.188
Min SN Hold		t_h	0.482

Logic Schematic



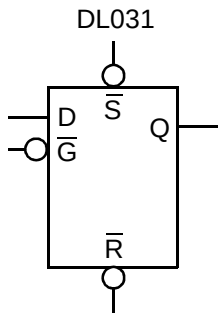
DL031

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DL031 is a transparent, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	X	H	NC
H	H	L	L	L
H	H	H	L	H

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.1
GN	1.0
SN	1.0
RN	1.1

Equivalent Gates 3.7

HDL Syntax

Verilog ..... DL031 *inst_name* (Q, D, GN, RN, SN);

VHDL..... *inst_name*: DL031 port map (Q, D, GN, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.664	nA
EQL_{pd}	6.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.440 0.492	0.486 0.556	0.569 0.672	0.680 0.833	0.749 0.934
GN	Q	t_{PLH} t_{PHL}	0.504 0.669	0.549 0.736	0.631 0.849	0.742 0.994	0.812 1.082
SN	Q	t_{PLH} t_{PHL}	0.146 0.202	0.186 0.253	0.259 0.349	0.362 0.494	0.428 0.596
RN	Q	t_{PLH} t_{PHL}	0.460 0.408	0.507 0.471	0.591 0.583	0.706 0.738	0.779 0.835

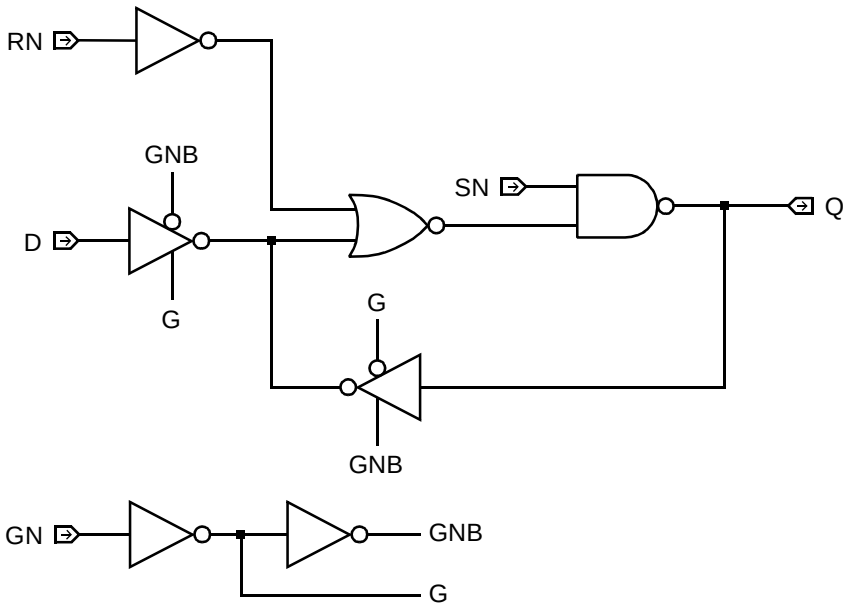
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.662
Min RN Width	Low	t_w	0.138
Min SN Width	Low	t_w	0.670
Min D Setup		t_{su}	0.491
Min D Hold		t_h	0.139
Min SN Setup		t_{su}	0.204
Min SN Hold		t_h	0.425
Min RN Setup		t_{su}	0.459
Min RN Hold		t_h	0.214

Logic Schematic



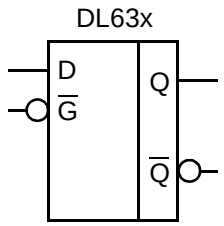
DL63x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

DL63x is a family of transparent, buffered D latches with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DL63x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL63x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL631	DL632	DL634	DL636
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL631	4.2	5.470	9.2
DL632	4.7	6.808	11.3
DL634	6.1	10.218	18.2
DL636	7.4	13.627	25.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL631	From: D To: Q	t_{PLH} t_{PHL}	0.561 0.589	0.627 0.670	0.715 0.787	0.825 0.939	0.904 1.052
	From: D To: QN	t_{PLH} t_{PHL}	0.467 0.498	0.528 0.587	0.616 0.705	0.729 0.850	0.812 0.953
	From: GN To: Q	t_{PLH} t_{PHL}	0.620 0.730	0.683 0.803	0.771 0.919	0.884 1.078	0.966 1.200
	From: GN To: QN	t_{PLH} t_{PHL}	0.614 0.554	0.673 0.643	0.760 0.762	0.876 0.906	0.962 1.008
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL632	From: D To: Q	t_{PLH} t_{PHL}	0.617 0.645	0.688 0.743	0.757 0.832	0.825 0.917	0.907 1.015
	From: D To: QN	t_{PLH} t_{PHL}	0.469 0.492	0.554 0.620	0.628 0.720	0.698 0.811	0.777 0.910
	From: GN To: Q	t_{PLH} t_{PHL}	0.679 0.797	0.747 0.895	0.816 0.988	0.887 1.078	0.972 1.182
	From: GN To: QN	t_{PLH} t_{PHL}	0.618 0.547	0.707 0.677	0.784 0.781	0.857 0.873	0.941 0.976
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DL634	From: D To: Q	t_{PLH} t_{PHL}	0.697 0.768	0.754 0.836	0.822 0.950	0.891 1.044	0.963 1.111
	From: D To: QN	t_{PLH} t_{PHL}	0.509 0.494	0.570 0.605	0.639 0.697	0.704 0.780	0.766 0.859
	From: GN To: Q	t_{PLH} t_{PHL}	0.744 0.902	0.833 1.013	0.901 1.101	0.958 1.182	1.011 1.260
	From: GN To: QN	t_{PLH} t_{PHL}	0.630 0.557	0.697 0.642	0.768 0.739	0.844 0.837	0.924 0.934

	Number of Equivalent Loads		1	14	29	44	58 (max)
DL636	From: D To: Q	t_{PLH} t_{PHL}	0.728 0.750	0.778 0.861	0.840 0.950	0.904 1.025	0.964 1.089
	From: D To: QN	t_{PLH} t_{PHL}	0.542 0.542	0.628 0.666	0.704 0.765	0.767 0.854	0.821 0.933
	From: GN To: Q	t_{PLH} t_{PHL}	0.785 0.917	0.832 0.996	0.892 1.082	0.960 1.166	1.029 1.243
	From: GN To: QN	t_{PLH} t_{PHL}	0.695 0.602	0.772 0.707	0.845 0.794	0.912 0.891	0.971 0.991

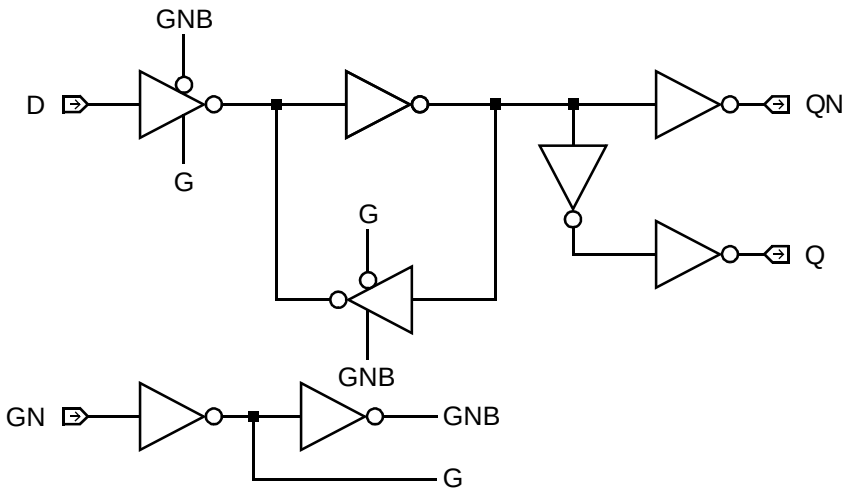
Delay will vary with input conditions. See page 2-Reference for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL631	DL632	DL634	DL636
Min GN Width	Low	t_w	0.521	0.555	0.591	0.644
Min D Setup		t_{su}	0.369	0.403	0.442	0.493
Min D Hold		t_h	0.138	0.138	0.138	0.138

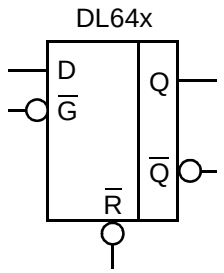
Logic Schematic



Description

DL64x is a family of transparent, buffered D latches with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

HDL Syntax

Verilog ..... DL64x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL64x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL641	DL642	DL644	DL646
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL641	4.2	5.575	9.6
DL642	4.5	6.900	12.0
DL644	7.4	12.375	23.6
DL646	8.4	15.116	29.3

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL641	From: D To: Q	t_{PLH} t_{PHL}	0.440 0.516	0.527 0.632	0.638 0.775	0.774 0.940	0.869 1.053
	From: D To: QN	t_{PLH} t_{PHL}	0.651 0.643	0.719 0.732	0.815 0.854	0.937 1.007	1.026 1.117
	From: GN To: Q	t_{PLH} t_{PHL}	0.504 0.673	0.593 0.786	0.703 0.926	0.831 1.090	0.919 1.203
	From: GN To: QN	t_{PLH} t_{PHL}	0.813 0.707	0.878 0.790	0.974 0.911	1.102 1.071	1.196 1.189
	From: RN To: Q	t_{PLH} t_{PHL}	0.461 0.372	0.548 0.479	0.663 0.616	0.803 0.782	0.901 0.898
	From: RN To: QN	t_{PLH} t_{PHL}	0.522 0.670	0.586 0.757	0.682 0.876	0.810 1.029	0.905 1.145
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL642	From: D To: Q	t_{PLH} t_{PHL}	0.460 0.532	0.576 0.705	0.670 0.834	0.755 0.946	0.849 1.067
	From: D To: QN	t_{PLH} t_{PHL}	0.762 0.735	0.827 0.841	0.893 0.940	0.960 1.036	1.040 1.148
	From: GN To: Q	t_{PLH} t_{PHL}	0.536 0.703	0.653 0.862	0.740 0.979	0.817 1.080	0.902 1.189
	From: GN To: QN	t_{PLH} t_{PHL}	0.944 0.813	1.008 0.917	1.061 1.009	1.110 1.095	1.164 1.192
	From: RN To: Q	t_{PLH} t_{PHL}	0.484 0.378	0.603 0.533	0.699 0.646	0.785 0.743	0.880 0.847
	From: RN To: QN	t_{PLH} t_{PHL}	0.582 0.769	0.648 0.872	0.718 0.965	0.789 1.054	0.876 1.157

	Number of Equivalent Loads		1	10	20	30	40 (max)
DL644	From: D To: Q	t_{PLH} t_{PHL}	0.716 0.622	0.802 0.740	0.862 0.834	0.913 0.921	0.962 1.004
	From: D To: QN	t_{PLH} t_{PHL}	0.760 0.848	0.825 0.958	0.887 1.043	0.946 1.119	1.003 1.198
	From: GN To: Q	t_{PLH} t_{PHL}	0.763 0.754	0.851 0.870	0.922 0.971	0.982 1.067	1.035 1.165
	From: GN To: QN	t_{PLH} t_{PHL}	0.922 0.920	0.965 0.994	1.019 1.086	1.077 1.182	1.136 1.282
	From: RN To: Q	t_{PLH} t_{PHL}	0.642 0.507	0.700 0.622	0.769 0.721	0.842 0.807	0.918 0.887
	From: RN To: QN	t_{PLH} t_{PHL}	0.638 0.804	0.707 0.872	0.768 0.954	0.823 1.043	0.874 1.139
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DL646	From: D To: Q	t_{PLH} t_{PHL}	0.744 0.662	0.806 0.741	0.852 0.809	0.890 0.869	0.924 0.925
	From: D To: QN	t_{PLH} t_{PHL}	0.849 0.965	0.889 1.027	0.922 1.079	0.952 1.123	0.979 1.163
	From: GN To: Q	t_{PLH} t_{PHL}	0.820 0.821	0.861 0.892	0.903 0.956	0.943 1.014	0.982 1.068
	From: GN To: QN	t_{PLH} t_{PHL}	0.987 1.026	1.029 1.059	1.065 1.111	1.096 1.173	1.124 1.244
	From: RN To: Q	t_{PLH} t_{PHL}	0.661 0.571	0.722 0.628	0.774 0.706	0.818 0.778	0.856 0.833
	From: RN To: QN	t_{PLH} t_{PHL}	0.722 0.876	0.753 0.944	0.791 1.001	0.832 1.057	0.874 1.116

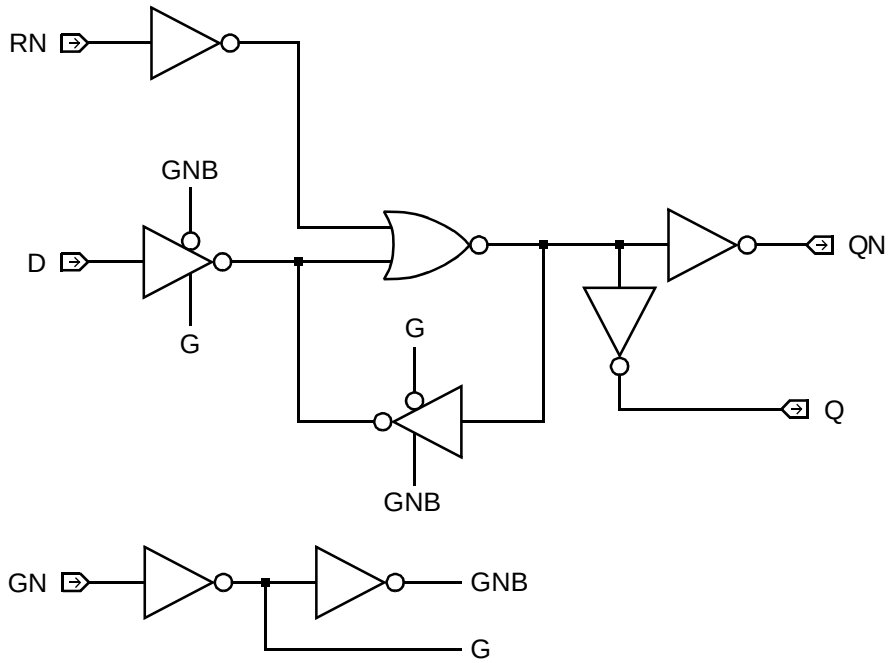
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL641	DL642	DL644	DL646
Min GN Width	Low	t_w	0.535	0.668	0.538	0.538
Min RN Width	Low	t_w	0.401	0.490	0.534	0.535
Min D Setup		t_{su}	0.535	0.668	0.388	0.388
Min D Hold		t_h	0.141	0.142	0.141	0.141
Min RN Setup		t_{su}	0.350	0.406	0.318	0.317
Min RN Hold		t_h	0.213	0.213	0.283	0.283

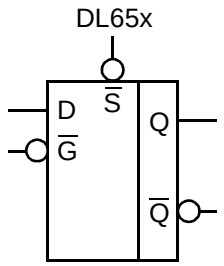
Logic Schematic



Description

DL65x is a family of transparent, buffered D latches with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

HDL Syntax

Verilog ..... DL65x *inst_name* (Q, QN, D, GN, SN);

VHDL..... *inst_name*: DL65x port map (Q, QN, D, GN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL651	DL652	DL654	DL656
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL651	4.7	5.934	9.8
DL652	5.0	7.272	12.2
DL654	6.9	12.053	22.0
DL656	8.2	14.807	27.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL651	From: D To: Q	t_{PLH} t_{PHL}	0.606 0.645	0.666 0.724	0.754 0.841	0.869 0.995	0.955 1.110
	From: D To: QN	t_{PLH} t_{PHL}	0.518 0.537	0.585 0.628	0.678 0.749	0.793 0.898	0.877 1.004
	From: GN To: Q	t_{PLH} t_{PHL}	0.673 0.794	0.729 0.861	0.816 0.973	0.935 1.137	1.026 1.267
	From: GN To: QN	t_{PLH} t_{PHL}	0.669 0.596	0.741 0.687	0.833 0.808	0.944 0.956	1.021 1.060
	From: SN To: Q	t_{PLH} t_{PHL}	0.408 0.448	0.466 0.527	0.557 0.643	0.682 0.795	0.778 0.908
	From: SN To: QN	t_{PLH} t_{PHL}	0.311 0.335	0.389 0.436	0.486 0.564	0.601 0.717	0.680 0.824
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL652	From: D To: Q	t_{PLH} t_{PHL}	0.682 0.703	0.739 0.802	0.805 0.896	0.876 0.987	0.967 1.095
	From: D To: QN	t_{PLH} t_{PHL}	0.521 0.539	0.611 0.665	0.689 0.772	0.762 0.870	0.844 0.981
	From: GN To: Q	t_{PLH} t_{PHL}	0.741 0.864	0.813 0.965	0.884 1.054	0.955 1.137	1.040 1.229
	From: GN To: QN	t_{PLH} t_{PHL}	0.675 0.603	0.772 0.737	0.848 0.839	0.916 0.930	0.990 1.029
	From: SN To: Q	t_{PLH} t_{PHL}	0.486 0.501	0.555 0.600	0.621 0.692	0.687 0.781	0.764 0.886
	From: SN To: QN	t_{PLH} t_{PHL}	0.319 0.344	0.415 0.485	0.491 0.587	0.563 0.677	0.653 0.781

	Number of Equivalent Loads		1	10	20	30	40 (max)
DL654	From: D To: Q	t_{PLH} t_{PHL}	0.619 0.674	0.681 0.757	0.757 0.855	0.838 0.957	0.921 1.060
	From: D To: QN	t_{PLH} t_{PHL}	0.792 0.772	0.867 0.867	0.925 0.959	0.978 1.047	1.030 1.138
	From: GN To: Q	t_{PLH} t_{PHL}	0.696 0.811	0.766 0.951	0.837 1.042	0.904 1.114	0.969 1.175
	From: GN To: QN	t_{PLH} t_{PHL}	0.941 0.851	0.985 0.924	1.048 1.014	1.121 1.109	1.201 1.206
	From: SN To: Q	t_{PLH} t_{PHL}	0.423 0.456	0.519 0.568	0.594 0.668	0.654 0.754	0.704 0.834
	From: SN To: QN	t_{PLH} t_{PHL}	0.572 0.590	0.639 0.687	0.701 0.775	0.757 0.850	0.810 0.919
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DL656	From: D To: Q	t_{PLH} t_{PHL}	0.653 0.725	0.718 0.829	0.794 0.919	0.871 0.999	0.944 1.067
	From: D To: QN	t_{PLH} t_{PHL}	0.877 0.863	0.926 0.930	0.988 1.019	1.051 1.114	1.112 1.207
	From: GN To: Q	t_{PLH} t_{PHL}	0.733 0.875	0.807 0.977	0.872 1.068	0.930 1.149	0.981 1.219
	From: GN To: QN	t_{PLH} t_{PHL}	1.059 0.941	1.111 1.013	1.157 1.099	1.197 1.187	1.231 1.269
	From: SN To: Q	t_{PLH} t_{PHL}	0.484 0.500	0.555 0.601	0.613 0.696	0.677 0.788	0.744 0.875
	From: SN To: QN	t_{PLH} t_{PHL}	0.656 0.682	0.730 0.780	0.798 0.863	0.858 0.935	0.908 0.997

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

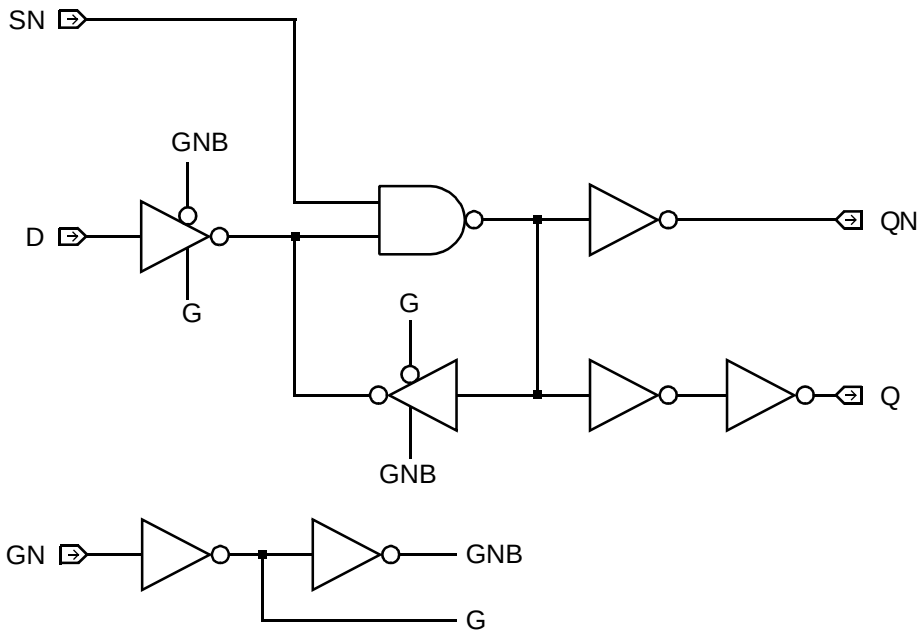
AMI500SXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL651	DL652	DL654	DL656
Min GN Width	Low	t_w	0.567	0.602	0.560	0.560
Min SN Width	Low	t_w	0.536	0.577	0.526	0.525
Min D Setup		t_{su}	0.412	0.446	0.406	0.405
Min D Hold		t_h	0.135	0.135	0.135	0.135
Min SN Setup		t_{su}	0.217	0.249	0.210	0.211
Min SN Hold		t_h	0.484	0.484	0.484	0.482

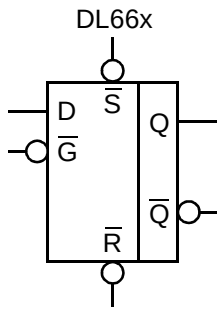
Logic Schematic



Description

DL66x is a family of transparent, buffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DL66x *inst_name* (Q, QN, D, GN, RN, SN);

VHDL..... *inst_name*: DL66x port map (Q, QN, D, GN, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL661	DL662	DL664	DL666
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	2.0	2.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL661	4.7	6.757	11.5
DL662	5.3	8.101	14.0
DL664	9.0	14.260	28.5
DL666	9.5	17.001	34.2

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL661	From: D To: Q	t_{PLH} t_{PHL}	0.730 0.758	0.793 0.830	0.878 0.940	0.982 1.090	1.057 1.204
	From: D To: QN	t_{PLH} t_{PHL}	0.639 0.672	0.708 0.769	0.802 0.893	0.916 1.041	0.997 1.145
	From: GN To: Q	t_{PLH} t_{PHL}	0.800 0.919	0.851 0.975	0.933 1.079	1.049 1.239	1.139 1.372
	From: GN To: QN	t_{PLH} t_{PHL}	0.802 0.729	0.876 0.814	0.969 0.937	1.079 1.097	1.156 1.214
	From: SN To: Q	t_{PLH} t_{PHL}	0.421 0.440	0.477 0.524	0.564 0.641	0.685 0.789	0.778 0.896
	From: SN To: QN	t_{PLH} t_{PHL}	0.323 0.349	0.404 0.450	0.502 0.581	0.617 0.738	0.695 0.848
	From: R To: Q	t_{PLH} t_{PHL}	0.755 0.666	0.815 0.747	0.899 0.859	1.007 1.001	1.086 1.103
	From: RN To: QN	t_{PLH} t_{PHL}	0.549 0.702	0.614 0.799	0.706 0.923	0.823 1.072	0.909 1.177
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL662	From: D To: Q	t_{PLH} t_{PHL}	0.808 0.831	0.872 0.938	0.937 1.034	1.003 1.125	1.081 1.230
	From: D To: QN	t_{PLH} t_{PHL}	0.649 0.666	0.745 0.792	0.822 0.900	0.892 1.001	0.970 1.115
	From: GN To: Q	t_{PLH} t_{PHL}	0.856 1.018	0.917 1.098	0.987 1.179	1.061 1.261	1.154 1.359
	From: GN To: QN	t_{PLH} t_{PHL}	0.815 0.717	0.913 0.849	0.989 0.957	1.056 1.055	1.130 1.165
	From: SN To: Q	t_{PLH} t_{PHL}	0.497 0.535	0.568 0.627	0.635 0.717	0.701 0.806	0.779 0.911
	From: SN To: QN	t_{PLH} t_{PHL}	0.340 0.362	0.444 0.506	0.525 0.612	0.596 0.706	0.675 0.813
	From: RN To: Q	t_{PLH} t_{PHL}	0.826 0.756	0.885 0.854	0.948 0.946	1.014 1.035	1.096 1.140
	From: RN To: QN	t_{PLH} t_{PHL}	0.561 0.688	0.662 0.826	0.741 0.930	0.810 1.022	0.885 1.123

	Number of Equivalent Loads		1	10	20	30	40 (max)
DL664	From: D To: Q	t_{PLH} t_{PHL}	0.726 0.707	0.814 0.803	0.888 0.898	0.952 0.988	1.012 1.074
	From: D To: QN	t_{PLH} t_{PHL}	0.801 0.888	0.876 0.998	0.943 1.092	1.005 1.174	1.062 1.247
	From: GN To: Q	t_{PLH} t_{PHL}	0.799 0.847	0.864 0.952	0.934 1.044	1.000 1.127	1.062 1.205
	From: GN To: QN	t_{PLH} t_{PHL}	0.958 0.966	1.015 1.052	1.080 1.139	1.147 1.212	1.215 1.267
	From: SN To: Q	t_{PLH} t_{PHL}	0.346 0.435	0.423 0.533	0.494 0.618	0.560 0.710	0.625 0.822
	From: SN To: QN	t_{PLH} t_{PHL}	0.545 0.501	0.631 0.599	0.680 0.693	0.744 0.772	0.806 0.840
	From: RN To: Q	t_{PLH} t_{PHL}	0.639 0.543	0.712 0.650	0.786 0.746	0.849 0.843	0.897 0.949
	From: RN To: QN	t_{PLH} t_{PHL}	0.667 0.797	0.737 0.887	0.806 0.965	0.872 1.034	0.935 1.098
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DL666	From: D To: Q	t_{PLH} t_{PHL}	0.863 0.781	0.921 0.890	0.982 0.996	1.052 1.094	1.124 1.184
	From: D To: QN	t_{PLH} t_{PHL}	0.980 1.040	1.024 1.135	1.077 1.231	1.130 1.322	1.180 1.406
	From: GN To: Q	t_{PLH} t_{PHL}	0.918 0.962	0.972 1.079	1.044 1.170	1.119 1.248	1.192 1.313
	From: GN To: QN	t_{PLH} t_{PHL}	1.151 1.142	1.198 1.245	1.257 1.321	1.319 1.384	1.379 1.436
	From: SN To: Q	t_{PLH} t_{PHL}	0.418 0.495	0.490 0.615	0.562 0.719	0.632 0.818	0.697 0.908
	From: SN To: QN	t_{PLH} t_{PHL}	0.668 0.624	0.745 0.697	0.812 0.792	0.874 0.891	0.930 0.986
	From: RN To: Q	t_{PLH} t_{PHL}	0.714 0.611	0.767 0.749	0.843 0.851	0.925 0.938	1.008 1.015
	From: RN To: QN	t_{PLH} t_{PHL}	0.816 0.931	0.875 1.048	0.938 1.133	0.999 1.204	1.055 1.262

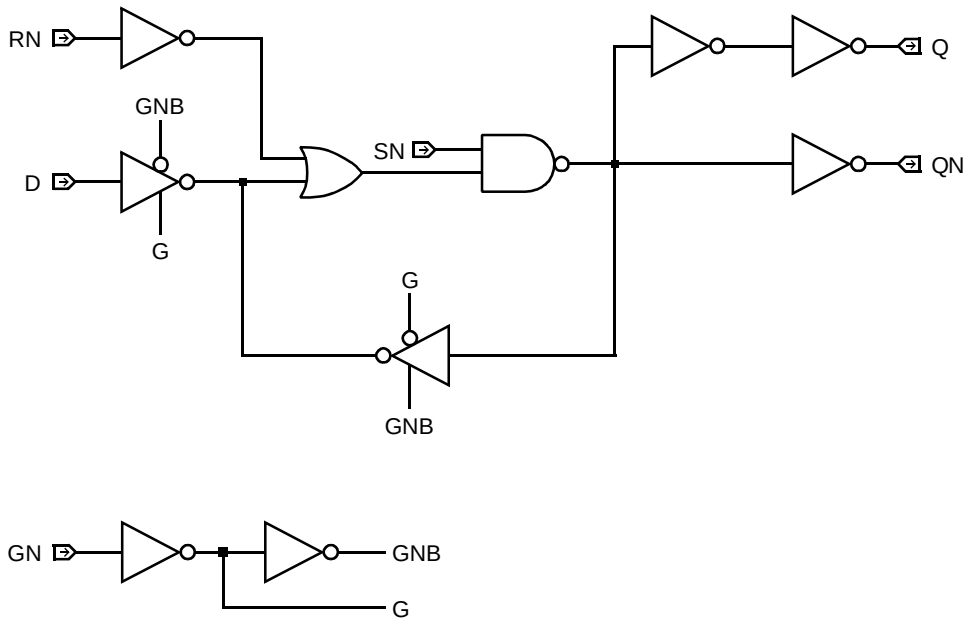
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL661	DL662	DL664	DL666
Min GN Width	Low	t_w	0.690	0.733	0.589	0.641
Min RN Width	Low	t_w	0.447	0.489	0.310	0.327
Min SN Width	Low	t_w	0.499	0.547	0.603	0.702
Min D Setup		t_{su}	0.526	0.568	0.439	0.491
Min D Hold		t_h	0.140	0.138	0.134	0.152
Min SN Setup		t_{su}	0.225	0.266	0.187	0.211
Min SN Hold		t_h	0.430	0.425	0.562	0.648
Min RN Setup		t_{su}	0.492	0.515	0.342	0.372
Min RN Hold		t_h	0.217	0.213	0.349	0.391

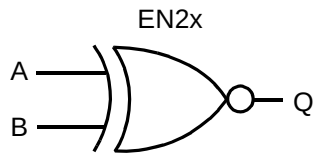
Logic Schematic



Description

EN2x is a family of 2-input gates which perform the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... EN2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EN2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EN21	EN22	EN23	EN24	EN26
A	2.0	4.0	4.0	4.0	4.0
B	2.0	4.0	4.0	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EN21	1.8	2.593	4.0
EN22	4.0	5.187	9.3
EN23	5.3	5.583	13.2
EN24	5.5	6.601	15.5
EN26	6.3	7.710	19.0

a. See page 2-13 for power equation.

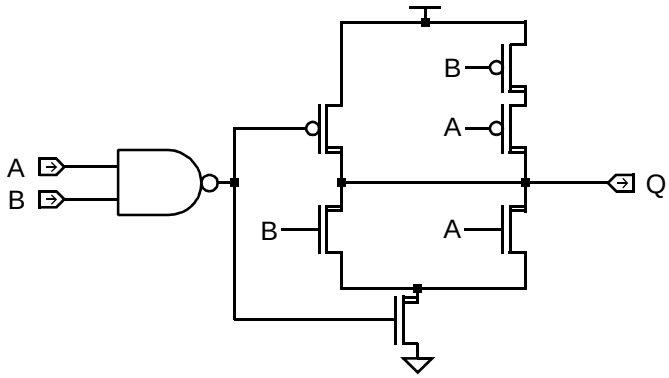
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

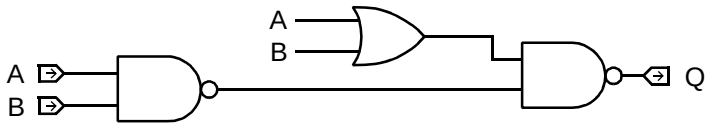
EN21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.263 0.186	0.292 0.247	0.349 0.353	0.435 0.510	0.492 0.627
EN22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.245 0.133	0.273 0.205	0.317 0.299	0.376 0.410	0.421 0.486
EN23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.240 0.438	0.320 0.557	0.395 0.663	0.469 0.764	0.555 0.879
EN24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.294 0.456	0.374 0.615	0.459 0.746	0.537 0.835	0.610 0.911
EN26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.350 0.534	0.434 0.674	0.505 0.794	0.578 0.900	0.653 0.995

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



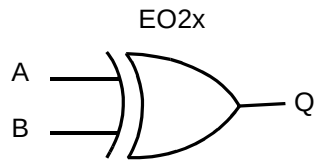
LOGICAL



Description

EO2x is a family of 2-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... EO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EO21	EO22	EO23	EO24	EO26
A	2.1	4.0	4.0	4.0	4.0
B	2.0	4.0	4.0	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO21	1.8	2.276	4.4
EO22	4.2	4.461	9.8
EO23	5.0	6.600	12.8
EO24	5.5	7.964	15.7
EO26	6.3	9.339	18.6

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

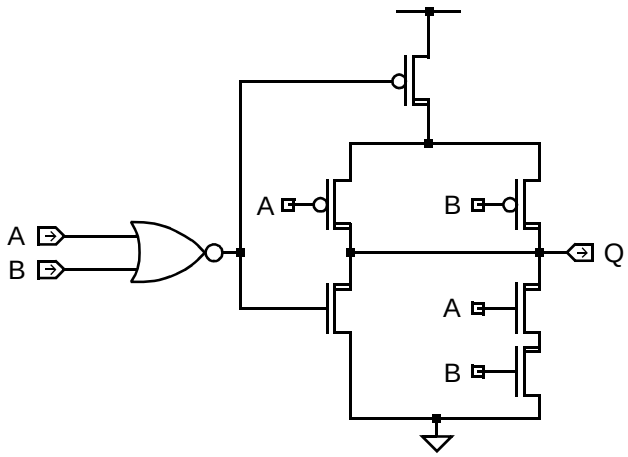
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

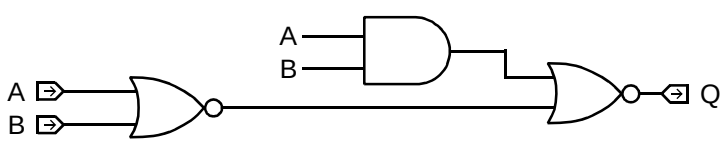
EO21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.304 0.207	0.350 0.274	0.446 0.403	0.597 0.596	0.700 0.727
EO22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.264 0.166	0.319 0.236	0.397 0.326	0.497 0.443	0.571 0.536
EO23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.224 0.390	0.314 0.510	0.384 0.608	0.452 0.698	0.537 0.799
EO24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.239 0.419	0.330 0.540	0.414 0.615	0.481 0.706	0.538 0.819
EO26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.268 0.455	0.372 0.573	0.464 0.673	0.535 0.773	0.588 0.867

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



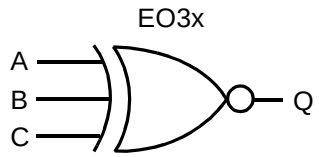
LOGICAL



Description

EO3x is a family of 3-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

HDL Syntax

Verilog ..... EO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: EO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	EO31	EO32	EO33	EO34	EO36
A	2.0	2.0	2.0	2.0	2.0
B	2.0	2.1	2.0	2.0	2.0
C	2.0	3.1	3.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO31	3.7	4.423	10.7
EO32	5.3	5.624	16.0
EO33	6.3	6.999	18.8
EO34	6.9	8.368	21.6
EO36	7.6	9.752	24.5

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

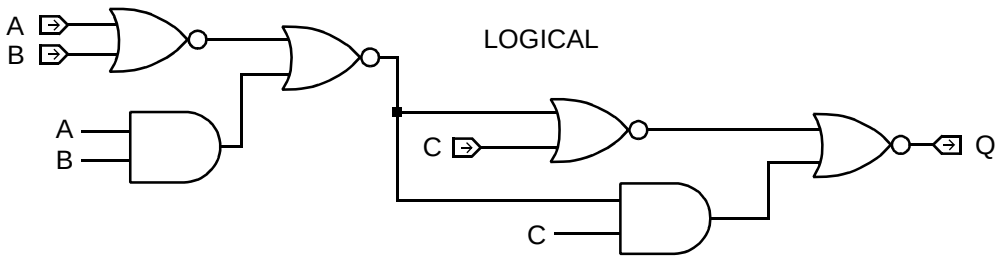
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.689 0.601	0.738 0.671	0.839 0.812	0.996 1.024	1.102 1.166
EO32	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.786 0.721	0.845 0.773	0.916 0.880	0.997 1.017	1.053 1.113
EO33	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.711 0.914	0.808 1.011	0.885 1.095	0.952 1.174	1.027 1.264
EO34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.776 0.923	0.845 1.052	0.919 1.144	0.990 1.234	1.061 1.326
EO36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.845 0.976	0.931 1.079	0.993 1.175	1.044 1.263	1.112 1.339

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

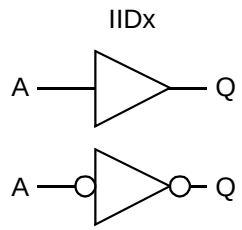
Logic Schematic



Description

IIDx is a family of non-inverting clock drivers with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... IIDx *inst_name* (Q, A);

VHDL..... *inst_name*: IIDx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads				
	IID1	IID2	IID3	IID4	IID6
A	1.0	1.0	2.0	1.9	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IID1	1.1	1.457	2.5
IID2	1.3	2.125	3.6
IID3	2.1	3.510	5.6
IID4	2.4	4.178	6.7
IID6	2.6	5.552	9.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

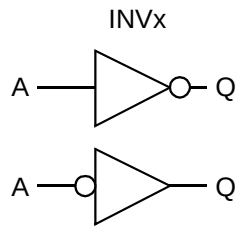
IID1	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.198 0.196	0.258 0.285	0.344 0.406	0.462 0.558	0.555 0.667
IID2	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.206 0.229	0.301 0.347	0.384 0.448	0.462 0.547	0.551 0.671
IID3	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.171 0.167	0.253 0.269	0.331 0.369	0.394 0.451	0.464 0.541
IID4	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.208 0.186	0.268 0.289	0.328 0.375	0.389 0.457	0.452 0.538
IID6	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.216 0.199	0.286 0.308	0.354 0.409	0.417 0.495	0.473 0.568

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

INVx is a family of inverters which perform the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

HDL Syntax

Verilog ..... INVx *inst_name* (Q, A);

VHDL..... *inst_name*: INVx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads					
	INV1	INV2	INV3	INV4	INV5	INV6
A	1.0	1.9	2.9	3.9	4.9	5.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
INV1	0.8	0.755	0.8
INV2	1.1	1.458	1.6
INV3	1.3	2.126	1.7
INV4	1.6	2.795	1.8
INV5	2.1	3.510	2.6
INV6	2.1	4.182	3.0

a. See page 2-13 power equation

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

INV1	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.077 0.143	0.152 0.237	0.253 0.369	0.371 0.547	0.451 0.684
INV2	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.056 0.099	0.147 0.208	0.224 0.301	0.292 0.389	0.368 0.492
INV3	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.047 0.067	0.143 0.181	0.218 0.290	0.274 0.375	0.330 0.464
INV4	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.042 0.075	0.121 0.168	0.192 0.253	0.258 0.341	0.323 0.431
INV5	**Number of Equivalent Loads**		**1**	**12**	**24**	**37**	**49 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.047 0.065	0.122 0.174	0.181 0.265	0.243 0.357	0.302 0.441
INV6	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.038 0.060	0.130 0.185	0.200 0.293	0.257 0.386	0.304 0.464

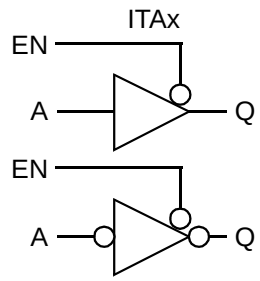
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ITAx is a family of non-inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

HDL Syntax

Verilog ..... ITAx *inst_name* (Q, A, EN);

VHDL..... *inst_name*: ITAx port map (Q, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITA1	ITA2	ITA4	ITA6
A	1.0	1.0	1.0	1.0
EN	1.5	2.1	3.2	4.4
Q	0.7	0.9	1.8	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITA1	1.8	2.239	4.3
ITA2	2.1	2.961	6.5
ITA4	3.2	4.460	11.3
ITA6	4.2	5.962	16.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITA1	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.272 0.273	0.805 0.936	1.394 1.654	1.931 2.313	2.523 3.048
	From: EN To: Q	t_{ZH} t_{ZL}	0.166 0.187	0.700 0.866	1.266 1.587	1.785 2.241	2.365 2.969
ITA2	**Number of Equivalent Loads**		**1**	**17**	**34**	**50**	**67 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.291 0.270	0.697 0.788	1.139 1.337	1.567 1.854	2.029 2.401
	From: EN To: Q	t_{ZH} t_{ZL}	0.141 0.143	0.561 0.679	0.981 1.233	1.386 1.750	1.828 2.295
ITA4	**Number of Equivalent Loads**		**1**	**28**	**57**	**86**	**114 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.314 0.371	0.679 0.795	1.066 1.257	1.456 1.728	1.839 2.189
	From: EN To: Q	t_{ZH} t_{ZL}	0.076 0.160	0.503 0.649	0.850 1.113	1.188 1.572	1.522 2.019
ITA6	**Number of Equivalent Loads**		**1**	**40**	**80**	**121**	**161 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.379 0.426	0.740 0.868	1.095 1.291	1.462 1.731	1.827 2.175
	From: EN To: Q	t_{ZH} t_{ZL}	0.050 0.173	0.499 0.637	0.826 1.071	1.133 1.522	1.420 1.967

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

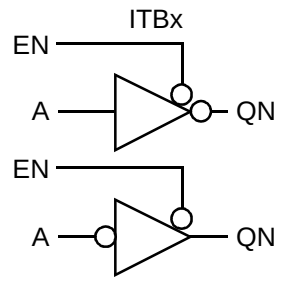
Delay (ns) From	To	Parameter	Cell			
			ITA1	**ITA2**	**ITA4**	**ITA6**
EN	Q	t_{HZ} t_{LZ}	0.125 0.144	0.124 0.162	0.122 0.220	0.122 0.272

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ITBx is a family of inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITBx *inst_name* (QN, A, EN);

VHDL..... *inst_name*: ITBx port map (QN, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITB1	ITB2	ITB4	ITB6
A	1.0	2.0	4.0	5.9
EN	1.5	2.1	3.2	4.4
QN	0.7	0.9	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITB1	1.3	1.524	2.6
ITB2	1.8	2.258	3.7
ITB4	2.9	3.759	6.6
ITB6	4.0	5.260	9.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITB1	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.154 0.194	0.711 0.885	1.286 1.590	1.806 2.229	2.388 2.952
	From: EN To: QN	t_{ZH} t_{ZL}	0.167 0.174	0.721 0.855	1.267 1.573	1.776 2.226	2.360 2.958
ITB2	**Number of Equivalent Loads**		**1**	**17**	**34**	**50**	**67 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.119 0.164	0.568 0.719	0.999 1.240	1.411 1.739	1.866 2.293
	From: EN To: QN	t_{ZH} t_{ZL}	0.074 0.140	0.569 0.692	0.997 1.249	1.388 1.762	1.801 2.300
ITB4	**Number of Equivalent Loads**		**1**	**28**	**57**	**86**	**114 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.117 0.133	0.491 0.625	0.854 1.086	1.230 1.547	1.616 2.005
	From: EN To: QN	t_{ZH} t_{ZL}	0.058 0.148	0.541 0.641	0.916 1.125	1.236 1.602	1.513 2.062
ITB6	**Number of Equivalent Loads**		**1**	**40**	**80**	**121**	**161 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.054 0.126	0.491 0.634	0.868 1.076	1.216 1.523	1.532 1.960
	From: EN To: QN	t_{ZH} t_{ZL}	0.121 0.125	0.475 0.632	0.806 1.084	1.147 1.530	1.485 1.960

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

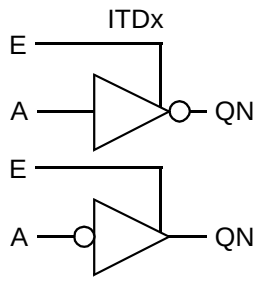
Delay (ns) From	To	Parameter	Cell ITB1	ITB2	ITB4	ITB6
EN	QN	t_{HZ} t_{LZ}	0.124 0.134	0.124 0.160	0.123 0.218	0.121 0.271

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ITD1x is a family of inverting internal tristate buffers with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITDx *inst_name* (QN, A, E);

VHDL..... *inst_name*: ITDx port map (QN, A, E);

Pin Loading

Pin Name	Equivalent Loads			
	ITD1	ITD2	ITD4	ITD6
A	1.0	2.0	4.0	5.9
E	1.4	1.8	2.6	3.5
QN	0.7	0.9	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITD1	1.3	1.524	2.7
ITD2	1.8	2.258	4.0
ITD4	2.9	3.759	7.2
ITD6	4.0	5.260	10.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITD1	**Number of Equivalent Loads**		**1**	**11**	**22**	**32**	**43 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.148 0.198	0.715 0.888	1.288 1.564	1.808 2.190	2.398 2.933
	From: E To: QN	t_{ZH} t_{ZL}	0.171 0.216	0.725 0.895	1.300 1.563	1.825 2.184	2.415 2.900
ITD2	**Number of Equivalent Loads**		**1**	**17**	**34**	**50**	**67 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.130 0.137	0.571 0.693	1.009 1.232	1.423 1.738	1.872 2.287
	From: E To: QN	t_{ZH} t_{ZL}	0.152 0.083	0.586 0.754	1.033 1.287	1.457 1.780	1.913 2.324
ITD4	**Number of Equivalent Loads**		**1**	**28**	**57**	**86**	**114 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.117 0.132	0.514 0.599	0.884 1.054	1.257 1.517	1.632 1.983
	From: E To: QN	t_{ZH} t_{ZL}	0.148 0.111	0.553 0.642	0.942 1.067	1.323 1.498	1.691 1.944
ITD6	**Number of Equivalent Loads**		**1**	**40**	**80**	**121**	**161 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.096 0.065	0.442 0.614	0.717 1.053	0.995 1.481	1.270 1.892
	From: E To: QN	t_{ZH} t_{ZL}	0.206 0.130	0.578 0.605	0.928 0.997	1.286 1.425	1.637 1.879

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

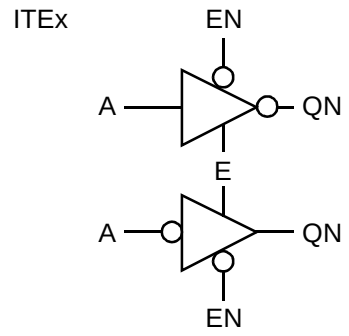
Delay (ns) From	To	Parameter	Cell ITD1	ITD2	ITD4	ITD6
E	QN	t_{HZ} t_{LZ}	0.144 0.071	0.195 0.071	0.293 0.070	0.387 0.069

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ITEx is a family of two-phase enable inverting internal tristate buffers.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

HDL Syntax

Verilog ..... ITEx *inst_name* (QN, A, E, EN);

VHDL..... *inst_name*: ITEx port map (QN, A, E, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITE1	ITE2	ITE4	ITE6
A	1.0	2.0	3.9	5.9
E	0.4	0.8	1.7	2.5
EN	0.6	1.1	2.3	3.4
QN	0.8	0.9	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITE1	1.1	0.821	1.3
ITE2	1.6	1.555	2.0
ITE4	2.4	3.044	4.1
ITE6	3.4	4.545	6.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITE1	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.146 0.199	0.712 0.864	1.287 1.584	1.814 2.234	2.422 2.946
	From: EN To: QN	t_{ZH}	0.188	0.779	1.367	1.887	2.469
	From: E To: QN	t_{ZL}	0.252	0.936	1.623	2.252	2.973
ITE2	Number of Equivalent Loads		1	17	34	50	67 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.098 0.137	0.566 0.683	1.015 1.243	1.426 1.759	1.861 2.298
	From: EN To: QN	t_{ZH}	0.161	0.689	1.106	1.467	1.836
	From: E To: QN	t_{ZL}	0.163	0.760	1.270	1.739	2.242
ITE4	Number of Equivalent Loads		1	28	57	86	114 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.104 0.149	0.544 0.593	0.910 1.042	1.255 1.514	1.585 2.005
	From: EN To: QN	t_{ZH}	0.029	0.502	0.916	1.286	1.618
	From: E To: QN	t_{ZL}	0.166	0.668	1.096	1.517	1.931
ITE6	Number of Equivalent Loads		1	40	80	121	161 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.068 0.140	0.492 0.615	0.853 1.027	1.186 1.463	1.489 1.918
	From: EN To: QN	t_{ZH}	0.131	0.564	0.884	1.215	1.559
	From: E To: QN	t_{ZL}	0.078	0.630	1.061	1.465	1.839

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ITE1	ITE2	ITE4	ITE6
EN	QN	t_{HZ}	0.125	0.124	0.124	0.122
E	QN	t_{LZ}	0.070	0.070	0.070	0.069

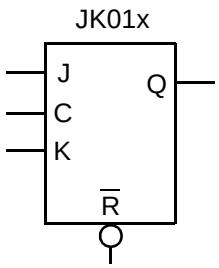
JK01x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

JK01x is a family of static, master-slave JK flip-flops. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)
L	X	X	X	L
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK01x *inst_name* (Q, C, J, K, RN);

VHDL..... *inst_name*: JK01x port map (Q, C, J, K, RN);

Pin Loading

Pin Name	Equivalent Loads	
	JK011	JK012
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
RN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK011	7.1	8.444	19.9
JK012	7.6	9.178	22.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	7	9 (max)
JK011	From: C To: Q	t_{PLH} t_{PHL}	0.721 0.630	0.772 0.688	0.879 0.794	1.049 0.943	1.166 1.039
	From: RN To: Q	t_{PHL}	0.323	0.372	0.454	0.568	0.640
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
JK012	From: C To: Q	t_{PLH} t_{PHL}	0.743 0.648	0.792 0.720	0.871 0.802	0.979 0.893	1.062 0.953
	From: RN To: Q	t_{PHL}	0.327	0.381	0.451	0.537	0.597

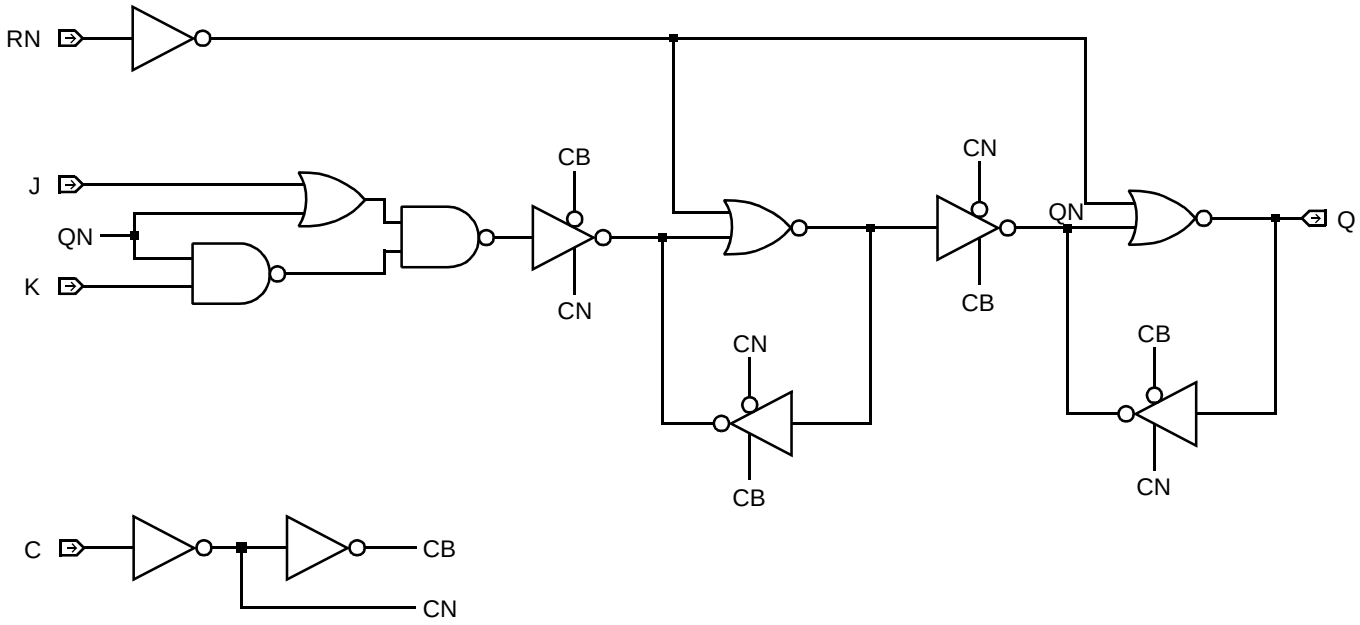
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK011	JK012
Min C Width	High	t_w	0.728	0.743
Min C Width	Low	t_w	0.675	0.673
Min RN Width	Low	t_w	0.578	0.628
Min J Setup		t_{su}	0.675	0.673
Min J Hold		t_h	0.173	0.173
Min K Setup		t_{su}	0.556	0.561
Min K Hold		t_h	0.173	0.173
Min RN Setup		t_{su}	0.320	0.360
Min RN Hold		t_h	0.346	0.345

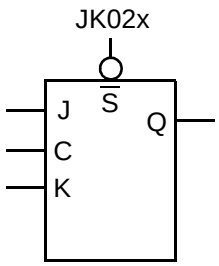
Logic Schematic



Description

JK02x is a family of static, master-slave JK flip-flops. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)
L	X	X	X	H
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK02x *inst_name* (Q, C, J, K, SN);

VHDL..... *inst_name*: JK02x port map (Q, C, J, K, SN);

Pin Loading

Pin Name	Equivalent Loads	
	JK021	JK022
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
SN	2.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK021	6.6	8.563	16.8
JK022	7.1	9.723	18.7

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	7	9 (max)
JK021	From: C To: Q	t_{PLH} t_{PHL}	0.698 0.634	0.738 0.699	0.821 0.821	0.949 0.993	1.036 1.104
	From: SN To: Q	t_{PLH}	0.130	0.169	0.240	0.349	0.418
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
JK022	From: C To: Q	t_{PLH} t_{PHL}	0.714 0.645	0.761 0.722	0.821 0.815	0.894 0.922	0.945 0.995
	From: SN To: Q	t_{PLH}	0.094	0.138	0.196	0.264	0.311

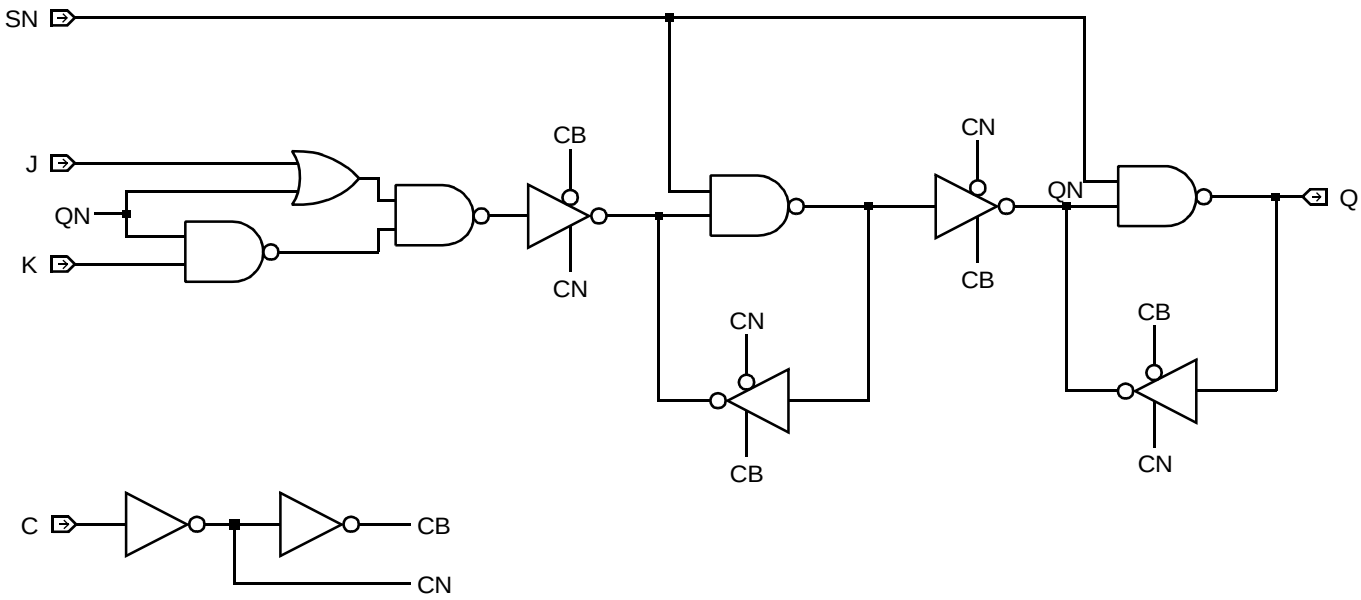
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK021	JK022
Min C Width	High	t_w	0.704	0.718
Min C Width	Low	t_w	0.676	0.670
Min SN Width	Low	t_w	0.915	0.940
Min J Setup		t_{su}	0.676	0.670
Min J Hold		t_h	0.172	0.172
Min K Setup		t_{su}	0.561	0.557
Min K Hold		t_h	0.172	0.172
Min SN Setup		t_{su}	0.174	0.171
Min SN Hold		t_h	0.567	0.568

Logic Schematic



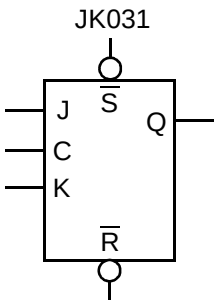
JK031

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

JK031 is a static, master-slave JK flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)
L	L	X	X	X	IL
L	H	X	X	X	L
H	L	X	X	X	H
H	H	L	L	↑	NC
H	H	L	H	↑	L
H	H	H	L	↑	H
H	H	H	H	↑	$\overline{Q(n)}$

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	1.0
SN	2.1
RN	1.0

Equivalent Gates 7.6

HDL Syntax

Verilog ..... JK031 *inst_name* (Q, C, J, K, RN, SN);

VHDL..... *inst_name*: JK031 port map (Q, C, J, K, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.700	nA
EQL_{pd}	21.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.792 0.681	0.870 0.758	1.003 0.890	1.178 1.061	1.285 1.166
RN	Q	t_{PHL}	0.361	0.424	0.550	0.725	0.837
SN	Q	t_{PLH}	0.132	0.167	0.232	0.332	0.393

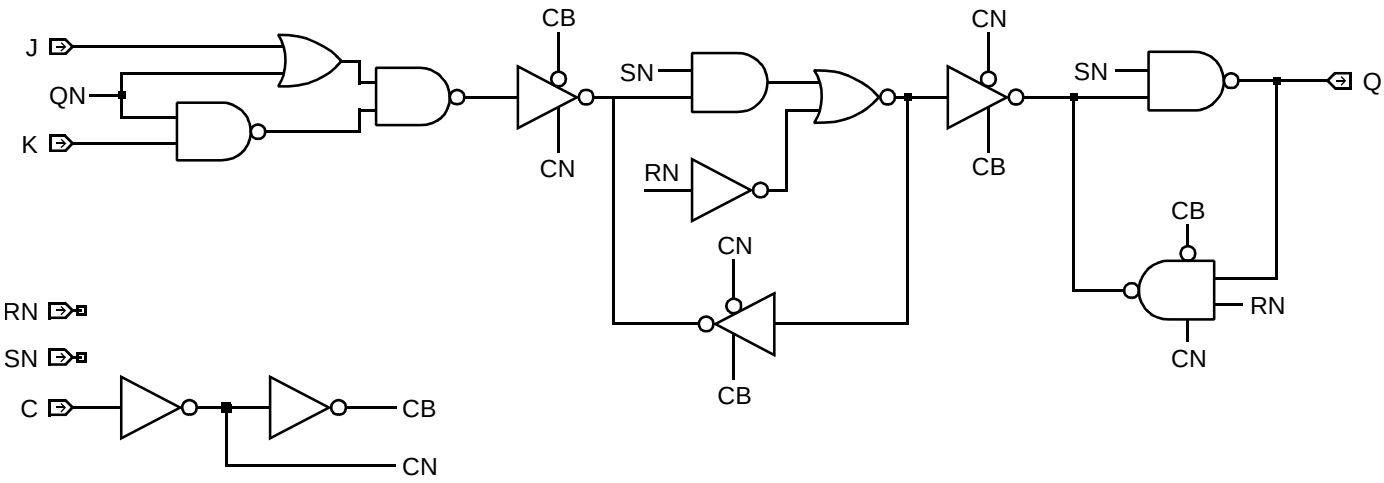
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.784
Min C Width	Low	t_w	0.721
Min RN Width	Low	t_w	0.614
Min SN Width	Low	t_w	0.895
Min J Setup		t_{su}	0.721
Min J Hold		t_h	0.172
Min K Setup		t_{su}	0.606
Min K Hold		t_h	0.172
Min RN Setup		t_{su}	0.374
Min RN Hold		t_h	0.344
Min SN Setup		t_{su}	0.215
Min SN Hold		t_h	0.566

Logic Schematic



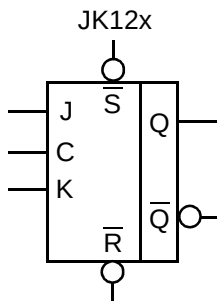
JK12x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

JK12x is a family of static, master-slave JK flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... JK12x *inst_name* (Q, QN, C, J, K, RN, SN);

VHDL..... *inst_name*: JK12x port map (Q, QN, C, J, K, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	JK121	JK122	JK124	JK126
J	1.0	1.0	1.0	1.0
K	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	2.1	2.1
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK121	8.7	11.113	25.1
JK122	9.8	13.837	31.2
JK124	11.1	16.576	37.0
JK126	12.4	19.661	43.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
JK121	From: C To: Q	t_{PLH} t_{PHL}	0.707 0.668	0.784 0.780	0.887 0.930	1.015 1.113	1.106 1.243
	From: C To: QN	t_{PLH} t_{PHL}	0.845 1.048	0.925 1.151	1.012 1.278	1.105 1.428	1.166 1.531
	From: RN To: Q	t_{PHL}	1.244	1.380	1.548	1.743	1.877
	From: RN To: QN	t_{PLH}	0.448	0.517	0.612	0.729	0.814
	From: SN To: Q	t_{PLH}	0.950	1.041	1.152	1.282	1.370
	From: SN To: QN	t_{PHL}	0.282	0.380	0.507	0.659	0.772
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
JK122	From: C To: Q	t_{PLH} t_{PHL}	1.114 0.949	1.181 1.059	1.246 1.148	1.309 1.230	1.385 1.324
	From: C To: QN	t_{PLH} t_{PHL}	0.621 0.740	0.704 0.845	0.777 0.944	0.846 1.041	0.925 1.155
	From: RN To: Q	t_{PHL}	0.686	0.815	0.916	1.006	1.104
	From: RN To: QN	t_{PLH}	1.108	1.159	1.218	1.282	1.363
	From: SN To: Q	t_{PLH}	0.449	0.543	0.618	0.685	0.758
	From: SN To: QN	t_{PHL}	0.889	0.985	1.070	1.150	1.242

AMI500SXSC 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	10	20	30	40 (max)
JK124	From: C To: Q	t_{PLH} t_{PHL}	1.203 0.983	1.289 1.133	1.348 1.231	1.396 1.327	1.438 1.427
	From: C To: QN	t_{PLH} t_{PHL}	0.705 0.809	0.763 0.956	0.840 1.051	0.911 1.125	0.970 1.188
	From: RN To: Q	t_{PHL}	0.721	0.900	1.011	1.107	1.188
	From: RN To: QN	t_{PLH}	1.210	1.288	1.342	1.385	1.423
	From: SN To: Q	t_{PLH}	0.495	0.590	0.669	0.742	0.810
	From: SN To: QN	t_{PHL}	0.977	1.059	1.153	1.248	1.344
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
JK126	From: C To: Q	t_{PLH} t_{PHL}	1.360 1.142	1.446 1.279	1.507 1.387	1.557 1.494	1.597 1.596
	From: C To: QN	t_{PLH} t_{PHL}	0.817 0.979	0.892 1.098	0.957 1.190	1.018 1.268	1.073 1.336
	From: RN To: Q	t_{PHL}	0.873	1.032	1.141	1.228	1.305
	From: RN To: QN	t_{PLH}	1.086	1.173	1.234	1.283	1.323
	From: SN To: Q	t_{PLH}	0.627	0.705	0.780	0.852	0.916
	From: SN To: QN	t_{PHL}	0.862	0.977	1.088	1.186	1.275

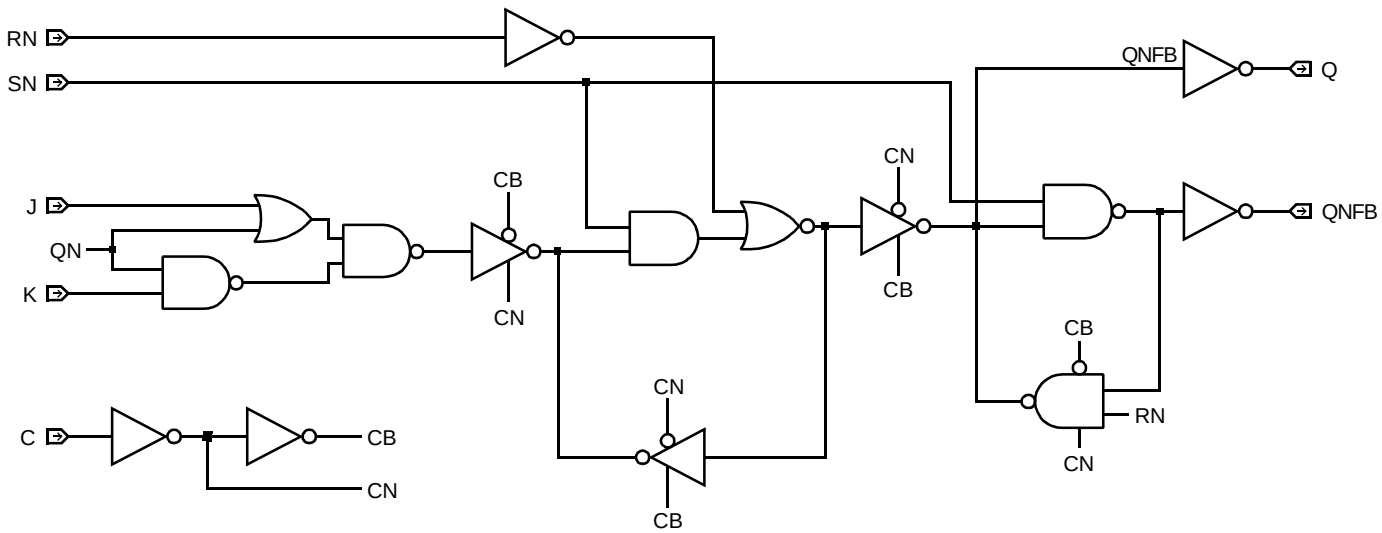
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			JK121	JK122	JK124	JK126
Min C Width	High	t_w	0.828	0.710	0.711	0.793
Min C Width	Low	t_w	0.720	0.720	0.720	0.721
Min RN Width	Low	t_w	0.613	0.613	0.613	0.613
Min SN Width	Low	t_w	0.791	0.587	0.588	0.485
Min J Setup		t_{su}	0.720	0.720	0.720	0.721
Min J Hold		t_h	0.172	0.172	0.172	0.180
Min K Setup		t_{su}	0.605	0.605	0.605	0.605
Min K Hold		t_h	0.172	0.172	0.172	0.180
Min RN Setup		t_{su}	0.374	0.375	0.375	0.375
Min RN Hold		t_h	0.344	0.344	0.344	0.352
Min SN Setup		t_{su}	0.214	0.214	0.214	0.214
Min SN Hold		t_h	0.565	0.565	0.565	0.582

Logic Schematic

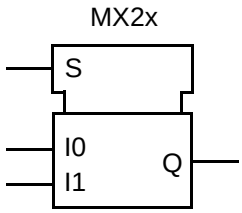


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

MX2x is a family of two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

HDL Syntax

Verilog ..... MX2x *inst_name* (Q, I0, I1, S);

VHDL..... *inst_name*: MX2x port map (Q, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MX21	MX22	MX24	MX26
I0	1.0	1.0	2.0	2.0
I1	1.0	1.0	2.0	2.0
S	1.5	1.5	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX21	2.1	2.616	5.2
MX22	2.4	3.285	6.4
MX24	4.5	7.182	13.0
MX26	5.0	8.552	15.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

MX21	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.304 0.336	0.378 0.432	0.477 0.562	0.602 0.721	0.691 0.835
	From: S To: Q	t_{PLH} t_{PHL}	0.406 0.484	0.473 0.587	0.570 0.717	0.695 0.872	0.788 0.980
MX22	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.343 0.359	0.449 0.502	0.530 0.618	0.600 0.724	0.678 0.843
	From: S To: Q	t_{PLH} t_{PHL}	0.438 0.517	0.537 0.664	0.619 0.775	0.695 0.872	0.779 0.978
MX24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.318 0.355	0.403 0.497	0.478 0.598	0.545 0.683	0.613 0.758
	From: S To: Q	t_{PLH} t_{PHL}	0.364 0.430	0.441 0.568	0.515 0.683	0.593 0.785	0.676 0.883
MX26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.369 0.393	0.458 0.515	0.537 0.623	0.615 0.726	0.689 0.829
	From: S To: Q	t_{PLH} t_{PHL}	0.413 0.507	0.478 0.659	0.559 0.776	0.642 0.874	0.721 0.956

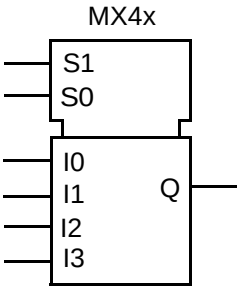
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

MX4x is a family of four-to-one digital multiplexers.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

HDL Syntax

Verilog ..... MX4x *inst_name* (Q, I0, I1, I2, I3, S0, S1);

VHDL..... *inst_name*: MX4x port map (Q, I0, I1, I2, I3, S0, S1);

Pin Loading

Pin Name	Equivalent Loads			
	MX41	MX42	MX44	MX46
I0	1.1	1.0	1.0	1.0
I1	1.1	1.0	1.0	1.0
I2	1.0	1.0	1.0	1.0
I3	1.0	1.0	1.0	1.0
S0	3.2	3.2	3.2	3.3
S1	3.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX41	4.7	5.370	14.4
MX42	6.1	9.369	19.5
MX44	7.4	11.919	25.7
MX46	7.9	13.277	28.1

a. See page 2-13 for power equation.

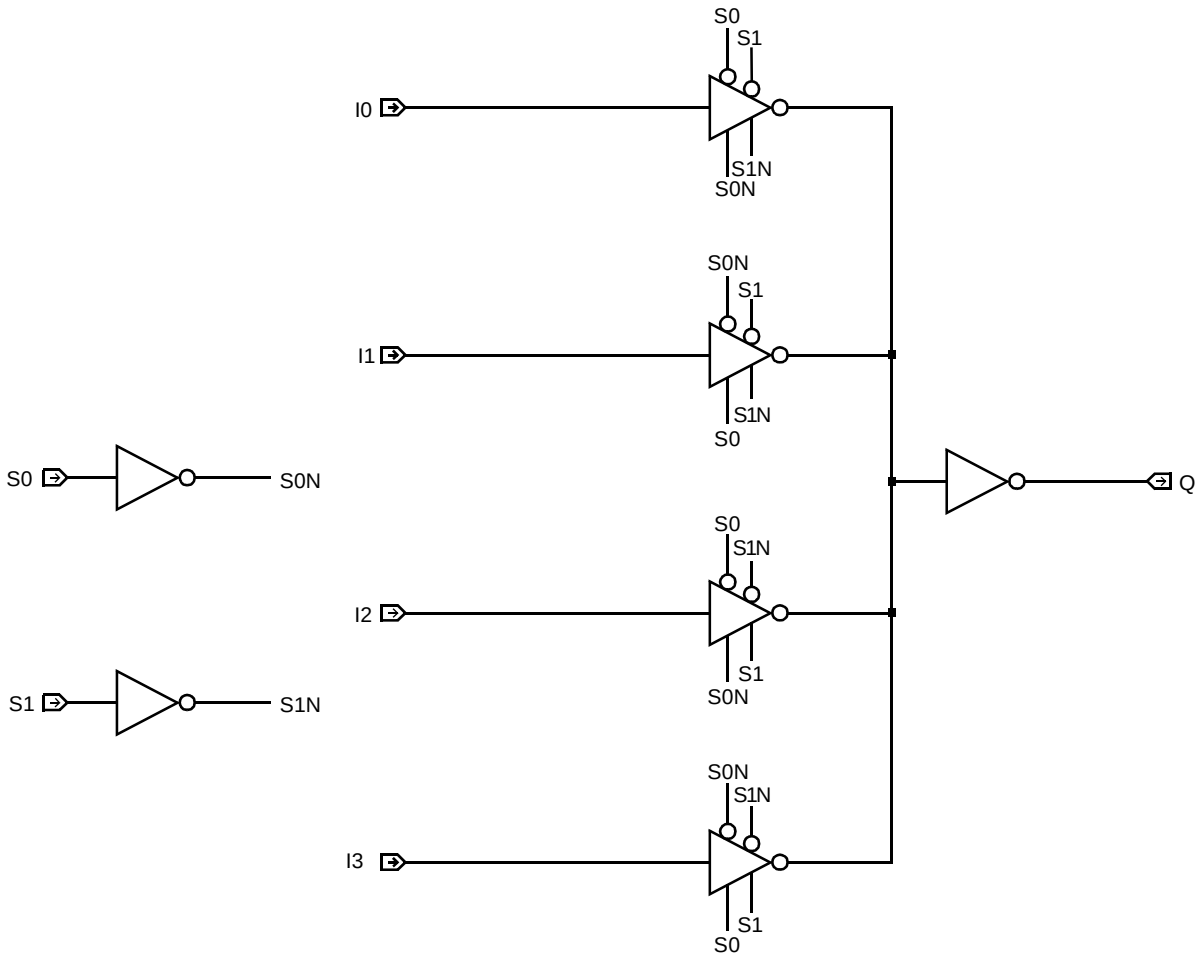
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
MX41	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.660 0.709	0.747 0.845	0.852 1.005	0.973 1.185	1.055 1.307
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.768 0.868	0.849 0.999	0.953 1.156	1.078 1.334	1.165 1.455
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
MX42	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.592 0.617	0.681 0.732	0.758 0.829	0.830 0.917	0.912 1.016
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.709 0.795	0.792 0.918	0.864 1.018	0.932 1.107	1.010 1.206
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
MX44	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.634 0.635	0.721 0.755	0.790 0.858	0.857 0.949	0.928 1.033
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.756 0.834	0.840 0.973	0.910 1.076	0.972 1.155	1.028 1.213
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
MX46	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.682 0.714	0.778 0.815	0.855 0.912	0.920 1.003	0.976 1.085
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.790 0.909	0.878 1.015	0.953 1.106	1.015 1.186	1.065 1.255

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

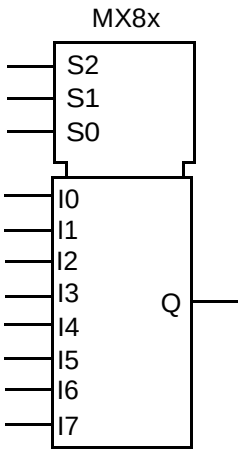
Logic Schematic



Description

MX8x is a family of eight-to-one digital multiplexers.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

HDL Syntax

Verilog ..... MX8x *inst_name* (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

VHDL..... *inst_name*: MX8x port map (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads			
	MX81	MX82	MX84	MX86
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
I2	1.0	1.0	1.0	1.0
I3	1.1	1.1	1.1	1.1
I4	1.0	1.0	1.0	1.0
I5	1.0	1.0	1.0	1.0
I6	1.0	1.0	1.0	1.0
I7	1.0	1.0	1.0	1.0
S0	5.4	5.5	5.5	5.5
S1	3.2	3.3	3.3	3.3
S2	2.1	2.2	3.2	3.2

AMI500SXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX81	9.8	13.448	33.3
MX82	11.9	18.193	43.5
MX84	11.1	16.934	42.3
MX86	11.9	18.318	45.3

a. See page 2-13 for power equation.

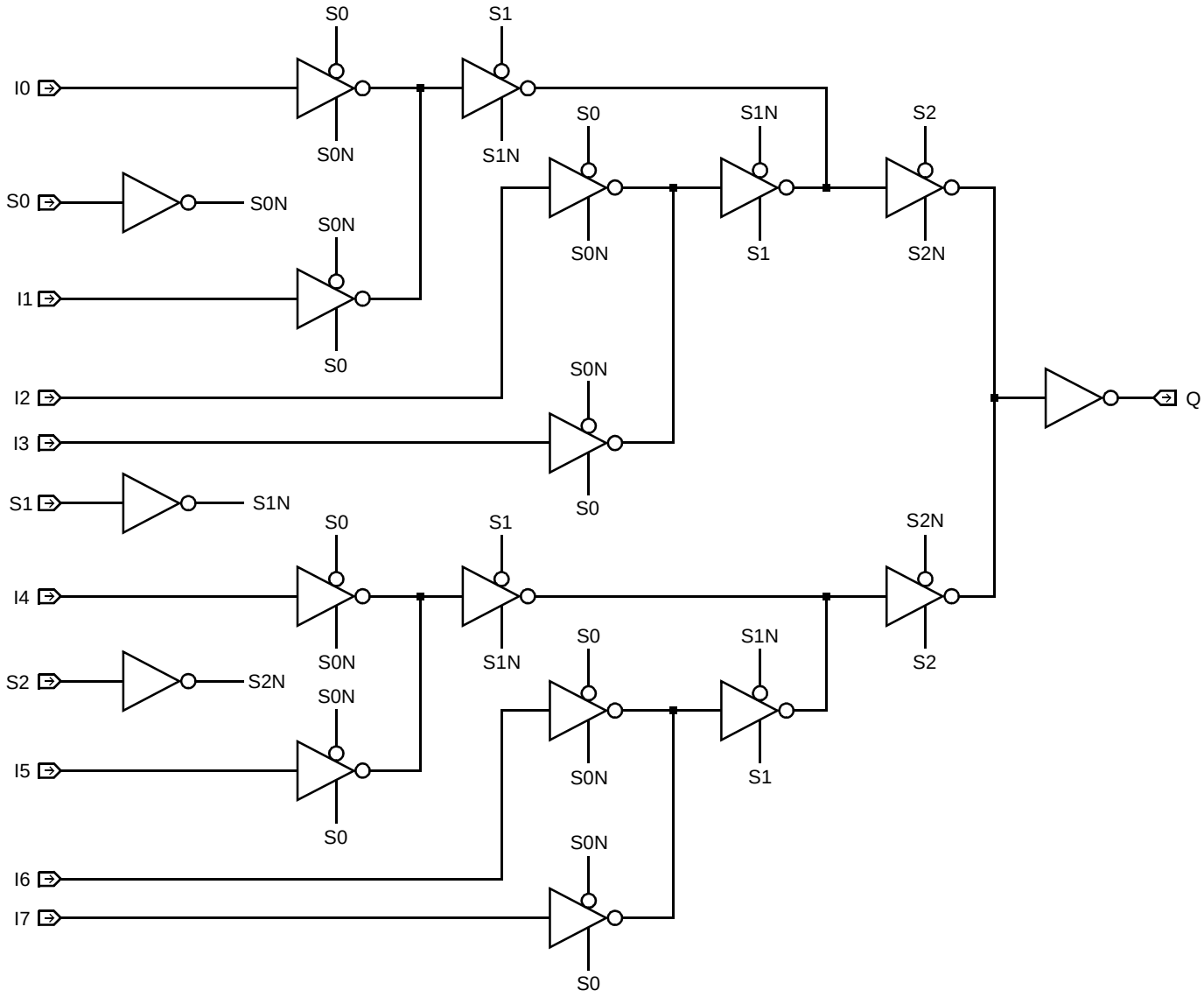
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

MX81	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.803 0.828	0.875 0.928	0.973 1.068	1.095 1.245	1.183 1.374
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.990 1.063	1.069 1.139	1.167 1.272	1.282 1.468	1.361 1.624
MX82	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.844 0.847	0.894 0.915	0.931 0.973	0.964 1.028	1.000 1.090
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.033 1.078	1.076 1.131	1.115 1.190	1.151 1.251	1.193 1.327
MX84	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.883 0.886	0.966 0.992	1.042 1.095	1.112 1.195	1.178 1.293
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.095 1.132	1.166 1.245	1.231 1.358	1.290 1.470	1.346 1.584
MX86	Number of Equivalent Loads		1	14	29	44	58 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.935 0.959	1.045 1.096	1.118 1.199	1.175 1.285	1.221 1.356
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.150 1.181	1.216 1.355	1.291 1.458	1.365 1.534	1.435 1.594

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

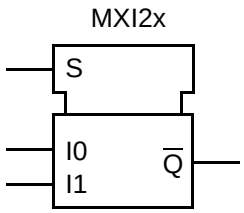


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

MXI2x is a family of inverting two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

HDL Syntax

Verilog ..... MXI2x *inst_name* (QN, I0, I1, S);

VHDL..... *inst_name*: MXI2x port map (QN, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MXI21	MXI22	MXI24	MXI26
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
S	1.5	1.5	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MXI21	2.6	3.330	6.8
MXI22	2.9	3.999	8.0
MXI24	4.2	7.081	12.9
MXI26	5.3	9.605	18.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

MXI21	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.393 0.433	0.457 0.515	0.552 0.638	0.675 0.801	0.767 0.923
	From: S To: QN	t_{PLH} t_{PHL}	0.559 0.535	0.625 0.618	0.716 0.737	0.829 0.890	0.911 1.003
MXI22	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.417 0.450	0.505 0.567	0.579 0.669	0.652 0.765	0.743 0.874
	From: S To: QN	t_{PLH} t_{PHL}	0.567 0.548	0.656 0.666	0.731 0.767	0.800 0.862	0.878 0.970
MXI24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.410 0.495	0.498 0.609	0.581 0.720	0.659 0.822	0.735 0.918
	From: S To: QN	t_{PLH} t_{PHL}	0.560 0.573	0.655 0.679	0.729 0.794	0.801 0.894	0.874 0.978
MXI26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.403 0.478	0.488 0.596	0.566 0.686	0.641 0.766	0.709 0.837
	From: S To: QN	t_{PLH} t_{PHL}	0.574 0.533	0.655 0.645	0.722 0.753	0.783 0.849	0.837 0.931

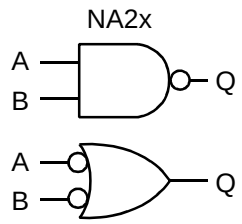
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA2x is a family of 2-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... NA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NA21	NA22	NA23	NA24	NA26
A	1.0	2.0	3.9	2.0	2.0
B	1.0	1.9	3.9	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA21	0	1.242	1.1
NA22	1.6	2.447	2.4
NA23	3.2	4.375	5.2
NA24	4.2	6.615	11.7
NA26	4.5	7.934	14.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.100 0.158	0.144 0.215	0.226 0.324	0.336 0.482	0.404 0.584
NA22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.078 0.123	0.124 0.181	0.180 0.256	0.246 0.349	0.292 0.416
NA23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.072 0.095	0.125 0.164	0.168 0.225	0.210 0.282	0.264 0.348
NA24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.274 0.334	0.347 0.426	0.420 0.521	0.488 0.615	0.553 0.710
NA26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.303 0.396	0.380 0.491	0.451 0.547	0.515 0.641	0.572 0.736

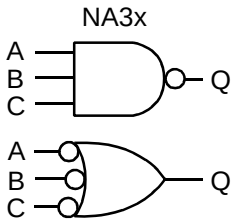
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA3x is a family of 3-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

HDL Syntax

Verilog ..... NA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NA31	NA32	NA33	NA34	NA36
A	1.0	1.9	2.0	2.0	2.0
B	1.0	1.9	2.0	1.9	2.0
C	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA31	1.3	1.652	1.7
NA32	2.4	3.234	3.1
NA33	4.0	5.420	9.0
NA34	4.7	7.454	13.1
NA36	5.5	8.826	16.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.124 0.199	0.166 0.277	0.244 0.424	0.282 0.494	0.356 0.628
NA32	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.096 0.157	0.120 0.194	0.182 0.284	0.238 0.372	0.273 0.435
NA33	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.294 0.366	0.378 0.483	0.452 0.581	0.522 0.670	0.602 0.771
NA34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.307 0.396	0.379 0.508	0.451 0.599	0.520 0.687	0.588 0.778
NA36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.346 0.439	0.425 0.533	0.494 0.623	0.557 0.708	0.612 0.786

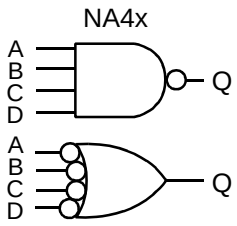
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA4x is a family of 4-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

HDL Syntax

Verilog ..... NA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NA41	NA42	NA43	NA44	NA46
A	1.0	2.0	1.9	1.9	2.0
B	1.0	2.0	1.9	1.9	2.0
C	1.0	2.0	1.9	1.9	2.0
D	1.0	2.1	1.9	1.9	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA41	1.8	2.012	2.5
NA42	2.9	3.907	3.9
NA43	5.0	6.175	10.9
NA44	5.8	8.203	14.7
NA46	6.0	9.568	17.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA41	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.145 0.225	0.197 0.296	0.246 0.361	0.291 0.426	0.375 0.565
NA42	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.113 0.171	0.139 0.209	0.187 0.279	0.252 0.382	0.292 0.452
NA43	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.325 0.415	0.414 0.519	0.488 0.617	0.556 0.711	0.634 0.822
NA44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.330 0.438	0.403 0.544	0.474 0.636	0.539 0.717	0.601 0.794
NA46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.416 0.512	0.477 0.623	0.553 0.720	0.632 0.806	0.707 0.881

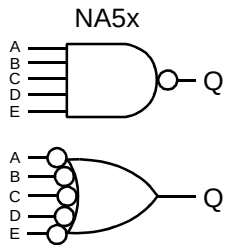
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA5x is a family of 5-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

HDL Syntax

Verilog ..... NA5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NA5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NA51	NA52	NA53	NA54	NA56
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.0	2.0	2.0
D	1.0	1.0	2.0	1.9	1.9
E	1.0	1.0	1.9	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA51	2.1	2.304	2.8
NA52	3.4	4.301	7.6
NA53	6.3	7.937	13.6
NA54	7.6	10.069	20.3
NA56	8.2	11.429	23.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.160 0.243	0.217 0.326	0.270 0.405	0.320 0.484	0.414 0.654
NA52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.331 0.432	0.401 0.524	0.498 0.648	0.618 0.802	0.705 0.912
NA53	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.310 0.447	0.397 0.575	0.472 0.680	0.542 0.775	0.620 0.881
NA54	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.323 0.473	0.392 0.599	0.466 0.694	0.541 0.787	0.615 0.881
NA56	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.359 0.570	0.433 0.680	0.501 0.773	0.568 0.867	0.629 0.953

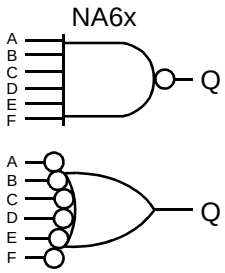
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA6x is a family of 6-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: NA6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads				
	NA61	NA62	NA63	NA64	NA66
A	1.0	2.0	2.0	2.0	1.9
B	1.0	2.0	1.9	2.0	2.0
C	1.0	1.9	1.9	1.9	1.9
D	1.0	1.9	1.9	1.9	1.9
E	1.0	1.9	1.9	1.9	1.9
F	1.0	1.9	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA61	3.4	4.707	8.4
NA62	7.6	9.540	18.7
NA63	7.9	10.233	20.4
NA64	8.4	10.916	21.5
NA66	9.0	12.278	24.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA61	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.339 0.457	0.404 0.543	0.497 0.665	0.616 0.822	0.702 0.936
NA62	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.295 0.419	0.373 0.537	0.449 0.639	0.522 0.733	0.609 0.841
NA63	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.308 0.440	0.391 0.568	0.467 0.677	0.528 0.761	0.593 0.848
NA64	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.332 0.466	0.405 0.589	0.479 0.696	0.549 0.799	0.616 0.908
NA66	Number of Equivalent Loads		1	14	29	44	58 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.361 0.521	0.418 0.673	0.492 0.792	0.570 0.888	0.645 0.965

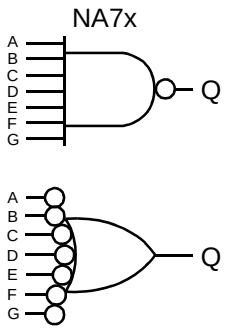
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA7x is a family of 7-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA7x *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: NA7x port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads				
	NA71	NA72	NA73	NA74	NA76
A	1.9	1.9	1.9	1.9	1.9
B	1.9	1.9	1.9	1.9	1.9
C	1.9	1.9	1.9	1.9	1.9
D	2.0	2.0	2.0	2.0	2.0
E	2.0	2.0	2.0	2.0	2.0
F	2.0	2.0	2.0	2.0	2.0
G	2.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA71	8.2	9.802	17.2
NA72	9.8	11.306	24.3
NA73	10.0	11.999	26.0
NA74	10.3	12.668	27.2
NA76	10.8	14.031	30.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA71	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.366 0.595	0.431 0.698	0.525 0.831	0.646 0.993	0.735 1.111
NA72	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.367 0.597	0.452 0.743	0.530 0.854	0.604 0.951	0.691 1.057
NA73	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.373 0.650	0.470 0.803	0.552 0.923	0.614 1.014	0.677 1.110
NA74	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.391 0.685	0.471 0.846	0.549 0.963	0.619 1.063	0.684 1.153
NA76	Number of Equivalent Loads		1	14	29	44	58 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.444 0.816	0.525 0.948	0.598 1.066	0.661 1.180	0.713 1.284

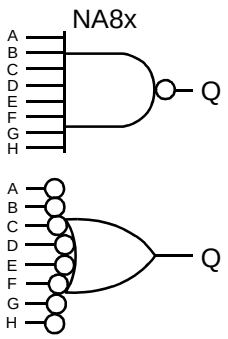
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NA8x is a family of 8-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA8x *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: NA8x port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads				
	NA81	NA82	NA83	NA84	NA86
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	1.0	1.9	1.9	1.9	1.9
D	1.0	2.0	1.9	1.9	1.9
E	1.0	1.9	1.9	1.9	1.9
F	1.0	1.9	2.0	2.0	2.0
G	1.0	2.0	2.0	2.0	2.0
H	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA81	4.0	5.381	9.2
NA82	10.3	12.146	25.7
NA83	10.6	12.839	27.5
NA84	10.8	13.507	28.6
NA86	11.3	14.869	31.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA81	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.372 0.484	0.441 0.580	0.534 0.707	0.648 0.861	0.729 0.970
NA82	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.368 0.590	0.458 0.729	0.535 0.839	0.608 0.939	0.691 1.048
NA83	Number of Equivalent Loads		1	8	16	23	31 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.382 0.636	0.465 0.793	0.543 0.908	0.605 0.991	0.672 1.078
NA84	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.391 0.681	0.488 0.819	0.564 0.909	0.626 1.023	0.682 1.170
NA86	Number of Equivalent Loads		1	14	29	44	58 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.437 0.760	0.515 0.915	0.588 1.035	0.656 1.147	0.716 1.251

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

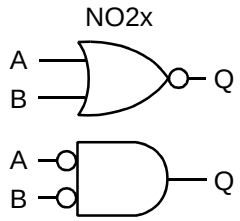
NO2x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NO2x is a family of 2-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

HDL Syntax

Verilog ..... NO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NO21	NO22	NO23	NO24	NO26
A	1.0	2.0	3.9	2.0	2.0
B	1.0	2.0	3.9	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO21	1.1	1.097	1.2
NO22	1.6	2.107	2.0
NO23	2.9	4.233	5.4
NO24	4.0	5.767	11.7
NO26	4.5	7.138	14.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.131 0.147	0.185 0.192	0.279 0.271	0.423 0.387	0.532 0.468
NO22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.096 0.113	0.157 0.161	0.234 0.222	0.336 0.299	0.422 0.357
NO23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.077 0.097	0.143 0.158	0.203 0.206	0.264 0.252	0.341 0.308
NO24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.327 0.285	0.405 0.392	0.475 0.489	0.537 0.576	0.594 0.657
NO26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.337 0.338	0.420 0.442	0.503 0.529	0.567 0.614	0.615 0.693

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

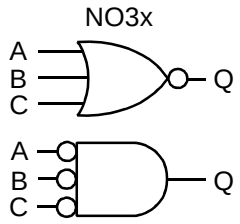
NO3x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NO3x is a family of 3-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

HDL Syntax

Verilog ..... NO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NO31	NO32	NO33	NO34	NO36
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO31	1.3	1.510	2.0
NO32	2.4	2.938	3.1
NO33	4.0	4.687	9.6
NO34	4.7	6.274	13.8
NO36	5.5	7.394	16.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.172 0.175	0.244 0.222	0.377 0.301	0.444 0.339	0.584 0.420
NO32	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.123 0.131	0.161 0.157	0.264 0.225	0.369 0.289	0.443 0.333
NO33	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.349 0.321	0.434 0.434	0.507 0.527	0.575 0.615	0.653 0.719
NO34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.411 0.414	0.474 0.547	0.527 0.647	0.592 0.736	0.673 0.820
NO36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.415 0.340	0.500 0.458	0.579 0.554	0.637 0.636	0.681 0.706

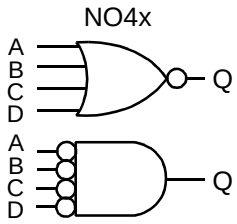
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NO4x is a family of 4-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... NO4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NO4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NO41	NO42	NO43	NO44	NO46
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.0	2.0	2.0
D	1.0	1.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO41	1.6	1.819	2.3
NO42	2.9	3.491	7.3
NO43	4.5	5.329	11.5
NO44	5.3	6.906	15.0
NO46	6.1	7.985	18.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO41	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.181 0.173	0.263 0.221	0.343 0.266	0.424 0.310	0.598 0.395
NO42	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.372 0.381	0.436 0.467	0.523 0.590	0.640 0.746	0.735 0.861
NO43	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.392 0.345	0.482 0.451	0.552 0.548	0.614 0.641	0.681 0.748
NO44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.444 0.320	0.497 0.424	0.557 0.522	0.627 0.614	0.705 0.703
NO46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.501 0.402	0.540 0.489	0.595 0.582	0.670 0.669	0.756 0.747

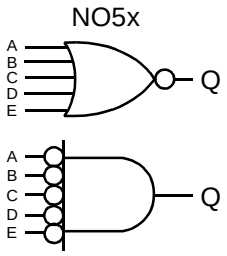
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

NO5x is a family of 5-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

HDL Syntax

Verilog ..... NO5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NO5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NO51	NO52	NO53	NO54	NO56
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.0	2.0	2.0
D	1.0	1.0	2.0	2.0	2.0
E	1.0	1.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
NO51	2.1	2.090	3.0
NO52	3.4	3.785	7.9
NO53	6.1	6.967	14.2
NO54	7.4	8.705	20.5
NO56	7.9	9.974	23.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.179 0.219	0.277 0.274	0.377 0.325	0.478 0.376	0.680 0.487
NO52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.369 0.385	0.441 0.475	0.534 0.599	0.646 0.753	0.724 0.864
NO53	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.345 0.370	0.443 0.492	0.520 0.591	0.590 0.681	0.668 0.782
NO54	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.382 0.362	0.455 0.484	0.518 0.585	0.586 0.670	0.666 0.747
NO56	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.411 0.399	0.502 0.524	0.579 0.603	0.644 0.685	0.696 0.772

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

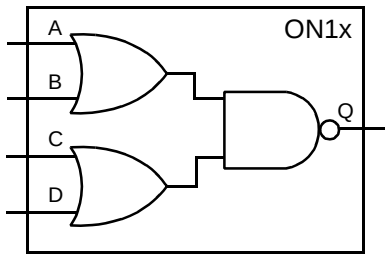
ON1x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON1x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON11	ON12	ON14	ON16
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON11	1.6	1.404	2.9
ON12	2.9	3.758	7.3
ON14	3.2	4.273	8.5
ON16	6.3	8.420	16.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

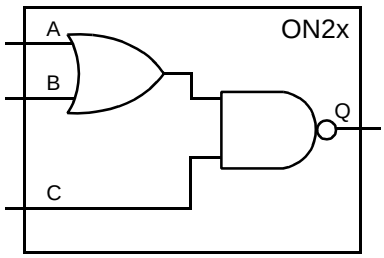
ON11	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.174 0.227	0.236 0.284	0.354 0.383	0.531 0.527	0.653 0.628
ON12	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.356 0.398	0.420 0.495	0.512 0.624	0.631 0.782	0.717 0.894
ON14	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.377 0.434	0.464 0.573	0.539 0.682	0.609 0.779	0.688 0.886
ON16	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.368 0.400	0.437 0.519	0.501 0.629	0.566 0.730	0.634 0.825

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON2x is a family of OR-NAND circuits consisting of one 2-input OR and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

HDL Syntax

Verilog ..... ON2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: ON2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	ON21	ON22	ON24	ON26
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON21	1.3	1.404	2.3
ON22	2.6	3.263	7.0
ON24	2.9	3.778	8.1
ON26	5.3	6.901	15.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.184 0.199	0.248 0.259	0.366 0.369	0.542 0.530	0.668 0.638
ON22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.359 0.393	0.419 0.484	0.514 0.612	0.639 0.773	0.728 0.890
ON24	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.384 0.431	0.472 0.563	0.547 0.672	0.615 0.772	0.693 0.884
ON26	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.356 0.385	0.421 0.522	0.487 0.633	0.555 0.729	0.629 0.816

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

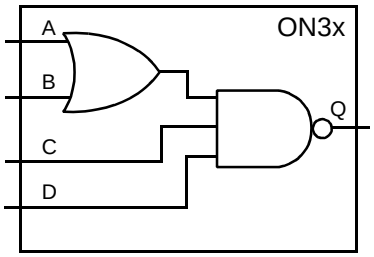
ON3x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON3x is a family of OR-NAND circuits consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON31	ON32	ON34	ON36
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON31	1.6	1.851	2.6
ON32	2.9	3.491	7.2
ON34	3.2	4.160	8.4
ON36	6.1	8.240	16.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.208 0.208	0.281 0.279	0.423 0.418	0.493 0.485	0.635 0.616
ON32	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.359 0.397	0.423 0.496	0.514 0.625	0.632 0.781	0.718 0.892
ON34	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.377 0.430	0.459 0.572	0.535 0.683	0.609 0.780	0.695 0.886
ON36	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.346 0.406	0.432 0.506	0.505 0.636	0.568 0.734	0.626 0.808

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

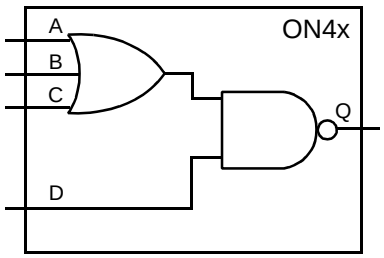
ON4x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON4x is a family of OR-NAND circuits consisting of one 3-input OR gate into and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON41	ON42	ON44	ON46
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON41	1.6	1.503	3.0
ON42	2.9	3.673	7.5
ON44	3.2	4.188	8.7
ON46	5.8	7.720	15.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.233 0.224	0.322 0.289	0.490 0.414	0.572 0.475	0.731 0.598
ON42	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.430 0.425	0.491 0.520	0.583 0.648	0.708 0.809	0.802 0.924
ON44	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.460 0.458	0.539 0.583	0.613 0.695	0.684 0.801	0.767 0.923
ON46	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.401 0.297	0.475 0.474	0.550 0.615	0.620 0.728	0.688 0.828

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

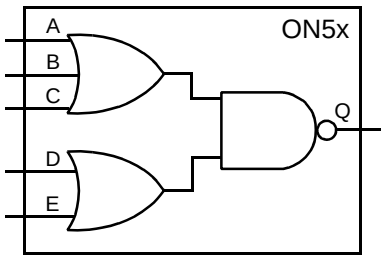
ON5x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON5x is a family of OR-NAND circuits consisting of one 3-input OR gate and one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON52	ON54	ON56
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON52	3.2	4.168	8.1
ON54	3.4	4.683	9.3
ON56	7.1	9.252	17.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.432 0.424	0.497 0.516	0.589 0.636	0.707 0.793	0.794 0.919
ON54	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.457 0.458	0.538 0.595	0.613 0.704	0.684 0.804	0.767 0.915
ON56	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.405 0.405	0.492 0.532	0.563 0.646	0.625 0.745	0.683 0.836

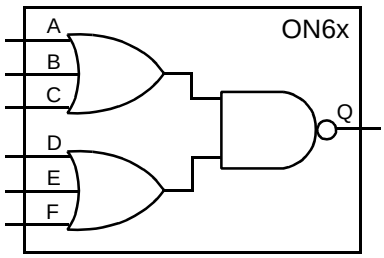
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON6x is a family of OR-NAND circuits consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON62	ON64	ON66
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON62	3.4	4.578	8.7
ON64	4.0	5.107	9.9
ON66	7.4	10.057	18.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON62	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.428 0.416	0.481 0.508	0.573 0.637	0.707 0.799	0.813 0.917
ON64	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.460 0.459	0.554 0.593	0.626 0.703	0.692 0.803	0.769 0.916
ON66	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.429 0.404	0.501 0.553	0.578 0.693	0.675 0.822	0.769 0.945

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

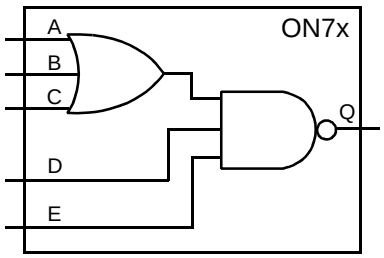
ON7x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON7x is a family of OR-NAND circuits consisting of one 3-input OR gate a two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

HDL Syntax

Verilog ..... ON7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON72	ON74	ON76
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON72	3.2	3.785	8.0
ON74	3.4	4.301	9.1
ON76	6.6	8.521	17.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON72	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.429 0.425	0.493 0.518	0.584 0.644	0.703 0.800	0.790 0.912
ON74	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.462 0.460	0.544 0.590	0.618 0.701	0.688 0.805	0.768 0.922
ON76	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.424 0.400	0.487 0.540	0.547 0.654	0.618 0.748	0.697 0.831

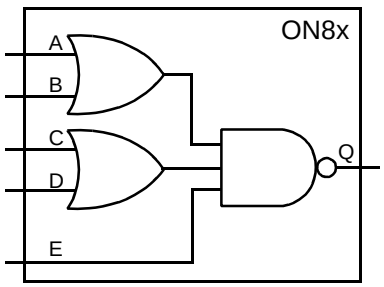
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON8x is a family of OR-NAND circuits consisting of two 2-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON82	ON84	ON86
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON82	4.0	4.742	9.8
ON84	4.2	5.257	10.9
ON86	7.6	10.315	20.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON82	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.392 0.466	0.459 0.576	0.556 0.724	0.682 0.907	0.775 1.039
ON84	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.405 0.522	0.500 0.680	0.576 0.802	0.644 0.911	0.721 1.029
ON86	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.365 0.455	0.437 0.613	0.513 0.734	0.586 0.832	0.659 0.923

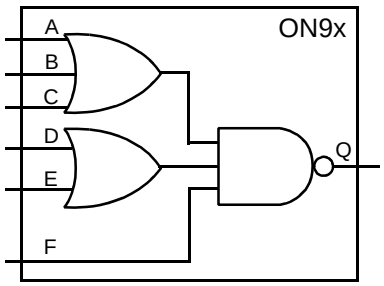
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ON9x is a family of OR-NAND circuits consisting of one 3-input OR gate, one 2-input OR gate, and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON92	ON94	ON96
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON92	4.2	5.152	10.4
ON94	4.5	5.667	11.6
ON96	8.2	11.134	21.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON92	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.463 0.504	0.526 0.616	0.621 0.760	0.750 0.930	0.846 1.048
ON94	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.488 0.546	0.577 0.700	0.652 0.821	0.720 0.930	0.798 1.051
ON96	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.440 0.481	0.518 0.632	0.582 0.752	0.641 0.858	0.697 0.961

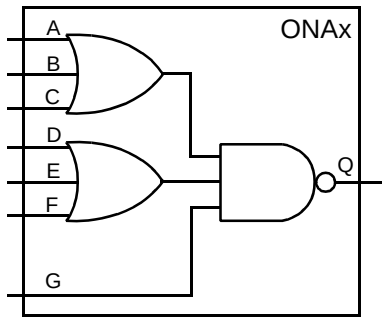
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONAx

Description

ONAx is a family of OR-NAND circuits consisting of two 3-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONAx port map (Q, A, B, C, D, E, F, G;)

Pin Loading

Pin Name	Equivalent Loads		
	ONA2	ONA4	ONA6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONA2	4.5	5.562	11.1
ONA4	4.7	6.077	12.2
ONA6	8.7	11.952	22.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONA2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.459 0.498	0.526 0.601	0.621 0.742	0.743 0.918	0.832 1.044
ONA4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.481 0.541	0.573 0.684	0.650 0.812	0.721 0.932	0.801 1.071
ONA6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.456 0.493	0.521 0.621	0.571 0.739	0.635 0.849	0.720 0.955

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

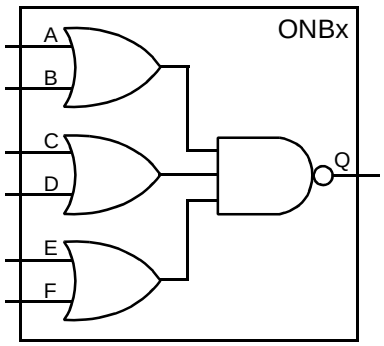
ONBx

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ONBx is a family of OR-NAND circuits consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ONBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ONBx port map (Q, A, B, C, D, E, F)

Pin Loading

Pin Name	Equivalent Loads		
	ONB2	ONB4	ONB6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONB2	4.0	5.224	10.3
ONB4	4.2	5.739	11.5
ONB6	8.4	11.318	21.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONB2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.385 0.471	0.451 0.578	0.548 0.725	0.672 0.911	0.764 1.045
ONB4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.405 0.526	0.495 0.673	0.573 0.796	0.646 0.909	0.729 1.037
ONB6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.369 0.473	0.438 0.621	0.514 0.724	0.589 0.826	0.662 0.929

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

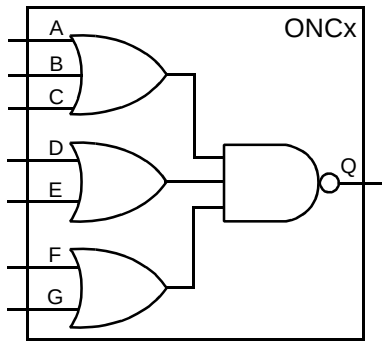
ONCx

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ONCx is a family of OR-NAND circuits consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ONC2	ONC4	ONC6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONC2	4.5	5.647	10.9
ONC4	4.7	6.163	12.1
ONC6	9.0	12.137	22.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONC2	Number of Equivalent Loads		1	3	6	10	13 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.464 0.490	0.523 0.595	0.613 0.740	0.734 0.922	0.826 1.054
ONC4	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.489 0.549	0.581 0.709	0.660 0.829	0.733 0.933	0.816 1.045
ONC6	Number of Equivalent Loads		1	10	20	30	40 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.432 0.505	0.522 0.646	0.593 0.761	0.654 0.861	0.710 0.953

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

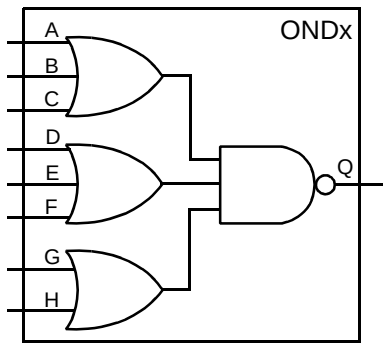
ONDx

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ONDx is a family of OR-NAND circuits consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

HDL Syntax

Verilog ..... ONDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ONDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	OND2	OND4	OND6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0
H	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OND2	4.7	6.057	11.6
OND4	5.0	6.573	12.8
OND6	9.5	12.956	23.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OND2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.464 0.496	0.521 0.610	0.611 0.758	0.733 0.935	0.827 1.059
OND4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.491 0.549	0.586 0.703	0.662 0.824	0.731 0.933	0.806 1.053
OND6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.429 0.487	0.514 0.635	0.586 0.750	0.647 0.851	0.700 0.946

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

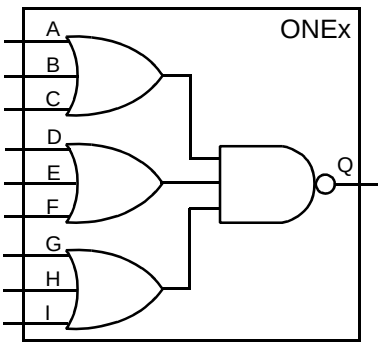
ONEx

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

ONEx is a family of OR-NAND circuits consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

HDL Syntax

Verilog ..... ONEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ONEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ONE2	ONE4	ONE6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0
H	1.0	1.0	2.0
I	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONE2	5.0	6.467	12.3
ONE4	5.5	6.996	13.4
ONE6	9.8	13.763	25.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

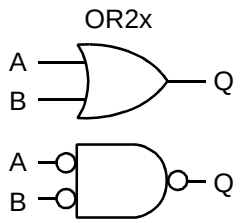
ONE2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.461 0.501	0.536 0.613	0.634 0.757	0.753 0.930	0.837 1.051
ONE4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.487 0.549	0.588 0.689	0.664 0.811	0.731 0.925	0.804 1.055
ONE6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.453 0.492	0.520 0.633	0.582 0.744	0.645 0.842	0.713 0.935

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

OR2x is a family of 2-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

HDL Syntax

Verilog ..... OR2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR21	OR22	OR24	OR26
A	1.0	1.0	2.0	2.0
B	1.0	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR21	1.3	1.645	2.9
OR22	1.6	2.199	4.1
OR24	3.2	4.384	8.8
OR26	4.0	5.768	11.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR21	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.210 0.268	0.276 0.362	0.364 0.489	0.480 0.649	0.572 0.768
OR22	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.230 0.307	0.316 0.447	0.388 0.557	0.456 0.655	0.536 0.763
OR24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.200 0.273	0.280 0.396	0.338 0.500	0.405 0.598	0.482 0.696
OR26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.236 0.352	0.313 0.463	0.382 0.565	0.446 0.666	0.504 0.766

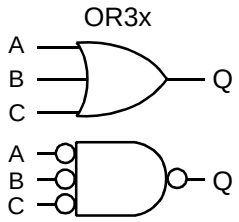
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

OR3x is a family of 3-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

HDL Syntax

Verilog ..... OR3x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR3x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR31	OR32	OR34	OR36
A	1.0	1.0	2.0	3.0
B	1.0	1.0	2.0	3.0
C	1.0	1.0	2.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR31	1.6	2.055	3.6
OR32	2.1	2.584	4.7
OR34	4.2	5.202	10.5
OR36	5.3	7.649	14.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR31	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.233 0.335	0.300 0.446	0.389 0.586	0.505 0.752	0.597 0.867
OR32	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.243 0.392	0.331 0.530	0.408 0.651	0.479 0.765	0.561 0.896
OR34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.212 0.352	0.285 0.484	0.362 0.626	0.436 0.733	0.510 0.818
OR36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.208 0.340	0.281 0.488	0.350 0.603	0.417 0.700	0.479 0.781

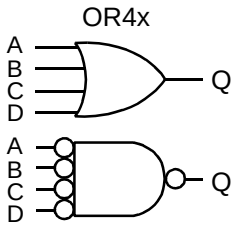
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

OR4x is a family of 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

HDL Syntax

Verilog ..... OR4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: OR4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	OR41	OR42	OR44	OR46
A	1.0	1.0	3.0	3.0
B	1.0	1.0	3.0	3.0
C	1.0	1.0	3.0	3.0
D	1.0	1.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR41	2.1	2.380	4.1
OR42	2.4	2.896	5.2
OR44	5.8	7.558	14.7
OR46	6.3	8.621	17.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR41	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.227 0.378	0.295 0.490	0.390 0.638	0.509 0.817	0.596 0.943
OR42	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.283 0.448	0.371 0.616	0.444 0.745	0.514 0.858	0.601 0.982
OR44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.205 0.337	0.282 0.491	0.354 0.606	0.421 0.713	0.484 0.818
OR46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.215 0.382	0.296 0.530	0.378 0.668	0.444 0.791	0.496 0.898

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORB

AMI500SXSC 0.5 micron CMOS Standard Cell

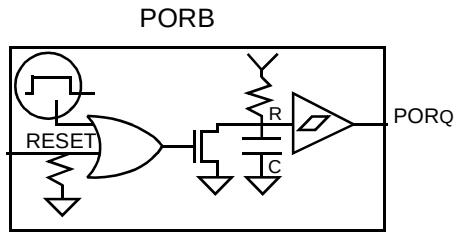
Description

PORB is a power-on-reset.

When power is applied, the PORQ output is asserted low for at least 2 microseconds after the logic circuits become operational. The active high RESET input also drives the PORQ signal to its active low state. Since the PORB is a corner function cell the RESET pin must be driven through the core.

For proper operation, user-designed external circuitry must provide a V_{DD} power slew rate of at least one volt per microsecond. This ensures that the reset pulse will be properly output when V_{DD} falls to zero and immediately returns to its valid range.

Logic Symbol



Truth Table

RESET	PORQ
L	H
H	L

Pin Loading

	Load
RESET	5.9 eql

HDL Syntax

Verilog ..... PORB *inst_name* (RESET, PORQ);

VHDL..... *inst_name*: PORB port map (RESET, PORQ);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	74.806	nA
EQL_{pd}	1664.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

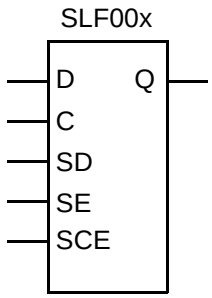
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
RESET	PORQ	t_{PLH}	4242.43				
RESET	PORQ	t_{PHL}	9.55				

Description

SLF00x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low.

Logic Symbol



Truth Table

C	D	SD	SE	SCE	Q
↑	H	X	L	L	H
↑	L	X	L	L	L
↑	X	H	H	L	H
↑	X	L	H	L	L
L	X	X	X	L	NC
L	H	X	L	H	H
L	L	X	L	H	L
L	X	H	H	H	H
L	X	L	H	H	L
H	X	X	X	H	NC

NC = No Change

HDL Syntax

Verilog ..... SLF00x *inst_name* (Q, C, D, SCE, SD, SE);

VHDL..... *inst_name*: SLF00x port map (Q, C, D, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF001	SLF002	SLF004	SLF006
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0

AMI500SXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF001	8.4	9.788	18.4
SLF002	9.2	11.205	21.9
SLF004	10.0	12.588	24.8
SLF006	10.6	13.959	27.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
SLF001	From: C To: Q	t_{PLH} t_{PHL}	0.990 1.182	1.062 1.295	1.170 1.435	1.311 1.601	1.417 1.716
	From: D To: Q	t_{PLH} t_{PHL}	0.892 1.050	0.982 1.153	1.089 1.293	1.211 1.471	1.293 1.599
	From: SCE To: Q	t_{PLH} t_{PHL}	0.759 0.894	0.839 0.999	0.948 1.139	1.082 1.312	1.178 1.434
	From: SD To: Q	t_{PLH} t_{PHL}	0.904 1.044	0.969 1.156	1.073 1.297	1.220 1.463	1.333 1.579
	From: SE To: Q	t_{PLH} t_{PHL}	0.970 1.177	1.038 1.287	1.143 1.429	1.288 1.596	1.398 1.713
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
SLF002	From: C To: Q	t_{PLH} t_{PHL}	0.950 1.117	1.035 1.233	1.104 1.332	1.167 1.423	1.237 1.528
	From: D To: Q	t_{PLH} t_{PHL}	0.858 1.026	0.948 1.149	1.026 1.247	1.100 1.335	1.185 1.434
	From: SCE To: Q	t_{PLH} t_{PHL}	0.685 0.833	0.785 0.963	0.871 1.069	0.951 1.165	1.042 1.271
	From: SD To: Q	t_{PLH} t_{PHL}	0.895 0.996	0.978 1.119	1.048 1.217	1.111 1.305	1.183 1.402
	From: SE To: Q	t_{PLH} t_{PHL}	0.952 1.140	1.026 1.262	1.096 1.360	1.165 1.448	1.246 1.547

	Number of Equivalent Loads		1	10	20	30	40 (max)
SLF004	From: C To: Q	t_{PLH} t_{PHL}	1.012 1.172	1.098 1.296	1.165 1.393	1.221 1.476	1.271 1.550
	From: D To: Q	t_{PLH} t_{PHL}	0.865 1.086	0.949 1.215	1.053 1.309	1.133 1.386	1.204 1.454
	From: SCE To: Q	t_{PLH} t_{PHL}	0.636 0.875	0.800 1.040	0.925 1.137	0.997 1.221	1.053 1.300
	From: SD To: Q	t_{PLH} t_{PHL}	0.908 1.034	1.008 1.161	1.078 1.270	1.135 1.368	1.184 1.458
	From: SE To: Q	t_{PLH} t_{PHL}	1.003 1.204	1.076 1.330	1.147 1.425	1.216 1.504	1.281 1.575
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
SLF006	From: C To: Q	t_{PLH} t_{PHL}	1.059 1.242	1.145 1.358	1.214 1.464	1.273 1.559	1.324 1.643
	From: D To: Q	t_{PLH} t_{PHL}	0.961 1.131	1.052 1.265	1.129 1.370	1.199 1.458	1.262 1.532
	From: SCE To: Q	t_{PLH} t_{PHL}	0.819 0.963	0.875 1.118	0.953 1.223	1.042 1.309	1.131 1.381
	From: SD To: Q	t_{PLH} t_{PHL}	0.988 1.135	1.049 1.257	1.126 1.357	1.206 1.444	1.283 1.518
	From: SE To: Q	t_{PLH} t_{PHL}	1.073 1.265	1.167 1.379	1.224 1.483	1.267 1.576	1.301 1.656

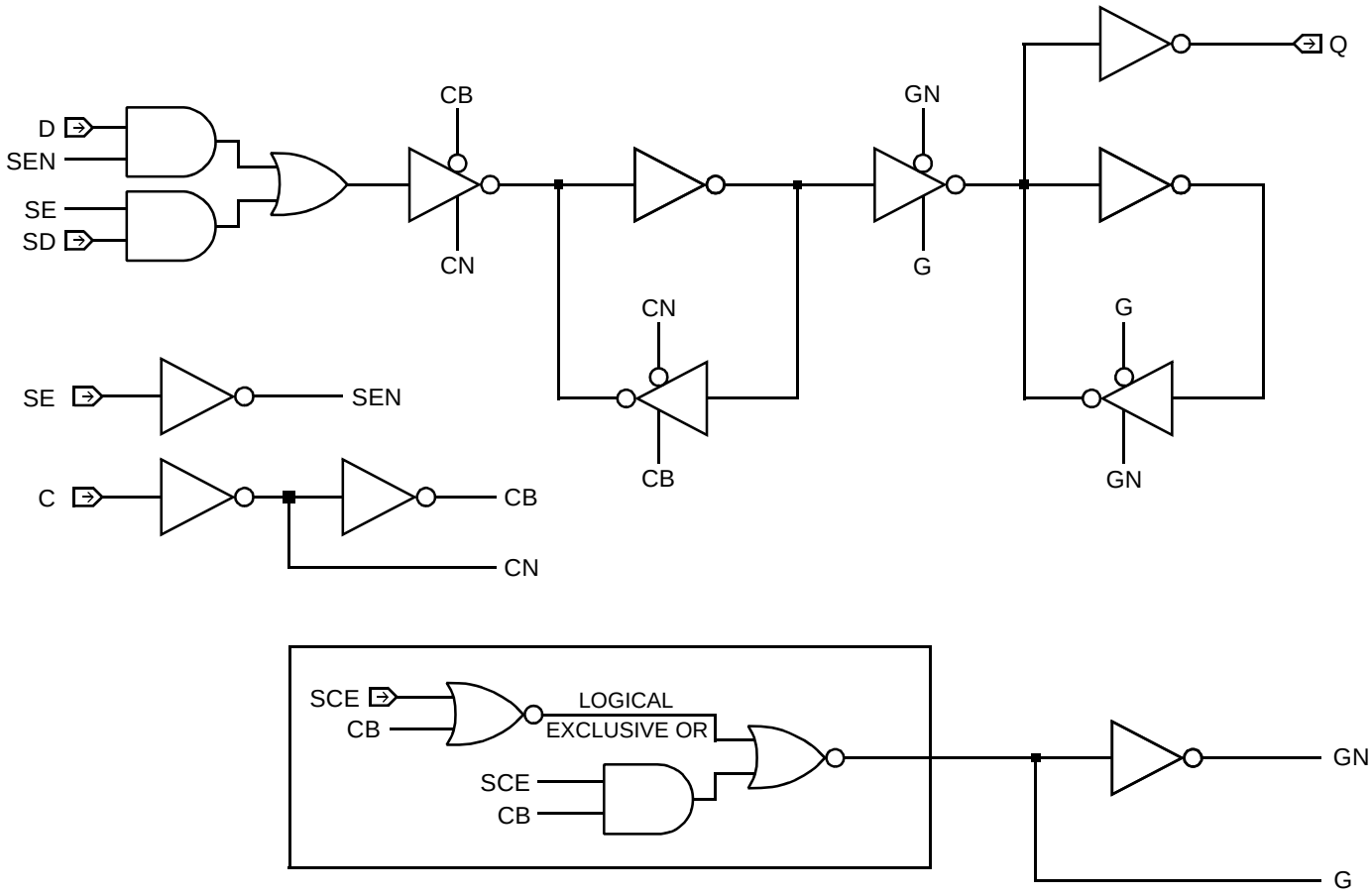
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF001	SLF002	SLF004	SLF006
Min C Width	High	t_w	1.077	1.065	1.136	1.208
Min C Width	Low	t_w	0.741	0.786	0.786	0.786
Min D Setup		t_{su}	0.607	0.657	0.657	0.657
Min D Hold		t_h	0.147	0.145	0.145	0.145
Min SD Setup		t_{su}	0.607	0.657	0.657	0.657
Min SD Hold		t_h	0.147	0.145	0.145	0.145
Min SE Setup		t_{su}	0.734	0.783	0.783	0.783
Min SE Hold		t_h	0.147	0.145	0.145	0.145
Min SCE Setup		t_{su}	0.839	0.831	0.902	0.974
Min SCE Hold		t_h	0.906	0.917	0.958	1.000

Logic Schematic



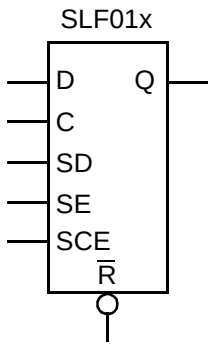
SLF01x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

SLF01x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. RESET is asynchronous and active low.

Logic Symbol



Truth Table

RN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF01x *inst_name* (Q, C, D, RN, SCE, SD, SE);

VHDL..... *inst_name*: SLF01x port map (Q, C, D, RN, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF011	SLF012	SLF014	SLF016
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF011	9.2	10.634	22.2
SLF012	10.3	12.064	25.8
SLF014	10.8	13.435	28.7
SLF016	11.6	15.422	32.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
SLF011	From: C To: Q	t_{PLH} t_{PHL}	0.983 1.181	1.051 1.270	1.147 1.404	1.272 1.584	1.363 1.720
	From: D To: Q	t_{PLH} t_{PHL}	0.954 1.083	1.027 1.196	1.124 1.332	1.243 1.488	1.328 1.595
	From: RN To: Q	t_{PLH} t_{PHL}	0.722 0.905	0.788 1.025	0.885 1.169	1.010 1.333	1.103 1.445
	From: SCE To: Q	t_{PLH} t_{PHL}	0.750 0.902	0.809 1.008	0.903 1.144	1.035 1.307	1.138 1.422
	From: SD To: Q	t_{PLH} t_{PHL}	0.985 1.059	1.049 1.157	1.145 1.294	1.272 1.467	1.367 1.593
	From: SE To: Q	t_{PLH} t_{PHL}	1.051 1.191	1.131 1.300	1.228 1.437	1.338 1.599	1.413 1.711
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
SLF012	From: C To: Q	t_{PLH} t_{PHL}	0.988 1.151	1.065 1.278	1.132 1.371	1.194 1.451	1.266 1.537
	From: D To: Q	t_{PLH} t_{PHL}	0.991 1.041	1.078 1.142	1.142 1.239	1.197 1.335	1.256 1.449
	From: RN To: Q	t_{PLH} t_{PHL}	0.730 1.101	0.808 1.268	0.885 1.392	0.962 1.501	1.054 1.619
	From: SCE To: Q	t_{PLH} t_{PHL}	0.686 0.843	0.781 0.961	0.861 1.064	0.935 1.163	1.018 1.280
	From: SD To: Q	t_{PLH} t_{PHL}	1.008 1.013	1.092 1.123	1.157 1.220	1.215 1.312	1.278 1.418
	From: SE To: Q	t_{PLH} t_{PHL}	1.070 1.162	1.150 1.292	1.216 1.384	1.277 1.463	1.345 1.547

	Number of Equivalent Loads		1	10	20	30	40 (max)
SLF014	From: C To: Q	t_{PLH} t_{PHL}	1.057 1.203	1.132 1.313	1.200 1.419	1.262 1.517	1.321 1.611
	From: D To: Q	t_{PLH} t_{PHL}	1.050 1.113	1.144 1.222	1.203 1.324	1.250 1.418	1.290 1.506
	From: RN To: Q	t_{PLH} t_{PHL}	0.779 1.355	0.889 1.496	0.965 1.640	1.019 1.779	1.061 1.915
	From: SCE To: Q	t_{PLH} t_{PHL}	0.772 0.909	0.888 1.034	0.987 1.141	1.079 1.235	1.168 1.321
	From: SD To: Q	t_{PLH} t_{PHL}	1.042 1.099	1.124 1.218	1.200 1.313	1.274 1.395	1.349 1.469
	From: SE To: Q	t_{PLH} t_{PHL}	1.107 1.225	1.192 1.355	1.261 1.447	1.320 1.523	1.374 1.589
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
SLF016	From: C To: Q	t_{PLH} t_{PHL}	1.356 1.397	1.411 1.475	1.477 1.562	1.539 1.655	1.618 1.743
	From: D To: Q	t_{PLH} t_{PHL}	1.362 1.302	1.443 1.380	1.486 1.470	1.518 1.560	1.542 1.644
	From: RN To: Q	t_{PLH} t_{PHL}	1.097 0.585	1.175 0.665	1.231 0.765	1.276 0.858	1.314 0.948
	From: SCE To: Q	t_{PLH} t_{PHL}	1.112 1.138	1.185 1.254	1.246 1.334	1.299 1.399	1.345 1.452
	From: SD To: Q	t_{PLH} t_{PHL}	1.344 1.277	1.417 1.363	1.476 1.451	1.527 1.535	1.569 1.610
	From: SE To: Q	t_{PLH} t_{PHL}	1.435 1.403	1.519 1.471	1.569 1.559	1.606 1.651	1.635 1.740

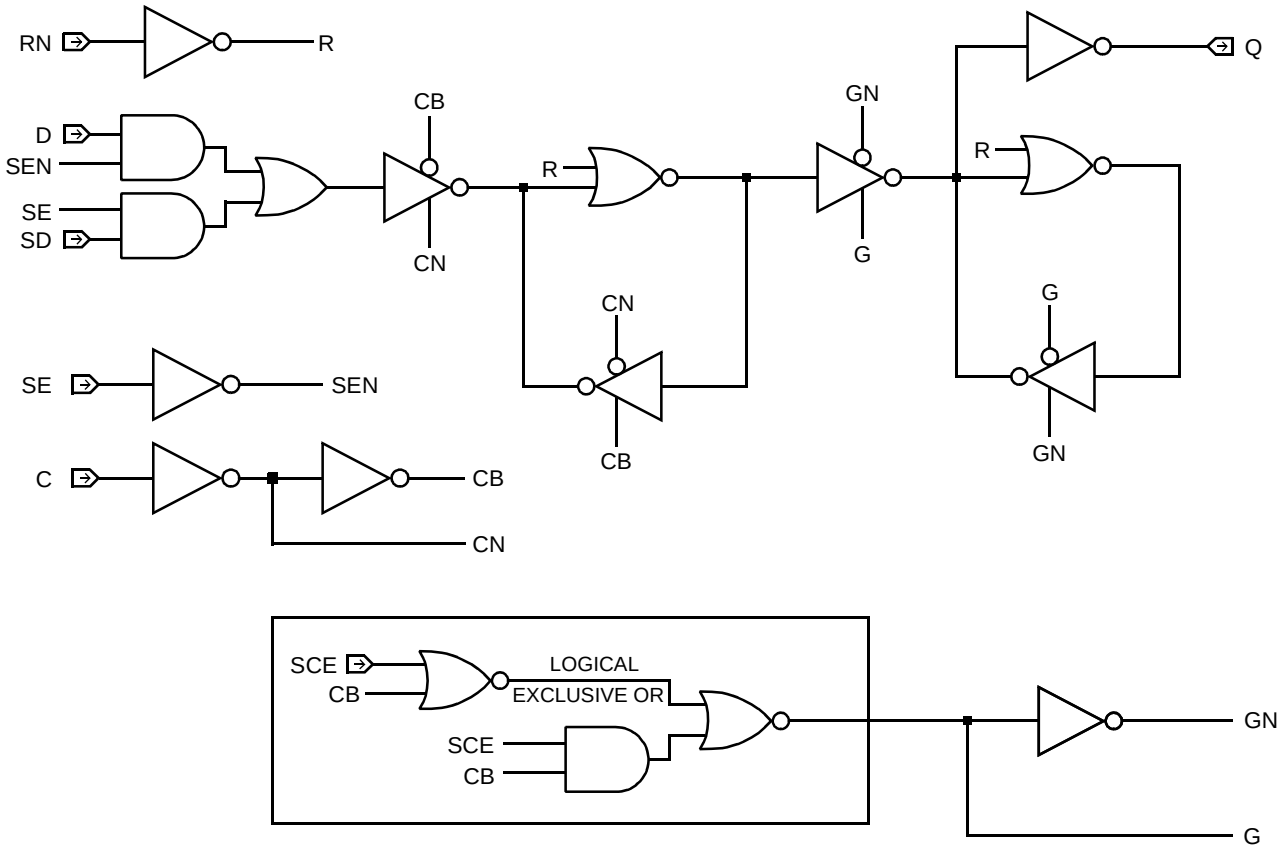
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF011	SLF012	SLF014	SLF016
Min C Width	High	t_w	1.101	1.083	1.152	1.101
Min C Width	Low	t_w	0.756	0.808	0.808	0.755
Min RN Width	Low	t_w	0.586	0.618	0.618	0.584
Min D Setup		t_{su}	0.625	0.680	0.680	0.625
Min D Hold		t_h	0.147	0.146	0.146	0.146
Min SD Setup		t_{su}	0.625	0.680	0.680	0.625
Min SD Hold		t_h	0.147	0.146	0.146	0.146
Min SE Setup		t_{su}	0.751	0.806	0.806	0.751
Min SE Hold		t_h	0.147	0.146	0.146	0.146
Min SCE Setup		t_{su}	0.864	0.850	0.918	0.868
Min SCE Hold		t_h	0.908	0.919	0.960	0.862
Min RN Setup		t_{su}	0.321	0.366	0.367	0.322
Min RN Hold		t_h	0.339	0.336	0.336	0.336

Logic Schematic



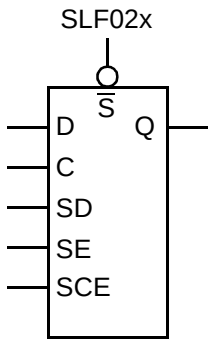
SLF02x

AMI500SXSC 0.5 micron CMOS Standard Cell

Description

SLF02x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET is asynchronous and active low.

Logic Symbol



Truth Table

SN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	H

NC = No Change

HDL Syntax

Verilog ..... SLF02x *inst_name* (Q, C, D, SCE, SD, SE, SN);

VHDL..... *inst_name*:SLF02x port map (Q, C, D, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF021	SLF022	SLF024	SLF026
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0
SN	2.0	2.1	2.1	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF021	9.0	10.703	19.2
SLF022	9.8	12.121	22.7
SLF024	10.3	13.491	25.6
SLF026	10.8	15.466	28.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
SLF021	From: C To: Q	t_{PLH} t_{PHL}	0.992 1.176	1.070 1.285	1.167 1.423	1.280 1.586	1.358 1.699
	From: D To: Q	t_{PLH} t_{PHL}	0.916 1.065	0.995 1.160	1.092 1.297	1.203 1.475	1.279 1.606
	From: SCE To: Q	t_{PLH} t_{PHL}	0.794 0.861	0.867 0.971	0.964 1.108	1.084 1.270	1.169 1.382
	From: SD To: Q	t_{PLH} t_{PHL}	0.943 1.060	1.030 1.178	1.123 1.314	1.221 1.465	1.285 1.566
	From: SE To: Q	t_{PLH} t_{PHL}	1.010 1.179	1.096 1.273	1.189 1.410	1.289 1.588	1.355 1.720
	From: SN To: Q	t_{PLH} t_{PHL}	0.653 0.609	0.737 0.741	0.838 0.909	0.954 1.110	1.032 1.251
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
SLF022	From: C To: Q	t_{PLH} t_{PHL}	0.963 1.161	1.043 1.252	1.110 1.351	1.172 1.454	1.243 1.582
	From: D To: Q	t_{PLH} t_{PHL}	0.941 1.065	1.015 1.192	1.082 1.290	1.147 1.376	1.223 1.469
	From: SCE To: Q	t_{PLH} t_{PHL}	0.743 0.830	0.831 0.967	0.906 1.076	0.976 1.174	1.055 1.282
	From: SD To: Q	t_{PLH} t_{PHL}	0.964 1.034	1.045 1.153	1.112 1.253	1.173 1.344	1.241 1.447
	From: SE To: Q	t_{PLH} t_{PHL}	1.028 1.174	1.107 1.267	1.174 1.367	1.236 1.469	1.306 1.596
	From: SN To: Q	t_{PLH} t_{PHL}	0.820 0.564	0.941 0.723	1.027 0.853	1.101 0.976	1.180 1.117

	Number of Equivalent Loads		1	10	20	30	40 (max)
SLF024	From: C To: Q	t_{PLH} t_{PHL}	1.022 1.230	1.100 1.366	1.165 1.457	1.226 1.529	1.307 1.591
	From: D To: Q	t_{PLH} t_{PHL}	0.981 1.119	1.023 1.228	1.093 1.334	1.181 1.434	1.281 1.531
	From: SCE To: Q	t_{PLH} t_{PHL}	0.799 0.901	0.882 1.033	0.960 1.138	1.031 1.229	1.099 1.311
	From: SD To: Q	t_{PLH} t_{PHL}	0.986 1.122	1.099 1.256	1.174 1.355	1.230 1.439	1.276 1.513
	From: SE To: Q	t_{PLH} t_{PHL}	1.066 1.248	1.141 1.390	1.214 1.482	1.284 1.560	1.352 1.632
	From: SN To: Q	t_{PLH} t_{PHL}	1.008 0.601	1.134 0.776	1.223 0.920	1.296 1.038	1.359 1.146
SLF026	Number of Equivalent Loads		1	14	29	44	58 (max)
	From: C To: Q	t_{PLH} t_{PHL}	1.254 1.437	1.306 1.491	1.374 1.580	1.445 1.687	1.514 1.799
	From: D To: Q	t_{PLH} t_{PHL}	1.184 1.329	1.260 1.408	1.319 1.495	1.369 1.582	1.411 1.661
	From: SCE To: Q	t_{PLH} t_{PHL}	1.043 1.154	1.110 1.263	1.175 1.345	1.234 1.412	1.287 1.468
	From: SD To: Q	t_{PLH} t_{PHL}	1.199 1.326	1.269 1.369	1.331 1.453	1.386 1.561	1.433 1.678
	From: SE To: Q	t_{PLH} t_{PHL}	1.283 1.473	1.311 1.579	1.373 1.649	1.456 1.704	1.550 1.749
	From: SN To: Q	t_{PLH} t_{PHL}	0.430 0.846	0.513 0.971	0.586 1.086	0.649 1.188	0.707 1.276

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

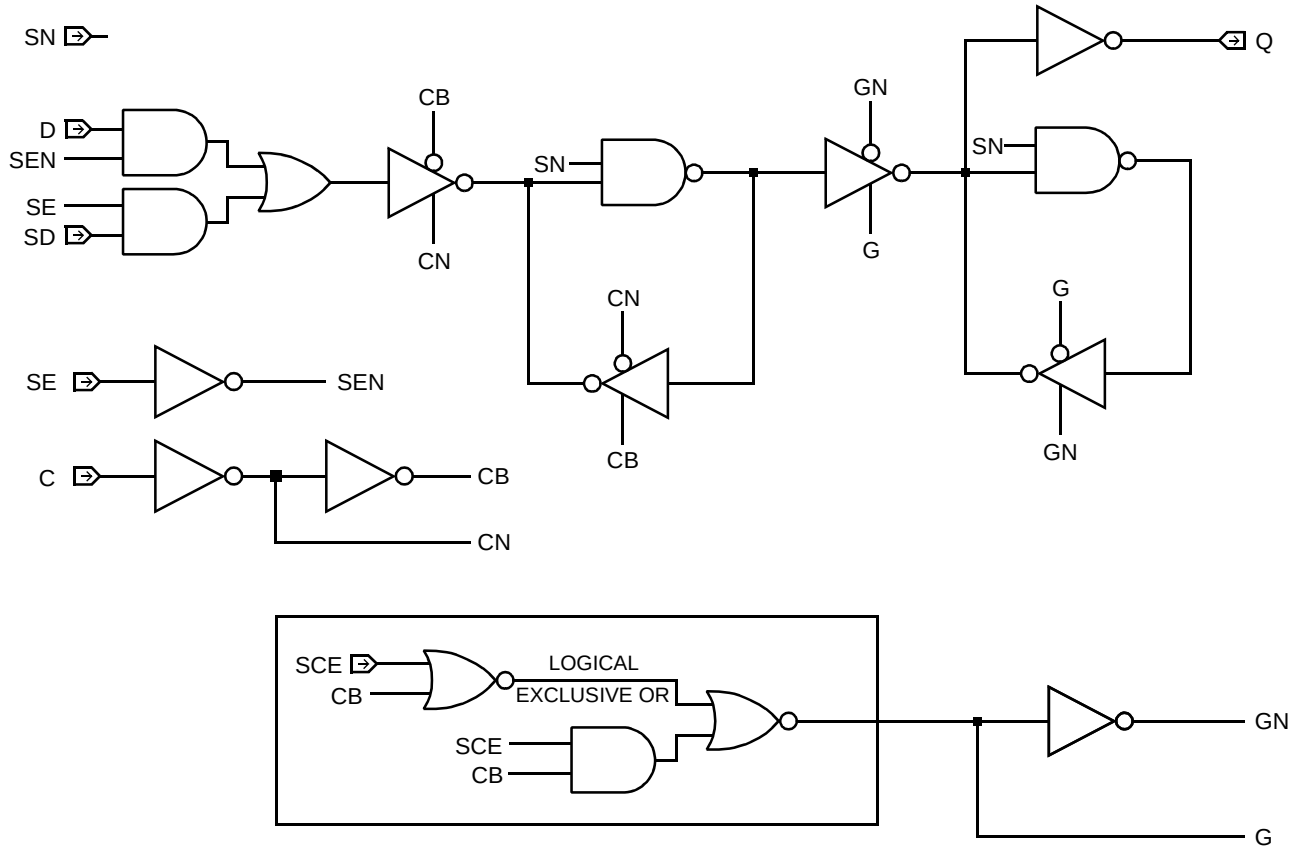
AMI500SXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF021	SLF022	SLF024	SLF026
Min C Width	High	t_w	1.074	1.090	1.164	1.107
Min C Width	Low	t_w	0.770	0.821	0.821	0.771
Min SN Width	Low	t_w	0.496	0.546	0.546	0.497
Min D Setup		t_{su}	0.640	0.693	0.693	0.641
Min D Hold		t_h	0.147	0.147	0.147	0.147
Min SD Setup		t_{su}	0.640	0.693	0.693	0.641
Min SD Hold		t_h	0.147	0.147	0.147	0.147
Min SE Setup		t_{su}	0.766	0.819	0.819	0.767
Min SE Hold		t_h	0.147	0.147	0.147	0.147
Min SCE Setup		t_{su}	0.838	0.856	0.930	0.872
Min SCE Hold		t_h	0.889	0.919	0.960	0.862
Min SN Setup		t_{su}	0.176	0.219	0.219	0.177
Min SN Hold		t_h	0.607	0.606	0.606	0.606

Logic Schematic

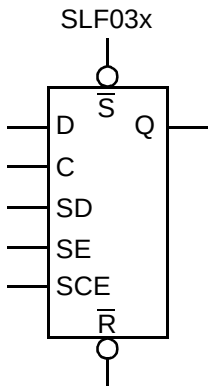


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

SLF03x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET and RESET are asynchronous and active low.

Logic Symbol



Truth Table

RN	SN	C	D	SD	SE	SCE	Q
H	H	↑	H	X	L	L	H
H	H	↑	L	X	L	L	L
H	H	↑	X	H	H	L	H
H	H	↑	X	L	H	L	L
H	H	L	X	X	X	L	NC
H	H	L	H	X	L	H	H
H	H	L	L	X	L	H	L
H	H	L	X	H	H	H	H
H	H	L	X	L	H	H	L
H	H	H	X	X	X	H	NC
H	L	X	X	X	X	X	H
L	X	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF03x *inst_name* (Q, C, D, RN, SCE, SD, SE, SN);

VHDL..... *inst_name*: SLF03x port map (Q, C, D, RN, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF031	SLF032	SLF034	SLF036
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0
SN	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF031	10.0	11.708	23.8
SLF032	11.1	13.158	27.4
SLF034	11.6	14.528	30.3
SLF036	11.5	15.899	33.2

a. See page 2-13 for power equation.

AMI500SXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	6	11	16	22 (max)
SLF031	From: C To: Q	t_{PLH} t_{PHL}	1.083 1.225	1.245 1.474	1.392 1.674	1.533 1.855	1.696 2.055
	From: D To: Q	t_{PLH} t_{PHL}	1.054 1.110	1.207 1.337	1.354 1.541	1.499 1.734	1.671 1.956
	From: RN To: Q	t_{PLH} t_{PHL}	0.790 0.919	0.972 1.185	1.135 1.415	1.289 1.631	1.468 1.876
	From: SCE To: Q	t_{PLH} t_{PHL}	0.839 0.867	1.028 1.129	1.188 1.341	1.335 1.533	1.502 1.746
	From: SD To: Q	t_{PLH} t_{PHL}	1.068 1.091	1.223 1.327	1.371 1.545	1.514 1.756	1.684 2.001
	From: SE To: Q	t_{PLH} t_{PHL}	1.143 1.203	1.321 1.443	1.466 1.660	1.597 1.866	1.743 2.105
	From: SN To: Q	t_{PLH} t_{PHL}	0.646 0.642	0.841 0.944	1.008 1.220	1.164 1.486	1.342 1.794
SLF032	Number of Equivalent Loads		1	6	11	16	22 (max)
	From: C To: Q	t_{PLH} t_{PHL}	1.089 1.198	1.177 1.296	1.241 1.394	1.296 1.492	1.355 1.610
	From: D To: Q	t_{PLH} t_{PHL}	1.084 1.108	1.167 1.227	1.232 1.324	1.291 1.413	1.355 1.512
	From: RN To: Q	t_{PLH} t_{PHL}	0.818 1.126	0.917 1.293	0.994 1.419	1.062 1.529	1.136 1.648
	From: SCE To: Q	t_{PLH} t_{PHL}	0.822 0.832	0.920 0.959	1.003 1.066	1.081 1.164	1.168 1.276
	From: SD To: Q	t_{PLH} t_{PHL}	1.070 1.082	1.155 1.207	1.234 1.303	1.311 1.387	1.400 1.480
	From: SE To: Q	t_{PLH} t_{PHL}	1.165 1.217	1.226 1.348	1.292 1.441	1.361 1.520	1.447 1.605
	From: SN To: Q	t_{PLH} t_{PHL}	0.839 0.611	0.949 0.775	1.031 0.908	1.102 1.028	1.180 1.162

	Number of Equivalent Loads		1	10	20	30	40 (max)
SLF034	From: C To: Q	t_{PLH} t_{PHL}	1.133 1.270	1.199 1.408	1.270 1.505	1.340 1.584	1.409 1.653
	From: D To: Q	t_{PLH} t_{PHL}	1.120 1.173	1.160 1.310	1.228 1.407	1.312 1.488	1.409 1.559
	From: RN To: Q	t_{PLH} t_{PHL}	0.867 1.426	0.968 1.604	1.046 1.733	1.106 1.833	1.154 1.915
	From: SCE To: Q	t_{PLH} t_{PHL}	0.922 0.905	1.012 1.022	1.075 1.131	1.127 1.231	1.172 1.326
	From: SD To: Q	t_{PLH} t_{PHL}	1.132 1.151	1.246 1.294	1.303 1.384	1.348 1.455	1.388 1.515
	From: SE To: Q	t_{PLH} t_{PHL}	1.193 1.273	1.268 1.359	1.340 1.467	1.406 1.583	1.469 1.704
	From: SN To: Q	t_{PLH} t_{PHL}	1.042 0.662	1.187 0.840	1.266 0.969	1.325 1.078	1.373 1.174
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
SLF036	From: C To: Q	t_{PLH} t_{PHL}	1.188 1.320	1.239 1.437	1.312 1.545	1.394 1.643	1.476 1.728
	From: D To: Q	t_{PLH} t_{PHL}	1.194 1.211	1.280 1.309	1.341 1.418	1.391 1.526	1.432 1.625
	From: RN To: Q	t_{PLH} t_{PHL}	0.923 1.647	1.002 1.782	1.086 1.938	1.168 2.094	1.242 2.240
	From: SCE To: Q	t_{PLH} t_{PHL}	0.934 0.960	1.026 1.114	1.112 1.219	1.188 1.302	1.253 1.369
	From: SD To: Q	t_{PLH} t_{PHL}	1.165 1.190	1.272 1.320	1.352 1.422	1.415 1.508	1.468 1.581
	From: SE To: Q	t_{PLH} t_{PHL}	1.260 1.339	1.317 1.433	1.391 1.539	1.467 1.645	1.541 1.742
	From: SN To: Q	t_{PLH} t_{PHL}	1.248 0.752	1.354 0.905	1.456 1.031	1.549 1.149	1.632 1.255

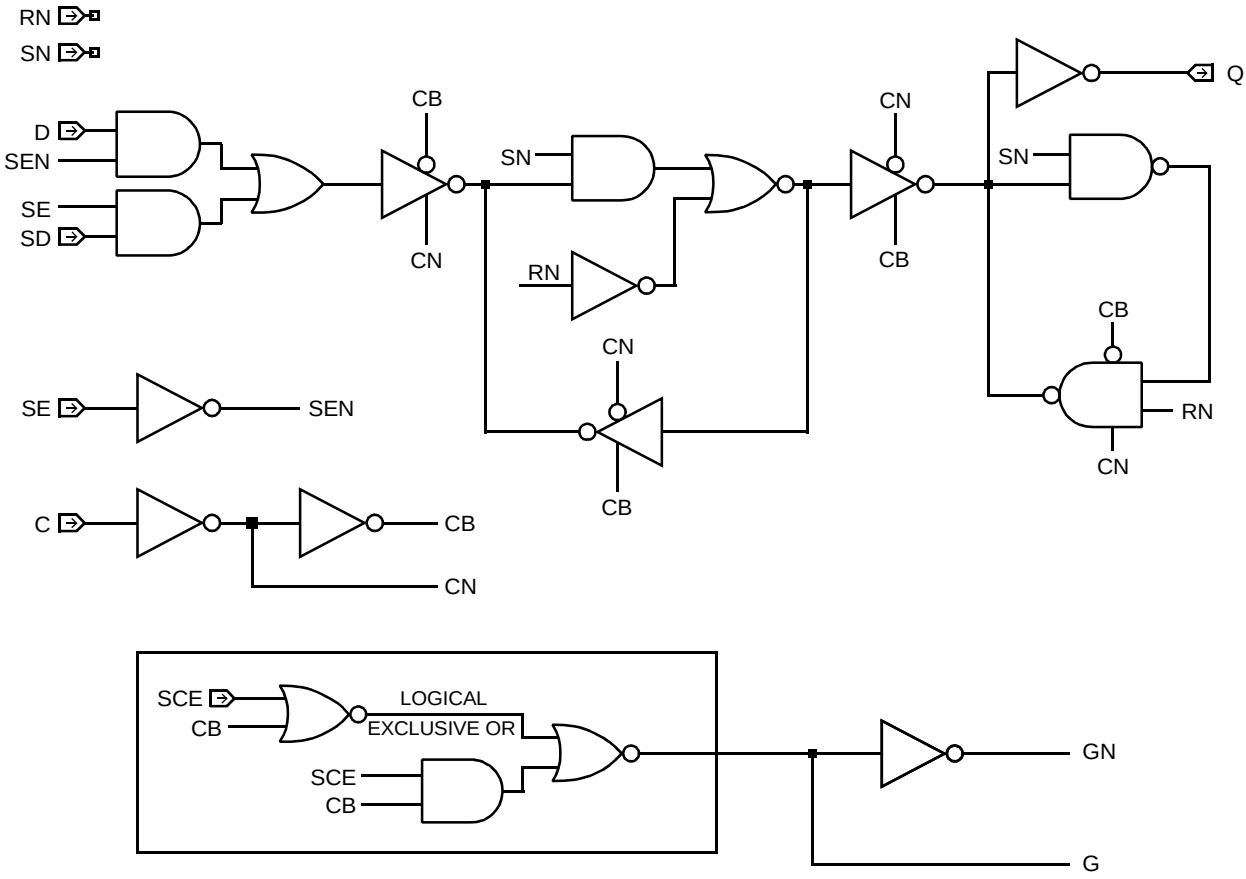
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF031	SLF032	SLF034	SLF036
Min C Width	High	t_w	1.114	1.117	1.190	1.261
Min C Width	Low	t_w	0.795	0.853	0.853	0.853
Min RN Width	Low	t_w	0.622	0.664	0.664	0.664
Min SN Width	Low	t_w	0.499	0.543	0.543	0.543
Min D Setup		t_{su}	0.665	0.726	0.726	0.726
Min D Hold		t_h	0.146	0.147	0.147	0.147
Min RN Setup		t_{su}	0.369	0.427	0.427	0.427
Min RN Hold		t_h	0.340	0.340	0.340	0.340
Min SCE Setup		t_{su}	0.887	0.889	0.967	1.040
Min SCE Hold		t_h	0.902	0.923	0.964	1.006
Min SD Setup		t_{su}	0.665	0.726	0.726	0.726
Min SD Hold		t_h	0.146	0.147	0.147	0.147
Min SE Setup		t_{su}	0.791	0.852	0.852	0.852
Min SE Hold		t_h	0.146	0.147	0.147	0.147
Min SN Setup		t_{su}	0.211	0.259	0.259	0.259
Min SN Hold		t_h	0.608	0.607	0.607	0.607

Logic Schematic

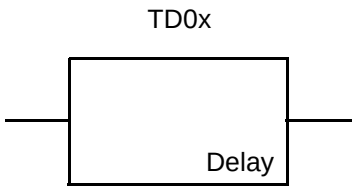


AMI500SXSC 0.5 micron CMOS Standard Cell

Description

TD0x is a family of non-inverting time delays.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... TD0x *inst_name* (Q, A);

VHDL..... *inst_name*: TD0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	TD02	TD03	TD08
A	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
TD02	5.3	5.505	16.1
TD03	6.9	7.899	29.3
TD08	14.8	15.294	63.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

TD02	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	2.031 2.033	2.105 2.140	2.167 2.227	2.226 2.306	2.292 2.393
TD03	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	3.091 3.160	3.163 3.225	3.226 3.309	3.286 3.406	3.354 3.534
TD08	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	8.238 8.228	8.292 8.255	8.354 8.318	8.421 8.416	8.506 8.579

Delay will vary with input conditions. See page 2-15 for interconnect estimates.