Application note

Using the NE5750 and NE5751 for audio processing

AN1741

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INTRODUCTION

The NE5750 and the NE5751 are two audio processor chips that can be used in RF communications. The chip-set processes a voice so that by the time it is transmitted and received, the quality is preserved. This is accomplished through the use of compression/expansion and pre-emphasis/ de-emphasis.

The audio processor chip-set (APROC) has a wide variety of high performance applications such as cellular phones, cordless voice microphones, cordless intercom systems, standard phones, and hand-held, base, or mobile two-way communications equipment.

Below is an outline of this application note:

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II. NE5750

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- Component list and layout









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VI. QUESTION AND ANSWER SECTION

I. WHAT IS AUDIO PROCESSING

HOW THE VOICE IS PROCESSED BY THE NE5750 and NE5751:

Audio processing begins when a person speaks into a microphone (see Figure 1). The signal is first amplified by the preamp, then screened by a bandpass filter. After the noise is filtered out, the voice signal is processed by the compressor. The function of the compressor is to attenuate loud voices and amplify soft ones. The upper voice frequencies are then amplified by pre-emphasis before their voltage amplitudes are restricted by the limiter and all-pass circuit. When this is completed, the processed voice is ready for transmission.

Since the voice signal was processed by the APROC before transmission, it must be unprocessed upon reception. The received signal is screened again so that the unwanted received noise is blocked before it goes

through de-emphasis. In de-emphasis, the upper voice frequencies are attenuated. Then the signal is expanded back to its primary dynamic range by the expandor. Because the voice is restored to its original state, it is ready for amplification by the power amp whose output can be connected to an external speaker. The receiving party will now be able to hear the transmitting party.

MORE DETAIL ON THE KEY FEATURES:

During compression, low level signals are amplified to "jump" over the transmitter channel noise, while the high level signals are compressed to prevent distortion. In general, because we are dealing with a limited dynamic range transmission medium, it is desirable to compress the signal prior to transmission. However, in order to preserve the dynamic range of the original voice signal, the compressed signal is expanded at reception. Figure 2 shows a diagram of a cordless phone application using companding. Note the signal-to-noise ratio with and without companding. Another key function of the APROC is the pre-emphasis/de-emphasis capability which is used to overcome the "colored" noise, present in all FM receivers, generated by the FM demodulator. This noise worsens at the upper voice band as shown in Figure 3. Therefore, to keep the same signal-to-noise ratio in the lower and upper voice bands, pre-emphasis/de-emphasis is required. A person with a high-pitched voice will now be heard just as well as a person with a low, deep voice.



Figure 3. Pre-emphasis Response

Another key stage of the APROC is the limiter with the all-pass circuit. Its main function is to limit the amplitude of the voice signal so that the maximum frequency deviation is limited to 12kHz. Cellular radio specifications allow for a 30kHz channel spacing with an audio bandwidth of 3kHz. Therefore, by Carson's rule the maximum frequency deviation of the limiter must be 12kHz as shown below.

1. Bandwidth	=	2 (Modulating Freq + Max Freq Dev)
or		max rioq 200)
2. Max Freq Dev	=	Bandwidth/2 -
		(Mod Freq)
	=	30kHz/2 - 3kHz
	=	15kHz-3kHz
	=	12kHz
PERFORMAN		

PERFORMANCE GRAPHS OF APROC DEMO-BOARD:

Figure 4 shows the general diagram of the audio processor chip set without the external components. External components for the chip set can be found in Figure 31, and the values were chosen for AMPS/TACS specs. To demonstrate the performance of the chip set, data was taken in the lab and resulted in the following figures.



Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

Figure 5 Description

Figure 5 reveals what the signal would look like on the bench with different input levels. Figures 5a, b, and c all use the same audio input signal. The audio signal (0-6kHz) varies from 20dB to -30dB in 10dB steps.

Figure 5a

This graph shows the Tx channel. Notice the signal's increase in amplitude as the frequency is increased due to pre-emphasis. Additionally, the slope of the signal decreases as the input increases.

The compressor function is readily shown where a 5dB change in the output level occurs for every 10dB change in the input.

Figure 5b

The 2:1 expansion of audio (20dB change for every 10dB), bandpass filtering and the de-emphasis filter response (300-3kHz) are shown. The graph shows the Rx channel. Notice the signal's decrease in amplitude as the frequency increases due to de-emphasis.

Figure 5c

This shows that a flat frequency response is achieved upon normal reception. Notice the 20dB gap, although the input steps are for 10dB. This is due to the noise canceller turning on. The decrease in amplitude for higher level, higher frequency tones is the result of the deviation limiter action.

After studying these figures, a designer will have a graphical understanding of how the APROC processes a signal.

Figure 6 shows the test set-up using the APROC demo-board to simulate a real cellular phone call. Audio noise is added to the input of the microphone and RF noise is added to the receiver. The table for Figures 7-10 describes what the associated waveforms reveal when certain key stages of the APROC are activated or bypassed.

As seen from the following figures, there is a definite advantage in using the chip set in high performance communication systems.



Figure 5.







Figure	Description
7	No noise gain is observed at the output of the Tx channel because of the noise canceller circuit.
8	Shows why companding and emphasis are needed to improve the quality of the audio signal when BASEBAND NOISE is present in the system
9	Shows why companding and emphasis are needed to improve the quality of the audio signal when RF NOISE is present in the system.
10	Shows that the sensitivity and the signal-to-noise ratio of a receiver improved due to audio processing.



Figure 8. Audio Output with Baseband Channel Noise

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II. NE5750

A CLOSER LOOK AT THE NE5750:

Referring to Figure 11, the NE5750 has seven main features which make this chip unique: preamp, noise canceller, VOX, compressor, expandor, buffer, and power amplifiers. (NOTE: All component labels in this section are referenced to Figure 11, unless otherwise indicated.)

Preamp:

The NE5750 provides a preamp with adjustable gain. This allows the designer to boost the low level audio signal coming out of the microphone. The microphone can be connected to Pin 1 through a DC blocking capacitor, C1 (see Figure 12). The input impedance at this Pin is $50k\Omega$.

The preamp gain of the NE5750 can be adjusted from 0dB to 40dB by an external resistor, R7, connected to Pin 2 through a capacitor C2. Below is a formula which allows the designer to determine the value of R7 for a certain value of gain.

FINAL AUDIO SENSITIVITY FOR 12dB SINAD No Comp. No P/D P/D only -85 Comp. and P/D (dBm) -95 -95 ⊥INI 100 ي 105 -110 -115 -20 -10 20 -30 0 10 Audio Level (dB) SIGNAL TO BACKGROUND NOISE (-100dBm RF) 70 BACKGROUND NOISE (dB) 0 0 0 00 00 Comp. and 50 -40 P/D on ٩ 20 No Comp. No P/D SIGNAL 10 0 -30 -20 -10 0 10 20 Audio Level (dB) SR00967

Figure 10.

R7 =
$$\begin{bmatrix} \frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1} \end{bmatrix} - 500$$
 (1)

Table 6.Calculated R7 Values for DifferentPreamp Gains

X (dB)	R7
0	Leave Pin 2 open
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

Noise Canceller:

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the noise canceller is to automatically provide a

set gain of either 0dB when no signal is present, or 10dB when a signal is present. With this feature, background noise is minimized from transmission.

If a designer wanted a preamp gain of 20dB, a $5k\Omega$ resistor would be required (see Table 6).

This automatic gain setting can only be implemented when the noise canceller circuitry is used in conjunction with the VOX circuitry. The threshold and attack and release time can be set externally. This will be described in more detail in the "VOX" section.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times (regardless of the presence of a signal). Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7.Setting Up the Gain of the NoiseCanceller

Din No.	Gain of Noise Canceller		
Pin No.	0dB	10dB	
3	Ground	Ground	
4	Ground	V _{CC}	
7	10k to GND	Ground	

The output of the noise canceller is accessible to the designer at Pin 24. C13 is used as a DC blocking capacitor.

VOX:

As mentioned earlier, the VOX circuitry works together with the noise canceller circuit. Pins 3, 4, 5, 6, and 7 all deal with the VOX's performance.

All of the resistor and capacitor values given in the NE5750 data sheet are chosen to meet AMPS/TACS specification for cellular radio. So any deviation from these values should be considered carefully if the application is in cellular radio.

Connected to Pin 3 is a resistor R2 and capacitor C15, as shown in Figure 13. These components set the gain of the VOX. The values

here are for internal use only and have no direct relationship with the performance. So the values should be kept as shown. In some special applications, R2 may be adjusted such that the voltage on Pin 4 can be increased. By increasing this voltage, the voltage on Pin 7 can be set to a higher range (more details later).

Pin 4 has C3 and R1 connected to it which affects the attack and release time of the VOX circuit. In general the attack time should be faster than the release time.

The values given for C3 and R1 provide an approximate attack time of 12ms and release time of 120ms. These values should be kept as shown.

The timing of the VOX circuit is important because it controls the gain of the noise canceller, and can also turn the transmitter on and off.

- VOX_{OUT} and VOX_{CTRL}

By using VOX_{OUT} and VOX_{CTRL}, Pins 5 and 6 respectively, the NE5750 can control the status of the transmitter. The VOX_{OUT} Pin should have a 10k Ω pull-up resistor to V_{CC}. When probing Pin 5, a logic '1' or '0' will be read. The VOX_{CTRL} pin should have a logic '1' or '0' connected to it. Table 8 shows how Pins 5 and 6 can be used:

Having a logic '0' on Pin 6 is sufficient in most applications. When voice is present, the noise canceller kicks on while the VOXout Pin supplies a logic '1'; when voice is not present, VOXout Pin supplies a logic '0'. In a cordless phone application this logic level could be used to turn the transmitter on and off, thereby conserving power for any battery operated applications.

Supplying a logic '1' on Pin 6 would cause the transmitter to stay on regardless of any signal input to Pin 1. However, the functionality of the noise canceller will still be signal dependent.



Figure 11. NE/SA5750 Application Demo-Board

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NE5750 Microphone Pin 1 Noise C1 Cancellation 50k Gain Control Pin 2 C2 0.5k 50k R₇ 50,000 R-500 X(dB) 10^{-} 20 "X" in dB SR00969

Figure 12. Setting Microphone Preamplifier Gain







Figure 14.

This condition is mainly used if the battery consumption is not a problem. Such a condition would be for any car cellular radios.



Figure 15. Compandor Dynamic Range

- setting the threshold

R3 at Pin 7 is used to set the threshold of the VOX. Setting the threshold determines the voltage level input at which the noise canceller and VOX will activate. Formula 4 shows how to calculate the VOX's threshold.

$$VOX_{\text{THRESH}} (\text{mV}) = 50\mu\text{A} \cdot \text{R3} (\text{K}\Omega)$$
(4)

Where R3 >
$$3k\Omega$$
)

If R3 = 5.6k, the measured voltage at Pin 7 should be approximately 280mV.

The way to adjust the VOX is to first determine what signal level is desired at Pin 1 to activate the VOX noise canceller circuits. Once that level is applied to Pin 1, connect a voltmeter to Pin 4. The voltage level measured here should be plugged into formula 4 to determine R3.

As mentioned earlier, the voltage at Pin 4 can be increased by R2. But one should only deviate from the R2 value if the voltage at Pin 7 cannot come down. In most cases, setting R2 to $43k\Omega$ and setting Pin 7 to the voltage at Pin 4 is sufficient.

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Figure 14 shows graphically how R3 and R2 affect the location of the "box". The "box" is always 10dB, which is due to the noise canceller circuit.

EXAMPLE I : Set the VOX threshold such that it "kicks on" when $30mV_{P-P}$ is applied to Pin 1 of the NE5750 with a preamp gain of 0dB.

Step 1: Make sure:

- a. Pin 7 is left open.
- b. The VOX attack and recovery components are in place at Pin 4.
- c. R2 and C15 are connected to Pin 3.
- d. If using the NE5750 alone, be sure to connect the preamp output (Pin 24) to the compressor input (Pin 23) with a DC blocking cap.
- e. The preamp gain is already set (in this instance the preamp gain is 0dB).
- f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional

Step 2: Apply a constant 1kHz sinewave signal to Pin 1 with the desired threshold. In this case, $30mV_{P-P}$.

Step 3: Measure the DC voltage on Pin 4; V4=260mV

Step 4: Calculate R3:

- $R3 = V4(V) / (50 \mu A)$
 - = 0.260/50μA
- = 5.2k

let's use a 5.3kΩ

Step 5: Connect R3 to Pin 7 and verify that VOX "kicks on" at the desired threshold.

- This set-up has the VOX kicking on at $30mV_{\text{P-P}}$ and kicking off at $11mV_{\text{P-P}}$

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Table 8.VOX Truth Table

Inp	outs	Out	outs
Voice (Pin 1)	VOX _{CTRL} (Pin 6 of NE5750)	Noise Canceller Gain	VOX _{OUT}
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: To apply a logic '0' on Pin 6 by the l^2C evaluation program, be sure that the VOX_{EN} is high, and low for a logic '1' on Pin 6. If the NE5750 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

Compandor:

- compressor

The compressor input at Pin 23 requires an external DC blocking capacitor (C12). The input impedance is roughly $50k\Omega$. Unlike the older compandors, this input can be directly driven from CMOS circuits (e.g. NE5751).

The gain from the preamp should be adjusted such that there is enough signal getting to the compandor. However, one must be careful not to overdrive the inputs. Additionally, do not forget the extra 10dB gain from the noise canceller (assuming it is being used).

Figure 15 shows the typical dynamic range of the compandor. The maximum input signal that the compressor can handle is $3.72V_{P,P}$ or 24.6dB. The minimum input is approximately $1.74mV_{P,P}$ or -42dB. Knowing that the 0dB point of the compandor is at 77.5mV_{RMS}, one can easily convert from volts to dB. Formula 5 shows the conversion from V_{RMS} to dB.

$$X(dB) = 20 \log \left(\frac{V_{RMS}}{77.5(mV_{RMS})} \right)$$
(5)

where X = value in dB V = voltage in RMS.

Usually it is easier to work in voltages, but in this case it is better to work in dB. If one knows the input signal in dB, the designer can predict the output of the compressor (also in dB) to be half or two times the input. For instance, if the input were 10dB, we could expect the output to be 5dB. On the other hand, if the input was -20dB, we could expect the output to be -10dB.

Capacitor C11 on Pin 22 controls both the attack and release time of the compressor. The attack time may be calculated by Formula 6.

Attack time =
$$\mathbf{R} \cdot \mathbf{C}$$
 (6)

where R=10k Ω

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NOTE: The release time is roughly 4 times slower than the attack time by design.

Release time = $4 \cdot \text{Attack time}$

Capacitor C10 on Pin 21 is used for AC bypassing. Capacitor C9 on Pins 19 and 20 is also for AC bypassing.

- expandor

The expandor input at Pin 17 requires an external DC blocking capacitor (C8). The input impedance is around $2.5k\Omega$. Referring to Figure 15, the input range of the expandor

is from 19.53mV_P-P (-21dB) to 903mV_P-P (12.3dB). The output range is from 1.74mV_P-P (-42dB) to 3.72V_P-P (24.6dB).

Capacitor C7 is used to set the attack and release time of the expandor. Formula 6 can also be used to determine those values.

- how to measure attack and recovery time

In this section we will briefly describe the bench procedure for measuring attack and recovery times. Additional information can be found in AN174 in the "Attack and Decay Time" section.

Let's assume that $C_{RECT} = 2\mu F$ and $R_{INTERNAL} = 10k$. Since $T = R \cdot C$, then T=20ms. If we wanted a different "RC" time constant we would change the C_{RECT} value ($R_{INTERNAL}$ is a fixed value).

Using these component values let's measure the attack and recovery times to see if the CCITT and EIA specifications are met.

measurement at compressor: EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 12dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "0.75" times the final steady state value, for a 12dB step down.

The compressor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Compressor Test

- Apply a 1kHz sinewave signal at 0dB to the input of the compressor (0dB is defined where the compandor passes the input signal through to the output — unity gain level for the APROC is 77.5mV_{RMS}.
- 2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
- 3. Connect an oscilloscope probe to the input of the compressor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:4 ratio is achieved on the screen of the oscilloscope (see Figure 16a).

Adjusting for a 1:4 ratio produces a 0dB to 12dB step at the input. The unit "1" represents the 0dB input level and the unit "4" represents the 12dB input level ($20\log (4/1) = 12dB$).

- 4. Connect another oscilloscope probe to the output of the compressor and observe the waveform (see Figure 16b). The "final steady-state" value for the attack time is "2" units while the release time is "1" unit. These output values are expected because, for a compressor, the ratio is 2:1 unless the input is at 0dB, in which case, the ratio is 1:1.
- 5. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figures 16c and 16d).

To measure the attack time (T_A) :

-According to the EIA specifications:

 $T_A = 1.5 \cdot Final Steady - State Value$

-therefore

 $T_A = 1.5 \cdot 2$ units = 3 units

-Measure the time it takes for the output to drop to the 3rd unit. According to Figure 16c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R) :

-According to the EIA specifications:







-therefore

 $T_A = 0.75 \cdot 1$ unit = 0.75 units

-Measure the amount of time it takes for the output to rise up to 0.75 units. According to Figure 16d, our release time is 13ms. Again the CCITT spec. is met.

measurement at expandor:

EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "0.57" times the final steady state value, for a 6dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 6dB step down.

The expandor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Expandor Test

- Apply a 1kHz sinewave signal at 0dB to the input of the expandor (0dB is defined where the compandor passes the input signal through to the output — unity gain level).
- 2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
- Connect an oscilloscope probe to the input of the expandor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:2 ratio is achieved on the screen of the oscilloscope (see Figure 17a).

Adjusting for a 1:2 ratio produces a 0dB to 6dB step at the input. The unit "1" represents the 0dB input level and the unit "2" represents the 6dB input level (20log(2/1)=6dB).

- 4. Connect another oscilloscope probe to the output of the expandor and observe the waveform (see Figure 17b). The "final steady-state" value for the attack time is "4" units while the release time is "1" unit.
- 5. These output values are expected because for an expandor the ratio is 1:2 unless the input is at 0dB, in which case, the ratio is 1:1.
- 6. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figures 17c and 17d).

To measure the attack time (T_A) :

-According to the EIA specifications:

 $T_A = 0.57 \cdot Final Steady - State Value$

-therefore

 $T_A = 0.57 \cdot 4$ units = 2.28 units

-Measure the time it takes for the output to reach 2.28 units. According to Figure 17c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R) :

-According to the EIA specs.:

 $T_R = 1.5 \cdot Final Steady - State Value$

-therefore

 $T_A = 1.5 \cdot 1$ unit = 1.5 units

-Measure the amount of time it takes for the output to drop to 1.5 units. According to Figure 17d, our release time is 13ms. Again the CCITT specification is met.

These results show that the release time is about 4 times slower than the attack time. All Signetics compandors are internally set up this way so that once the attack time is set by C_{RECT} , the release time is automatically set.



Figure 18. Speaker Amplifier for the NE5750



Figure 19. Setting Gain for Earphone Amplifier

Special Note: In AN174, Figures 10 and 11 show the X-axis as being in fractions of the time constant. The way to clarify this is by multiplying 20ms to these numbers to convert them to the measured attack and recovery time. The 20ms comes from the "RC" time constant which can be varied by varying the C_{RECT} value. But again, once these numbers are converted, one can see that these figures show similar results as ours in the lab.

Amplifier Section:

-speaker amplifier

The speaker amplifier is a unity gain amplifier with a high input impedance. Located on Pin 11, the output of the amplifier, are two capacitors C5 and C16. Capacitor C5 is for DC blocking, while C16 is for high pass filtering.

Since the amplifier's input is not directly accessible to the designer (see Figure 18), it is impossible to exceed a gain of one. However, if external attenuation is desired, use formula 7 to determine the series resistor that would connect to Pin 14.

$$A_{V} = \frac{-R_{F}}{R_{IN}}$$

$$= \frac{-50k}{(50k + R_{S})}$$
(7)

In most cases, the attenuation takes place in the NE5751 before the signal gets to the amplifier. Therefore, adding external attenuation is rare.

-earphone amplifier:

Unlike the speaker amplifier, the gain of the earphone amplifier can be set by external resistors. In this case, the required output and input are directly accessible. Figure 19 is a diagram of the earphone amplifier with the required equations. Sidetone gain can also be implemented with an external resistor.

How To Power Down

"Power down" or "power up" can be implemented by Pin 10 of the NE5750. When Pin 10 is connected to V_{CC} , the chip is in the "power up" state. In this mode, the chip is fully functional. However, when Pin 10 is connected to ground, the chip is in the "power down" state where the current consumption drops dramatically (CMOS or TTL levels will suffice). In this mode, the chip is not expected to be functional, but all of the capacitors remain charged so that "power up" can occur quickly. Having this capability allows the system to conserve battery power.



Figure 20. NE5751 Tx Bandpass Filter

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III. NE5751

A CLOSER LOOK AT THE NE5751:

Figure 24 shows a block diagram of the NE5751. Key functions for this chip include a TX bandpass filter, TX pre-emphasis filter, TX low pass filter, summing amplifier, RX bandpass filter, RX de-emphasis, programmable DTMF generator, programmable attenuator, and an $l^2 C$ bus interface.

-TX path

The input and output of the TX bandpass filter are located on Pins 3 and 4, respectively. The 4th-order Chebyshev bandpass filter is designed to pass 300 to 3000Hz (voice band). (see Figure 20).

The input to the pre-emphasis circuit is accessible through Pin 5. This filter shapes the spectrum with a +6dB per octave slope in the pass band (see Figure 21). The output is then connected internally to a low pass filter and limiter circuit (see Figure 22). The functions of the last two filters guarantee that the 12kHz maximum frequency deviation for cellular radio is not violated.

The output of the limiter filter (Pin 23) and the output of the programmable DTMF generator (Pin 22) can be connected to the input of the summing amplifier. The gain of this amplifier can be controlled with external resistors. In Figure 24, the resistors are all 51k Ω which creates a unity gain configuration. The output of the amp is then connected to the transmitter.



The Limiter and All-pass Circuit:

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC should be less than 12kHz regardless of the input signal. Figure 23 shows the equipment used for the test measurements and how the

signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference, then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 26)

Formula 8 was used to calculate maximum frequency deviation from the waveforms shown in Figure 26.

Max Freq Dev with All-Pass Ckt = (8) $\frac{BW_{F}}{BW_{R}} \cdot 8kHz$

where

 BW_F = the bottom waveform's peak-to-peak voltage from one of the observed Figures.

 BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure.

Table 9. Maximum Frequency Deviation Results for the 12kHzTest

Frequency (Hz)	With All-Pass (kHz)
300	5.91
500	9.04
800	10.09
1000	10.09
1200	10.09
2000	11.13
3000	10.78

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5750 and NE5751 will meet the 12kHz AMPS specification. If a customer needs further assurance that the 12kHz specification will be satisfied, an Automatic Level Control (ALC) circuit can be placed after the summing amplifier output of the NE5751. Keep in mind, though, that this ALC will only provide attenuation.

- RX path

For the receive side of the NE5751, the signal goes to the input of the RX bandpass filter (Pin 13) which has the same characteristics as the TX bandpass filter. The only difference is that this filter also has a stop-band notch filter at 6kHz to reject the Supervisory Audio Tone (SAT) signals as seen in Figure 27.

The output is then internally connected to the de-emphasis filter. This filter provides a -6dB/octave slope over the passband to compensate for the pre-emphasis function (see Figure 28).

The attenuator can be digitally programmed by I^2C . The input signal level can be attenuated 16 steps in 2dB increments. This gives a range from 0dB to -30dB. The attenuator error is shown in Figure 29.







Figure 23. Test Set-up and Tx Path of Signal

I²C Bus Interface:

The NE5751 is controlled by a serial control bus comprised of a clock input, serial bus address, serial clock line, and serial data line.

A designer who is unfamiliar with I²C can refer to the following documents for assistance: 1) I²C Bus Specification and 2) Signetics AN168. Both of these documents can be found in the 1989 Signetics Linear Data Manual or the 1991 RF Communications Handbook.

The clock input requires an input frequency of 1.2MHz. This frequency is vital for the operation of the part because it effects the DTMF generator and the 3dB point of all the switch capacitor filters.

The output of the DTMF generator can be determined by Formula 8.

Low Freq =
$$\frac{\frac{\text{Clock Input Freq}}{12}}{\text{LD}}$$
 (8a)

where LD is the value of the register This translates to: DTMF LO REG = 100000/ LO REG (Hz)

$$High Freq = \frac{\frac{Clock Input Freq}{6}}{HD}$$
(8b)

where HD is the value of the register

This translates to: DTMF HI REG = 200000/ HI REG (Hz)

Table 10 can be used to help the designer program the DTMF generator.

There are a few key points that should not be overlooked when programming the NE5751. The control registers consist of the

- 1. Register map
- 2. Signal path register
- 3. Volume control and test register
- 4. High tone DTMF register
- 5. Low tone DTMF register

To generate a single tone from the DTMF generator, use the appropriate registers (high or low DTMF) and load the other one with a '0', '1', or '2' to silence it.

The order of these registers is important. If the programmer wanted to turn down the volume, he/she would have to re-program the register map, signal path, and then give the new data to the volume control and test register.

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Figure 24. NE/SA5751 Test and Application Circuit

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Number Dialed	High Freq.	Low Freq.	DTMF HI	DTMF LO
1	1209	697	A5	8F
2	1336	697	96	8F
3	1477	697	87	8F
4	1209	770	A5	82
5	1336	770	96	82
6	1477	770	87	82
7	1209	852	A5	75
8	1336	852	96	75
9	1447	852	87	75
0	1336	941	96	6A
*	1209	941	A5	6A
#	1477	941	87	6A

Maximum Frequency Deviation Results for the 12kHz Test Tahla 10

IV. APROC DEMO-BOARD

About the APROC demo-board:

The NE5750/51 demo-board layout can be seen in Figures 30, 31, and 32. It incorporates the use of DIP packages. However, an SO adapter could be made to test the SO APROC chips.

A separate board is used to interface the APROC demo-board with the computer's parallel port. This converter utilizes the 74LS05 as a buffer scheme.

An I²C program for the APROC is provided so that a designer can easily program and evaluate the chip set. This eliminates the need to write an evaluation program. However, it does not eliminate the need for a final system program.

The evaluation program has a graphic display that shows the transmit and receive path of the APROC on the terminal, as seen in Figure 33. By selecting a function, one can toggle the space bar on the key board to turn on or off any key features. The designer could also type in the codes for any registers to control the functions.

Figure 25 shows how the interface board and the demo-board can be used in conjunction with a computer. Once everything is connected properly, one can make his own evaluations on the chip set.



Figure 25. Interfacing the APROC Demo-board with the I²C **Evaluation Program**



Figure 26. Results From the 12kHz Maximum Frequency Deviation Test



Figure 27. NE5751 Rx Bandpass Filter

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Figure 28. NE5751 Rx De-emphasis

How to Power Down on the NE5750/51 Demo-Board:

In general, power down mode is a condition where a system has just enough power to "stay alive" and, therefore, is not expected to be fully operational. When called upon, the system can quickly get out of this mode and into the power up mode and be ready to perform its functions. This fast reaction time is possible because all of the capacitors have maintained their charges. This is because power was not cut-off completely. The power down function reduces overall current consumption when the system is not fully operational, and is especially helpful when the system is operating from a battery powered source.

There are three power down conditions when we refer to to the NE5750/51 demo-board. They are listed and described as follows:

ا1.0– 0

4

8

1. NE5750 Power Down



Figure 29. NE5751 Attenuation Error

16

Attenuation in dB

20

24

28

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12

- to reduce current consumption

- to maintain all DC voltages on the device pin to keep the capacitors charged

How To:

- use hardware switch on demo-board which forces Pin 10 to ground
- or use a CMOS logic output into Pin 10

Benefits:

- reduces current consumption while maintaining readiness
- current drops from 8.4mA to 1.8mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

2. NE5751 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device $\ensuremath{\mathsf{Pin}}$ to keep the capacitors charged up

- to open all voice paths so that no signals will flow

How To:

- program the $\ensuremath{I^2C}$ bus under the condition that all registers are set to zero

Benefits:

- all the registers are always at zero when powering up from the power down mode

- reduces current consumption while maintaining readiness
- current drops from 2.7mA to 1.1mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

Definition:

-the NE5750 and NE5751 demo-board is in the power down mode when:

- 1. The transmitter and receiver are muted on the NE5751
- 2. The NE5751 is powered down (all registers are set to zero), and
- 3. The NE5750 is powered down

How to Power Down the Chip-Set Properly (1st Choice): Please follow this recommended sequence;

1. Mute both the transmitter and receiver on the NE5751.

2. Program the following registers as follows: Signal Path Register: 00000000

Volume Control Register: 00000000

High DTMF Register: 00

Low DTMF Register: 00

3. Power Down the NE5750.

How to Simulate the Power Down on the Chip-Set (2nd choice)* Please follow this recommended sequence;

1. Program the following registers as follows:

Signal Path Register: 00010000

Volume Control Register: 01100000

High DTMF Register: 00

Low DTMF Register: 00

2. Power Down the NE5750

*NOTE: this method is only used when the NE5751 mute switches are not accessible, by design.

Comments

- 1. Muting both the transmitter and receiver on the NE5751 can be done by the two "hardware" switches on the demo-board (forces Pins 11 and 12 to V_{CC}).
- 2. Powering down the NE5751 can be done by programming the correct assigned register to zero (For more details, consult the NE5751 data sheet).
- Powering down the NE5750 can be done by the "hardware" switch on the demo-board (forces Pin 10 to ground).
- 4. When coming out of the power down mode to the power up mode, reverse the procedure given above.
- 5. If functions are activated while in the power down mode before power up occurs, the "chip-set power down" is no longer valid.
- 6. We recommend that a 2.2μ F capacitor be placed between the NE5751 de-emphasis output to the NE5750 expandor input. The purpose of this capacitor is to block any DC offset that might occur between the two chips while in the power down mode. If this capacitor is not used, an abnormal reaction might occur where white noise is generated.

V. NE5750 DEMO-BOARD

Figure 34 shows the layout for the NE5750 demo-board. This board can be used to evaluate the NE5750, alone, and allows the designer

to do extensive testing without having to worry about other external factors. Again, this board makes use of dip packages only. However, a SO adapter can be made to implement the SO version of the NE5750.

VI. QUESTION AND ANSWER SECTION

NE5750 and NE5751 (APROC):

- **Q:** Is it OK to connect the V_{REF} pins together for the NE5750 and NE5751? My circuit seems to be working properly.
- A: No, this is not a good idea. Although both V_{REF}s are at 2.5V (V_{REF} =V_{CC}/2), there is no guarantee that they will be exactly equal over temperature. One of the V_{REF}s might influence the function of the other chip which, in turn, might have a detrimental effect on the performance of the chips.
- **Q:** Will the APROC chip set work for TACS, NMT or NAMPS specifications as it does for AMPS specification?
- A: The APROC was designed to meet AMPS and TACS specifications, however, as it stands now, the chip set will also meet the NAMPs requirements. The chip set will not work for NMT specifications.
- **Q:** In the power down mode, is it OK to program the DTMF registers before powering up?
- A: No. This will break the rules of powering down. All the registers are set to zero in this mode. Please review the section on powering down the chip set properly.

NE5750:

- **Q:** Even though I have all the required external components in place on Pins 1,2,3,4,5,6 and 7, my VOX circuit does not work. What is wrong?
- A: The VOX circuit is not a trivial connection. Even though all the components are connected, be sure that the output of the NE5750 noise canceller is AC coupled to the input of the compressor to complete the VOX loop. This holds true if the NE5750 is used alone. However, if the NE5751 is used make sure that the signal is fed from the band-pass filter to the input of the NE5750 compressor input. For further advice, please read example 1 in the "setting the threshold" section of this application note.
- Q: Do I have to use I²C if I use the NE5750 alone?
- A: No, the NE5750 can be used by itself and does not require the use of I^2C .
- Q: Can I speed up the release time of the compressor?
- A: Not directly. The release time is dependent on the attack time setting. Once the attack time is set by C11 on Pin 22 of the NE5750, the release time is set internally to be four times slower. So to increase the release time requires that the attack time be increased. One should be careful because setting the attack time too fast could cause more distortion on the output.

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- **Q:** The NE5750 compressor input impedance is around 50kΩ. Why is this impedance higher than that of others in your family of compandors?
- A: The NE5750 was designed to be compatible with the NE5751. The NE5750 compressor input was modified to accept CMOS driven outputs like the NE5751. This internal modification eliminates the need for an external buffer.

NE5751:

- Q: Can I change the filter characteristics?
- A: Yes, by changing the master clock input frequency the 3dB points will be effected. For example, if F=1.2MHz, then BPF1=3kHz. Now, if F=600kHz, BPF1=1.5kHz; and if F=2.4MHz, BPF1=6kHz. This type of application is not recommended because the part was not designed to be used this way and, therefore, performance will not be guaranteed. Additionally, the DTMF generator will be off in frequency from the calculated values because of the assumption of a 1.2MHz clock, and the I²C interface will not be functional.
- **Q:** Besides I²C, can I communicate to the NE5751 with another type of operating scheme?
- A: Yes, by bit banging. Instead of using the I²C hardware one can supply the clock and data defined in the I²C protocol software. But this takes up a lot of memory, therefore, it is preferable to implement the I²C hardware.

- **Q:** The limiter seems to work when I overdrive the input with a strong signal. However, when I try to pass DTMF tones, the limiter's level varies when switches T3/T5 and T4 are set to different settings Why is this? Isn't the output supposed to stay constant regardless of the input being overdriven or passing DTMF tones?
- A: Yes, the limiter should hold the output constant when an overdriven signal is applied, but only when the switches are used properly. When passing DTMF tones, T1, T2, and T4 should be left open, while T3/T5 are closed. The voice path should be disconnected when DTMF tones are being passed. Hence, T3/T5 should be left open when DTMF is not used.
- **Q:** When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?
- A: The way to make it stay on longer than 96ms is to re-load the DTMF registers (re-program the DTMF registers before 96ms expires).

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"Audio Processing for Cellular Radio or High Performance Transceivers", proceedings of R.F. Expo 1989, A. Fotowat, S. Navid, L. Engh, pp. 195-203.

"Designing Cellular Radios with the Philips Components-Signetics Cellular Chip Set", Cellular Radio Chip Set Design Manual, Feb. 25, 1990.

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TROL TROL



Figure 31. NE5750, NE5751 Cellular Radio Application Circuit

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Component Functions

- R1 Pull-up resistor for VOXOUT logic levels
- Sets gain of VOX, but for internal use only effects voltage on Pin 4 R2
- Used to set release time of VOX R3
- R4 Sets threshold level of VOX
- R5 Feedback resistor for ear amplifier
- R6 Sets gain of ear amplifier for the side tone input
- R7 Used in conjunction with C10 to filter out unwanted noise. Optional
- R8 Sets gain of ear amplifier
- Used to bias up Pin 14 to 2.5V by connecting $V_{\ensuremath{\mathsf{THRESH}}}$ to $V_{\ensuremath{\mathsf{REF}}}$ without R9 loading down VREF source
- R10 Input resistor for summing amp out. Can be used to set gain of signal
- Input resistor for summing amp out. Can be used to set the gain of the DTMF R11
- R12 Input resistor for summing amp. Can be used to set gain of the side tone input
- R13 Feedback resistor for summing amp. Can be used to set gain of all the inputs
- R14 Used to set gain of the preamp of NE5750 (OPTIONAL)
- JUMPER J1
- J2 JUMPER

- Bypass cap for VCC of NE5750 C1
- C2 Bypass cap for VCC of NE5750
- C4 DC blocking cap for mic input
- C5 DC blocking cap for mic gain setting resistor
- C7 Used to set attack a release time of VOX
- Used to AC ground the VREF pin (5750) C8
- C9 DC blocking cap for speaker out
- C10 filter for speaker out
- C12 Sets attack and release time of compressor
- C13 Used to AC short the DC path for the compressor
- Provides AC path to the VOX circuitry C14
- C16 **OPTIONAL.** Basically to filter out noise Sets attack and release time for the expandor
- C17
- C18 Used to AC ground VREF pin (5751)
- C19 Bypass cap for V_{CC} of NE5751
- C20 DC blocking cap for receiver input
- DC blocking cap for ear amplifier output C21
- C22 Sets gain of VOX, internal use only
- DC blocking cap for summing amp out C23
- Bypass cap for VCC of NE5751 C24

NOTE: The board is constructed in such a way as to allow a single power supply to power the chip set, or for each chip to be powered by a separate power supply. Using separate power supplies will permit monitoring of current consumption of each part when Jumpers 3 and 4 are removed.

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Figure 32. Parts and Function List of APROC Demo-board



Figure 33. Graphical Display of the I²C Evaluation Program



Figure 34. NE5750 Demo-board Layout

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Figure 35.