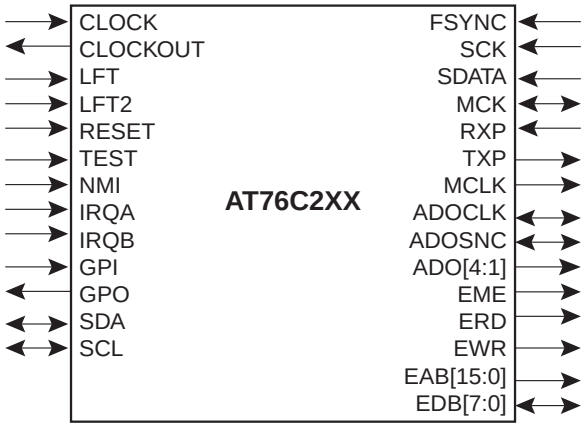
Features

- **5.1-channel Dolby Digital (AC-3)[1]**
- **Supports all Dolby Digital Configurations**
  - **Accepts Datastreams Encoded at Up to 640K bps**
- **Supports 8 Audio Channels**
- **Decodes Dolby Digital, DTS, MPEG-2, and AAC**
- **Provides Extra MIPS for User-defined Post-processing Functions**
- **All Audio Input/output Provides up to 24-bit Precision at Sample Rates of 32, 44.1, 48, and 96 kHz**
- **Internal IEC 958 Receiver (AES/EBU, S/PDIF)**
- **Supports Liner PCM Streams up to 96 kHz**
- **Auto-detection of Compressed Audio Formats**
- **IEC 958 Single-ended (S/PDIF) Transmitter for Audio Data and Dolby Digital Bitstreams**
- **Programmable Audio Data Output Interface Allows Compatibility with Many D/A Converters**
- **Provides Dolby Bass Redirection**
- **Programmable Center, Surround and Front Channel Delays**
- **Pink Noise Generation for Calibration of all Channels**
- **3.3-Volt Core and I/O**
- **64-pin PQFP Package**

Description

The AT76C2XX is a high-performance, low-cost, solution for the full decoding of Dolby® Digital (AC-3®) audio streams. The AT76C2XX, based on Atmel's high-performance 24-bit DSP, contains all the necessary interfaces to design stand-alone Dolby Digital receiver/decoder systems targeted for home theater products. The AT76C2XX accepts data from an IEC 958-compatible interface (AES/EBU or S/PDIF), or directly from an A/D converter, and generates up to 8 channels of audio. These channels can provide the one sub-woofer and five high-quality full-bandwidth channels (5.1) that are fully compliant with all the functions of the 5.1 channel Dolby Digital standard[2]. All program code is also integrated inside the chip, therefore eliminating the need for external SRAM, and minimizing system cost.



Notes: 1. This implementation has not yet completed the evaluation process by Dolby Laboratories and is offered subject to obtaining approval.

2. DTS is a registered trademark of Digital Theatre Systems.

A High-Performance Dolby Digital (AC-3®) Decoder

AT76C2XX Summary

A complete datasheet is available under NDA. Please contact:

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The AT76C2XX is based on a high-performance programmable digital signal processor capable of decoding Dolby Digital (AC-3) bitstreams. It contains the necessary hardware resources to run the Dolby Digital program, but can also be used as a high-performance, general-purpose audio encoder/decoder chip. The AT76C2XX can decode Dolby Digital bitstreams generating up to 6 independent audio channels (3 forward channels, 2 rear channels, and a sub-woofer channel). Alternately, the AT76C2XX can decode audio in the DTS and MUSICAM formats. The AT76C2XX is targeted for home-theater and multimedia products, providing users with the ultimate surround sound experience.

All Dolby Digital software is integrated inside the chip and supports all data rates and sampling frequencies used in the standard. The AT76C2XX can handle Dolby Digital bit streams encoded at rates of up to 640K bps and 48 kHz. In addition, for PCM processing, the AT76C2XX is capable of capturing and generating audio samples at sampling frequencies up to 96 kHz. It is also designed to decode multichannel Dolby Digital bit streams and downmix to two output channels in the 2/0 (Lt, Rt) Dolby ProLogic channel configuration mode. Output PCM samples of 24-bit precision can be produced, or they may be rounded to 20, 18, or 16 bits. The AT76C2XX is capable of generating the sampling rate and bit clocks necessary to drive external D/A converters directly, or it can accept these clocks from an external source. The internal memory resources are shown in the following table.

Memory Type	X Data	Y Data	Program	Total
Data Memory	8K x 24	2K x 24	1K x 40	35K bytes
Program Memory		2K x 24	3K x 40	21K bytes

Architecture

The main functional units of this chip are the Program Control Unit, the Address Generation Unit, the Data Arithmetic/Logic Unit, the External Interface Unit, and the System Stack. There are three 16-bit unidirectional address buses, providing support for three separate memories of up to 64K words each. The Program Address Bus (PAB) controls access to the program memory, while internal data memory is addressed by either the X address bus or Y address bus (XAB, YAB). Similarly, there is one bidirectional 40-bit program bus and two bidirectional 24-bit data buses. The Program Data Bus (PDB) is used to fetch instructions from the program address space to the instruction decoding unit. It can also be used to load the program memory with code from external memory during a bootstrapping operation. The other data buses (XDB, YDB) transfer to and from the X data address space and the Y data address space, respectively. Operations on each of the three data buses can occur independently of other data transfers, and all may be in use simultaneously, depending on the instruction being executed.

General Architectural Features:

- 45 MHz instruction clock (45 MIPS)
- Two 24-bit datapaths, one 40-bit datapath
- 16-bit addressing
- Three-stage instruction pipeline: fetch, decode, execute
- 4K x 40 program memory, 8K x 24 X data memory, 4K x 24 Y data memory
- High degree of parallelism due to 40-bit instruction words - up to 2 parallel data moves per instruction
- Addressing modes include index-based, circular, and bit-reversed indexed (for radix-2 FFTs)
- Zero-overhead single and block instruction repeats
- Nestable block repeats
- Two 56-bit accumulator registers
- ALU performs multiply and accumulate plus convergent rounding in one clock cycle
- Saturation logic for overflow protection
- 15 x 32 hardware stack
- External memory interface provides program/data bootstrapping capability
- Three external interrupts - two maskable, one non-maskable
- Support for zero-overhead, fast automatic return interrupts
- General purpose output pin for control of external devices
- Programmable interrupt/reset timer
- Two PLLs - one for internal logic clocks, one for D/A converter clocks
- Sleep (standby) mode
- 3.3-Volt core and I/O