Features

- DAVIC/DVB/ETS300.429/ITU-T J.83 Annex A, C Fully Compliant
- Direct IF Sampling (No Second IF Down Conversion Required) or Baseband Input
- Internal 10-bit A/D Converter or Possibility to Use External A/D
- 1024, 512, 256, 128, 64, 32, 16 QAM And QPSK Demodulation
- Roll-off Factor Adapted to Raised-cosine Filtered Signal (0.11 to 0.4)
- Fully Digital Timing Recovery
- Variable Symbol Rate Recovery
- Anti-aliasing Continuously Variable Digital Filtering with Symbol Rate Adaptive Bandwidth (1 to 18.75M Baud at the Same Sampling Frequency)
- Fully Digital Carrier Recovery (Coherent or Differential For QPSK)
- Robust Equalizer Acquisition
- Selectable Transversal or Decision Feedback Equalizer
- Dual Phase/Frequency Offset Recovery Up To 12% of the Symbol Rate with no Degradation
- MPEG2 Frame Synchronization
- Reed-Solomon Decoder (204, 188, 8)
- De-interleaving (I = 12 and I = 17)
- Energy Dispersal Descrambling
- 2-wire Serial Interface (2WSI) Switch for Separate Bi-directional 2WSI Bus-to-tuner To Avoid Phase Noise Problems Due to 2WSI
- Integrated Clock Reference for Tuner, Especially Designed For NIU in CAN
- Two AGCs: Analog and Digital Gains
- Three Program Identifiers (PIDS) Filtering
- IRQ Interrupt Request Generation to Simplify Monitoring
- Bit Error Rate and Packet Error Rate Monitoring
- Signal-to-noise Ratio Estimation, Residual Phase Noise Estimation
- Automatic Spectrum Inversion
- JTAG Support
- 0.35µ CMOS Technology, 3.3V Operation
- Available in a 144-lead LQFP Package

Description

The AT76C651B is a DVB-compliant Quadrature Amplitude Modulation (QAM) demodulation circuit, which can be used in DVB and other applications using Quadrature Phase Shift Keying (QPSK) or QAM transmission systems. The signal, after output from tuner and adjacent channels rejection filter, is sampled at Intermediate Frequency (IF).

The signal is converted to digital format and goes through several processing steps required for demodulation: automatic gain control, baseband down conversion, timing recovery with anti-aliasing filtering, square root raised-cosine receive filtering, carrier recovery and digital gain control and equalization (linear and decision feedback dual structure). The output from demodulation then goes through forward error decoding: DVB/DAVIC de-mapping, frame synchronization, de-interleaving, Reed-Solomon decoding and spectrum de-randomization. The output before decoding may also be output directly for use with post-processing devices in applications other than DVB.

An additional block situated in the back-end may be used to filter out programmable PIDs, providing additional flexibility in interactive solutions or DVB data-broadcast PC receive cards.

It is especially designed for modem implementations with a 24-bit mask on one PID (medium access control) and can be used for return channel implementation.

Digital Reception/ Transmission IC Integrated DVB® -compliant QAM Demodulator

AT76C651B

Summary

Rev. 1375BS–11/01

Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

Table 1. Signal Description

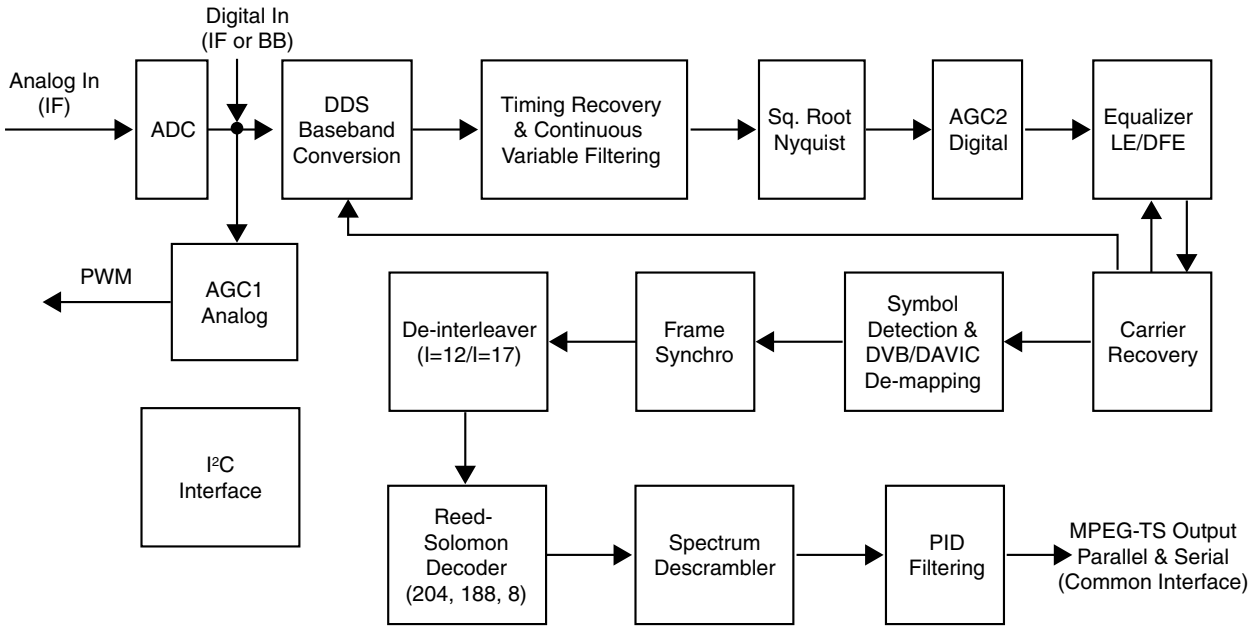
Signal Name	Function	Number of I/Os	Pull-up	Voltage	Direction
2WSIADDR	2WSI circuit address selection	2	No	V_{DD3}	I
2WSISDA	SDA line of 2WSI	1	R = 15 kΩ	V_{DD5}	I/O
2WSISCL	SCL line of 2WSI	1	No	V_{DD5}	I
T2WSISDA	2WSI bus data line SDA to/from tuner through bi-directional switch	1	R = 15 kΩ	V_{DD5}	I/O
T2WSISCL	2WSI bus clock SCL to tuner through switch	1	No	V_{DD5}	O
IFIBB	IF 6 MSBs or I-baseband digital input	6	No	V_{DD3}	I
IFQBB	IF 4 LSBs or Q-baseband digital input 4 MSBs	4	No	V_{DD3}	I
QBB	Q-baseband digital input (2 LSBs)	2	No	V_{DD3}	I
PLLCTRL	PLL division/bypass control	3	No	V_{DD3}	I
XOCLK	Crystal oscillator input	1	No	V_{DD3}	I
XTAL_I	Crystal input	1	No	V_{DD3}	I
XTAL_O	Crystal output	1	No	V_{DD3}	O
OSCMODE	Oscillator input mode (low for crystal, high for XO)	1	No	V_{DD3}	I
LFTPLL	Low pass filter input to PLL	1	No	V_{DD3}	A
EXTADC	External AD converter. High = external, low = internal	1	No	V_{DD3}	I
ADCLK	Sampling clock for external AD converter	1	No	V_{DD3}	O
TDI	JTAG	1	No	V_{DD3}	I
TDO	JTAG	1	No	V_{DD3}	O
TMS	JTAG	1	No	V_{DD3}	I
TCK	JTAG	1	No	V_{DD3}	I
TRST	JTAG	1	No	V_{DD3}	I
DATAOUT	MPEG2-TS parallel byte <0:7> or serial bit stream output <0>	8	No	V_{DD3}	O
CORFAIL	RS packets not corrected	1	No	V_{DD3}	O
CORBYTE	Corrected byte indicator	1	No	V_{DD3}	O
DATAVALID	MPEG2-TS byte or bit output enable active at level 0 or on both edges	1	No	V_{DD3}	O
FRMSTART	Start of MPEG2-TS frame	1	No	V_{DD3}	O
FRMVALID	Valid MPEG2-TS frame control in parallel mode output	1	No	V_{DD3}	O
FLAGPID	PID filtering indicator	2	No	V_{DD3}	O
IRQ	Interrupt request. Open drain (pull-up or pull-down depends on 2WSI configuration).	1	No	V_{DD3}	O
LOCK1	Maskable lock signal 1	1	No	V_{DD3}	O
LOCK2	Maskable lock signal 2	1	No	V_{DD3}	O
CSTPWM	Configurable value output with PWM	1	No	V_{DD5}	O
AGC	Analog automatic gain control PWM	1	No	V_{DD5}	O

Table 1. Signal Description (Continued)

Signal Name	Function	Number of I/Os	Pull-up	Voltage	Direction
TUNCLK	4 MHz reference oscillator output to tuner (configurable by 2WSI)	1	No	V_{DD5}	O
REF2CLK	Half digital clock	1	No	V_{DD3}	O
PHASYM	Test output signal	1	No	V_{DD3}	O
ENSYM	Test output signal	1	No	V_{DD3}	O
ADIN1	Differential input with C_{IN} = 2 pF	1	No	1V pp	I
ADIN0	Differential input with C_{IN} = 2 pF	1	No	1V pp	I
ADREF	Reference voltage for differential input	1	No	$V_{DD3}/2$	O
VREFN(1)	Internal reference voltage test pin.	1	No		O
VREFP(1)	Internal reference voltage test pin.	1	No		O
ADBG(1)	Bandgap reference voltage test pin	1	No	1.25V	O
GND	Ground				GND
2WSIGND	2WSI ground				GND
VDD	+3.3V supply			V_{DD3}	PWR
2WSIVDD	2WSI power supply			V_{DD5}	PWR
TESTMODE	Test pin. Low for normal operation.	1	No	V_{DD3}	I/O
RESET	Hard reset of circuit	1	No	V_{DD3}	I

Note: 1. To achieve noise immunity and improved results at A-to-D conversion, capacitors may be added to GND on these pins (100 nF, ceramic/ 10 µF, tantalum).

Figure 1. AT76C651B Block Diagram



Functional Description

The following sections describe the main functions of all blocks included in the AT76C651B QAM demodulation IC.

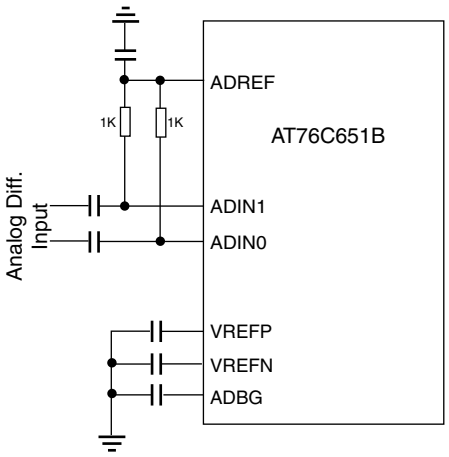
Analog-to-digital Converter (ADC)

A 10-bit analog-to-digital converter (maximum sampling frequency 32 MHz, maximum signal frequency 65 MHz) is integrated into the device. The converter samples the IF input, producing a digital spectrum around IF (and its images). The sample and hold operates at frequencies up to 65 MHz, thus enabling sub-sampling capability for signals at IF frequency up to about 65 MHz. The A/D converter is only usable when the signal is in IF frequency. In this case, inputs IFIBB, IFQBB and QBB should be pulled down to ground. It is also possible to use a 10-bit external A/D in case of a signal in IF frequency.

In case of a signal in baseband, two external 6-bit ADCs must be used. The sampling clock of the ADCs must be taken on pin ADCLK of the chip. The digital outputs of the ADCs must connect input IFIBB5 to IFIBB0 for I input, input IFQBB3 to IFQBB0 and QBB1 to QBB0 for Q input (MSB to LSB). Sampling phase should be configured as described in the ADC register ADCLKCFG.

The sampling clock frequency (on ADCLK) is equal to the input frequency if the PLL is used (either with a crystal oscillator XO) or half the oscillator frequency if the PLL is bypassed. Two examples: If a 28 MHz crystal is used, the sampling frequency is 28 MHz; if a 60 MHz XO is used, the sampling frequency is 30 MHz.

Figure 2. ADC Input and Configuration



DC Offset Control

An internal DC-offset compensation is done on the I and Q baseband signals in order to compensate potential offsets created by AD converters.

Direct Digital Synthesizer (DDS) – Coarse Tuning

An IF-to-baseband conversion from the IF digital image is then performed. This digital image frequency is configurable, which reduces the constraint on the relation between the SAW filter center frequency and the chip oscillator. The frequency of the DDS is further adjusted by the carrier frequency recovery in order to adjust exactly the received spectrum to the receive filter.

"Analog" Automatic Gain Control (AGC1)

The signal level at the ADC input is adjusted through a first AGC loop. The power estimation block estimates the signal level at the output of the ADC, compares it to a given level and generates a Pulse Width Modulation (PWM) signal, which controls the analog gain. The PWM output generates a very stable control. Since power estimation is done by digital loop control, only the output is given in PWM format for simpler implementation on board (only an RC filter with about 1 kHz cut-off bandwidth is required), whose frequency is $f_{PWM} = f_{REF}/2$. The power

estimation is made over the entire signal sampled by the ADC, thus including the adjacent channels and the target signal. This ensures that no analog saturation can happen due to the AGC feedback.

Also, the power estimation of the analog gain control can be used in conjunction with the AGC2 level (which indicates the power of the QAM signal only) in order to compute the power of adjacent channels. This may be used to adjust the takeover point (TOP) of external amplifiers when several amplifiers are required on the board (typically in the tuner and after the SAW filter). Note that an 2WSI-controllable PWM is available for this purpose.

Digital Timing Recovery

The baseband conversion output is then fed to the timing recovery block. This block integrates a digital timing loop, which estimates the best resampling time. This information is provided to a time-continuous filter, which interpolates the baseband signal and produces QAM symbols at the recovered symbol rate.

The interpolating filter's main property is its continuously autoadaptive bandwidth, which allows the demodulator to recover a wide range of symbol rate $1/T_S$ with the same performance and avoids signal aliasing during resampling operation.

Square Root Raised-cosine Nyquist Receive Filter (SRRC)

The SRRC filter, with roll-off factor allowing demodulation of raised-cosine transmitted signals from 0.11 to 0.4, receives the signal from the timing recovery output and ensures an out-of-band rejection higher than 43 dB. This significant rejection increases the back-off margin of the receiver against adjacent channels.

Digital Automatic Gain Control (AGC2)

The internal digital AGC performs a fine adjustment of the signal level at the equalizer input. This AGC only takes into account the QAM signal itself, since adjacent channels have been filtered out by the SRRC, and thus compensates digitally the analog AGC, which may have reduced the input power due to adjacent channels.

Equalizer

The equalizer is based on algorithms that provide blind and robust acquisition. The equalizer compensates for the different impairments encountered on the network. Two equalizer structures can be selected: transversal (powerful for long echoes) or decision feedback (powerful for strong short echoes).

The equalizer central tap position is configurable. This allows an optimal compensation for post and pre-cursor echoes. The equalizer comprises 32 taps, which represents a length of about 6.2 microseconds at 5M bauds. This allows a large compensation for echoes with significant delays, and a total compensation for significant (small attenuation) short echoes.

Carrier Recovery – Fine Tuning

The carrier recovery block allows the acquisition and tracking of a frequency offset as high as 12% of the symbol rate, even for low signal-to-noise ratios. The phase comparator algorithm provides a high-phase noise tolerance, which reduces the tuner cost. The frequency offset recovered by the chip can be monitored through the 2WSI interface. This information can be used to readjust the tuner frequency in order to reduce the analog filtering degradation on the signal and thus improves the bit error rate. This information is also provided automatically to the DDS in order to recover the frequency with complete accuracy before receive filtering.

Differential Demodulation for QPSK

A differential demodulation can be used in a strongly distorted environment in the case of differentially encoded QPSK demodulation. This mode provides a stronger robustness against phase noise but reduces the performance of the receiver by 3 dB, as shown in theory. 2WSI register QAMSEL must be configured to set this mode.

Phase and Additive Noise Estimation

Phase noise and additive noise estimations are performed. This information can be used to select the best carrier loop bandwidth giving the best trade-off between phase noise and additive noise. The phase noise can come from the tuner and/or the LNB in MMDS application. This feature can also be used to remotely monitor the various problems encountered by an STB or cable modem at the user installation.

Symbol Detection and DVB/DAVIC De-mapping

The output is fed to the symbol threshold detector, then to the differential decoder and finally to the DVB or DAVIC de-mapper, which produces the recovered bit stream sent to the Forward Error Correction (FEC).

Frame Synchronization

The first function performed by the FEC is the frame synchronization. The bit stream is decomposed into packets of 204 bytes at the output, starting with a frame synchronization word.

De-interleaving

The packets are then de-interleaved. Two depths can be selected for the interleaver: 12 (DVB/DAVIC) and 17. The depth 17 increases the robustness of the system against impulse noise but assumes the signal has been interleaved with the same value as the modulator.

Reed-Solomon Decoder

The de-interleaved output is sent to the Reed-Solomon (RS) input, which performs a correction of a maximum of eight errors (bytes) per packet. The RS also provides other information regarding the uncorrected packets and the position of the corrected bytes in the packet, if there are any.

Spectrum Descrambler

After RS decoding, the packets are descrambled for energy dispersal removal.

PID Filtering

A Program Identifier (PID) filtering can be performed on the MPEG2 Transport Stream (TS) before feeding the packets to the output. Three PIDs can be selected at the same time. This block outputs an enable signal on the packet stream that goes to the component interfaced with the QAM demodulator. This provides an interesting feature for on- board PC implementations, where either data or video and audio are processed directly by the PC processor. A mask is provided for one of the PIDs, offering a filter on the overall MPEG-TS packet header.

Note that one of the PIDs can be selected, so that a special enable output can be used to filter out all MPEG-TS packets containing MAC messages (for in-band return channel implementations of the DVB-RC specification). This stream contains all the control information for the return channel, and is required by other components used for the return channel.

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