Features

- 80C51 Core with 12 or 6 Clocks Per Instruction
- 768 bytes RAM
- AT83C5123 with 16K bytes ROM
- AT83EB5123 with 16K bytes ROM and EEPROM data 256 bytes (AT24C02)
- Multi-protocol Smart Card Interface
  - Certified According to ISO7816, EMV2000, GIE-CB and WHQM Standards
  - Asynchronous Protocols T = 0 and T = 1, with Direct and Inverse Modes
  - Step-up/down Converter with Programmable Voltage Output: 5V and 3V (60 mA), 1.8V (20 mA)
  - 4 kV ESD Protection (MIL/STD 833 Class 3)
- Alternate Card Support with CLK, IO and RST
- USB Module 4 Endpoints Programmable with In or Out Directions and with ISO, Bulk or Interrupt Transfers
- UART with Integrated Baud Rate Generator (BRG)
- 8 MHz On-chip Oscillator
- Analog PLL for 96 MHz Synthesis Possible 48 MHz Clock Input
- Two 16-bit Timer/Counters: T0 and T1
- Two 8 bits I/O Ports, One 2 bits
- Four LED Outputs with Programmable Current Sources: 2-4-10 mA
- Hardware Watchdog and Power Fail Detector (PFD)
- Idle and Power-down Modes
- Self-powered USB
- Low Power
  - 30 mA Max Operating Current (at F_{MAX} X2)
  - 120 µA Maximum Power-down Current at 5.4V (without Smart Card and USB)
- Voltage Ranges 3.6V to 5.5V
- Commercial and Industrial Temperature Ranges
- Packages: PLCC28, VQFP32

Description

AT83C5123 and AT83EB5123 are high performance derivatives of the 80C51 8-bit microcontrollers optimized for USB Smart Card Reader applications.

The devices retain the features of the Atmel 80C51 with 16K bytes ROM capacity, 768 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) with baud rate generator (BRG) and an on-chip oscillator.

In addition, they both have a USB 2.0 full speed function controller with four Endpoints, a multi protocol smart card interface, four programmable LED current sources (2-4-10 mA) and a hardware watchdog.

Development of application is done with AT85C122 or AT89C5122. These versions allow code to be loaded by In-System Programming (ISP) software residing in the on-chip ROM from USB or UART.

The devices have 2 software-selectable modes of reduced activity for further reduction in power consumption.

C51 Microcontroller with USB and Smart Card Reader Interfaces

AT83C5123
AT83EB5123

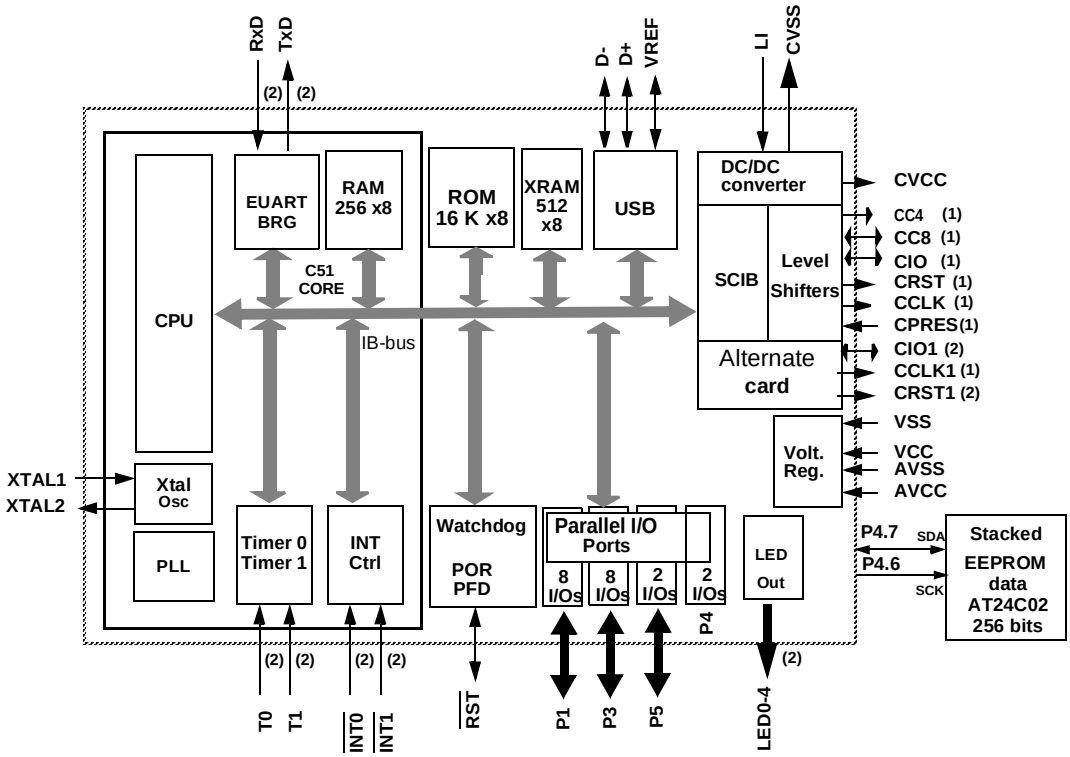
Advance Information

Summary

4201AS–SCR–11/02

Note: This is a summary document. For more information, please contact cardreader@atmel.nto.com.

Block Diagram



Notes: 1. Alternate function of port 1
2. Alternate function of port 3

Pin Descriptions

Pinouts

Figure 1. PLCC28 Pinout

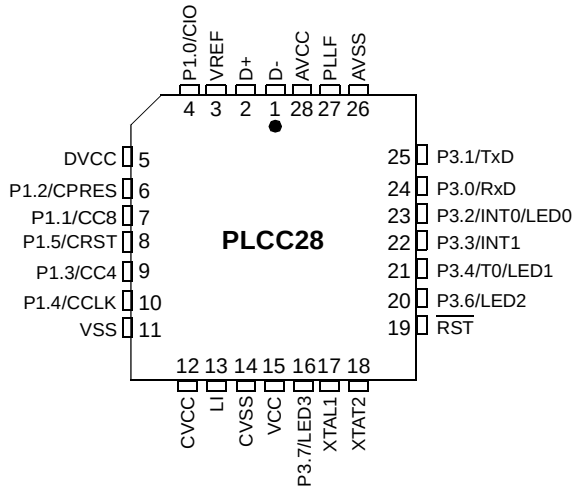
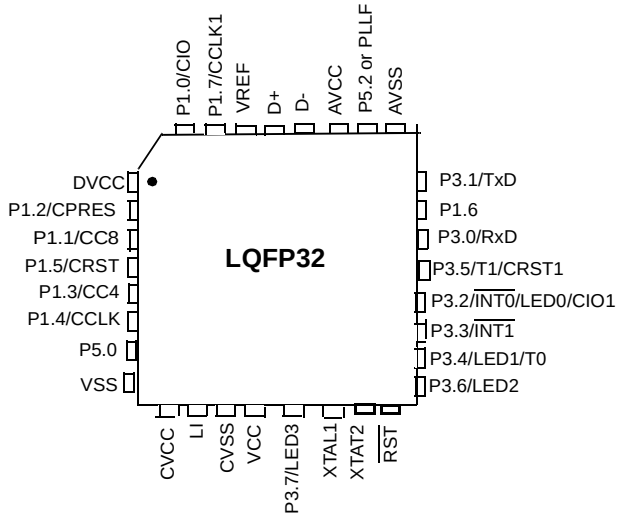


Figure 2. LQFP32 Pinout



Pin Descriptions

All the AT83C5123 signals are detailed in Table 1:

Table 1. Pin Description

Port	Pin Number PLCC28	Pin Number LQFP32	Internal Power Supply	ESD	Type	Reset Level	Alt 1	Alt 2	Reset Config	Comments
P1.0			CVCC	8 kV	I/O	0	CIO		Port51	CVCC inactive at reset
P1.1			CVCC	8 kV	O	0	CC8		Port51	CVCC inactive at reset
P1.2			VCC	4 kV	I/O	1	CPRES		Port51	Weak & medium pull-ups can be disconnected
P1.3			CVCC	8 kV	I/O	0	CC4		Port51	CVCC inactive at reset
P1.4			CVCC	8 kV	O	0	CCLK		Push-Pull	CVCC inactive at reset
P1.5			CVCC	8 kV	O	0	CRST		Push-Pull	CVCC inactive at reset
P1.6			VCC	2 kV	I/O	1				
P1.7			VCC	2 kV	I/O	1	CCLK1		Port51	
P3.0			VCC	2 kV	I/O	1	RxD		Port51	
P3.1			VCC	2 kV	I/O	1	TxD		Port51	
P3.2			VCC	2 kV	I/O	1	INT0	LED0	Port51	
P3.3			VCC	2 kV	I/O	1	INT1		Port51	
P3.4			VCC	2 kV	I/O	1	T0	LED1	Port51	
P3.5			VCC	2 kV	I/O	1	T1		Port51	
P3.6			VCC	2 kV	I/O	1		LED2	Port51	
P3.7			VCC	2 kV	I/O	1		LED3	Port51	
P5.0			VCC	2 kV	I/O	1			Port51	
P5.2			VCC	2 kV	I/O	1			Port51	
$\overline{RST}$					I		**Reset Input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{RST}$ when the device is in Idle mode or Power-down mode returns the device to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.			

Table 2. Pin Description

Signal Name	Pin Number PLCC28	Pin Number VQFP32	Internal Power Supply	Type	Comments
D+			DVCC	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 KΩ pull-up to VREF for full speed
D-			DVCC	I/O	USB Negative Data Upstream Port
VREF			AVCC	O	**USB Voltage Reference**: 3.0 < VREF < 3.6V VREF can be connected to D+ with a 1.5 KΩ resistor. The VREF voltage is cotrolled by software.
XTAL1			VCC	I	**Input to the on-chip invertor oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.
XTAL2			VCC	O	**Output of the on-chip invertor oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.
AVCC				PWR	**Alternate Supply Voltage** AVCC is used to supply the on-chip PLL and the USB drivers
DVCC				PWR	**Digital Supply Voltage** DVCC output is used to power the internal logic – Capacitor has to be connected.
VCC				PWR	**Supply Voltage** VCC is used to power the internal voltage regulators and internal I/O's.
LI				PWR	**DC/DC Input** LI must be tied to VCC through an external coil (typically 4.7 µH) and provides the current for the pump charge of the DC/DC converter.
CVCC				PWR	**Card Supply Voltage** CVCC is the programmable voltage output for the Card interface. It must be connected to an external decoupling capacitor.
CVSS				GND	**DC/DC Ground** CVSS is used to sink high shunt currents from the external coil.
VSS				GND	**Digital Ground** VSS is used to supply the buffer ring and the digital core.
AVSS				GND	**Alternate Ground** AVSS is used to supply the on-chip PLL and the USB drivers.

SFR Mapping

The Special Function Registers (SFRs) of the AT83C5123 and AT83EB5123 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P1, P3, P4, P5
- Timer registers: TCON, TH0, TH1, TMOD, TL0, TL1,
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- BRG (Baud Rate Generator) registers: BRL , BDRCON
- Power, Clock and PLL control registers: PCON, CKRL, CKCON0 , CKCON1, CKSEL, PLLCON, PLLDIV
- Hardware Watchdog Timer registers: WDTRST, WDTPRG
- Interrupt system registers: IE0, IPL0, IPH0 , IE1 , IPL1 , IPH1
- LED register: LEDCON0
- USB registers: Uxxx (14 registers)
- Others: AUXR, AUXR1 ,
- Smart Card Interface: SCSR, SCCON/SCETU0, SCISR/SCETU1, SCIER/SCIIR, SCTBUF/SCRBUF, SCGT0/SCWT0, SCGT1/SCWT1, SCICR/SCWT2, SCCLK
- DC/DC converter: DCCKPS

Table 3 shows all SFRs with their address and their reset value.

Table 3. SFR Table

	Bit Addressable	Non-Bit Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000							ICON 0000 0000	FFh
F0h	B 0000 0000	LEDCON0 0000 0000							F7h
E8h	P5 XXXX X111								EFh
E0h	ACC 0000 0000		UBYCTX 0000 0000						E7h
D8h									DFh
D0h	PSW 0000 0000				UEPCONX 1000 0000	UEPRST 0000 0000			D7h
C8h							UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4 11XX XXXX	0 RESERVED XXXX XXXX 1 SCCLK XX10 1111	UEPIEN 0000 0000				USBADDR 0000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0 X000 000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0000 0000	DCCON 000XX000	BFh
B0h	P3 1111 1111	IEN1 XXXX X000	IPL1 XXXX X000	IPH1 XXXX X111	0 SCWT0(1) 0000 0000 1 SCGT0(1) 0000 0000	0 SCWT1(1) 0000 0000 1 SCGT1(1) 0000 0000	0 SCWT2(1) 0000 0000 1 SCICR(1) 0000 0000	IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000	0 SCTBUF(1) 0000 0000 1 SCRBUF 0000 000	SCSR XXXX XXXX	0 SCCON(1) 0000 0000 1 SCETU0 0000 0000	0 SCISR(1) 1000 0000 1 SCETU1(1) 0000 0000	0 SCIIR(1) 0000 0000 1 SCIER(1) 0000 0000	CKCON1 0000 0000	AFh
A0h		ISEL XXXX 1100	AUXR1 XX1X X0X0	PLLCON 0000 0000	PLLDIV 0000 0000		WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000					9Fh
90h	P1 1111 1111	PMOD0 0000 0000						CKRL XXXX 1111	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 0X0X 0000	CKCON0 X0X0 X000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL XXXX XXX0		PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Note: 1. Mapping is done using SCRS bit in SCSR register: if SCRS=0, upper cell, if SCRS=1, lower cell.

The Special Function Registers (SFRs) of the AT83C5123 and AT83EB5123 fall into the following categories:

Table 4. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word								
SP	81h	Stack Pointer LSB of SPX								
DPL	82h	Data Pointer Low byte LSB of DPTR								
DPH	83h	Data Pointer High byte MSB of DPTR								

Table 5. I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P1	90h	Port 1								
P3	B0h	Port 3								
P4	C0h	Port 4								
P5	E8h	Port 5								
PMOD0	91h	Port Mode Register 0	-	-	-	-	CPRESRES	-	-	-

Table 6. Timers SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TH0	8Ch	Timer/Counter 0 High byte								
TL0	8Ah	Timer/Counter 0 Low byte								
TH1	8Dh	Timer/Counter 1 High byte								
TL1	8Bh	Timer/Counter 1 Low byte								
TCON	88h	Timer/Counter 0 and 1 control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program	-	-	-	-	-	S2	S1	S0

Table 7. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								

Table 8. Baud Rate Generator SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
BRL	9Ah	Baud Rate Reload								
BDRCON	9Bh	Baud Rate Control	-	-	-	BRR	TBCK	RBCK	SPD	SRC

Table 9. Power, Clock and PLL SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
CKCON0	8Fh	Clock Control 0	-	WDX2	-	-	-	T1X2	T0X2	X2
CKCON1	AFh	Clock Control 1	-	-	-	-	-	-	-	-
CKSEL	85h	Clock Selection	-	-	-	-	-	-	-	CKS
CKRL	97h	Clock Reload Register	-	-	-	-	CKREL3	CKREL2	CKREL1	CKREL0
PLLCON	A3h	PLL Control Register	-	-	-	-	-	EXT48	PLLEN	PLOCK
PLLDIV	A4h	PLL Divider register	R3	R2	R1	R0	N3	N2	N1	N0

Table 10. SCIB SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCGT0	B4h	Smart Card Transmit Guard Time Register 0	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0
SCGT1	B5h	Smart Card Transmit Guard Time Register 1	-	-	-	-	-	-	-	GT8
SCWT0	B4h	Smart Card Character/ Block Wait Time Register 0	WT7	WT6	WT5	WT4	WT3	WT2	WT1	WT0
SCWT1	B5h	Smart Card Character/ Block Wait Time Register 1	WT15	WT14	WT13	WT12	WT11	WT10	WT9	WT8
SCWT2	B6h	Smart Card Character/ Block Wait Time Register 2	WT23	WT22	WT21	WT20	WT19	WT18	WT17	WT16
SCICR	B6h	Smart Card Interface Control Register	RESET	CARDDET	VCARD1	VCARD0	UART	WTEN	CREP	CONV
SCCON	ACh	Smart Card Interface Contacts Register	CLK	-	CARDC8	CARDC4	CARDIO	CARDCLK	CARDRST	CARDVCC
SCETU0	ACh	Smart Card ETU Register 0	ETU7	ETU6	ETU5	ETU4	ETU3	ETU2	ETU1	ETU0
SCISR	ADh	Smart Card UART Interface Status Register (Read Only)	SCTBE	CARDIN	ICARDOVF	VCARDOK	SCWTO	SCTI	SCRI	SCPE
SCETU1	ADh	Smart Card ETU Register 1	COMP	-	-	-	-	ETU10	ETU9	ETU8
SCIIR	AEh	Smart Card UART Interrupt Identification Register (Read Only)	SCTBI	-	ICARDERR	VCARDERR	SCWTI	SCTI	SCRI	SCPI
SCIER	AEh	Smart Card UART Interrupt Enable Register	ESCTBI	-	ICARDER	EVCARDER	ESCWTI	ESCTI	ESCRI	ESCPI
SCSR	ABh	Smart Card Selection Register	-	-	-	CREPSEL	ALTKPS1	ALTKPS0	SCCLK1	SCRS
SCTBUF	AAh	Smart Card Transmit Buffer Register (Write Only)	Can store a new byte to be transmitted on the I/O pin when SCTBE is set. Bit ordering on the I/O pin depends on the convention							
SCRBUF	AAh	Smart Card Receive Buffer Register (Read Only)	Provides the byte received from the I/O pin when SCRI is set. Bit ordering on the I/O pin depends on the covention.							
SCICLK	C1h	Smart Card Frequency Prescaler Register	-	-	SCICLK5	SCICLK4	SCICLK3	SCICLK2	SCICLK1	SCICLK0
DCCKPS	BFh	DC/DC Converter Reload Register	REG_MODE	ICC_CTRL	BOOST1	BOOST0	DCCKPS3	DCCKPS2	DCCKPS1	DCCKPS0

Note: 1. The SCIB's SFRs are classified in two address banks. The selection between bank0 and bank1 is done by bit SCRS (SCRS.0)

Table 11. Interrupt SFRs

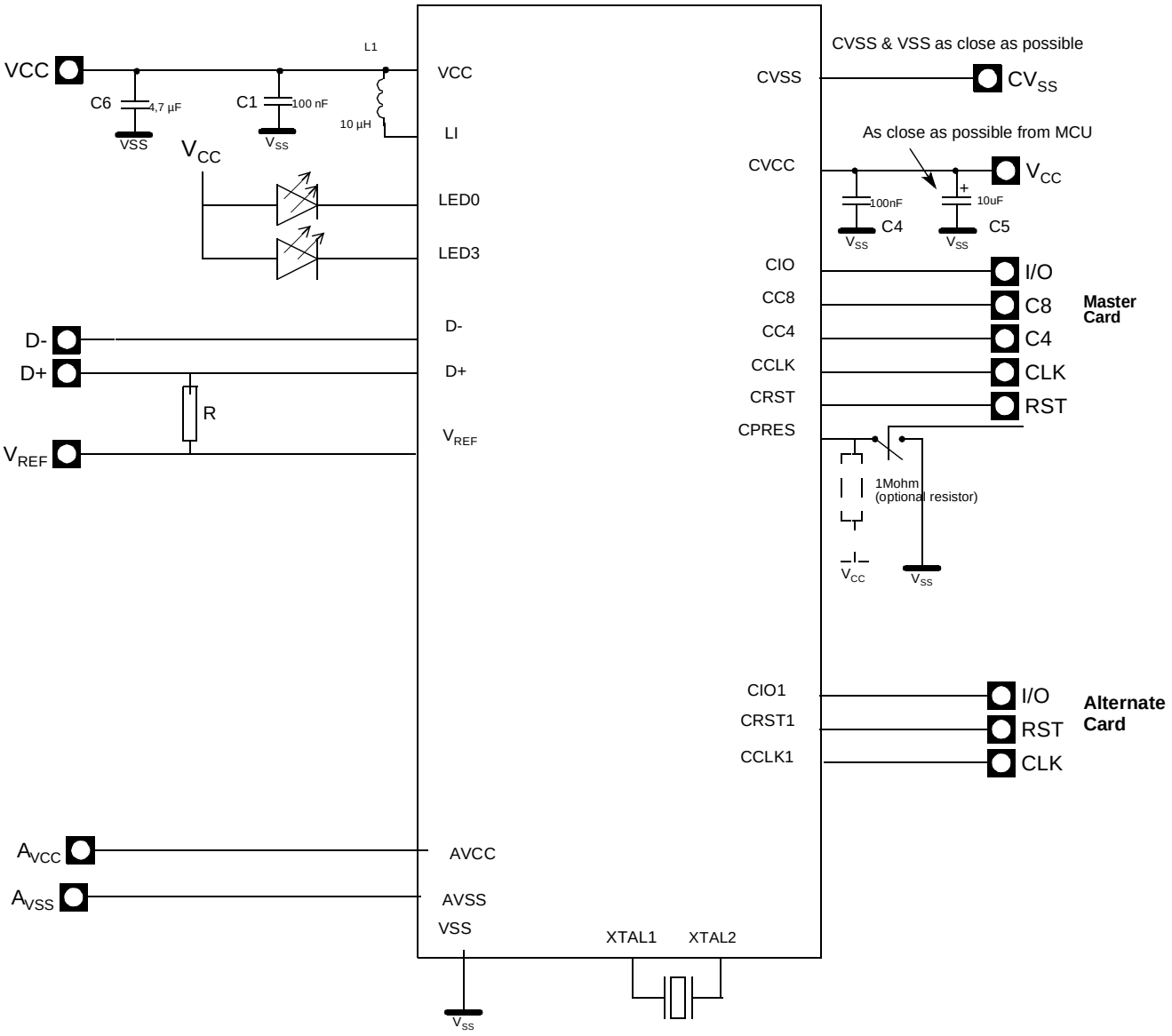
Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	-	-	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	EEMU	EUSB	EPCM	-	ESCI	ESPI	-	EKB
IPL0	B8h	Interrupt Priority Control Low 0	-	-	-	PSL	PT1L	PX1L	PT0L	PX0L
IPH0	B7h	Interrupt Priority Control High 0	-	-	-	PSH	PT1H	PX1H	PT0H	PX0H
IPL1	B2h	Interrupt Priority Control Low 1	PEMUL	PUSBL	-	-	PSCIL	PSPIL	-	PKBL
IPH1	B3h	Interrupt Priority Control High 1	PEMUH	PUSBH	-	-	PSCIH	PSPIH	-	PKBH
ISEL	A1h	Interrupt Enable Register	CPLEV	OEIT	PRESIT	RXIT	OELEV	OEEN	PRESEN	RXEN

Table 12. USB SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	DETACH	UPRSM	RMWUPE	CONFG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
USBINT	BDh	USB Global Interrupt	-	-	WUPCPU	EORINT	SOFINT	-	-	SPINT
USBIEN	BEh	USB Global Interrupt Enable	-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT
UEPNUM	C7h	USB Endpoint Number	-	-	-	-	EPNUM3	EPNUM2	EPNUM1	EPNUM0
UEPCONX	D4h	USB Endpoint X Control	EPEN	NAKIEN	NAKOUT	NAKIN	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	RXOUTB1	STALLRQ	TXRDY	STL/CRC	RXSETUP	RXOUTB0	TXCMP
UEPRST	D5h	USB Endpoint Reset	-	EP6RST	EP5RST	EP4RST	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt	-	EP6INT	EP5INT	EP4INT	EP3INT	EP2INT	EP1INT	EP0INT
UEPIEN	C2h	USB Endpoint Interrupt Enable	-	EP6INTE	EP5INTE	EP4INTE	EP3INTE	EP2INTE	EP1INTE	EP0INTE
UEPDATX	CFh	USB Endpoint X FIFO Data	FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0
UBYCTX	E2h	USB Byte Counter Low (EP X)	-	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0
UFNUML	BAh	USB Frame Number Low	FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0
UFNUMH	BBh	USB Frame Number High	-	-	CRCOK	CRCERR	-	FNUM10	FNUM9	FNUM8

Typical Application

Figure 3. Typical Application Diagram



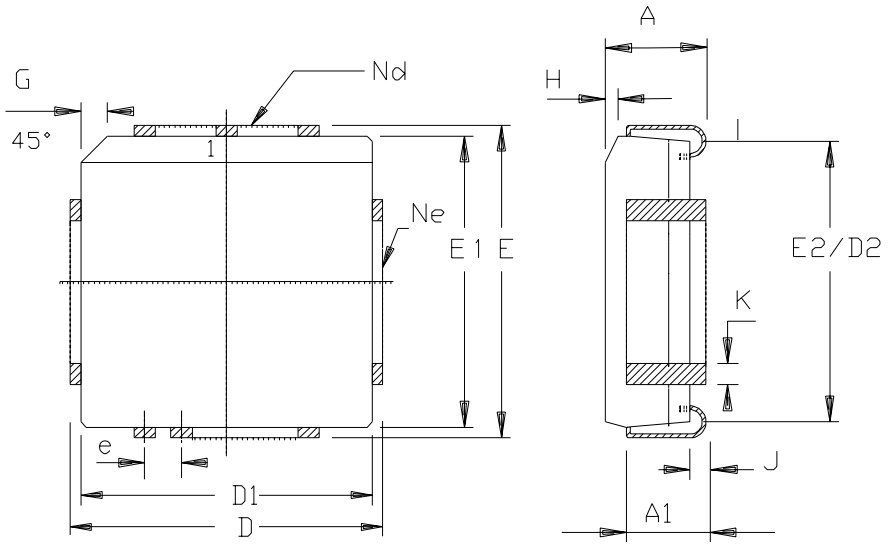
Ordering Information

Table 13. Possible Order Entries

Part Number	Memory Size (bytes)	Supply Voltage (V)	Temperature Range	Max Frequency (MHz)	Package	Packing
AT83C5123xxx-RATIM	16K ROM	3.6 - 5.5	Industrial	32	VQFP32	Tray
AT83C5123xxx-RARIM	16K ROM	3.6 - 5.5	Industrial	32	VQFP32	Reel
AT83C5123xxx-SISIM	16K ROM	3.6 - 5.5	Industrial	32	PLCC28	Stick
AT83C5123xxx-SIRIM	16K ROM	3.6 - 5.5	Industrial	32	PLCC28	Reel
AT83EB5123xxx-RATIM	16K ROM + 256 EEPROM	3.6 - 5.5	Industrial	32	VQFP32	Tray
AT83EB5123xxx-RARIM	16K ROM + 256 EEPROM	3.6 - 5.5	Industrial	32	VQFP32	Reel
AT83EB5123xxx-SISIM	16K ROM + 256 EEPROM	3.6 - 5.5	Industrial	32	PLCC28	Stick
AT83EB5123xxx-SIRIM	16K ROM + 256 EEPROM	3.6 - 5.5	Industrial	32	PLCC28	Reel

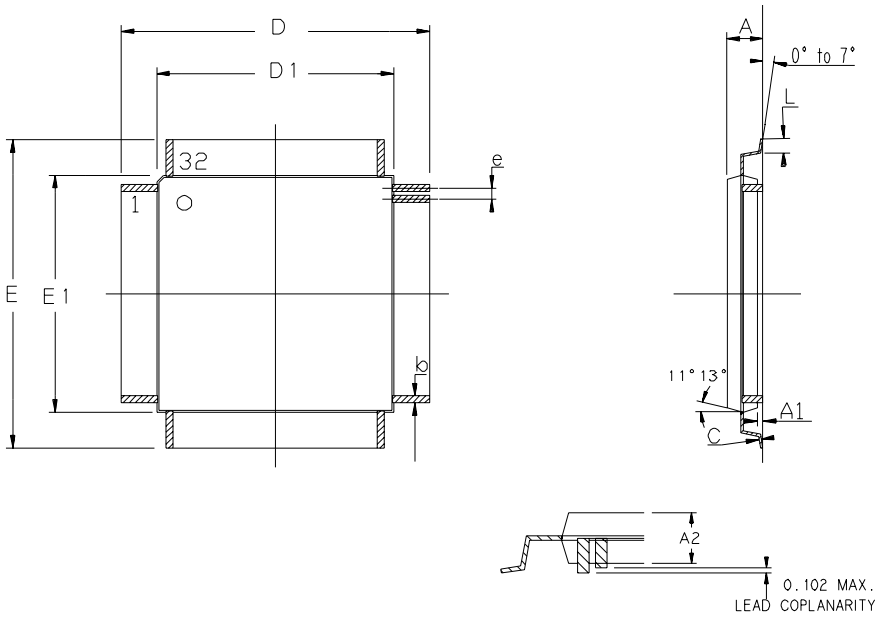
Package Drawings

PLCC28



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	12.32	12.57	.485	.495
D1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
E	12.32	12.57	.485	.495
E1	11.43	11.58	.450	.456
E2	9.91	10.92	.390	.430
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	7		7	
Ne	7		7	
PKG STD	00			

VQFP32



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
C	0.09	0.20	.004	.008
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
b	0.30	0.45	.012	.018

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