Features

- **Programmable Audio Output for Interfacing with Common Audio DAC**
  - **PCM Format Compatible**
  - **I^2S Format Compatible**
- **8-bit MCU C51 Core-based (F_{MAX} = 20 MHz)**
- **2304 bytes of Internal RAM**
- **64K Bytes of Code Memory**
  - **Flash: AT89C5132, ROM: AT83C5132(1)**
- **4K Bytes of Boot Flash Memory (AT89C5132)**
  - **ISP: Download from USB or UART to Any External Memory Cards**
- **USB Rev 1.1 Controller**
  - **"Full Speed" Data Transmission**
- **Built-in PLL for USB Clock**
- **MultiMedia Card® Interface Compatibility**
- **Atmel DataFlash® SPI Interface Compatibility**
- **IDE/ATAPI Interface**
- **2 Channels 10-bit ADC, 8 kHz (8-True Bit)**
  - **Battery Voltage Monitoring**
  - **Voice Recording Controlled by Software**
- **Up to 44 bits for General-purpose I/Os for**
  - **4-bit Interrupt Keyboard Port for a 4 x n Matrix**
  - **SmartMedia® Software Interface**
- **Standard Two 16-bit Timers/Counters**
- **Hardware Watchdog Timer**
- **Standard Full Duplex UART with Baud Rate Generator**
- **SPI Master and Slave Modes Controller**
- **Power Management**
  - **Power-on Reset**
  - **Software Programmable MCU Clock**
  - **Idle Mode, Power-down Mode**
- **Operating Conditions**
  - **3V, ±10%, 25 mA Typical Operating at 25°C**
  - **Temperature Range: -40°C to +85°C**
- **Packages**
  - **TQFP80, TQFP64, BGA81(1)**
  - **Dice**

Note: 1. Contact Atmel for availability.

Description

The AT8xC5132 devices are mass storage devices controlling data exchange between various Flash modules, HDD and CD-ROM.

The AT89C5132 includes 64K Bytes of Flash memory and allows In-System Programming through an embedded 4K Bytes of Boot Flash memory.

The AT83C5132 includes 64K Bytes of ROM memory.

The AT8xC5132 includes 2304 bytes of RAM memory.

The AT8xC5132 provide all the necessary features for man-machine interface like timers, keyboard port, serial or parallel interface (USB, SPI, IDE), ADC input, I^2S output, and all external memory interface (NAND or NOR Flash, SmartMedia, MultiMedia, and DataFlash Cards).

Typical Applications

- Flash Recorder/Writer
- PDAs, Camera, Mobile Phone
- PC Add-on

USB Microcontroller with 64K Byetes ROM or Flash

AT83C5132
AT89C5132

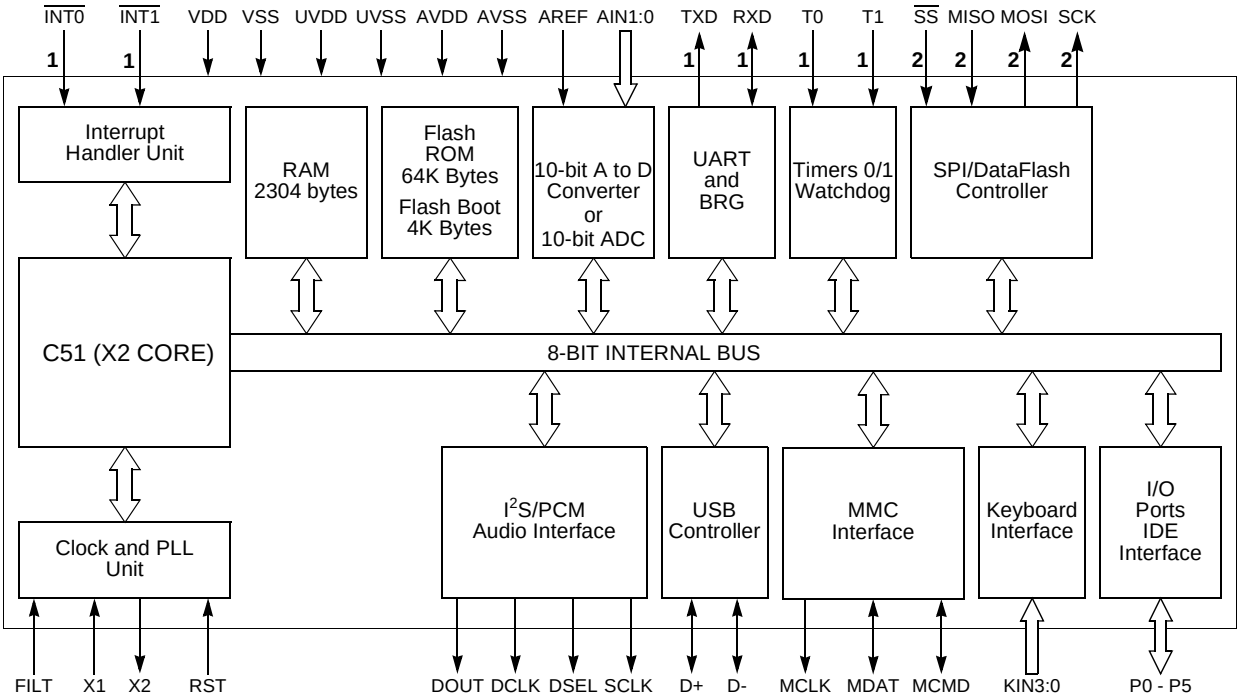
Preliminary

Summary

Rev. 4176A–8051–08/02

Block Diagram

Figure 1. AT8xC5132 Block Diagram



Notes: 1. Alternate function of Port 3
2. Alternate function of Port 4

Pin Configurations

Figure 2. AT8xC5132, 80-pin TQFP Package

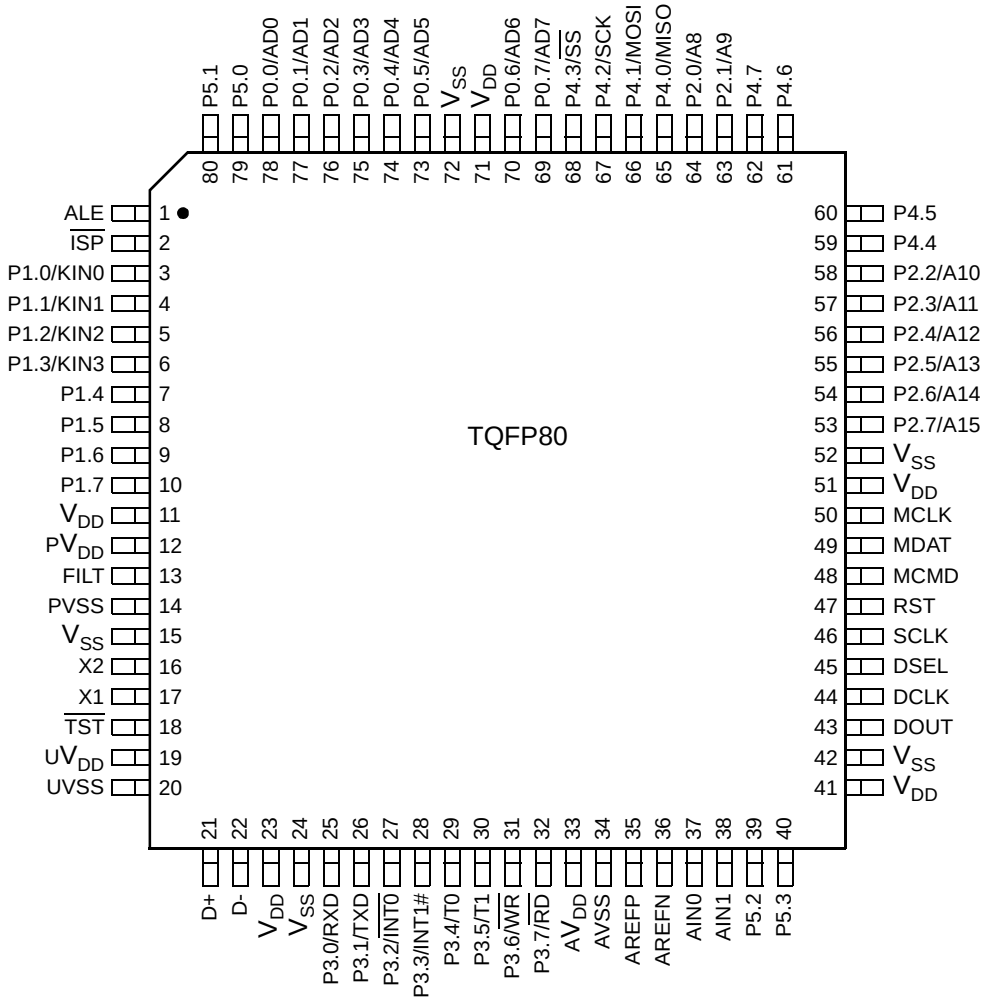


Figure 3. AT8xC5132, 64-pin TQFP

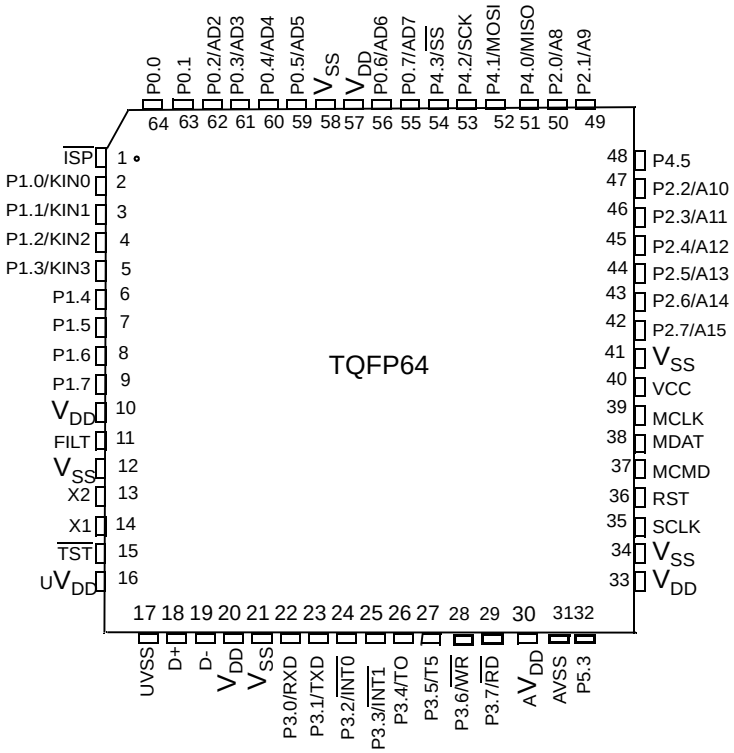
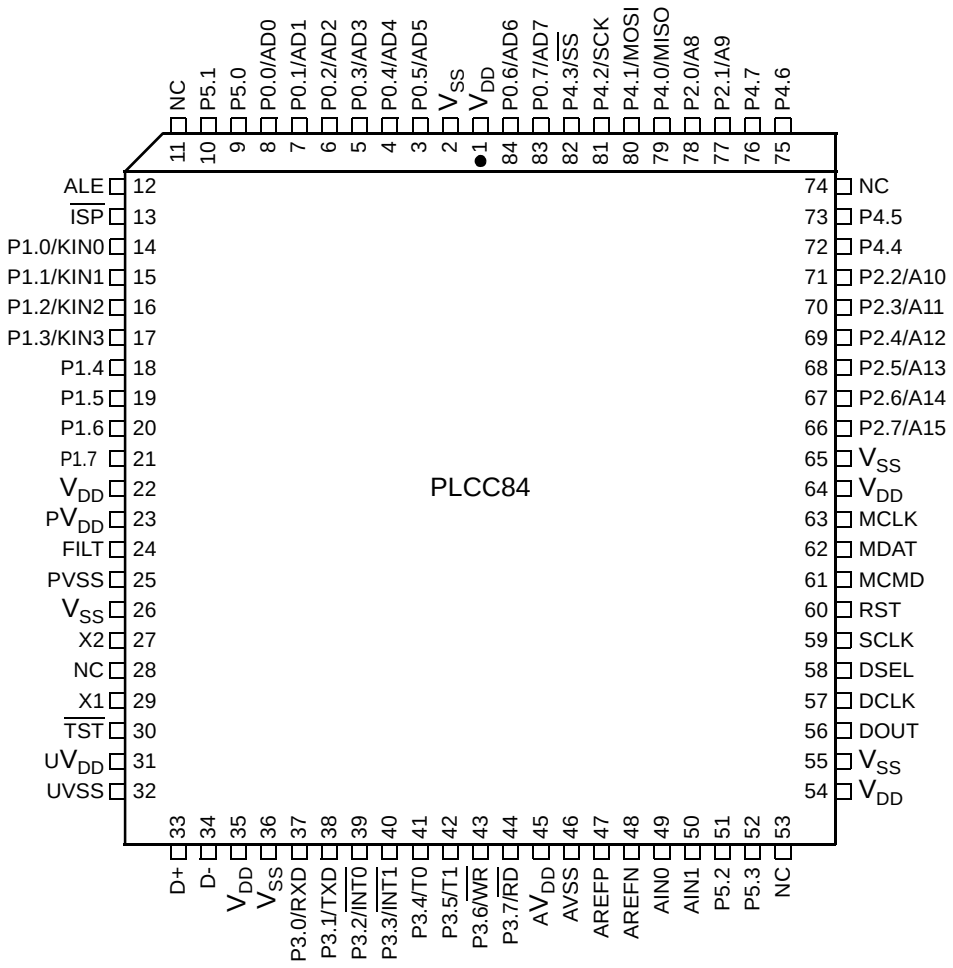


Figure 4. AT8xC5132, 84-pin PLCC Package[1]



Note: 1. For development board only.

Pin Description

All AT8xC5132 signals are detailed by functionality in Table 1 through Table 14.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0 SCL SDA
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.7:0	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	RXD TXD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4.7:0	I/O	**Port 4** P4 is an 8-bit bidirectional I/O port with internal pull-ups.	MISO MOSI SCK SS#
P5.3:0	I/O	**Port 5** P5 is a 4-bit bidirectional I/O port with internal pull-ups.	-

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL Low Pass Filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
INT0#	I	**Timer 0 Gate Input** INT0 serves as external run control for Timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** INT0# input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on INT0#. If bit IT0 is cleared, bit IE0 is set by a low level on INT0#.	P3.2
INT1#	I	**Timer 1 Gate Input** INT1 serves as external run control for Timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** INT1# input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on INT1#. If bit IT1 is cleared, bit IE1 is set by a low level on INT1#.	P3.3
T0	I	**Timer 0 External Clock Input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 kΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6. MutiMedia Card Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 7. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 8. Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P4.0
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P4.1
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P4.2
SS#	I	**SPI Slave Select Line** When in controlled slave mode, $\overline{SS}$ enables the slave mode.	P4.3

Table 9. Specific Controller

Signal Name	Type	Description	Alternate Function
SCL	I/O	Reserved Do not set this bit.	P1.6
SDA	I/O	Reserved Do not set this bit.	P1.7

Table 10. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AV_{SS}.	-

Table 11. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 12. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
$\overline{ISP}$	I/O	**ISP Enable Input** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
$\overline{RD}$	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
$\overline{WR}$	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6

Table 13. System Signal Description

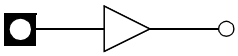
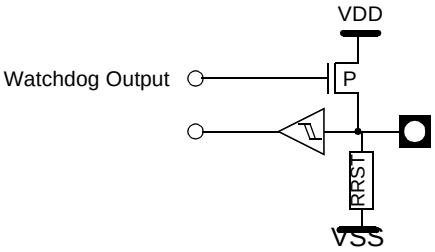
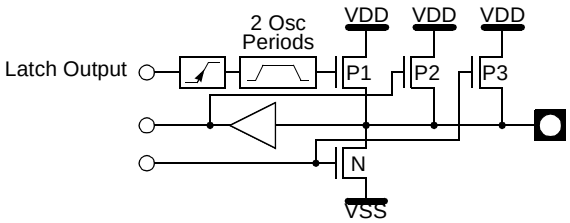
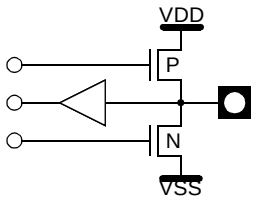
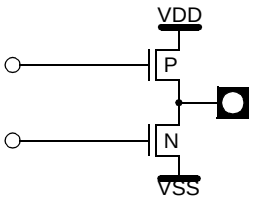
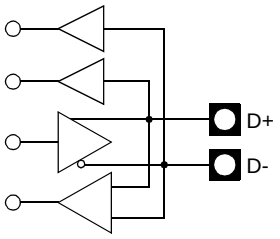
Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-down mode returns the chip to normal operation.	-
$\overline{TST}$	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 14. Power Signal Description

Signal Name	Type	Description	Alternate Function
VDD	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
AVDD	PWR	**Analog Supply Voltage** Connect this pin to +3V supply voltage.	-
AVSS	GND	**Analog Ground** Connect this pin to ground.	-
PVDD	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UVDD	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-
UVSS	GND	**USB Ground** Connect this pin to ground.	-

Internal Pin Structure

Table 15. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	$\overline{TST}$
	Input/Output	RST
	Input/Output	P1 P2[3] P3 P4 P53:0
	Input/Output	P0 MCMD MDAT $\overline{ISP}$
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes: 1. For information on resistors value, input/output levels, and drive capability, refer to the AT8xC5132 full Datasheet.
2. In Port 2, P_1 transistor is continuously driven when outputing a high level bit address (A15:8).

Application Information

Figure 5. AT8xC5132 Typical Application with On-board Atmel DataFlash

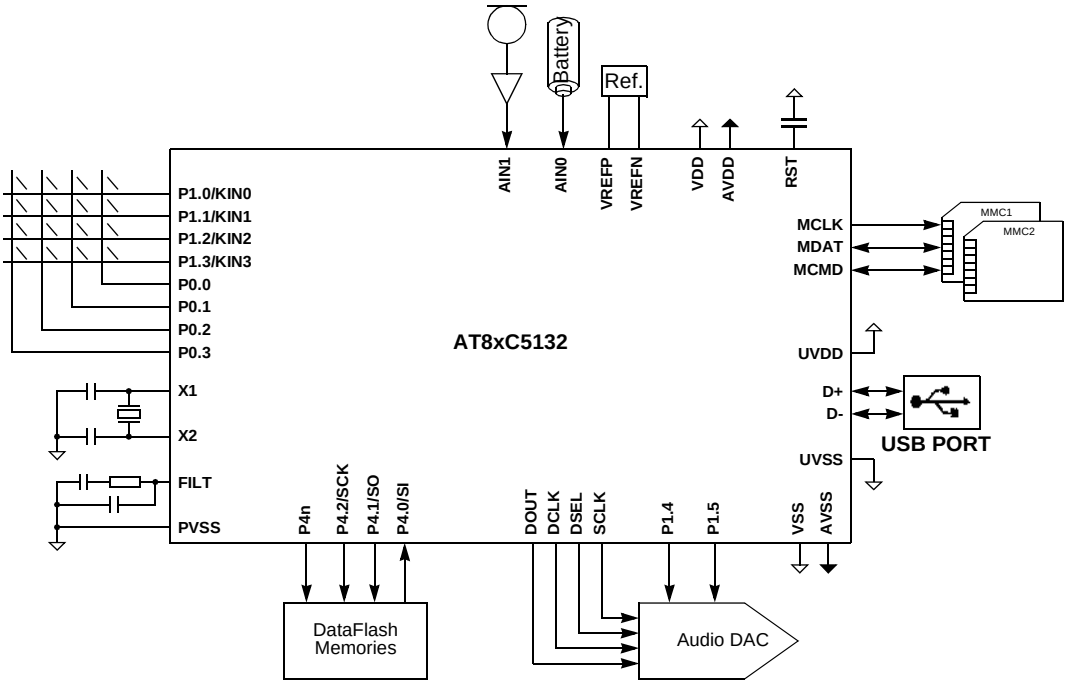


Figure 6. AT8xC5132 Typical Application with On-board Atmel DataFlash and LCD

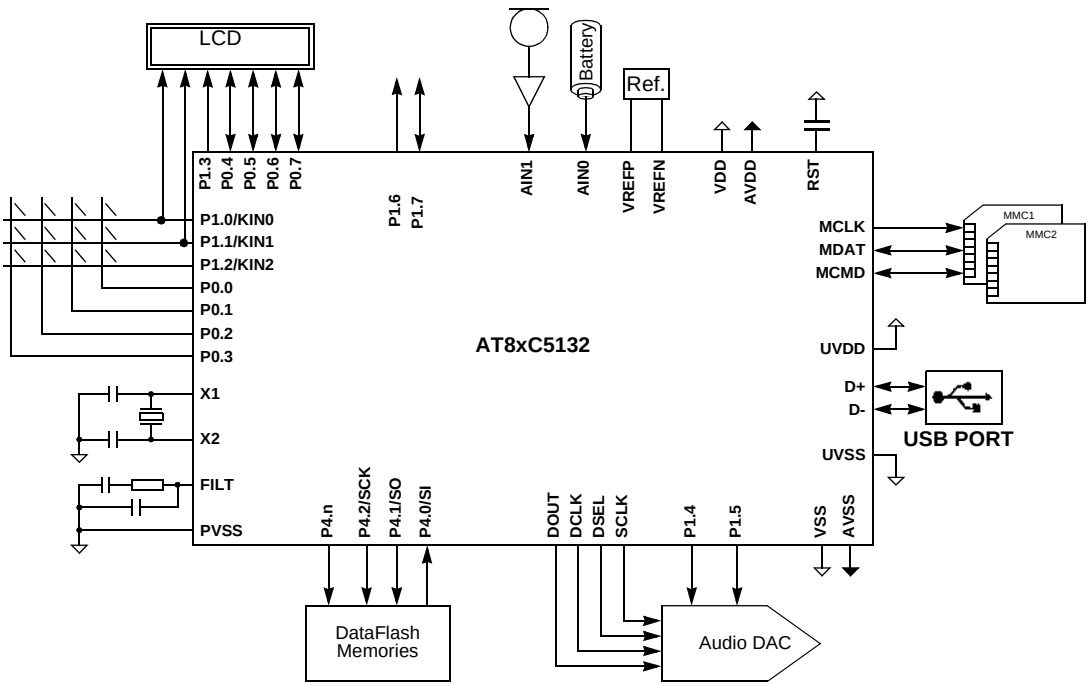


Figure 7. AT8xC5132 Typical Application with On-board SSFDC Flash

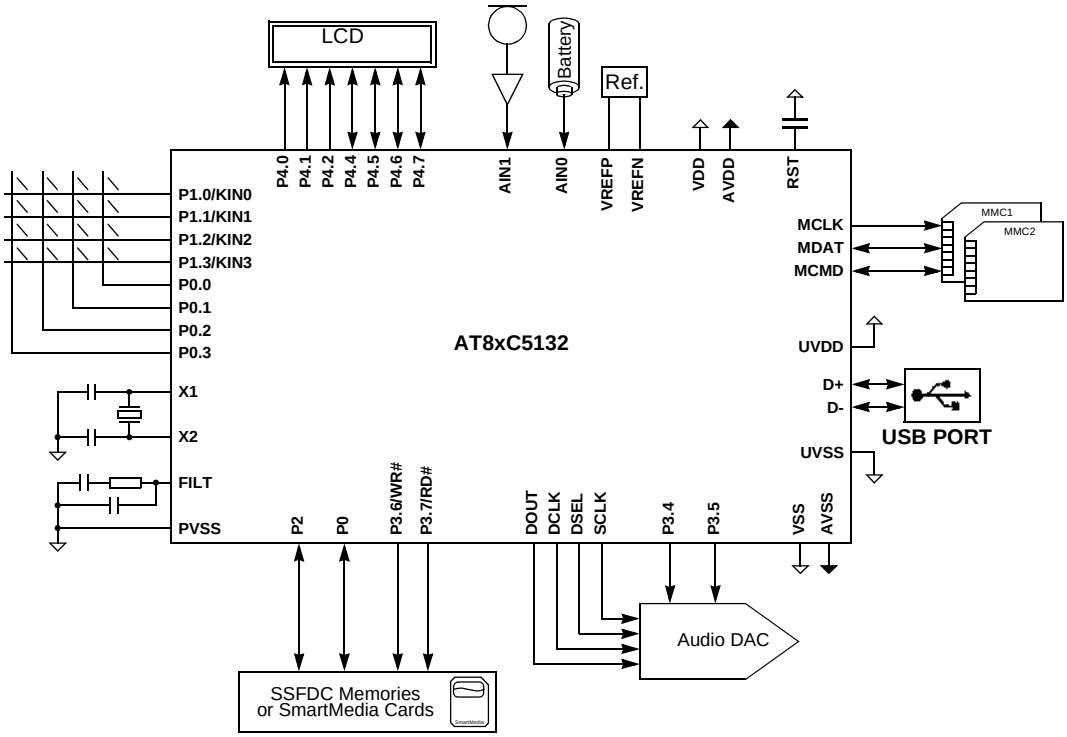
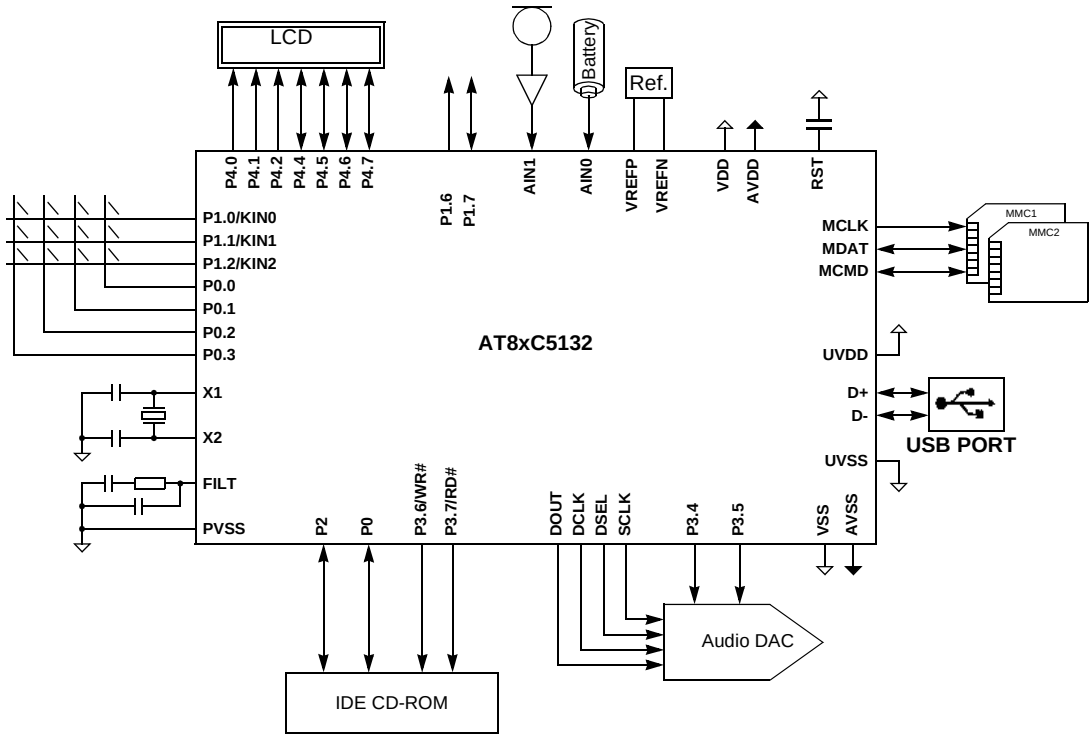


Figure 8. AT8xC5132 Typical Application with IDE CD-ROM Drive



Address Spaces

The AT8xC5132 derivatives implement four different address spaces:

- Program/Code Memory
- Boot Memory
- Data Memory
- Special Function Registers (SFRs)

Code Memory

The AT89C5132 and AT83C5132 implement 64K Bytes of on-chip program/code memory. The AT83C5132 product provides the internal program/code memory in ROM technology while the AT89C5132 product provides it in Flash technology.

The Flash memory increases ROM functionality by enabling in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing Flash cells is generated on-chip using the standard V_{DD} voltage. Thus, the AT89C5132 can be programmed using only one voltage and allows in application software programming commonly known as IAP. Hardware programming mode is also available using specific programming tools.

Boot Memory

The AT89C5132 implements 4K Bytes of on-chip boot memory provided in Flash technology. This boot memory is delivered programmed with a standard bootloader software allowing in system programming commonly known as ISP. It also contains some Application Programming Interfaces routines commonly known as API allowing user to develop his own bootloader.

Data Memory

The AT8xC5132 derivatives implement 2304 bytes of on-chip data RAM. This memory is divided in two separate areas:

- 256 bytes of on-chip RAM memory (standard C51 memory).
- 2048 bytes of on-chip expanded RAM memory (ERAM accessible via MOVX instructions).

Special Function Registers

The Special Function Registers (SFRs) of the AT8xC5132 derivatives fall into the categories detailed in Table 16 through Table 31. The relative addresses of these SFRs are provided together with their reset values in Table 32. In this table, the bit-addressable registers are identified by Note 1.

Table 16. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
DPL	82h	Data Pointer Low byte								
DPH	83h	Data Pointer High byte								

Table 17. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	-	-	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	-	EXT16	M0	DPHDIS	XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	-	-	ENBOOT	-	GF3	0	-	DPS
NVERS	FBh	Version Number	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0

Table 18. PLL and System Clock SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CKCON	8Fh	Clock Control	-	-	-	-	-	-	-	X2
PLLCON	E9h	PLL Control	R1	R0	-	-	PLLRES	-	PLLEN	PLOCK
PLLNDIV	EEh	PLL N Divider	-	N6	N5	N4	N3	N2	N1	N0
PLLRDIV	EFh	PLL R Divider	R9	R8	R7	R6	R5	R4	R3	R2

Table 19. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EAUD	-	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	-	EUSB	-	EKB	EADC	ESPI	EI2C	EMMC
IPH0	B7h	Interrupt Priority Control High 0	-	IPHAUD	-	IPHS	IPHT1	IPHX1	IPHT0	IPHX0
IPL0	B8h	Interrupt Priority Control Low 0	-	IPLAUD	-	IPLS	IPLT1	IPLX1	IPLT0	IPLX0
IPH1	B3h	Interrupt Priority Control High 1	-	IPHUSB	-	IPHKB	IPHADC	IPHSPI	IPHI2C	IPHMMC
IPL1	B2h	Interrupt Priority Control Low 1	-	IPLUSB	-	IPLKB	IPLADC	IPLSPI	IPLI2C	IPLMMC

Table 20. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P5	D8h	4-bit Port 5	-	-	-	-				

Table 21. Flash Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
FCON	D1h	Flash Control	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY

Table 22. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
TL0	8Ah	Timer/Counter 0 Low Byte								
TH0	8Ch	Timer/Counter 0 High Byte								
TL1	8Bh	Timer/Counter 1 Low Byte								

Table 22. Timer SFRs (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TH1	8Dh	Timer/Counter 1 High Byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program	-	-	-	-	-	WTO2	WTO1	WTO0

Table 23. Audio Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
AUDCON0	9Ah	Audio Control 0	JUST4	JUST3	JUST2	JUST1	JUST0	POL	DSIZ	HLR
AUDCON1	9Bh	Audio Control 1	SRC	DRQEN	MSREQ	MUDRN	-	DUP1	DUP0	AUDEN
AUDSTA	9Ch	Audio Status	SREQ	UDRN	AUBUSY	-	-	-	-	-
AUDDAT	9Dh	Audio Data	AUD7	AUD6	AUD5	AUD4	AUD3	AUD2	AUD1	AUD0
AUDCLK	ECh	Audio Clock Divider	-	-	-	AUCD4	AUCD3	AUCD2	AUCD1	AUCD0

Table 24. USB Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	-	UPRSM	RMWUPE	CONFG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
USBINT	BDh	USB Global Interrupt	-	-	WUPCPU	EORINT	SOFINT	-	-	SPINT
USBIEN	BEh	USB Global Interrupt Enable	-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT
UEPNUM	C7h	USB Endpoint Number	-	-	-	-	-	-	EPNUM1	EPNUM0
UEPCONX	D4h	USB Endpoint X Control	EPEN	-	-	-	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	-	STALLRQ	TXRDY	STLCRC	RXSETUP	RXOUT	TXCMP
UEPRST	D5h	USB Endpoint Reset	-	-	-	-	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt	-	-	-	-	EP3INT	EP2INT	EP1INT	EP0INT
UEPIEN	C2h	USB Endpoint Interrupt Enable	-	-	-	-	EP3INTE	EP2INTE	EP1INTE	EP0INTE
UEPDATX	CFh	USB Endpoint X Fifo Data	FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0
UBYCTX	E2h	USB Endpoint X Byte Counter	-	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0
UFNUML	BAh	USB Frame Number Low	FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0

Table 24. USB Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
UFNUMH	BBh	USB Frame Number High	-	-	CRCOK	CRCERR	-	FNUM10	FNUM9	FNUM8
USBCLK	EAh	USB Clock Divider	-	-	-	-	-	-	USBCD1	USBCD0

Table 25. MMC Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MMCON0	E4h	MMC Control 0	DRPTR	DTPTR	CRPTR	CTPTR	MBLOCK	DFMT	RFMT	CRCDIS
MMCON1	E5h	MMC Control 1	BLEN3	BLEN2	BLEN1	BLEN0	DATDIR	DATEN	RESPEN	CMDEN
MMCON2	E6h	MMC Control 2	MMCEN	DCR	CCR	-	-	DATD1	DATD0	FLOWC
MMSTA	DEh	MMC Control and Status	-	-	CBUSY	CRC16S	DATFS	CRC7S	RESPFS	CFLCK
MMINT	E7h	MMC Interrupt	MCBI	EORI	EOCI	EOFI	F2FI	F1FI	F2EI	F1EI
MMMSK	DFh	MMC Interrupt Mask	MCBM	EORM	EOCM	EOFM	F2FM	F1FM	F2EM	F1EM
MMCMD	DDh	MMC Command	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
MMDAT	DCh	MMC Data	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
MMCLK	EDh	MMC Clock Divider	MMCD7	MMCD6	MMCD5	MMCD4	MMCD3	MMCD2	MMCD1	MMCD0

Table 26. IDE Interface SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DAT16H	F9h	High Order Data Byte	D15	D14	D13	D12	D11	D10	D9	D8

Table 27. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	92h	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC
BRL	91h	Baud Rate Reload								

Table 28. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	-	MODF	-	-	-	-
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 29. Specific Controller

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Reserved	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSSTA	94h	Reserved	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Reserved	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
SSADR	96h	Reserved	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 30. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBCON	A3h	Keyboard Control	KINL3	KINL2	KINL1	KINL0	KINM3	KINM2	KINM1	KINM0
KBSTA	A4h	Keyboard Status	KPDE	-	-	-	KINF3	KINF2	KINF1	KINF0

Table 31. A/D Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ADCON	F3h	ADC Control	-	ADIDL	ADEN	ADEOC	ADSST	-	-	ADCS
ADCLK	F2h	ADC Clock Divider	-	-	-	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
ADDL	F4h	ADC Data Low Byte	-	-	-	-	-	-	ADAT1	ADAT0
ADDH	F5h	ADC Data High Byte	ADAT9	ADAT8	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2

Table 32. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	DAT16H XXXX XXXX		NVERS(2) 1000 0010					FFh
F0h	B(1) 0000 0000		ADCLK 0000 0000	ADCON 0000 0000	ADDL 0000 0000	ADDH 0000 0000			F7h
E8h		PLLCON 0000 1000	USBCLK 0000 0000		AUDCLK 0000 0000	MMCLK 0000 0000	PLLNDIV 0000 0000	PLLRDIV 0000 0000	EFh
E0h	ACC(1) 0000 0000		UBYCTLX 0000 0000		MMCON0 0000 0000	MMCON1 0000 0000	MMCON2 0000 0000	MMINT 0000 0011	E7h
D8h	P5(1) XXXX 1111				MMDAT 1111 1111	MMCMD 1111 1111	MMSTA 0000 0000	MMMSK 1111 1111	DFh
D0h	PSW1 0000 0000	FCON(3) 1111 0000(4)			UEPCONX 0000 0000	UEPRST 0000 0000			D7h
C8h							UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4(1) 1111 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0(1) X000 0000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0001 0000		BFh
B0h	P3(1) 1111 1111	IEN1 0000 0000	IPL1 0000 0000	IPH1 0000 0000				IPH0 X000 0000	B7h
A8h	IEN0(1) 0000 0000	SADDR 0000 0000							AFh
A0h	P2(1) 1111 1111		AUXR1 XXXX 00X0	KBCON 0000 1111	KBSTA 0000 0000		WDTRST XXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	AUDCON0 0000 1000	AUDCON1 1011 0010	AUDSTA 1100 0000	AUDDAT 1111 1111			9Fh
90h	P1(1) 1111 1111	BRL 0000 0000	BDRCON XXX0 0000	SSCON 0000 0000	SSSTA 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON(1) 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X000 1101	CKCON 0000 000X(5)	8Fh
80h	P0(1) 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON XXXX 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. SFR registers with least significant nibble address equal to 0 or 8 are bit-addressable.
2. NVERS reset value depends on the silicon version.
3. FCON register is only available in AT89C5132 product.
4. FCON reset value is 00h in case of reset with hardware condition.
5. CKCON reset value depends on the X2B bit (programmed or unprogrammed) in the Hardware Byte.

In-System and In-Application Programming

As described in the section “Program/Code Memory” of the AT8xC5132 datasheet, The AT89C5132 implements a 4K Bytes Flash boot memory. This boot memory is delivered programmed with a standard bootloader software allowing In-System Programming (ISP). It also contains some Application Programming Interface routines named API routines allowing In Application Programming (IAP) by using user’s own bootloader.

In-System Programming

The ISP boot process is divided in two different processes: the hardware and software boot process detailed in the following sections.

Hardware Boot Process

As detailed in Figure 9, there are two hardware conditions that allow the user to execute the bootloader: the hardware and the programmed conditions.

Hardware Condition

The hardware condition is based on the $\overline{\text{ISP}}$ pin. When driving this pin to low level, the chip reset forces the execution of the bootloader software.

The hardware condition takes precedence on the programmed condition and always allows in-system recovery when the user’s memory has been corrupted.

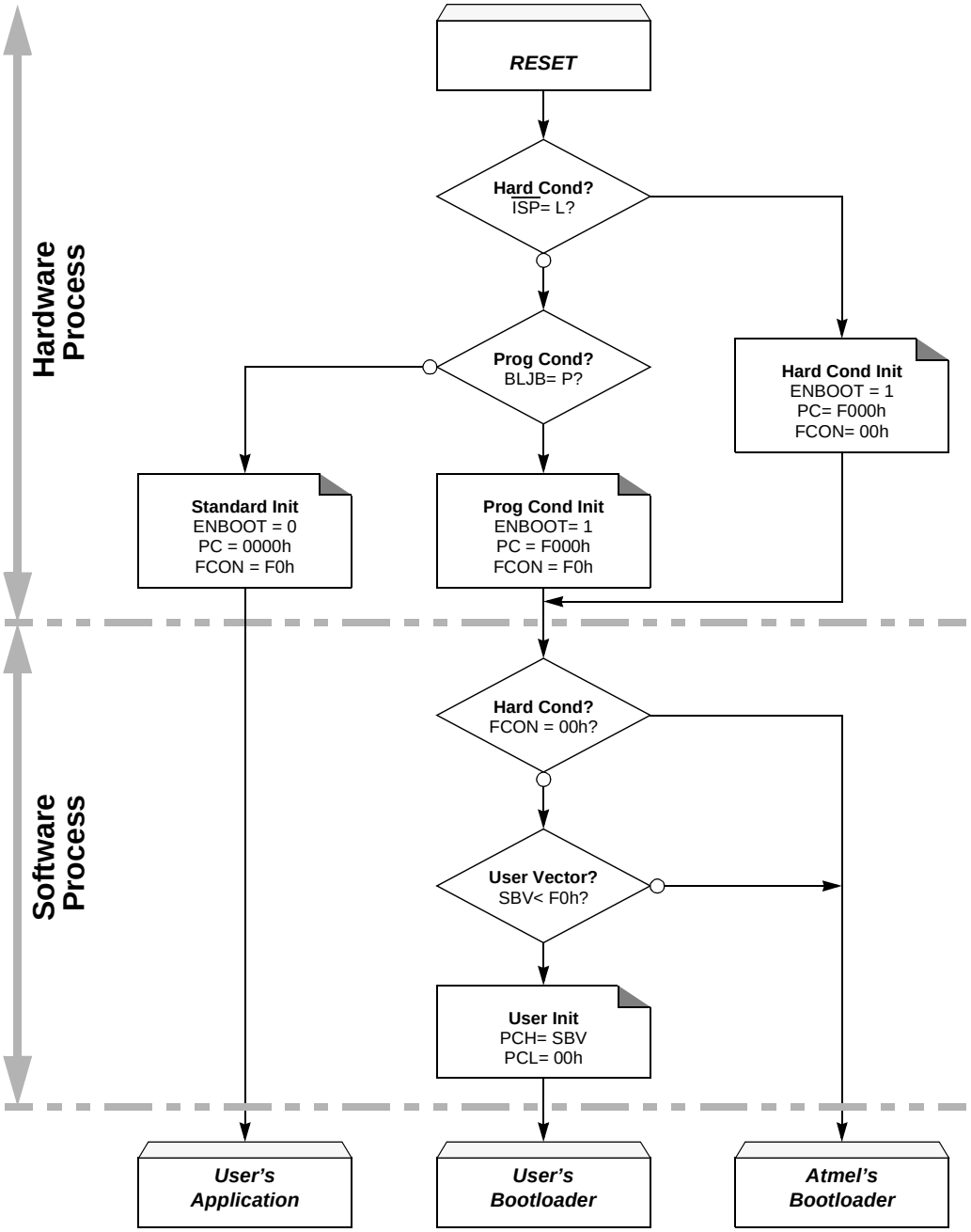
Programmed Condition

The programmed condition is based on the Bootloader Jump Bit (BLJB) in the hardware security bytes (HSB). When this bit is programmed (by hardware or software programming mode), the chip reset forces the execution of the bootloader software.

Software Boot Process

Whatever the physical medium may be, the bootloader software always starts execution by testing FCON to know if execution comes from hardware or programmed condition. If it is from hardware condition, Atmel’s bootloader is executed. If it is from programmed condition, the Software Boot Vector (SBV) is used to build a 16-bit address, SBV content being the MSB and the LSB at 00h. If this address is valid (< F000h), a jump occurs at this address to execute the user’s bootloader. Otherwise, jump is performed to Atmel’s bootloader. This implies that the user’s bootloader does not execute any code mapped from F000h to FFFFh.

Figure 9. Boot Process Algorithm



In-Application Programming

The IAP is based on several Application Program Interface routines (APIs) that may be called by the user's bootloader to allow programming of the Flash memory.

Peripherals

The AT8xC5132 peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC5132 complete datasheet.

Clock Generator System

The AT8xC5132 internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

Ports

The AT8xC5132 implement five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/Os, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/Os and alternate functions.

Timers/Counters

The AT8xC5132 implement the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

Watchdog Timer

The AT8xC5132 implement a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

Audio Output Interface

The AT8xC5132 implements an audio output interface allowing the decoded audio bitstream to be output in various formats. They are compatible with right and left justification PCM and I^2S formats and the on-chip PLL allows connection of almost all commercial audio DAC families available on the market.

Universal Serial Bus Interface

The AT8xC5132 implements a full-speed Universal Serial Bus Interface. The USB interface can be used for the following purposes:

- Download of files by supporting the USB mass storage class.
- In-System Programming by supporting the USB firmware upgrade class.

MultiMedia Card Interface

The AT8xC5132 implements a MultiMedia Card (MMC) interface compliant to the V2.2 specification in MultiMedia Card mode. The MMC allows storage of files in removable Flash memory cards that can be easily plugged or removed from the application. It can also be used for In-System Programming.

IDE/ATAPI Interface

The AT8xC5132 provide an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash™ cards, Hard Disk Drive, etc. It consists of a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In-System Programming using CD-ROM.

Serial I/O Interface

The AT8xC5132 implement a serial port with its own baud rate generator providing one single synchronous communication mode and three full-duplex UART communication modes. It is provided for the following purposes:

- In-System Programming
- Remote control of the AT8xC5132 by a host

Serial Peripheral Interface

The AT8xC5132 implement a Serial Peripheral Interface (SPI) supporting master and slave modes. It is provided for the following purposes:

- Interfacing DataFlash memory and DataFlash cards
- Remote control of the AT8xC5132 by a host
- In-System Programming

A/D Controller

The AT8xC5132 implement a 2-channel 10-bit (8 true bits) analog to digital converter (ADC). It is provided for the following purposes:

- Battery monitoring.
- Voice recording.
- Corded remote control.

Keyboard Interface

The AT8xC5132 implements a keyboard interface allowing connection of 4 x n matrix keyboard. It is based on 4 inputs with programmable interrupt capability on both high or low level. These inputs are available as alternate function of P1.3:0 and allow exit from idle and power-down modes.

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