Features

General

- High-performance, Low-power secureAVR™ RISC Architecture
  - 133 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low-power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V
- Operating Ranges: from 2.7V to 5.5V
- Compliant With EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules and Industry-standard Packages

Memory

- 48K Bytes of ROM Program Memory
- 2K Bytes of EEPROM, Including 64-byte OTP Area and 192-byte Bit-addressable Area
  - 1 to 64-byte Program/Erase
  - 2 ms Program, 2 ms Erase
  - Typically 1,000,000 Write/Erase Cycles
  - 10 Years Data Retention
- 1K Bytes of RAM

Peripherals

- ISO 7816 Controller
  - Up to 625 kbs at 5 MHz
  - Compliant with T = 0 and T = 1 Protocols
- One I/O Port
- Programmable Internal Oscillator (Up to 16 MHz on ROM)
- One 16-bit Timer
- Random Number Generator (RNG)
- 2-level, 5-vector Interrupt Controller
- Checksum Accelerator
- CRC 16 Engine (Compliant with ISO/IEC 3309)
- Hardware DES and Triple DES Is DPA Resistant

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management/Access

Development Tools

- Hardware/Software Development Support on Voyager Emulation Platform (ATV2)
- IAR Systems C-Spy® Debugger or AVR Studio® Version 4.06 or later
- Software Libraries and Application Notes

Secure Microcontroller for Smart Cards

AT90SC4802R

Preliminary

Rev. 1579AS–SMIC–25Nov02

Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Description

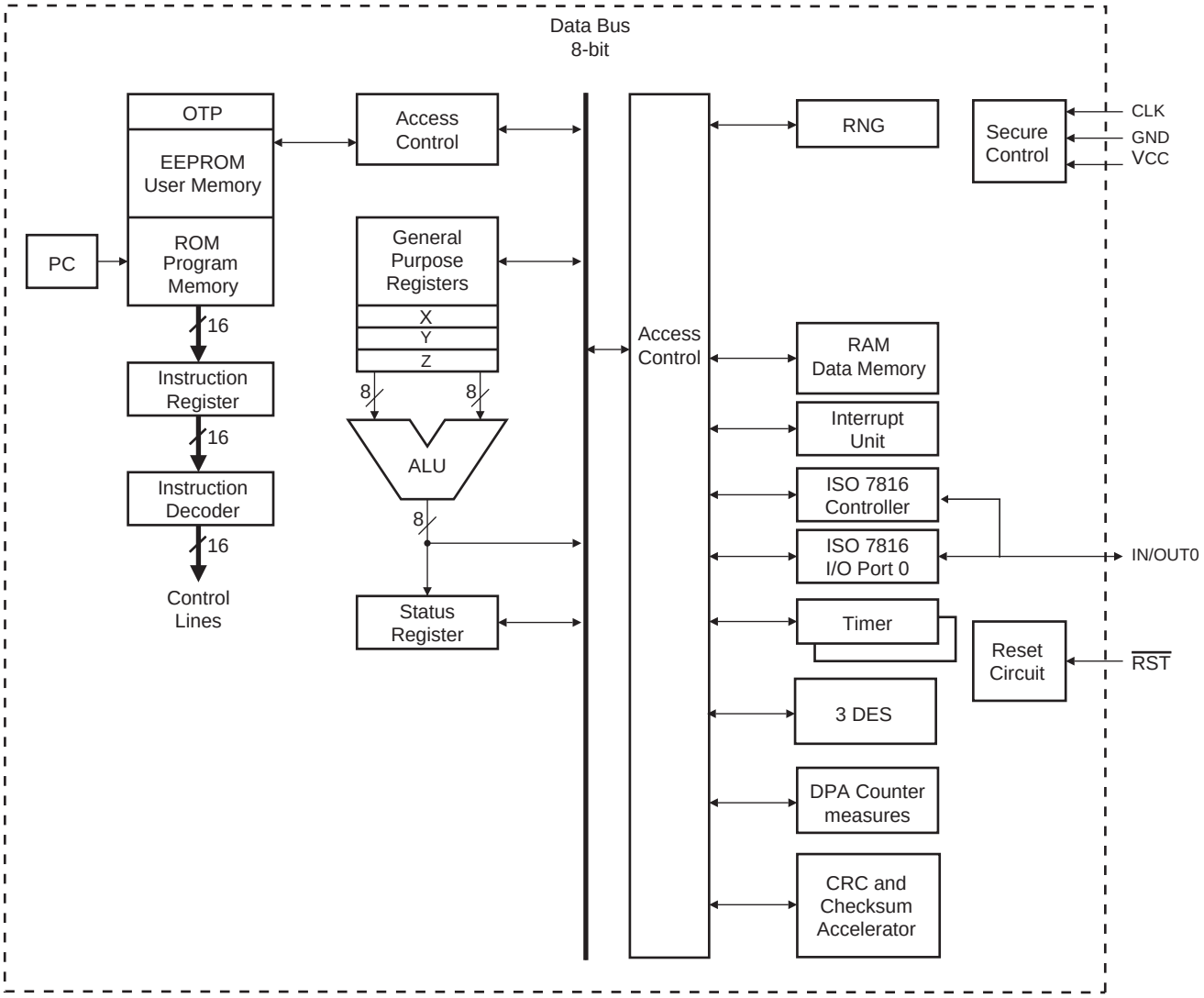
The AT90SC4802R is a low-power, high-performance, 8-/16-bit microcontroller, based on the secureAVR™ RISC architecture, with ROM program memory and EEPROM data memory. By executing powerful instructions in a single clock cycle, the AT90SC4802R achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The AT90SC4802R uses the secureAVR architecture that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data, and also provides a number of new functional and security features.

Additional security features include power, frequency and protection logic, logical scrambling on program data and addresses, power analysis countermeasures, and memory accesses controlled by a supervisor mode.

A block diagram of the AT90SC4802R is shown in Figure 1.

Figure 1. AT90SC4802R Secure AVR RISC Architecture



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