Features

- **Next Generation Equivalent of ATF20V8B (ATF20V8BQ, ATF22V10BQC)**
- **Complimentary Easy-to-use Atmel-WinCUPL Design Software**
- **"Z" Zero Power Compared to "L" Low Power**
- **Edge-sensing Zero Standby Power (10 µA Typical) (CQZ)**
- **Pin-controlled Zero Standby Power (10 µA Typical) Option (C, CQ)**
- **User-controlled Power-down Pin (C, CQ)**
- **High-speed Electrically Erasable Programmable Logic Devices**
  - **5 ns Maximum Pin-to-pin Delay (C)**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **Pin-keeper Feature Holds Inputs and I/Os to Previous Logic States**
  - **PCI Compliant**
- **High-reliability EE Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000V ESD Protection**
  - **200 mA Latch-up Immunity**
- **Commercial and Industrial Temperature Ranges**

AT20V8C Family High-performance EE PLD

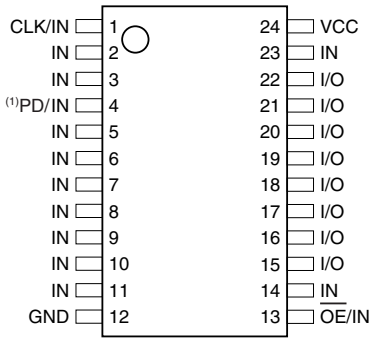
ATF20V8C
ATF20V8CQ
ATF20V8CQZ

Pin Configurations

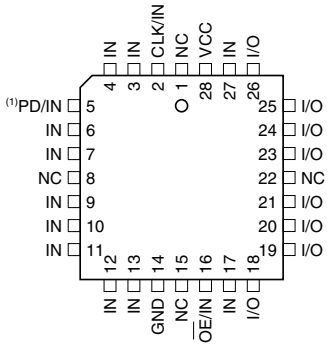
All Pinouts Top View

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
$\overline{OE}$	Output Enable
NC	No Internal Connection
VCC	+5V Supply
PD	Power-down

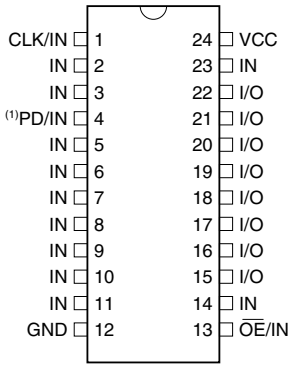
TSSOP



PLCC



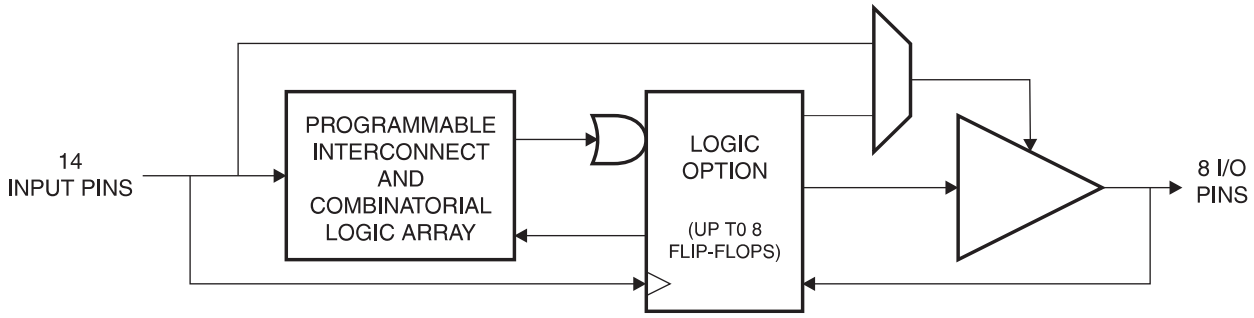
DIP/SOIC



Note: 1. PD on C and CQ only.

Rev. 0408H–04/01

Block Diagram



Description

The ATF20V8C is a high-performance CMOS (electrically erasable) programmable logic device (PLD) that utilizes Atmel's proven electrically erasable technology. Speeds down to 5 ns and power dissipation as low as 10 µA are offered. All speed ranges are specified over the full 5V ± 10% range for industrial temperature ranges, and 5V ± 5% for commercial ranges.

The ATF20V8C(Q) provides a high-speed CMOS PLD solution with maximum pin-to-pin delay of 5 ns. The ATF20V8C(Q) also has a user-controlled power-down feature, offering "zero" standby power (10 µA typical). The user-controlled power-down feature allows the user to manage total system power to meet specific application requirements and enhance reliability without sacrificing speed.

The ATF20V8CQZ provides the zero power CMOS PLD solution, with "zero" standby power (10 µA typical). The device powers down automatically through Atmel's patented Input Transition Detection (ITD) circuitry to the "zero" standby power mode when all inputs are idle.

Pin "keeper" circuits on input and output pins reduce static power consumed by pull-ups.

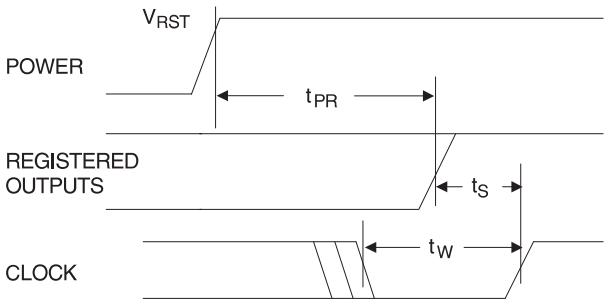
The ATF20V8C(Q)(Z) is the industry-standard 20V8 architecture. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

Power-up Reset

The registers in the ATF20V8Cs are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR}.



Preload of Registered Outputs

The ATF20V8C registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF20V8C's fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

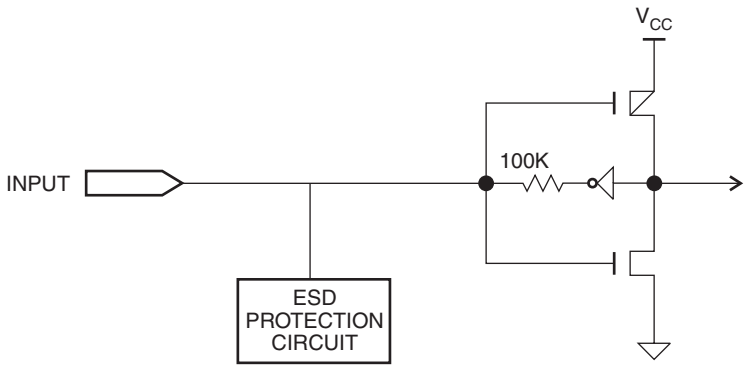
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. For further information, see the Configurable Logic data book section titled, "CMOS PLD Programming Hardware and Software Support."

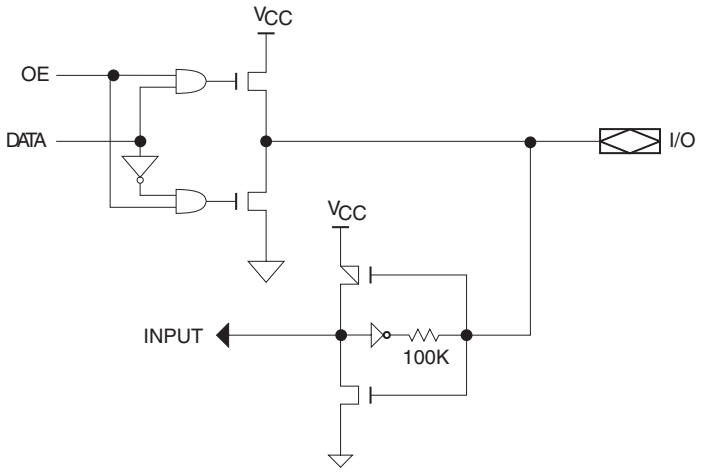
Input and I/O Pull-ups

All ATF20V8C family members have internal input and I/O "pin-keeper" circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The logic option and functional diagrams describe the ATF20V8C architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output or dedicated input.

The ATF20V8C's macrocell can be configured in one of three different modes. Each mode makes the ATF20V8Cs look like a different device. The ATF20V8Cs can be a registered output, combinatorial I/O, combinatorial output or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20V8Cs have a user-controlled power-down pin, which, when active, allows the user to place the device into a "zero" standby power-down mode. The device can also operate at high speed. Maximum pin-to-pin delays of 5 ns are offered. Static power loss due to pull-up resistors is eliminated by using input and output pin "keeper" circuits that hold pins to their previous logic levels when idle.

The universal architecture of the ATF20V8Cs can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer and the ATF20V8Cs can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents the ATF20V8Cs. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8	P20V8
CUPL	G20V8MS	G20V8MA	G20V8	G20V8A
LOG/iC	GAL20V8_R(1)	GAL20V8_C7(1)	GAL20V8_C8(1)	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8
PLDesigner	P20V8	P20V8	P20V8	P20V8
Tango-PLD	G20V8	G20V8	G20V8	G20V8

Note: 1. Only applicable for version 3.4 or lower.

Registered Mode

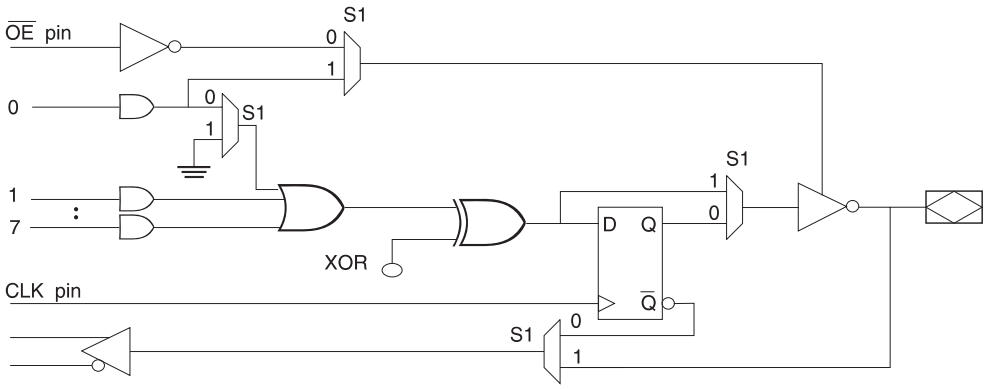
PAL Device Emulation/PAL Replacement

The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

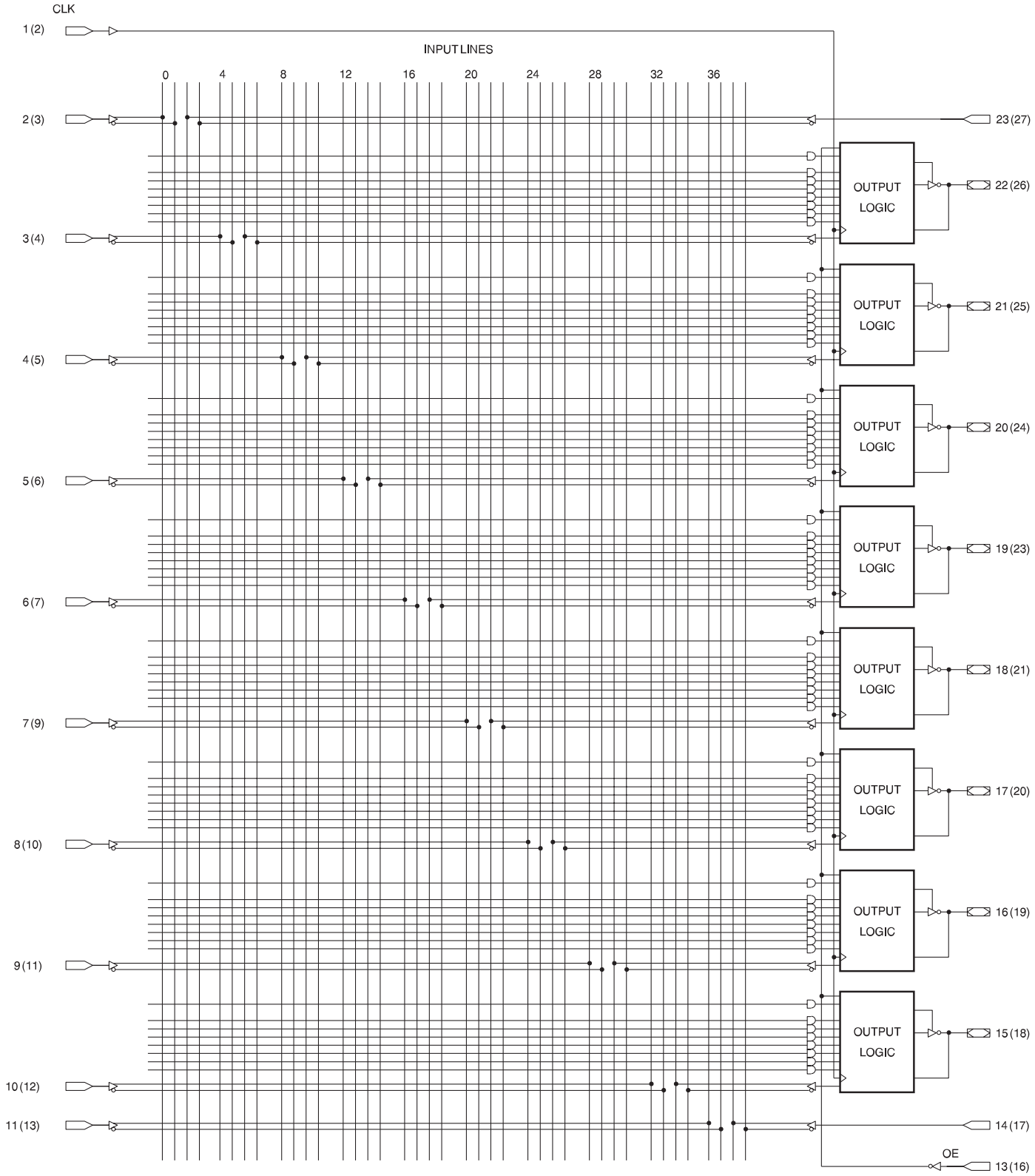
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

20R8	20RP8
20R6	20RP6
20R4	20RP4

Registered Mode Operation



Registered Mode Logic Diagram



Complex Mode

PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

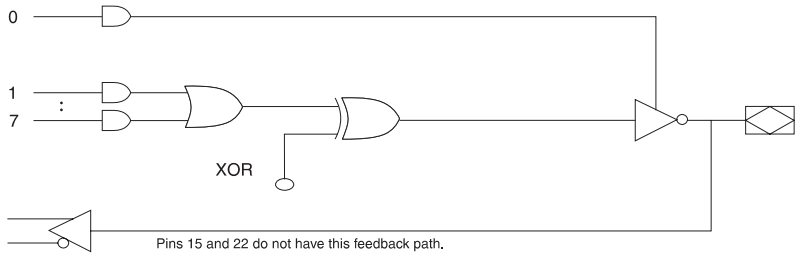
Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

20L8

20H8

20P8

Complex Mode Operation



Simple Mode

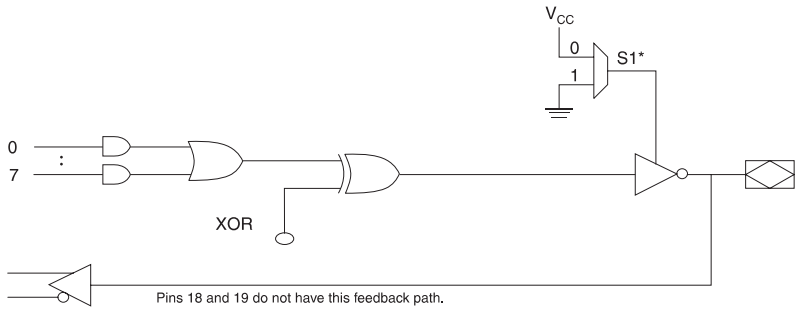
PAL Device Emulation/PAL Replacement

In the Simple Mode, eight product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

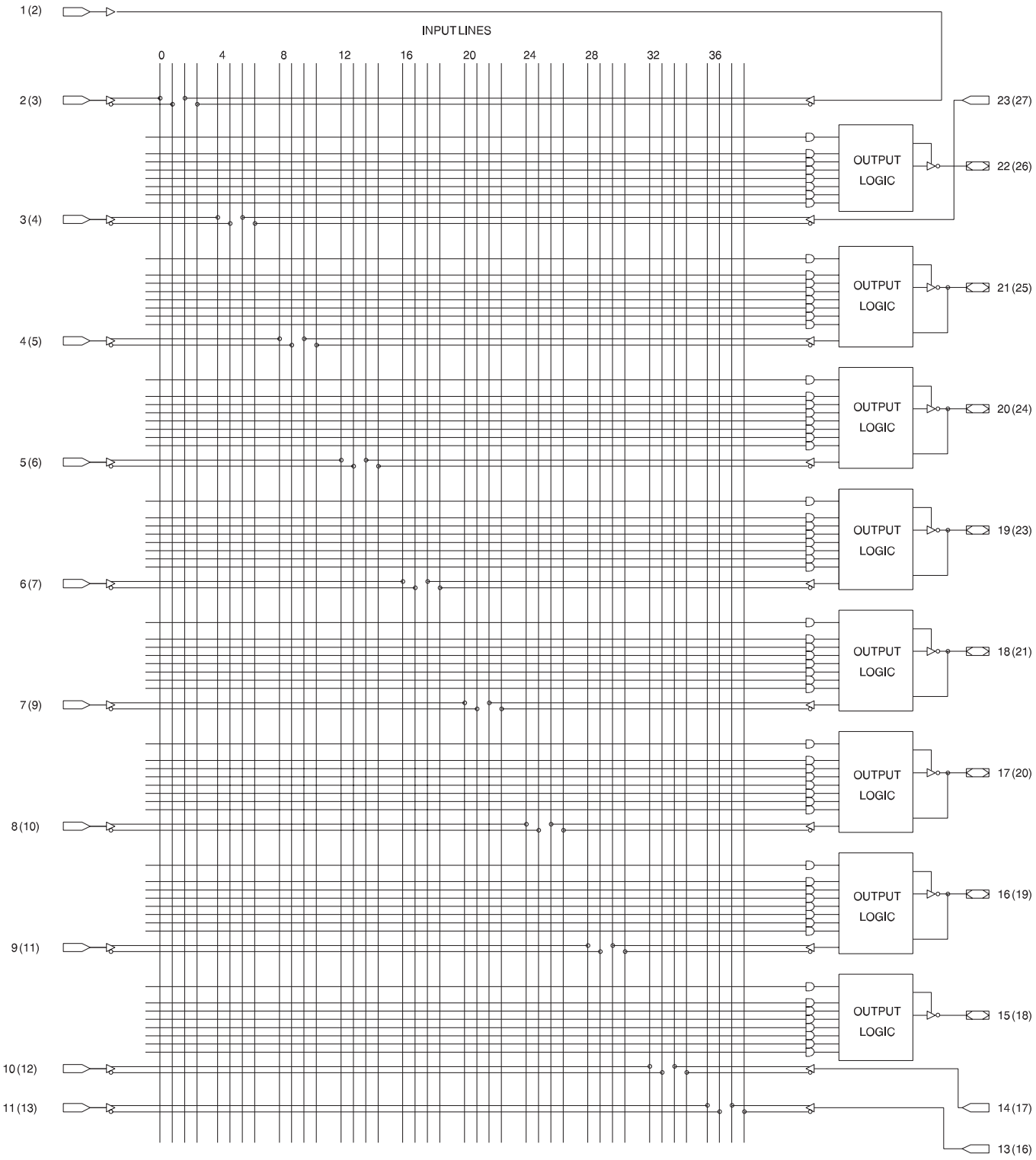
14L8	14H8	14P8
16L6	18H6	16P6
18L4	18H4	18P4
20L2	20H2	20P2

Simple Mode Option

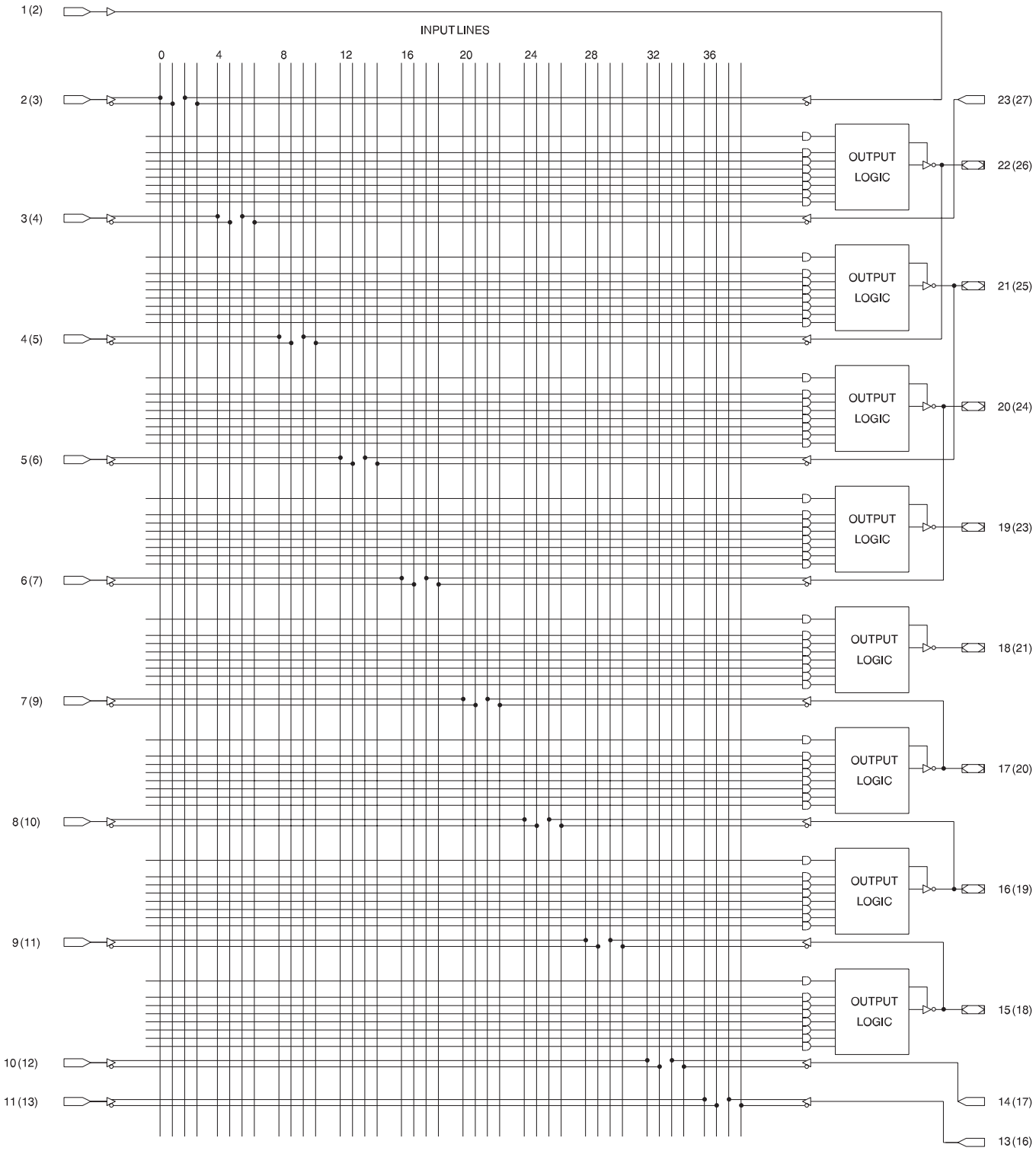


* - Pins 18 and 19 are always enabled.

Complex Mode Logic Diagram



Simple Mode Logic Diagram



Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground during Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

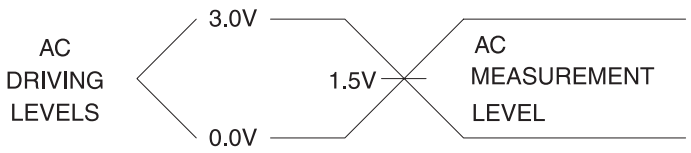
Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%

Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

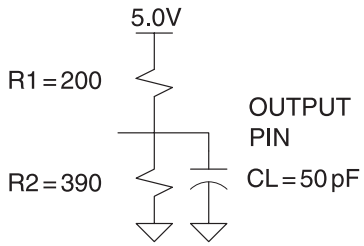
Input Test Waveforms and Measurement Levels



t_R, t_F < 1.5 ns (10% to 90%)

Output Test Loads

Commercial



Pin Capacitance

f = 1 MHz, T = 25°C[1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

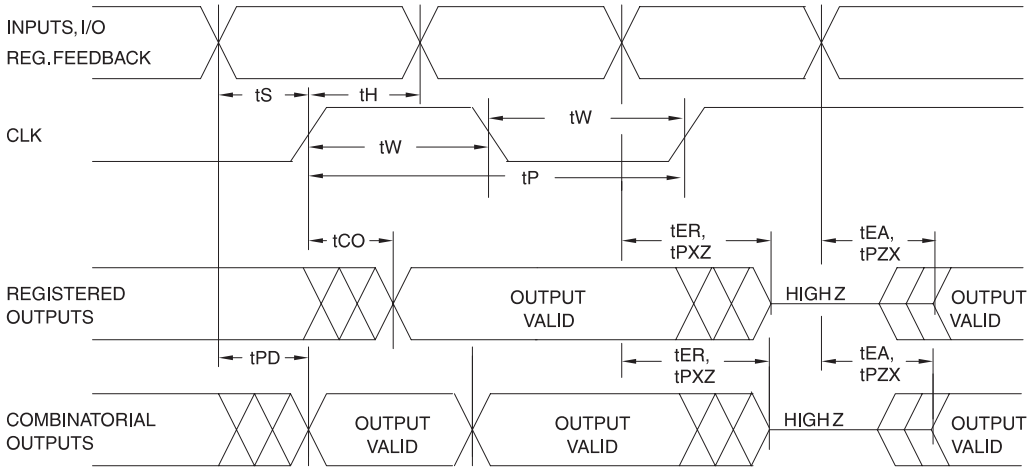
ATF20V8C DC Characteristics

V_{CC} = 5.0V and T_A = 25°C

Symbol	Parameter	Condition				Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)					-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$						10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = Max, V_{IN} = Max, Outputs Open	C-5		Com.		60	90	mA
			C-5		Ind.		60	100	mA
			C-7		Com.		60	90	mA
			C-7		Ind.		60	100	mA
			C-10		Com.		60	80	mA
			C-10		Ind.		60	90	mA
			C-15		Com.		60	80	mA
			C-15		Ind.		60	90	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open, f = 15 MHz	C-5		Com.		70	110	mA
			C-5		Ind.		70	125	mA
			C-7		Com.		70	110	mA
			C-7		Ind.		70	125	mA
			C-10		Com.		60	90	mA
			C-10		Ind.		60	105	mA
			C-15		Com.		60	90	mA
			C-15		Ind.		60	105	mA
IOS[1]	Output Short Circuit Current	V_{OUT} = 0.5V						-130	mA
V_{IL}	Input Low Voltage					-0.5		0.8	V
V_{IH}	Input High Voltage					2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA		Com., Ind.			0.5	V
			I_{OL} = 16 mA					0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = -4.0 mA			2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. All values are at V_{CC} and T_A=25°C.
3. Shaded area indicates preliminary data.

AC Waveforms(1)



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

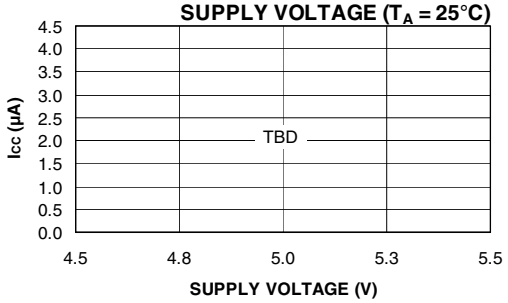
ATF20V8C Family AC Characteristics(1)

Symbol	Parameter		C-5		C-7		C-10		C-15		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-registered Output	8 outputs switching	3	5	3	7.5	3	10	3	15	ns
		1 output switching				7				10	ns
t_{CF}	Clock to Feedback			3		3		6		8	ns
t_{CO}	Clock to Output		2	4	2	5	2	7	2	10	ns
t_S	Input or Feedback Setup Time		3		5		7.5		12		ns
t_H	Hold Time		0		0		0		0		ns
t_P	Clock Period		6		8		12		16		ns
t_W	Clock Width		3		4		6		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$			143		100		68		45	MHz
	Internal Feedback $1/(t_S + t_{CF})$			167		125		74		50	MHz
	No Feedback $1/(t_P)$		7	167		125		83		62	MHz
t_{EA}	Input to Output Enable – Product Term		3	6	3	9	3	10	3	15	ns
t_{ER}	Input to Output Disable – Product Term		2	6	2	9	2	10	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	5	2	6	2	10	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	5	1.5	6	1.5	10	1.5	15	ns

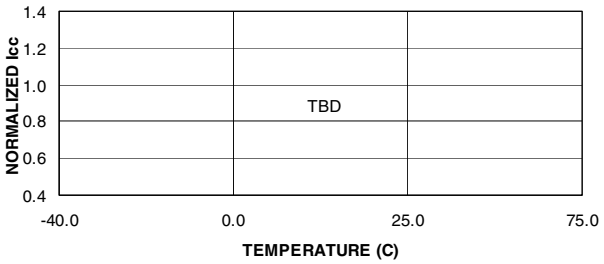
Notes: 1. See ordering information for valid part numbers and speed grades.
2. Shaded area indicates preliminary data.

ATF20V8C Characteristic Curves

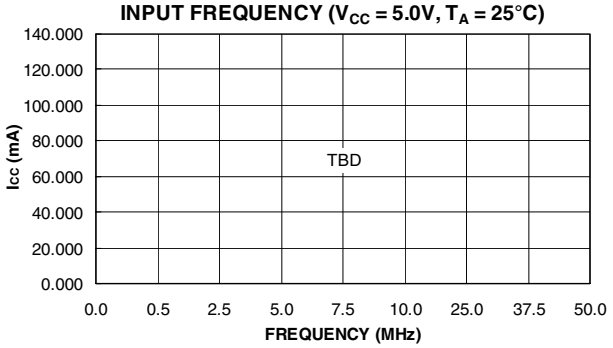
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



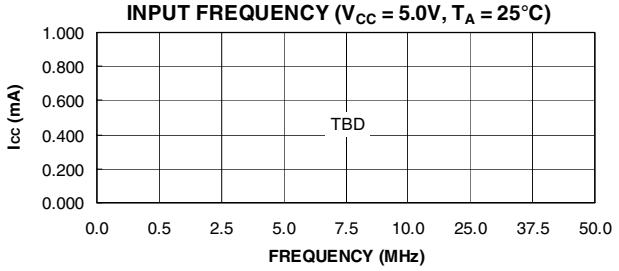
NORMALIZED I_{CC} VS. TEMP



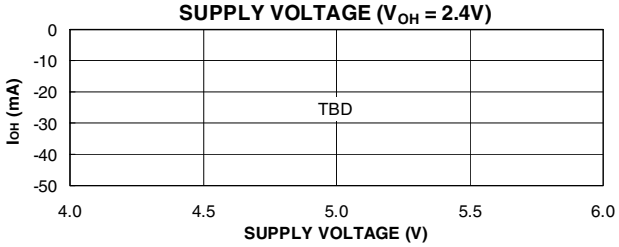
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



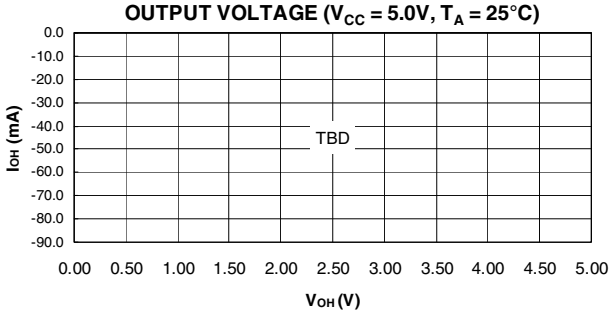
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



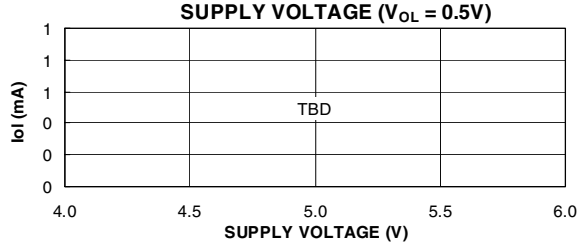
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



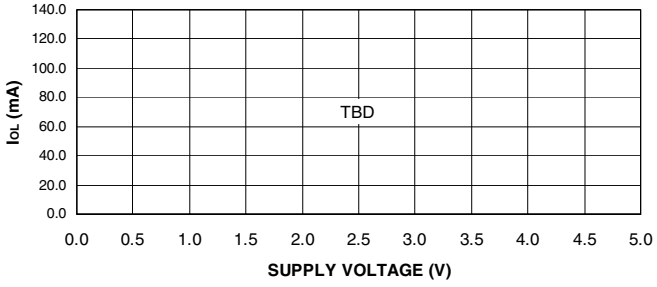
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)

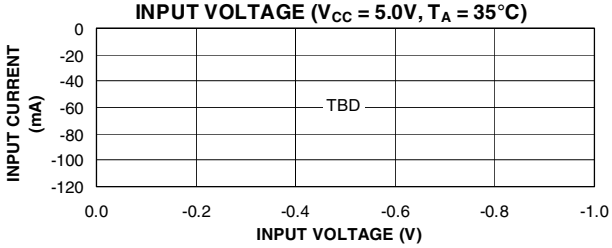


OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)

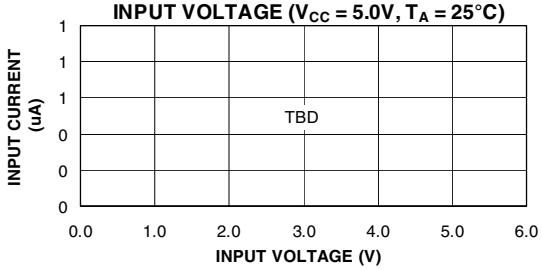


ATF20V8C Characteristic Curves (Continued)

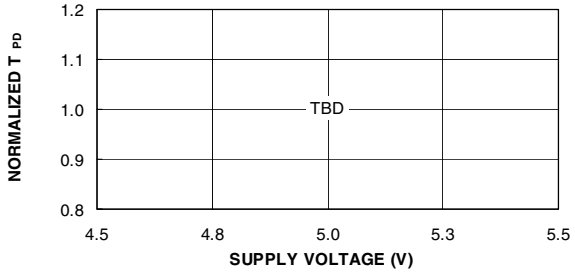
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



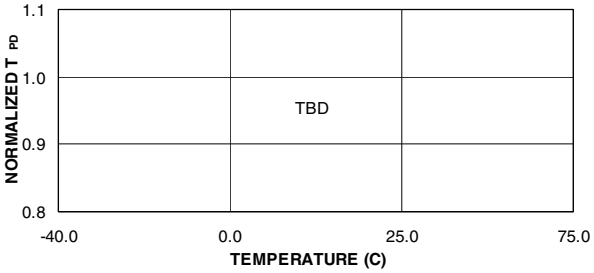
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



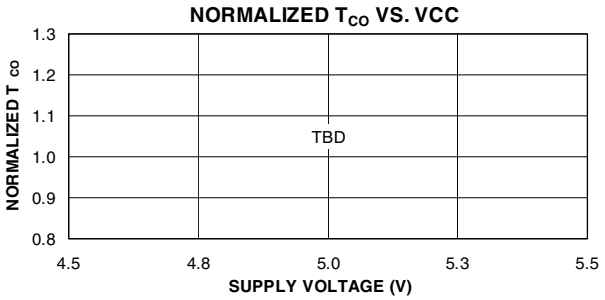
NORMALIZED T_{PD} VS. VCC



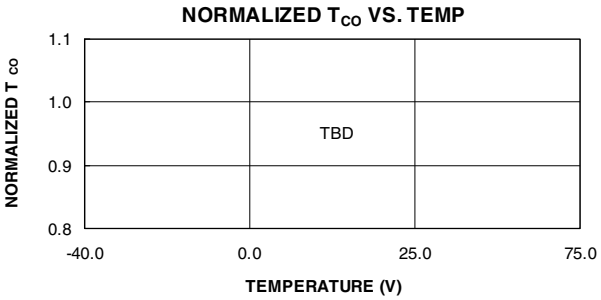
NORMALIZED T_{PD} VS. TEMP



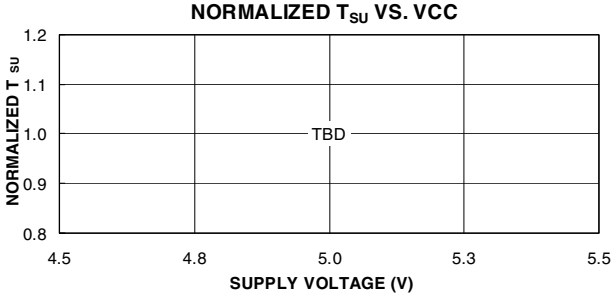
NORMALIZED T_{CO} VS. VCC



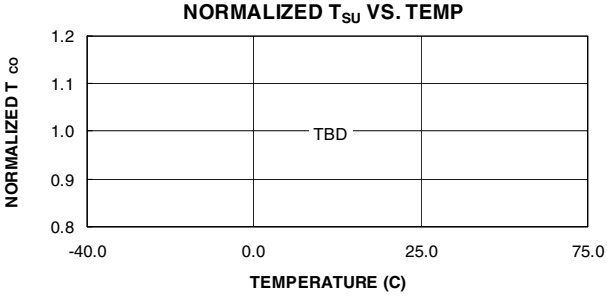
NORMALIZED T_{CO} VS. TEMP



NORMALIZED T_{SU} VS. VCC

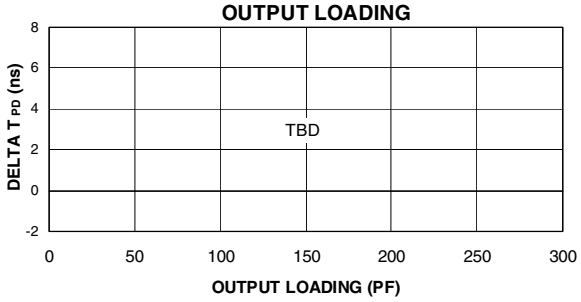


NORMALIZED T_{SU} VS. TEMP

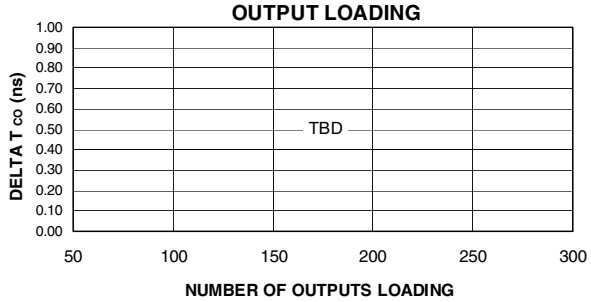


ATF20V8C Characteristic Curves (Continued)

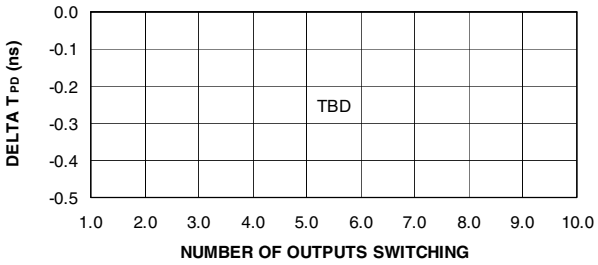
DELTA T_{PD} VS. OUTPUT LOADING



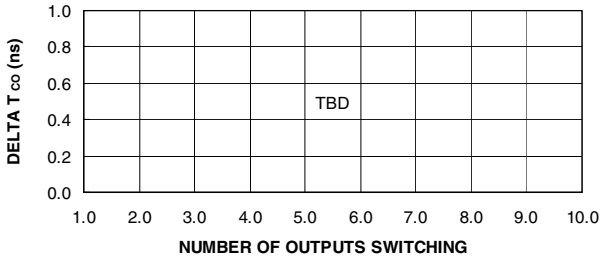
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF20V8CQ DC Characteristics

V_{CC} = 5.0V and T_A = 25°C

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = Max, V_{IN} = Max, Outputs Open	CQ-10, -15	Com.		10	25	µA
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open, f = 15 MHz	CQ-10, 15	Com.		40	55	mA
IOS[1]	Output Short Circuit Current	V_{OUT} = 0.5V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA	Com., Ind.			0.5	V
			I_{OL} = 16 mA				0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Shaded areas indicate preliminary data.

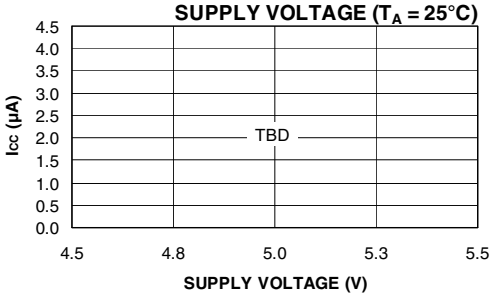
ATF20V8CQ AC Characteristics(1)

Symbol	Parameter		CQ-10 Min	CQ-10 Max	Units
t_{PD}	Input or Feedback to Non-registered Output	8 outputs switching	3	10	ns
		1 output switching			ns
t_{CF}	Clock to Feedback			6	ns
t_{CO}	Clock to Output		2	7	ns
t_S	Input or Feedback Setup Time		7.5		ns
t_H	Hold Time		0		ns
t_P	Clock Period		12		ns
t_W	Clock Width		6		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$			68	MHz
	Internal Feedback $1/(t_S + t_{CF})$			74	MHz
	No Feedback $1/(t_P)$			83	MHz
t_{EA}	Input to Output Enable – Product Term		3	10	ns
t_{ER}	Input to Output Disable – Product Term		2	10	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	10	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	10	ns

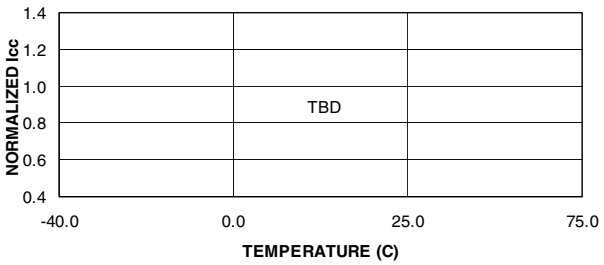
Notes: 1. See ordering information for valid part numbers and speed grades.
2. All values are at V_{CC}=5V and T_A=25°C.
3. Shaded areas indicate preliminary data.

ATF20V8CQ Characteristic Curves

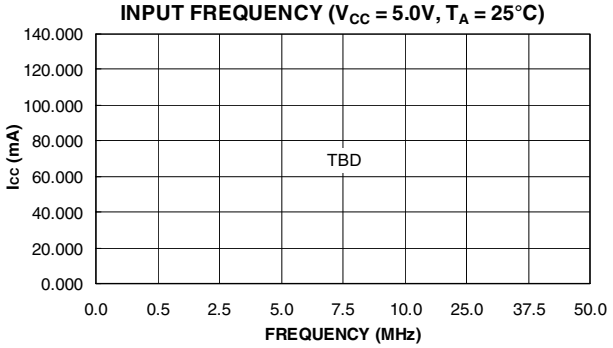
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



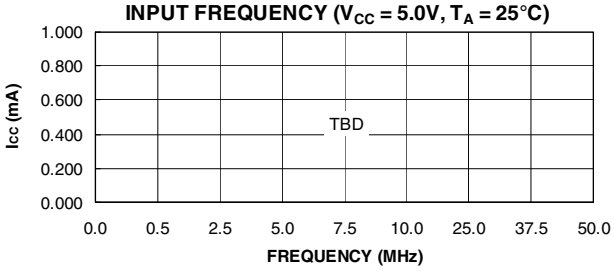
NORMALIZED I_{CC} VS. TEMP



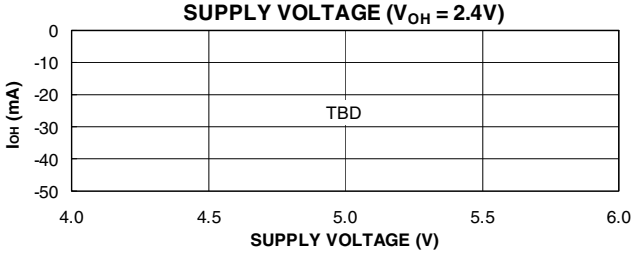
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



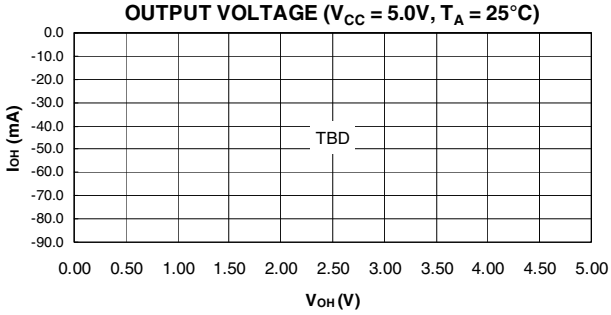
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



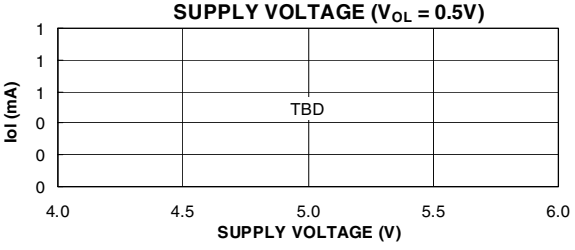
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



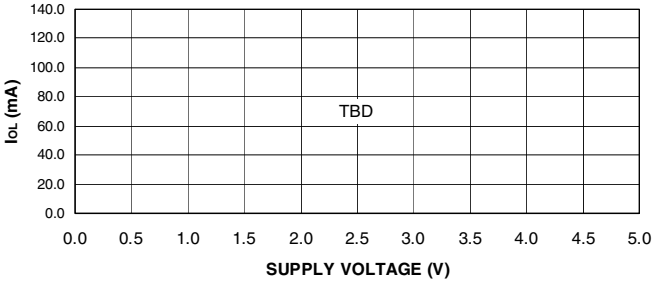
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)

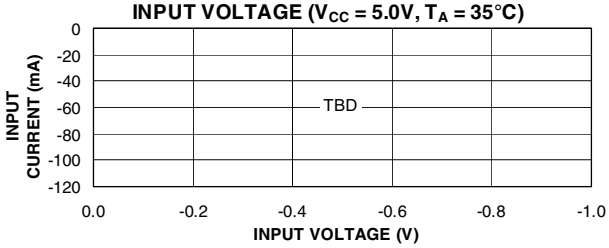


OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)

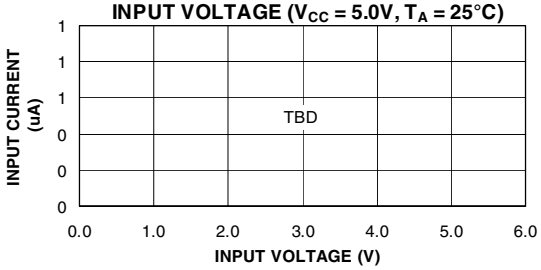


ATF20V8CQ Characteristic Curves (Continued)

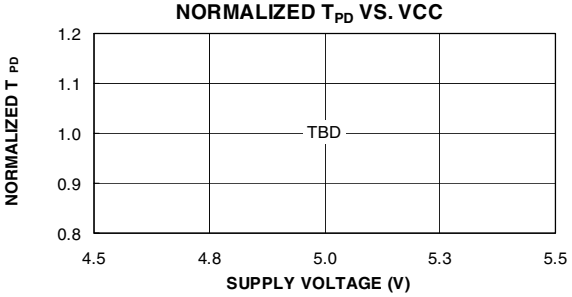
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



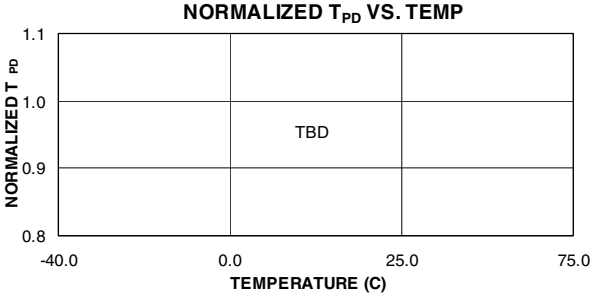
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



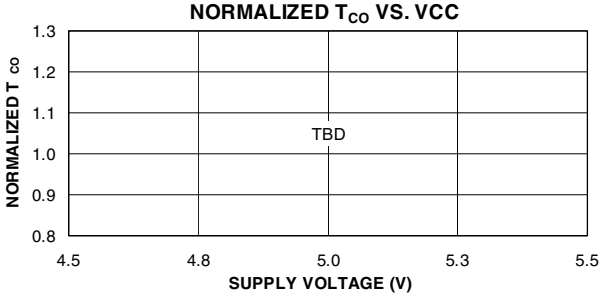
NORMALIZED T_{PD} VS. VCC



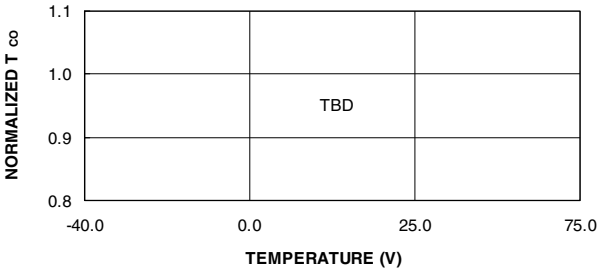
NORMALIZED T_{PD} VS. TEMP



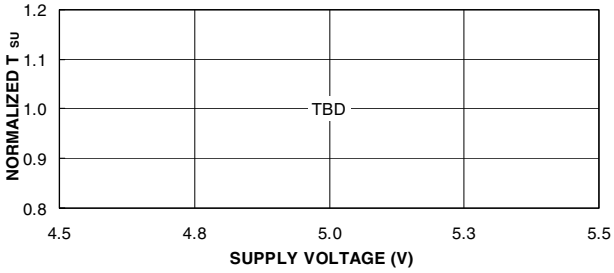
NORMALIZED T_{CO} VS. VCC



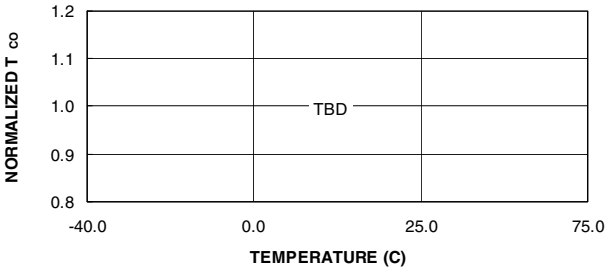
NORMALIZED T_{CO} VS. TEMP



NORMALIZED T_{SU} VS. VCC

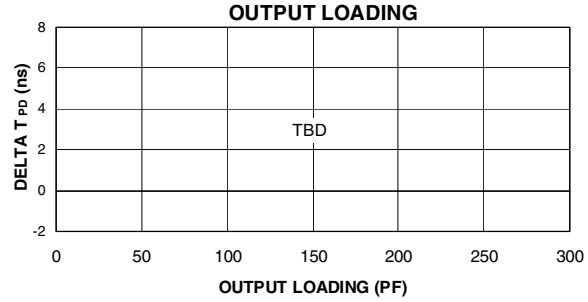


NORMALIZED T_{SU} VS. TEMP

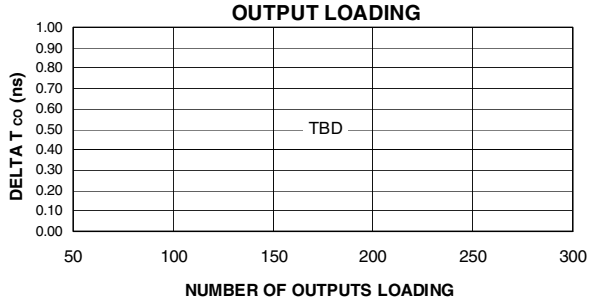


ATF20V8CQ Characteristic Curves (Continued)

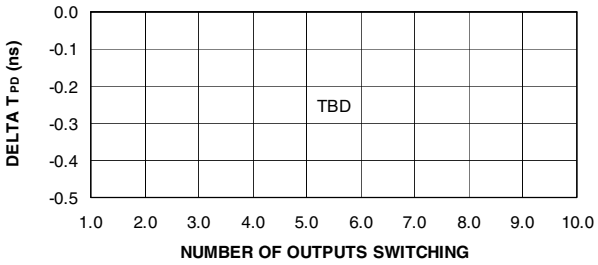
DELTA T_{PD} VS. OUTPUT LOADING



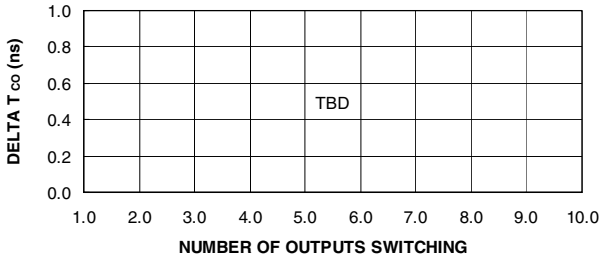
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF20V8CQZ DC Characteristics

V_{CC} = 5.0V and T_A = 25°C

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = Max, V_{IN} = Max, Outputs Open	CQZ-15	Com.		10	25	µA
				Ind.		10	50	µA
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open, f = 15 MHz	CQZ-15	Com.		20	35	mA
				Ind.		20	40	mA
IOS[1]	Output Short Circuit Current	V_{OUT} = 0.5V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA	Com., Ind.			0.5	V
			I_{OL} = 16 mA				0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. All values are at V_{CC}=5V and T_A=25°C.
3. Shaded areas indicate preliminary data.

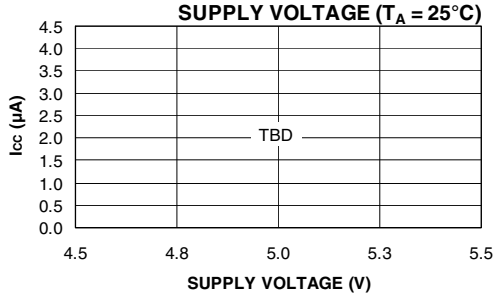
ATF20V8CQZ AC Characteristics(1)

Symbol	Parameter		CQZ-15 Min	CQZ-15 Max	Units
t_{PD}	Input or Feedback to Non-registered Output	8 outputs switching	3	15	ns
		1 output switching		10	ns
t_{CF}	Clock to Feedback			8	ns
t_{CO}	Clock to Output		2	10	ns
t_S	Input or Feedback Setup Time		12		ns
t_H	Hold Time		0		ns
t_P	Clock Period		16		ns
t_W	Clock Width		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$			45	MHz
	Internal Feedback $1/(t_S + t_{CF})$			50	MHz
	No Feedback $1/(t_P)$			62	MHz
t_{EA}	Input to Output Enable – Product Term		3	15	ns
t_{ER}	Input to Output Disable – Product Term		2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	15	ns

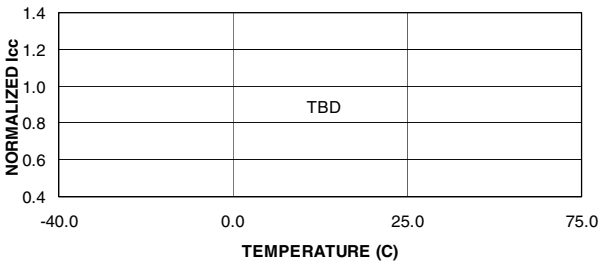
Notes: 1. See ordering information for valid part numbers and speed grades.
2. Shaded areas indicate preliminary data.

ATF20V8CQZ Characteristic Curves

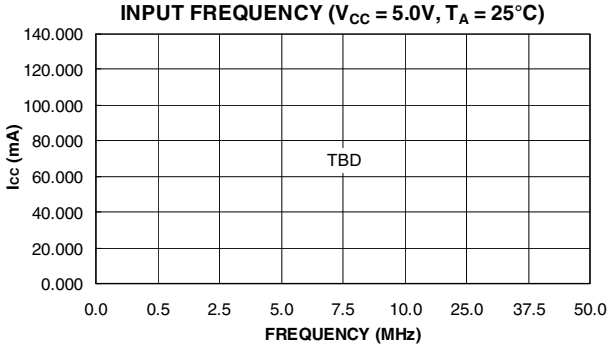
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



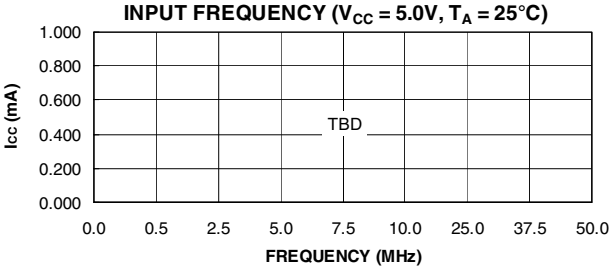
NORMALIZED I_{CC} VS. TEMP



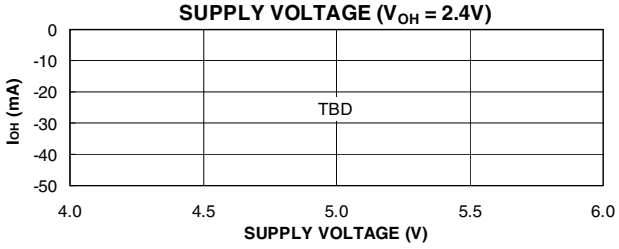
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



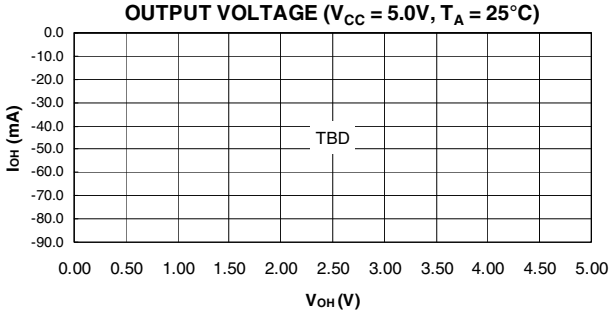
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



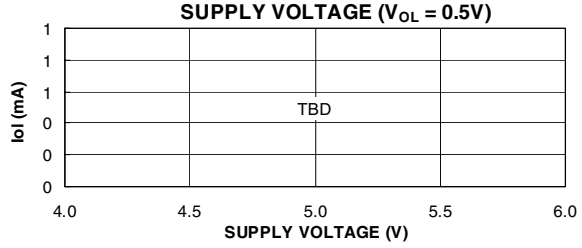
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



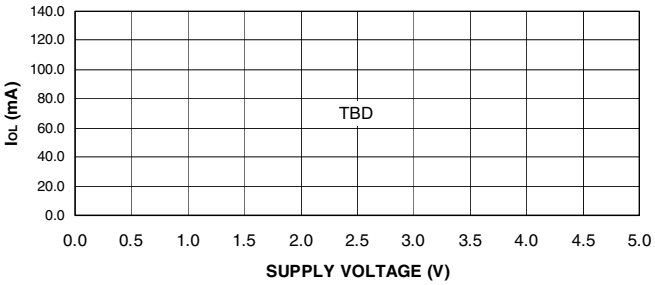
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)

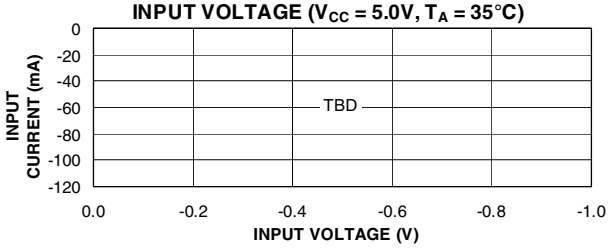


OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)

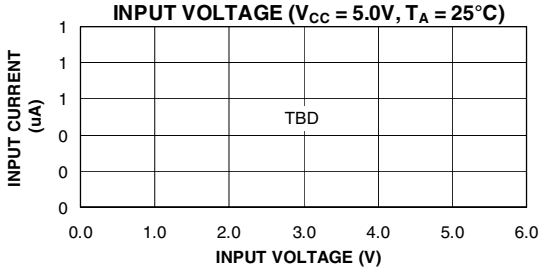


ATF20V8CQZ-15 Characteristic Curves (Continued)

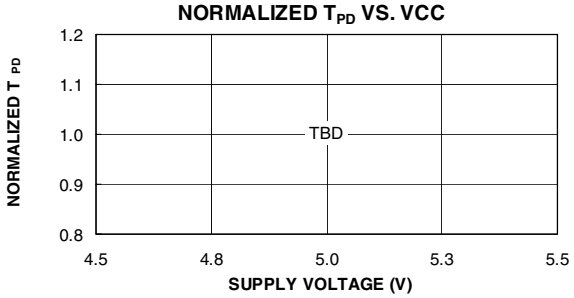
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



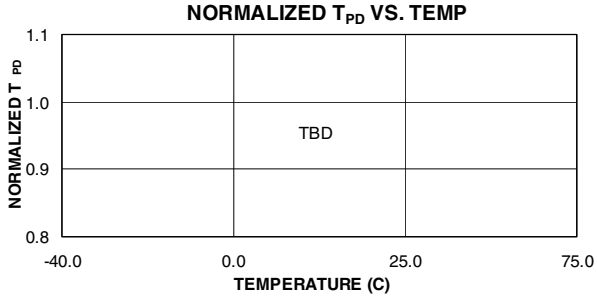
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



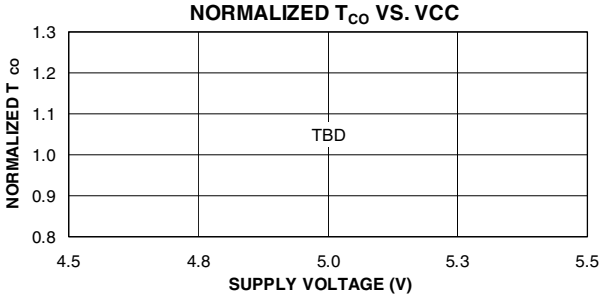
NORMALIZED T_{PD} VS. VCC



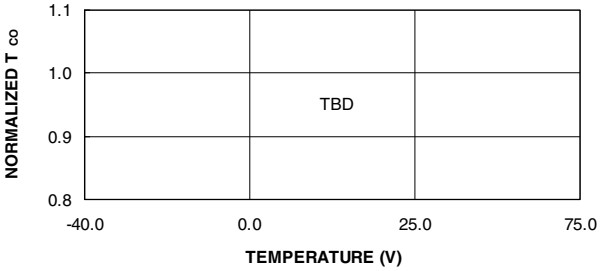
NORMALIZED T_{PD} VS. TEMP



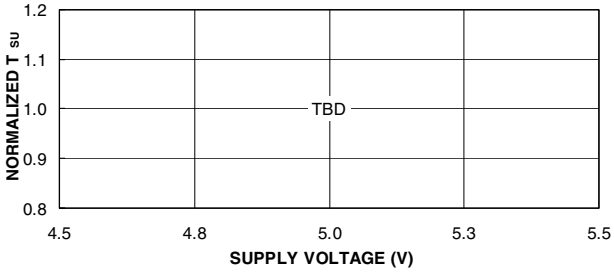
NORMALIZED T_{CO} VS. VCC



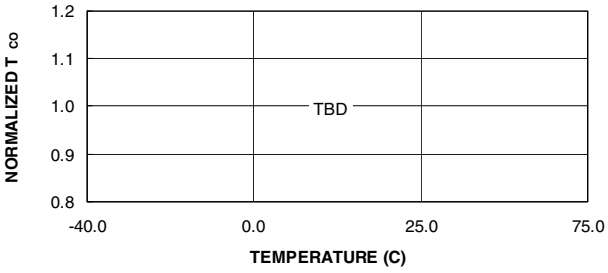
NORMALIZED T_{CO} VS. TEMP



NORMALIZED T_{SU} VS. VCC

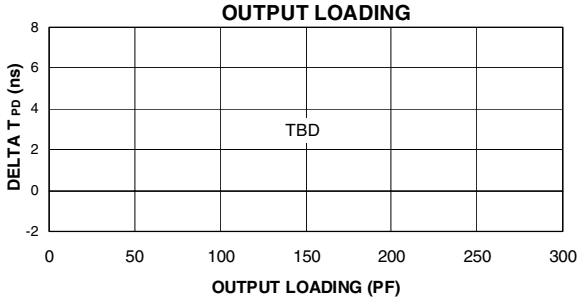


NORMALIZED T_{SU} VS. TEMP

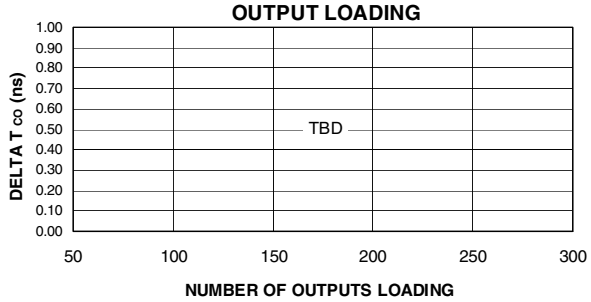


ATF20V8CQZ-15 Characteristic Curves (Continued)

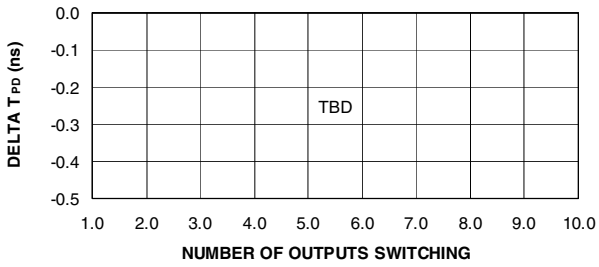
DELTA T_{PD} VS. OUTPUT LOADING



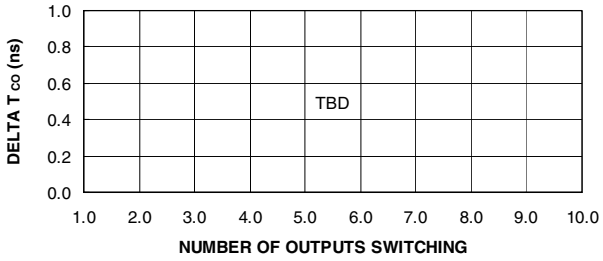
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



ATF20V8C Family Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	3	4	ATF20V8C-5JC	28J	Commercial (0°C to 70°C)
7.5	3.5	4.5	ATF20V8C-7JC ATF20V8C-7PC ATF20V8C-7SC ATF20V8C-7XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF20V8C-7JI ATF20V8C-7PI ATF20V8C-7SI ATF20V8C-7XI	28J 24P3 24S 24X	Industrial (-40°C to 85°C)
10	4.5	6.5	ATF20V8C-10JC ATF20V8C-10PC ATF20V8C-10SC ATF20V8C-10XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF20V8C-10JI ATF20V8C-10PI ATF20V8C-10SI ATF20V8C-10XI	28J 24P3 24S 24X	Industrial (-40°C to 85°C)
15	10	8	ATF20V8C-15JC ATF20V8C-15PC ATF20V8C-15SC ATF20V8C-15XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF20V8C-15JI ATF20V8C-15PI ATF20V8C-15SI ATF20V8C-15XI	28J 24P3 24S 24X	Industrial (-40°C to 85°C)
10	7.5	7	ATF20V8CQ-10JC ATF20V8CQ-10PC ATF20V8CQ-10SC ATF20V8CQ-10XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF20V8CQ-10JI ATF20V8CQ-10PI ATF20V8CQ-10SI ATF20V8CQ-10XI	28J 24P3 24S 24X	Industrial (-40°C to 85°C)
15	10	8	ATF20V8CQZ-15JC ATF20V8CQZ-15PC ATF20V8CQZ-15SC ATF20V8CQZ-15XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF20V8CQZ-15JI ATF20V8CQZ-15PI ATF20V8CQZ-15SI ATF20V8CQZ-15XI	28J 24P3 24S 24X	Industrial (-40°C to 85°C)

Note: 1. Shaded areas indicate preliminary data.

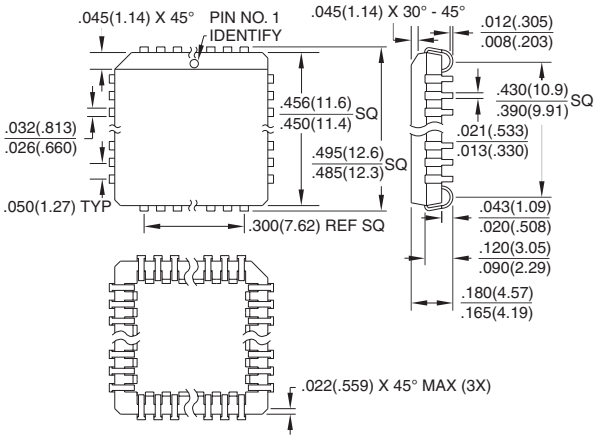
Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

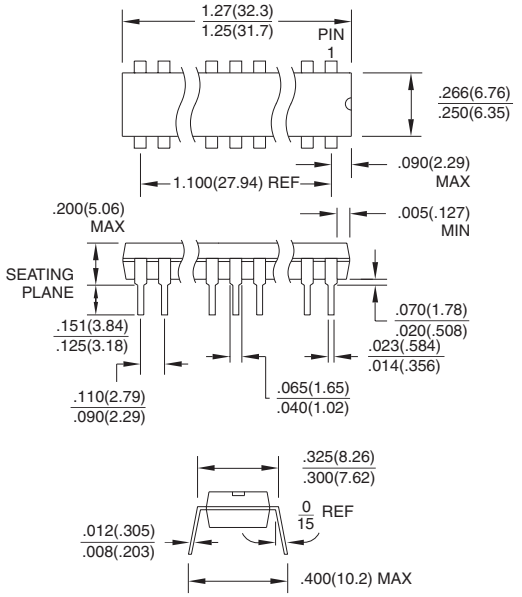
Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)
24P3	24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

Packaging Information

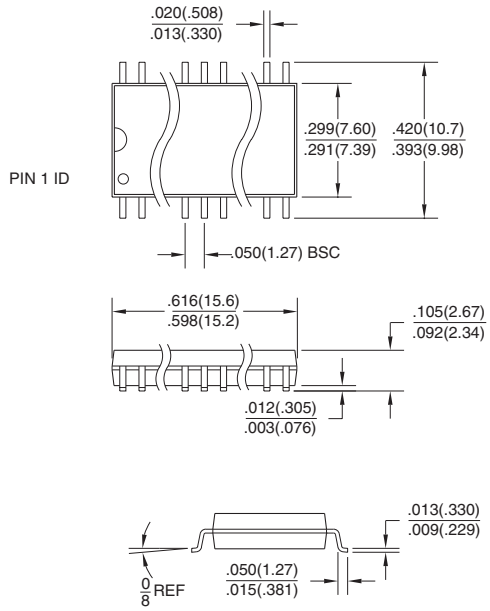
28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AB



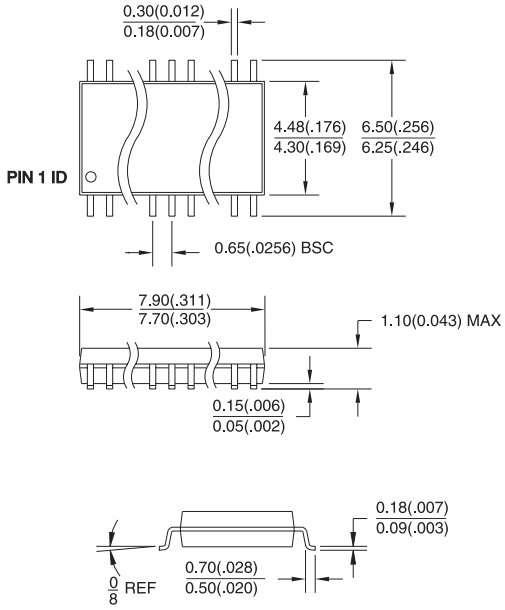
24P3, 24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AF



24S, 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



24X, 24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
Dimensions in Millimeters and (Inches)



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