Audio sound processor with BBE®*

BH3868BFS

BH3868BFS is a Audio sound processor IC developed for TV. This IC is built-in volume, balance, tone, surround, BBE processor and AGC. This IC can be easily controlled by tow-wire serial control (I^2C BUS).

* BBE is a registered trade mark of BBE Sound Inc.

Note : I^2C BUS is a registered trade mark of Philips.

●Applications

Suitable for TV, TV-radio, PC-TV, mini-component and car audio system, etc.

●Features

1) Volume (main volume), balance (right/left), tone (bass and treble), surround (mode and effect), BBE processor (effect) can be controlled by I^2C-BUS.
2) Volume is VCA with low distortion rate and low noise and can restrain the step noise.
3) The reference voltage source is stable, only a few external devices are required because I/O buffer is contained, and the package is suitable for space-saving design for SSOP-A32.
4) Sound spread can be controlled by the matrix surround and effect adjustment.
5) The built-in AGC circuit can absorb the volume difference between input sources.
6) The contained BBE processor, which reproduce an original sound, controls the effect.

●Absolute maximum ratings (Ta=25°C)

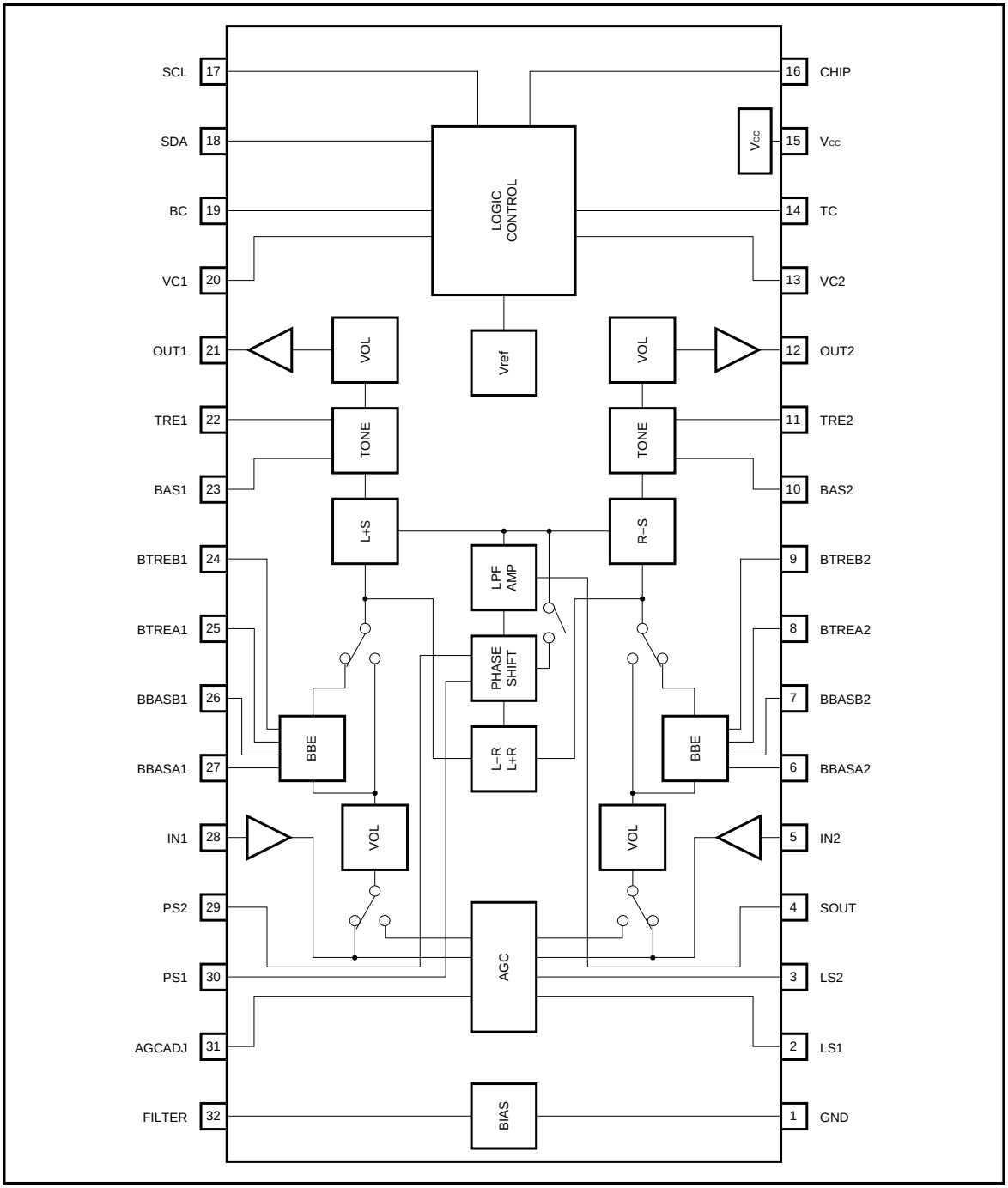
Parameter	Symbol	Limits	Unit
Impressed voltage	V_{CC}	10.0	V
Power dissipation	Pd	850*	mW
Operating temperature range	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +150	°C

* When mounted on a glass epoxy board 70mm × 70mm × 1.6mm.
Reduced by 6.8mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	7.0	–	9.5	V

●**Block diagram**

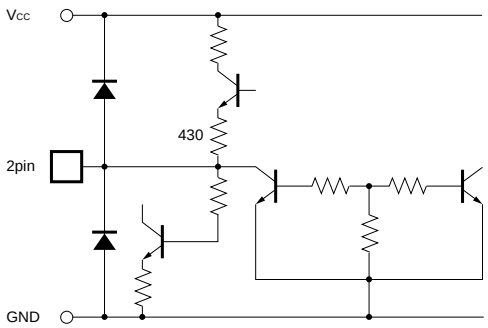
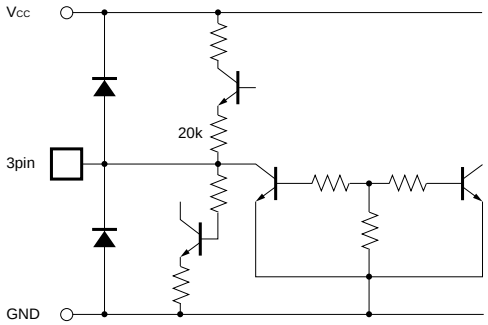
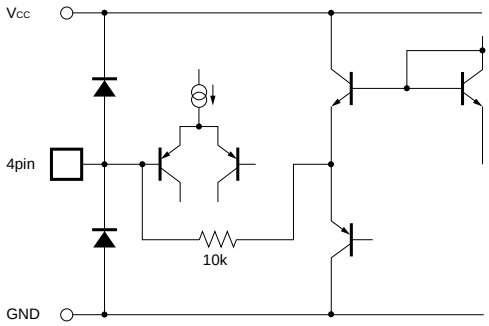
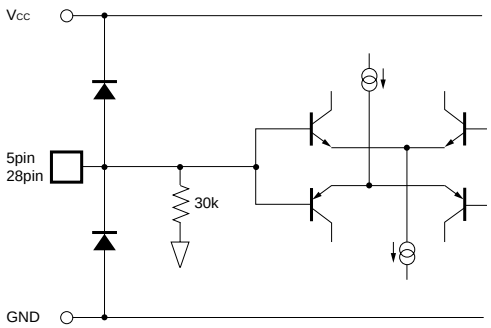


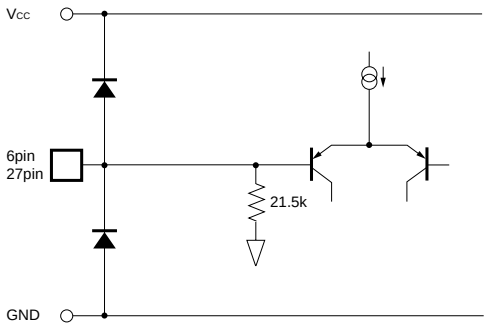
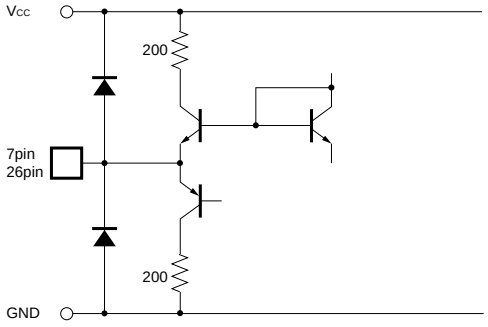
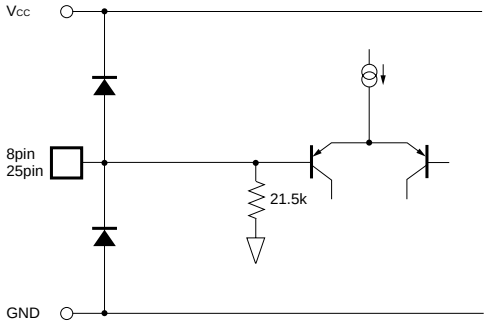
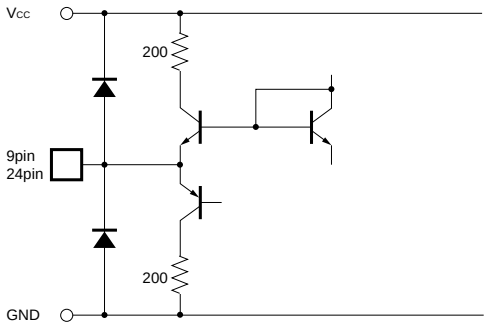
●Pin descriptions

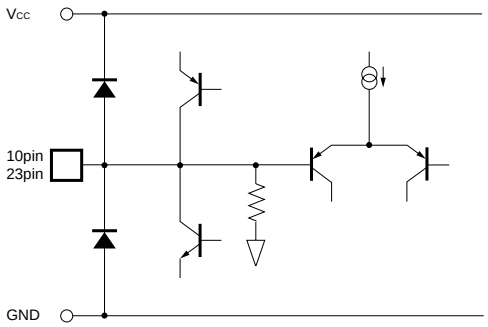
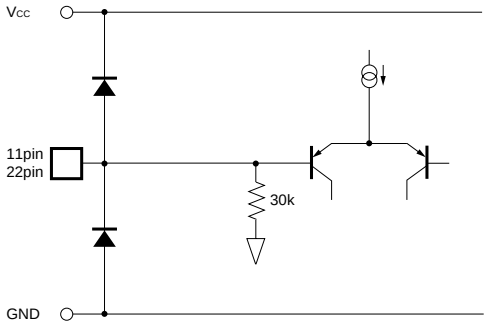
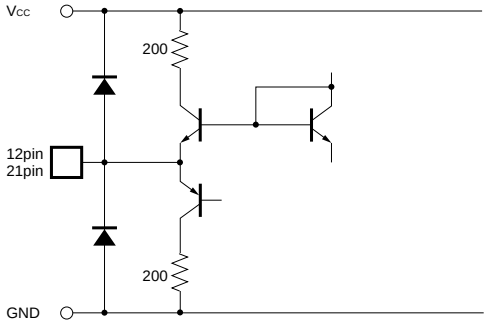
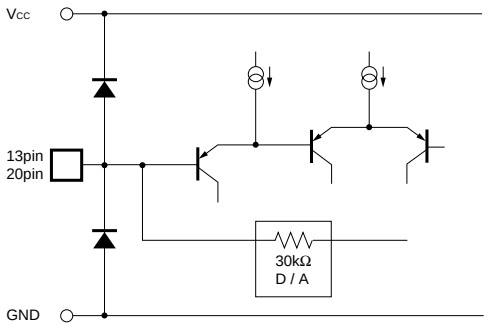
Pin No.	Pin name	Function
1	GND	Ground terminal
2	LS1	ALC detector terminal at suppression side
3	LS2	ALC detector terminal at amplification side
4	SOUT	Surround signal output terminal
5	IN2	2ch sound signal input terminal
6	BBASA2	2chBBE contour frequency setting terminal
7	BBASB2	2chBBE contour frequency setting terminal
8	BTREA2	2chBBE process frequency setting terminal
9	BTREB2	2chBBE process frequency setting terminal
10	BAS2	2ch bass fc setting terminal
11	TRE2	2ch treble fc setting terminal
12	OUT2	2ch sound signal output terminal
13	VC2	2ch volume control terminal
14	TC	Treble control terminal
15	V_{CC}	Power supply terminal
16	CHIP	Chip select terminal
17	SCL	I^2C clock input terminal
18	SDA	I^2C data input terminal
19	BC	Bass control terminal
20	VC1	1ch volume control terminal
21	OUT1	1ch sound signal output terminal
22	TRE1	1ch treble fc setting terminal
23	BAS1	1ch bass fc setting terminal
24	BTREB1	1chBBE process frequency setting terminal
25	BTREA1	1chBBE process frequency setting terminal
26	BBASB1	1chBBE contour frequency setting terminal
27	BBASA1	1chBBE contour frequency setting terminal
28	IN1	1ch sound signal input terminal
29	PS1	1st phase shift setting terminal
30	PS2	2nd phase shift setting terminal
31	AGCADJ	AGC suppression level setting terminal
32	FILTER	Filter terminal

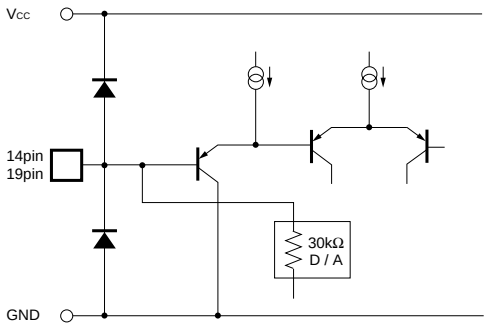
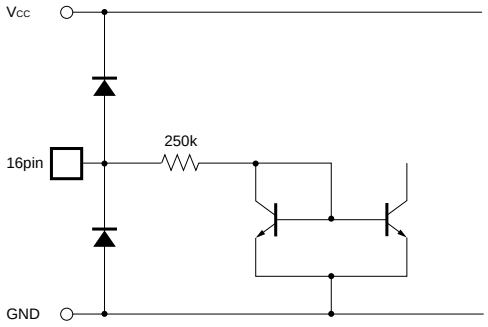
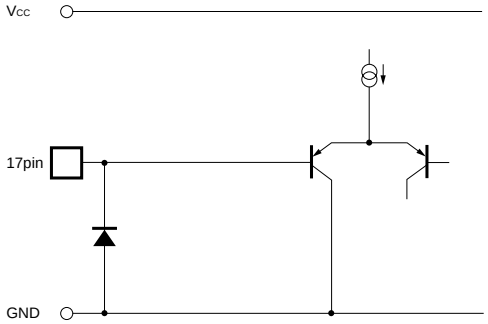
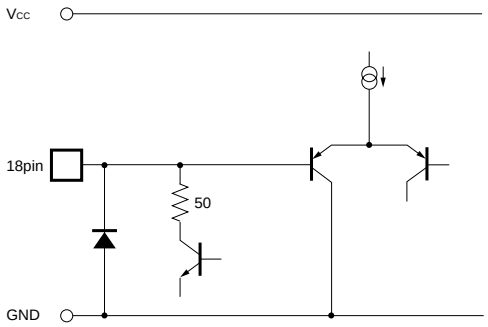
●Input output circuits

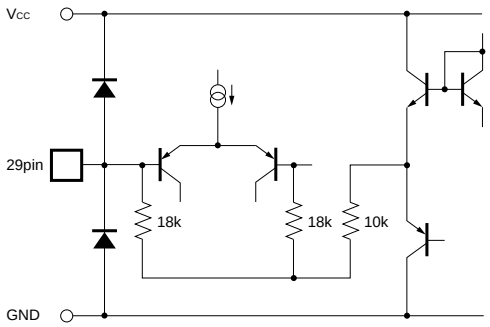
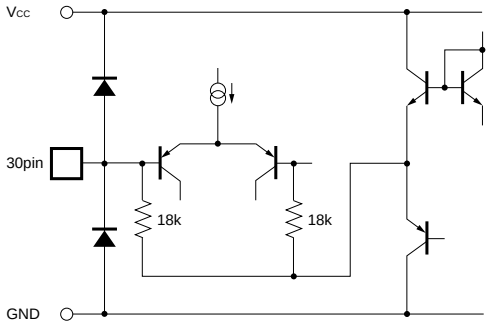
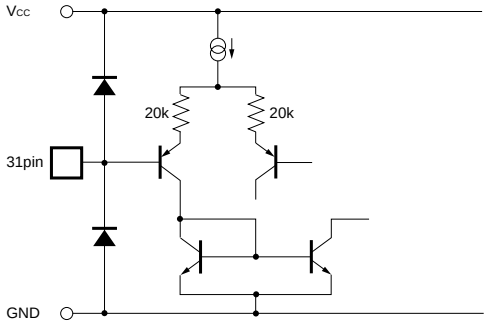
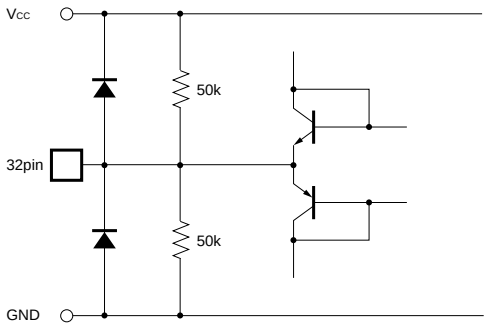
The terminal voltage shall be on when the data 0V volume=minimum, tone=flat, BBE=OFF, surround=OFF and AGC=OFF after the power supply Vcc=9.0(V) has been turned on, and any external devices shall comply with the measurement circuit diagram.

Pin. No	Pin name	Terminal voltage	Equivalent circuit	Description
2	LS1	0V		Terminal to set a time constant at a side for suppressing a signal level of AGC.
3	LS2	0V		Terminal to set a time constant at a side for amplifying a signal level of AGC.
4	SOUT	4.5V		Terminal for output of surround and pseudo stereo and to set a frequency characteristic.
5 28	IN2 IN1	4.5V		Terminal for sound signal input.

Pin. No	Pin name	Terminal voltage	Equivalent circuit	Description
6 27	BBASA2 BBASA1	4.5V		Terminal to set a contour frequency of BBE.
7 26	BBASB2 BBASB1	4.5V		Terminal to set a contour frequency of BBE.
8 25	BTREA2 BTREA1	4.5V		Terminal to set a process frequency of BBE.
9 24	BTREB2 BTREB1	4.5V		Terminal to set a process frequency of BBE.

Pin. No	Pin name	Terminal voltage	Equivalent circuit	Description
10 23	BAS2 BAS1	4.5V		Terminal to the cutoff frequency of bass tone control.
11 22	TRE2 TRE1	4.5V		Terminal to the cutoff frequency of treble tone control.
12 21	OUT2 OUT1	4.5V		Terminal for sound signal output.
13 20	VC2 VC1	0V		Terminal equipped with an external circuit to prevent a shock sound upon volume switching.

Pin. No	Pin name	Terminal voltage	Equivalent circuit	Description
14 19	TC BC	1.94V		Terminal equipped with an external circuit to prevent a shock sound upon tone switching.
16	CHIP	–		Chip select terminal.
17	SCL	–		Clock input terminal for I²C BUS controller.
18	SDA	–		Data input terminal for I²C BUS controller.

Pin. No	Pin name	Terminal voltage	Equivalent circuit	Description
29	PS1	4.5V		Terminal to set the 1st phase shift.
30	PS2	4.5V		Terminal to set the 2nd phase shift.
31	AGCADJ	–		Terminal to set the cut levle of AGC.
32	FILTER	4.5V		Filter terminal.

●**Electrical characteristics**

(unless otherwise noted, Ta=25°C, V_{CC}=9V, f=1kHz, BW=20kHz, VOL=MAX, surround = OFF, TONE=FLAT, AGC=OFF, BBE=OFF, AGCADJ=3.45V, R_R=600Ω, R_L=10kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current upon no signal	I_Q	–	30	45	mA	No signal
Maximum input	V_{IM}	2.8	3.0	–	Vrms	THD=1%, VOL=–20dB (ATT)
Maximum output	V_{OM}	2.2	2.5	–	Vrms	THD=1%
Voltage gain	G_V	–1.5	0	1.5	dB	V_{IN}=1Vrms
Maximum attenuation	ATT	90	110	–	dB	V_{IN}=1Vrms
Cross-talk	V_{CT}	70	80	–	dB	V_{IN}=1Vrms
Bass control range	VBMax.	12	15	18	dB	100Hz, V_{IN}=100mVrms
	VBMin.	–18	–15	–12	dB	100Hz, V_{IN}=100mVrms
Treble control range	VTMax.	12	15	18	dB	10kHz, V_{IN}=100mVrms
	VTMin.	–18	–15	–12	dB	10kHz, V_{IN}=100mVrms
Surround effect control range	G_{SR}	7	10	13	dB	V_{IN}=1Vrms
BBE Contour control range	G_{PS}	9	10	11	dB	100Hz, V_{IN}=100mVrms
BBE Process control range	G_{PH}	9	10	11	dB	10kHz, V_{IN}=100mVrms
AGC I/O level 1	A_{GC1}	0.7	1.0	1.4	mVrms	V_{IN}=1.0mVrms
AGC I/O level 2	A_{GC2}	50	75	100	mVrms	V_{IN}=50mVrms
AGC I/O level 3	A_{GC3}	150	200	250	mVrms	V_{IN}=200mVrms
AGC I/O level 4	A_{GC4}	200	280	360	mVrms	V_{IN}=1.0Vrms
Total harmonic distortion	THD	–	0.01	0.1	%	V_O=0.5Vrms, BPF=400Hz~30kHz
Output noise voltage	V_{NO1}	–	48	75	μVrms	No signal, VOL=Max. Rg=0 ＊
Residual output noise voltage	VM_{NO}	–	2.5	10	μVrms	No signal, VOL=–∞, Rg=0 ＊
Channel balance	G_{CA}	–1.5	0	1.5	dB	Measured based on CH1.
Input impedance	R_{IN}	20	30	40	kΩ	f=1kHz
Output impedance	R_{OUT}	–	–	10	Ω	f=1kHz
Ripple rejection	RR	40	–	–	V	f=100Hz, V_{RR}=100mVrms
Input voltage "H"	V_{IH}	3	5	5.5	V	SCL, SDA
Input voltage "L"	V_{IL}	–0.5	0	1.5	V	SCL, SDA

＊ Measured by VP-9690A of Matsushita (detection of mean value and indication of root-mean-value).
◎ Radiation resistance is not included in the design.
◎ The I/O phase of signal is the same.

●Control signal specification

(1) Electrical specifications and timing for bus lines and I/O stages

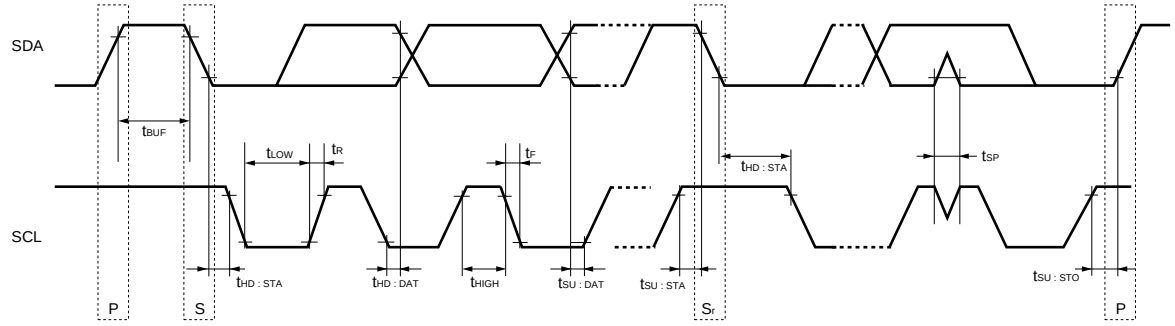


Fig.1 Definition of timing on the I²C BUS

Table B Characteristics of the SDA and SCL bus lines for I²C BUS devices

Parameter	Symbol	Min.	Max.	Unit
SCL clock fequency	f_{SCL}	0	100	kHz
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD\ ;\ STA}$	4.0	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	µs
Set-up time for a repeated START condition	$t_{SU\ ;\ STA}$	4.7	–	µs
Data hold time	$t_{HD\ ;\ DAT}$	0*	–	µs
Data set-up time	$t_{SU\ ;\ DAT}$	250	–	ns
Rise time of both SDA and SCL signals	t_R	–	1000	ns
Fall time of both SDA and SCL signals	t_F	–	300	ns
Set-up time for STOP condition	$t_{SU\ ;\ STO}$	4.0	–	µs
Capacitive load for each bus line	Cb	–	400	pF

All values referred to $V_{IH\ min.}$ and $V_{IL\ max.}$ Levels (see Table C).

* A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ min.}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

Table C Characteristics of the SDA and SCL I/O stages for I^2C BUS devices

Parameter	Symbol	Min.	Max.	Unit
LOW level input voltage :				
fixed input levels	V_{IL}	–0.5	1.5	V
V_{DD}-related input levels		(–0.5)	(0.3 V_{DD})	
HIGH level input voltage :				
fixed input levels	V_{IH}	3.0	∗1	V
V_{DD}-related input levels		(0.7 V_{DD})	(∗1)	
Hysteresis of Schmitt trigger inputs :				
Fixed input levels	V_{hys}	n/a	n/a	V
V_{DD}-related input levels		(n/a)	(n/a)	
Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	n/a	n/a	ns
LOW level output voltage (open drain or open collector) :				
at 3mA sink current	V_{OL1}	0	0.4	V
at 6mA sink current	(V_{OL2})	(n/a)	(n/a)	
Output fall time from $V_{IH\ min.}$ to $V_{IL\ max.}$ with a bus capacitance from 10pF to 400pF :				
with up to 3mA sink current at V_{OL1}	t_{OF}	–	250∗2	ns
with up to 6mA sink current at V_{OL2}		(n/a)	(n/a)	
Input current each I/O pin with an input voltage between 0.4V and 0.9 $V_{DDmax.}$	I_I	–10	10	μA
Capacitance for each I/O pin.	C_I	–	10	pF

n/a = not applicable

∗1 maximum V_{IH}=$V_{DDmax.}$ + 0.5V

∗2 Cb=capacitance of one bus line in pF. Note that the maximum t_F for the SDA and SCL bus lines quoted in Table B (300ns) is longer than the specified maximum t_{OF} for the output stages (250ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.1 without exceeding the maximum specified t_F.

The above-mentioned characteristics are theoretical values based on IC design and the delivery inspection does not guarantee anything. If any trouble is made, we will take necessary arrangements and actions in our faith.

(2) I^2C BUS format

- S =Start condition (Recognition of start bit)
- Slave Address =Recognition of IC. The high order 7 bits are optional. The least significant bit is “L” for writing.
- A =Acknowledge bit (Recognition of acknowledgement)
- Select Address =Selection of 1ch volume, 2ch volume, BBE effect, bass+BBE, treble+MUTE and AGC+matrix surround.
- Data =Data on volume and tone.
- P =Stop condition (Recognition of stop bit)

Slave Address of BH3868BFS

Fixing 16pin to Vcc

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	R / W
1	0	0	0	0	0	1	0

Making 16pin OPEN

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	R / W
1	0	0	0	0	0	0	0

(3) Setting of Select Address

	Parameter	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
0	1ch Volume	0	0	0	0	0	0	0	0
1	2ch Volume	0	0	0	0	0	0	0	1
2	BBE Processor	0	0	0	0	0	0	1	0
3	BBE, Bass	0	0	0	0	0	0	1	1
4	MUTE, Treble	0	0	0	0	0	1	0	0
5	AGC, Surround	0	0	0	0	0	1	0	1

Upon transferring consecutive data, the select address circulates because of the automatic increment function as follows:

0→1→2→3→4→5

The circulation starts from the select address specified first.

It doesn't patrol from selection address 5 to selection address 0.

(4) Data Configuration

	Parameter	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
0	1ch Volume	1ch Volume							
1	2ch Volume	2ch Volume							
2	BBE Processor	Process				Contour			
3	BBE, Bass	BBE	Bass						
4	MUTE, Treble	MUTE	Treble						
5	AGC, Surround	AGC	SON	SSTE	SMON	LOOP	Surround Effect		

Volume : all H : ATT 0dB
all L : ATT -∞dB

BBE Processor : all H : Max.
all L : Min.

Bass / Treble : all H : Max.
all L : Min.

Surround Effect : all H : Max.
all L : Min.

BBE : H : ON L : OFF
AGC : H : ON L : OFF(AGC : Auto Gain Control)
MUTE : H : ON L : OFF
LOOP : H : ON L : OFF(LOOP : surround effect enhanceer)
SSTE : H : ON L : OFF(SSTE : Surround STEreo)
SMON : H : ON L : OFF(SMON : Surround MONoral)
SON : H : ON L : OFF(SON : Surround ON)

Note : It is advisable to apply MUTE upon switching the mode and gain of BBE and SURROUND.

Volume Gain setting list

Gain (dB)	Hex. Notation	D7	D6	D5	D4	D3	D2	D1	D0
0	FFH	1	1	1	1	1	1	1	1
–1	EAH	1	1	1	0	1	0	1	0
–2	DFH	1	1	0	1	1	1	1	1
–3	D6H	1	1	0	1	0	1	1	0
–4	CFH	1	1	0	0	1	1	1	1
–5	C8H	1	1	0	0	1	0	0	0
–6	C2H	1	1	0	0	0	0	1	0
–7	B9H	1	0	1	1	1	0	0	1
–8	B8H	1	0	1	1	1	0	0	0
–9	B3H	1	0	1	1	0	0	1	1
–10	AEH	1	0	1	0	1	1	1	0
–11	AAH	1	0	1	0	1	0	1	0
–12	A6H	1	0	1	0	0	1	1	0
–13	A2H	1	0	1	0	0	0	1	0
–14	9EH	1	0	0	1	1	1	1	0
–15	9AH	1	0	0	1	1	0	1	0
–16	96H	1	0	0	1	0	1	1	0
–17	93H	1	0	0	1	0	0	1	1
–18	90H	1	0	0	1	0	0	0	0
–19	8CH	1	0	0	0	1	1	0	0
–20	89H	1	0	0	0	1	0	0	1
–22	83H	1	0	0	0	0	0	1	1
–24	7DH	0	1	1	1	1	1	0	1
–26	78H	0	1	1	1	1	0	0	0
–28	72H	0	1	1	1	0	0	1	0
–30	6DH	0	1	1	0	1	1	0	1
–32	68H	0	1	1	0	1	0	0	0
–34	64H	0	1	1	0	0	1	0	0
–36	5FH	0	1	0	1	1	1	1	1
–38	5BH	0	1	0	1	1	0	1	1
–40	57H	0	1	0	1	0	1	1	1
–42	52H	0	1	0	1	0	0	1	0
–44	4FH	0	1	0	0	1	1	1	1
–46	4BH	0	1	0	0	1	0	1	1
–48	47H	0	1	0	0	0	1	1	1
–50	42H	0	1	0	0	0	0	1	0
–52	40H	0	1	0	0	0	0	0	0
–54	3DH	0	0	1	1	1	1	0	1
–56	3AH	0	0	1	1	1	0	1	0
–58	37H	0	0	1	1	0	1	1	1
–60	34H	0	0	1	1	0	1	0	0

Gain (dB)	Hex. Notation	D7	D6	D5	D4	D3	D2	D1	D0
–62	32H	0	0	1	1	0	0	1	0
–64	2FH	0	0	1	0	1	1	1	1
–66	2DH	0	0	1	0	1	1	0	1
–68	2AH	0	0	1	0	1	0	1	0
–70	28H	0	0	1	0	1	0	0	0
–72	26H	0	0	1	0	0	1	1	0
–74	24H	0	0	1	0	0	1	0	0
–76	22H	0	0	1	0	0	0	1	0
–78	20H	0	0	1	0	0	0	0	0
–80	1EH	0	0	0	1	1	1	1	0
–82	1DH	0	0	0	1	1	1	0	1
–84	1BH	0	0	0	1	1	0	1	1
–∞	00H	0	0	0	0	0	0	0	0

Treble / Bass setting list

Treble Gain

Gain (dB)	Hex. Notation	D6	D5	D4	D3	D2	D1	D0
+15	7FH	1	1	1	1	1	1	1
+15	3FH	0	1	1	1	1	1	1
+14	36H	0	1	1	0	1	1	0
+12	32H	0	1	1	0	0	1	0
+10	2FH	0	1	0	1	1	1	1
+8	2DH	0	1	0	1	1	0	1
+6	2BH	0	1	0	1	0	1	1
+4	29H	0	1	0	1	0	0	1
+2	26H	0	1	0	0	1	1	0
0	20H	0	1	0	0	0	0	0
–2	1AH	0	0	1	1	0	1	0
–4	17H	0	0	1	0	1	1	1
–6	15H	0	0	1	0	1	0	1
–8	13H	0	0	1	0	0	1	1
–10	11H	0	0	1	0	0	0	1
–12	0EH	0	0	0	1	1	1	0
–14	0AH	0	0	0	1	0	1	0
–15	00H	0	0	0	0	0	0	0

Bass Gain

Gain (dB)	Hex. Notation	D6	D5	D4	D3	D2	D1	D0
+15	7FH	1	1	1	1	1	1	1
+15	3FH	0	1	1	1	1	1	1
+14	36H	0	1	1	0	1	1	0
+12	32H	0	1	1	0	0	1	0
+10	2FH	0	1	0	1	1	1	1
+8	2DH	0	1	0	1	1	0	1
+6	2BH	0	1	0	1	0	1	1
+4	29H	0	1	0	1	0	0	1
+2	26H	0	1	0	0	1	1	0
0	20H	0	1	0	0	0	0	0
−2	1AH	0	0	1	1	0	1	0
−4	17H	0	0	1	0	1	1	1
−6	15H	0	0	1	0	1	0	1
−8	13H	0	0	1	0	0	1	1
−10	11H	0	0	1	0	0	0	1
−12	0EH	0	0	0	1	1	1	0
−14	0AH	0	0	0	1	0	1	0
−15	00H	0	0	0	0	0	0	0

BBE Gain
Process

Gain (dB)	Hex. Notation	D7	D6	D5	D4
10.0	FH	1	1	1	1
9.0	EH	1	1	1	0
8.0	DH	1	1	0	1
7.0	CH	1	1	0	0
6.0	BH	1	0	1	1
5.5	AH	1	0	1	0
5.0	9H	1	0	0	1
4.5	8H	1	0	0	0
4.0	7H	0	1	1	1
3.5	6H	0	1	1	0
3.0	5H	0	1	0	1
2.5	4H	0	1	0	0
2.0	3H	0	0	1	1
1.5	2H	0	0	1	0
1.0	1H	0	0	0	1
0.5	0H	0	0	0	0

Contour

Gain (dB)	Hex Notation	D3	D2	D1	D0
10.0	FH	1	1	1	1
9.0	EH	1	1	1	0
8.0	DH	1	1	0	1
7.0	CH	1	1	0	0
6.0	BH	1	0	1	1
5.5	AH	1	0	1	0
5.0	9H	1	0	0	1
4.5	8H	1	0	0	0
4.0	7H	0	1	1	1
3.5	6H	0	1	1	0
3.0	5H	0	1	0	1
2.5	4H	0	1	0	0
2.0	3H	0	0	1	1
1.5	2H	0	0	1	0
1.0	1H	0	0	0	1
0.5	0H	0	0	0	0

Surround Gain setting list

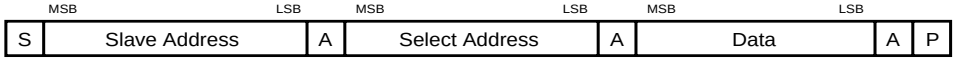
Gain (dB)	Hex. Notation	D2	D1	D0
10	7H	1	1	1
9	6H	1	1	0
8	5H	1	0	1
7	4H	1	0	0
6	3H	0	1	1
5	2H	0	1	0
4	1H	0	0	1
3	0H	0	0	0

Reference value : The setting table is a reference value persistently and the sctual use condition sometimes changes the gain of volume, the tone, surround.
In case of data setting, we request confirmation.

(5) Notes on Data Transfer

This IC is equipped with the automatic increment function to improve the rate of data transfer. In addition to the data format shown in the under-mentioned Basic Format, the other data format Automatic Increment is also available for the data transfer.

1) Basic format



2) Automatic Increment (The Select Address is incremented (by one) according to the number of data.)

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data1, Data2, · · · · ·, DataN	A	P

Example : <1> Data 1 shall be set as the data of the address specified by the Select Address.
<2> Data 2 shall be set as the data of the address specified by the Select Address +1.
<3> Data N shall be set as the data of the address specified by the Select Address +N–1.

3) Configuration Unavailable for Transfer (In this case, the Select Address 1 only is set.)

	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	Select Address 2	A	Data	A	P

Note : If any data is sent as the Select Address 2 immediately after the Data, such data is recognized as the Data, not the Select Address 2.

●AGC

(1) Level Setting

The AGC suppression level can be set by the voltage of the AGDADJ terminal (31pin). Assuming that the suppression level is GC (mVrms) and the AGCADJ voltage is ADJ (V), setting can be expressed as follows:

GC=–286×ADJ+1186

The under-mentioned table shows a guideline of setting.

Suppression Level (mVrms)	AGCADJ Terminal Voltage (V)
100	3.8
200	3.45
300	3.1
400	2.75

The level specified by the electrical characteristic is AGCADJ=3.45 (V) and the suppression level is approximately 200 (mVrms). Use the suppression level in a rage from 100 (mVrms) to 400 (mVrms). The under-mentioned chart shows the characteristic when the suppression level is set to 100 (mVrms), 200 (mVrms), 300 (mVrms) and 400 (mVrms).

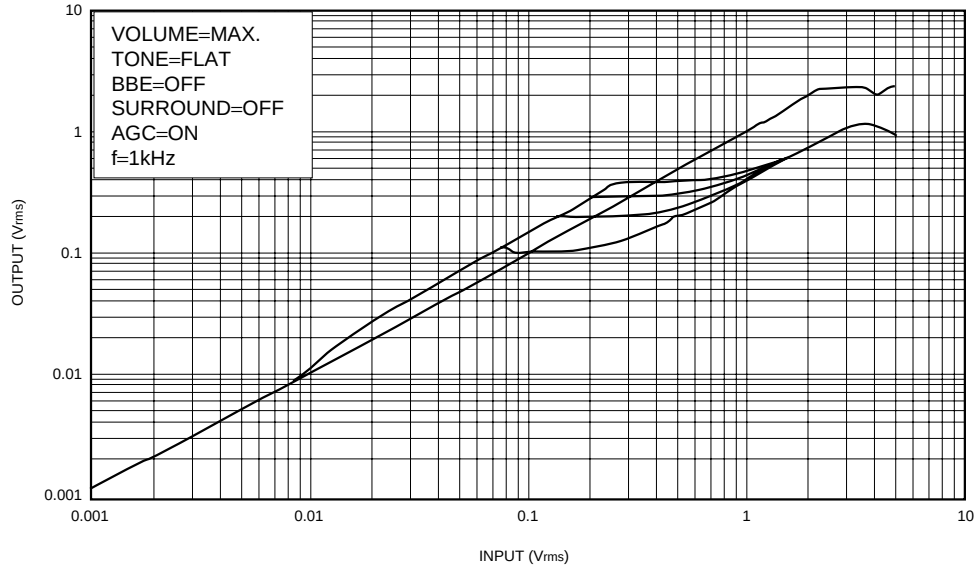
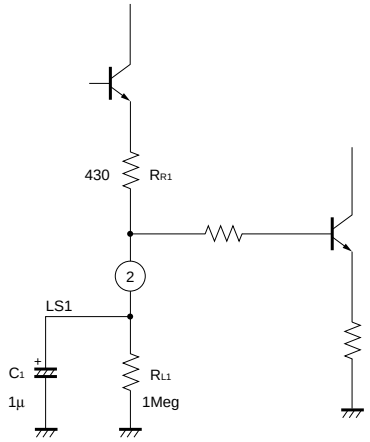


Fig.2 AGC characteristics

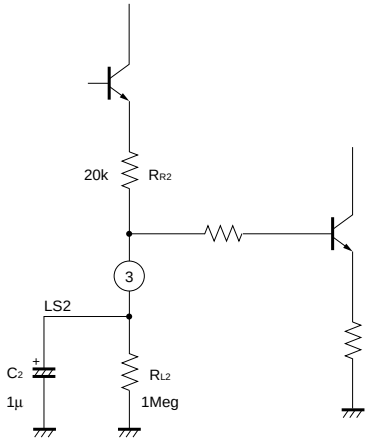
(2) Setting of Attack Time and Release Time

In this IC, the Attack Time and Release Time can be set in the boost side and cut side of AGC separately.



Detector circuit of suppression

- Attack Time : $R_{R1} \times C_1$
- Recovery Time : $R_{L1} \times C_1$



Detector circuit of amplification

- Attack Time : $R_{R2} \times C_2$
- Recovery Time : $R_{L2} \times C_2$

The Attack Time and Recovery Time shall be set by a resistor in IC and external capacitor and resistor. The internal resistance is R_{R1}=430Ω and R_{R2}=20KΩ (Typ).

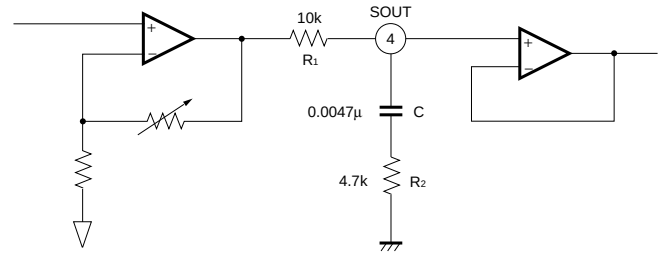
If the constant of capacitor C_2 of LS2 decreases, an amplification starting point is shifted in a direction of smaller input voltage. Moreover, the distortion rate also changes and becomes worse.

If the constant of capacitor C_1 of LS1C_1 decreases, the distortion rate becomes worse. If the resistance value of R_{L1} increases, the suppression is reduced.

●SURROUND

(1) Setting of Frequency Characteristic

This IC has an output terminal (4pin) for the surround signal. The surround characteristic can be varied by adding an appropriate filter to this terminal. An example of characteristic that low-pass filter has been set is shown below :



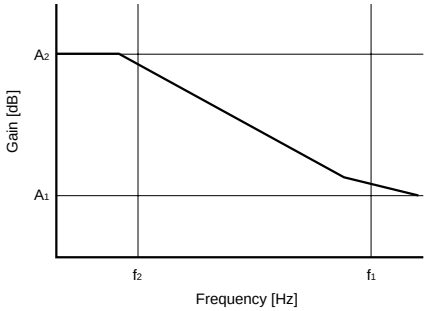
An amplifier to define the sound effect.

$$f_1 = \frac{1}{2\pi C R_2}$$

$$f_2 = \frac{1}{2\pi C(R_1 + R_2)}$$

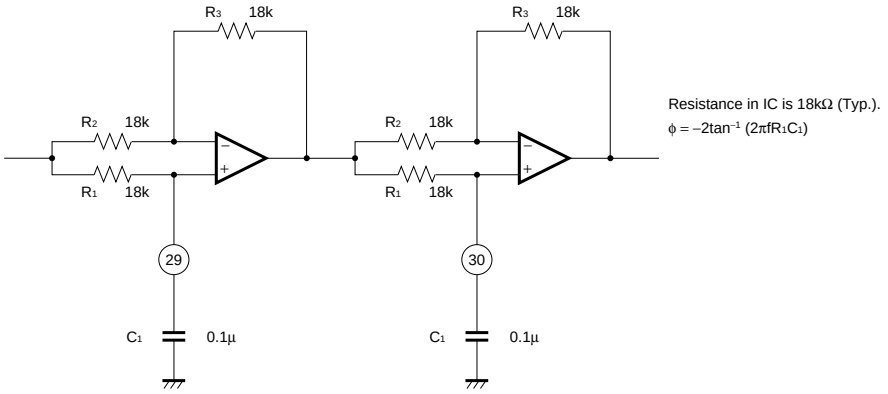
$$A_1 = \frac{R_2}{R_1 + R_2}$$

$$A_2 = 1$$



(2) Setting of Phase Shifter

This IC contains two stages of phase shifters. If none of two stages of phase shifters are not used, the pseudo-stereo function is also unavailable. If only one of these phase shifters is used, the normal of pseudo stereo may be spoiled.



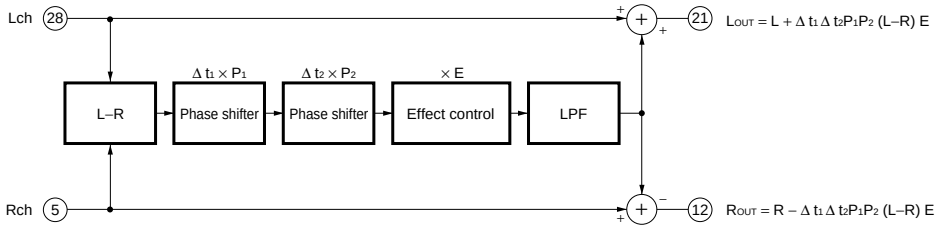
(3) Surround and Pseudo-Stereo Operation

$\Delta t_1 \Delta t_2$: Time delayed by a phase shifter

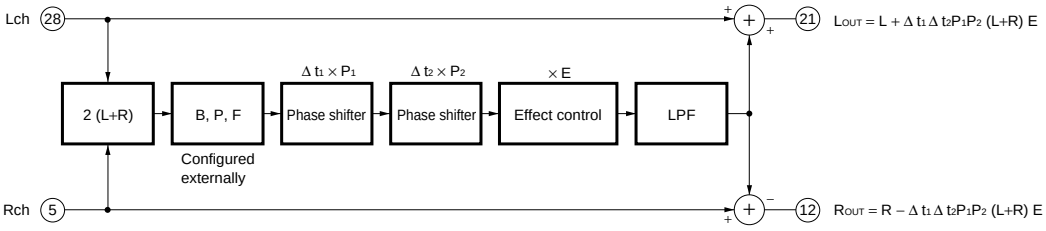
P_1 P_2 : Attenuation made by a phase shifter

E : Surround effect

1) Surround



2) Pseudo stereo



The above-mentioned figures show the block diagram of surround and pseudo stereo ICs. The characteristics of surround and pseudo stereo can be varied by changing the effect. Moreover, the number of states of phase shifters can be increased by turning on a switch of loop. However, an operation becomes unstable if the gain of effect is increased while the switch of loop remains turning on. Therefore, the effect should be approximately 6 dB. Upon switching the surround and pseudo stereo to each other, be sure to turn on a switch at the stereo surround side of SSTE to prevent a shock sound.

●BBE

This IC is equipped with BBE to achieve the clear sound. The characteristic can be changed by an external constant. If any constant other than recommendable ones is used, please ask BBE for confirmation.

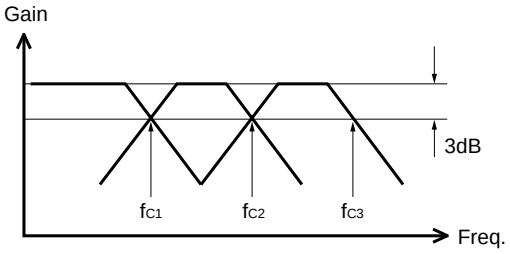
Frequency setting

$$f_{C1} = \frac{1}{2\pi \times 21.5k \times C1} = \frac{1}{2\pi \times 21.5k \times 0.033\mu} \fallingdotseq 224Hz$$

$$f_{C2} = \frac{1}{2\pi \times 21.5k \times C2} = \frac{1}{2\pi \times 21.5k \times 0.0033\mu} \fallingdotseq 2.24kHz$$

$$f_{C3} = \frac{1}{2\pi \times 21.5k \times C3} = \frac{1}{2\pi \times 56.2k \times 47p} \fallingdotseq 60.3kHz$$

C1=Capacity between 6pin–7pin, and 27pin–26pin.
C2=Capacity between 8pin–9pin, and 25pin–24pin.

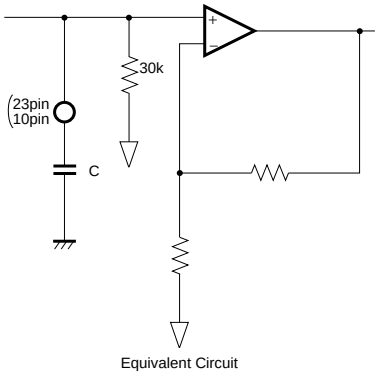


f_{C3} is fixed at the inside.

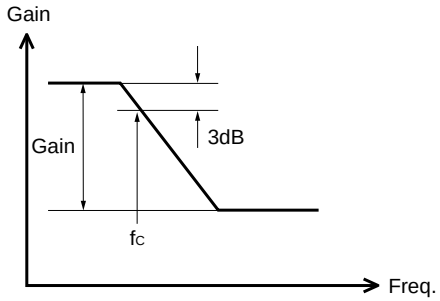
●Tone control

Setting of bass frequency

$$f_C = \frac{1}{2\pi \times 30k \times C} \text{ (Hz)}$$



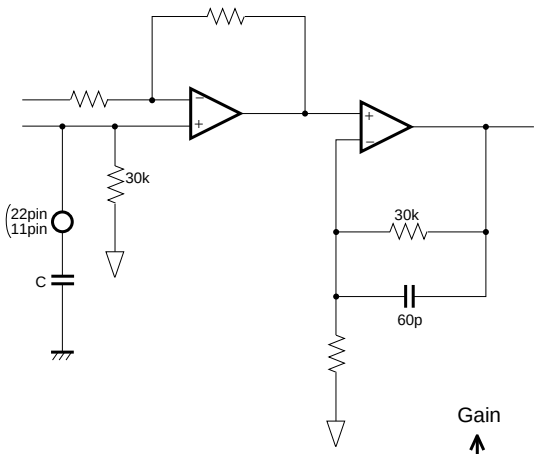
Equivalent Circuit



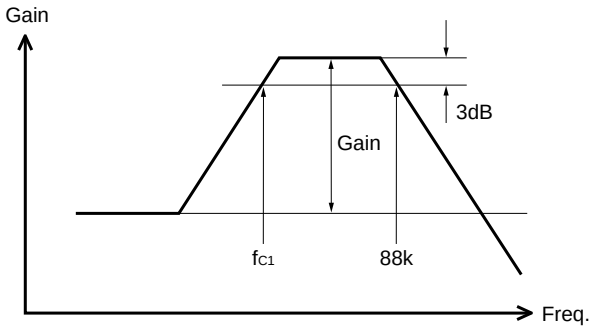
Setting of treble frequncy

$$f_{C1} = \frac{1}{2\pi \times 30k \times C} \text{ (Hz)}$$

$$f_{C2} = \frac{1}{2\pi \times 30k \times 60p} \fallingdotseq 88k \text{ (Hz)}$$



Equivalent Circuit



●**Application**

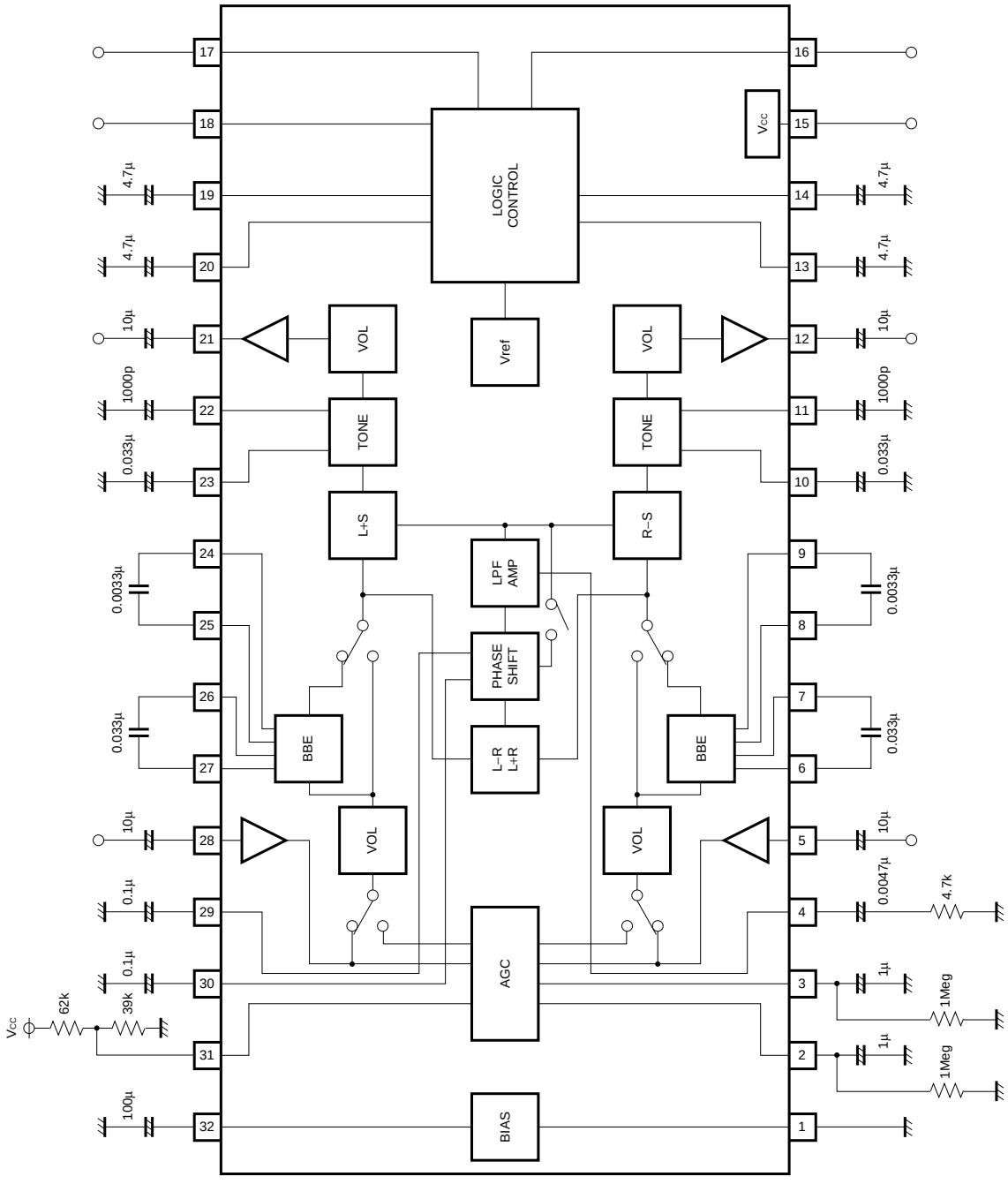


Fig.3

●**Electrical characteristics curve**

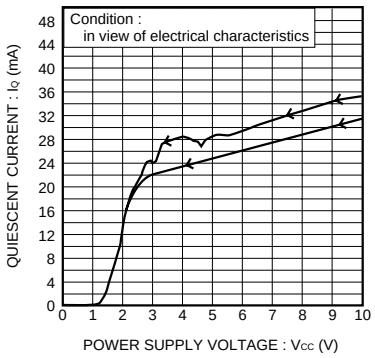


Fig.4 Quiescent current

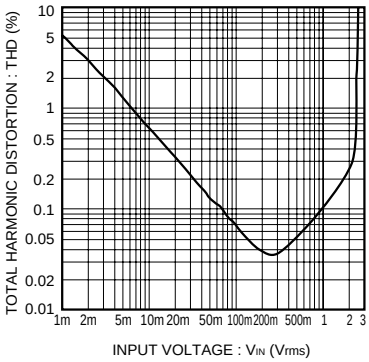


Fig.5 THD

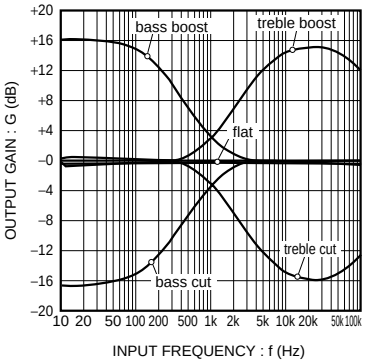


Fig.6 Tone frequency

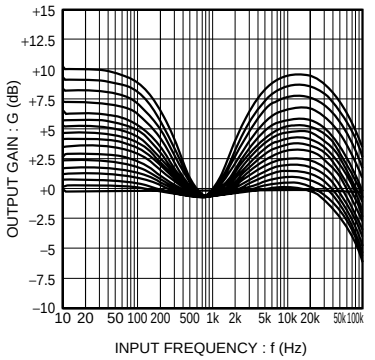


Fig.7 BBE frequency

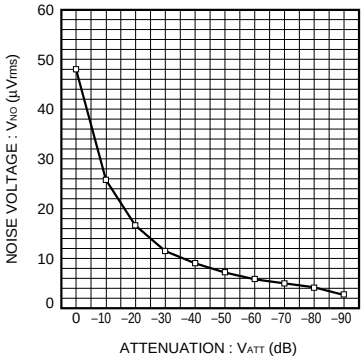


Fig.8 Noise level

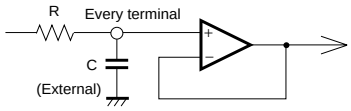
●**Operation notes**

1. We trust that an example of application circuits are recommendable and we would like to ask you to check the under-mentioned notes and the characteristics carefully. If you will modify and external circuit constant upon use, you should allow for not only static characteristics but also transient characteristics, unexpected variation of external components and our ICs.

2. Operating power supply voltage range
   Basic circuit function and operation can be guaranteed within the operating temperature range and within the operating power supply voltage range. Upon use, check those ranges carefully and specify the content, element, voltage and temperature.

3. Step switching noise

In an example of application circuit, an example of constant is set on VC1, VC2, TC and BC terminals. This constant varies depending on signal level setting, actual wiring pattern, etc. Specify each constant under careful study and examination. The internal equivalent circuit is shown below. (A primary integration circuit is set for gradual variation.)



	R value (kΩ)
VC1, VC2, TC, BC	30

4. Level setting of volume and tone

Attenuation to control serial data is stated as a reference value in our specifications.
An internal D/A converter is configured by the R-2R method and, therefore, there is any data also in an area in which some data are not consecutive. Use is for fine adjustment.
However, the volume must be within 8 bits (256 steps) and the tone must be 7 bits (64+1 steps).

5. I^2C BUS control

High-frequency digital signal is inputted into the SCL terminal and SDA terminal. Therefore, However, wire not to interfere any analog signal system line.

6. Power-on Reset

This IC contains a circuit for initialization when the power supply turns on. Every channel volume has been set to become −∞ when the power supply turns on. When the power supply is turned ON once and OFF and then ON again immediately, the said description may not be achieved if any load remains in a capacitor. In this case, apply muting until a command of I^2C BUS has been sent.

7. Capacitor of VREF (8pin)

100μF is recommended as the capacity of power supply filter attached to VREF. If this capacity is decreased, the maximum attenuation of volume is deteriorated and the cross-talk also tends to become worse. This IC contains a precharge circuit and discharge circuit for capacitor attached to VREF.

●BBE process

The BBE sound processor considers a loudspeaker and amplifier as total audio system, reproduces accurately “Rise of Sound” which characterizes the sound, by an appropriate signal processing at a stage before amplifier input, and makes the playback sound an original one as naturally as possible.

●Problem in Sound Reproduction with Audio System and BBE Process

In general, for the natural sound, treble harmonic element is generated first and then bass basic wave element is produced. This is the same with the attack part which shows the characteristics of various musical instruments. The amplitude element, which forms a frequency element and envelope at the rise of sound, expresses the character of the sound. Therefore, to reproduce any sound with a playback system, it is very important to express accurately the rise of sound against the original sound. However, there is unavoidable mismatch between a loudspeaker and amplifier of today's audio playback system.

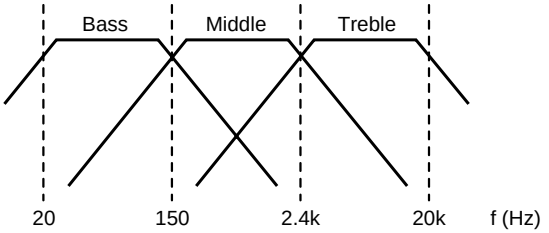
For example, a power amplifier with transistor operates as constant-voltage source, but mismatch cannot be avoided because one loudspeaker is a current element. Moreover, the impedance characteristic of loudspeaker is affected considerably by electric reactance of voice coil or mechanical reactance of cone assembly. As a result, the rise of sound is distorted and the phase of playback sound is deviated. Furthermore, due to the increase of treble impedance, the loudspeaker amplitude is reduced and the harmonic element is deteriorated. So the treble element is easy to be masked by a consequent middle tone element of high level, and the rise of sound is hard to be produced accurately.

BBE has been developed to solve those problems. BBE is a technology to reproduce the sound clearness more naturally by moving the delayed harmonic before the basic wave first to construct the same wave as that of the natural sound and then boosting slightly the treble which is easy to be attenuated. Because of the synergistic effect of phase correction and treble boost, the same clearness can be obtained by approximately half boost in comparison with a simple boost of equalizer. It has been ten years or more since BBE was introduced into many recording studios, PA, SR sites and broadcasting stations, and 100,000 or more units of BBE for professional have been using. BBE is designated by many musicians to improve the sound of vocal and musical instruments.

●Principle of Operation

To solve the problems in audio playback system mentioned in the previous page, the BBE processor processes a signal as follows:

●Phase Correction



By dividing the input signal to three frequency bands, "Bass" (20 to 150 Hz), "Middle" (150Hz to 2.4kHz) and "Treble" (2.4k to 20kHz), and by adding them again, the phase difference –360° in Treble and –180° in Middle against Base are generated. These phase differences adjusts the time delay characteristic in every frequency band and minimizes the distortion of the rise of sound.

●Revision of harmonic element

Gain is applied to Treble, because the harmonic element (Treble element), of which gain is expected to be deteriorated depending on the loudspeaker characteristic, must be enhanced. However, if Treble is clear, it may seem that Bass is insufficient. This can be corrected by applying the gain to Bass.

There are many audio system characteristics. The most suitable correction effect for your system can be obtained by BBE.

●License agreement about patent and trademark

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For such trademark and patent of BBE, please contact :

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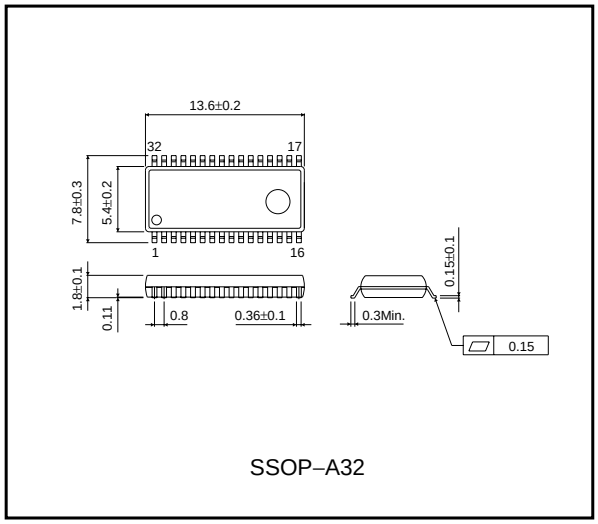
Fax:(714)896-0736

●External dimensions (Units : mm)



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