

# Read/Write Amplifier for FDD

## BH6629BFS

The BH6629BFS, a read/write IC designed for floppy disk drives, has a recording system that puts top priority on saddle margin. Offers multi-step switching of write current, while density and inner edge/outer edge are switched internally.

### ●Applications

Floppy disk drives (1MB and 2MB drives)

### ●Features

- 1) Internal active filter switch.
- 2) Time domain filter (with internal switching based on transfer rate).
- 3) Internal switching of write current density and inner track/outer track.

### ●Absolute maximum ratings (unless otherwise noted, Ta=25°C)

| Parameter             | Symbol           | Limits                    | Unit |
|-----------------------|------------------|---------------------------|------|
| Supply voltage        | V <sub>CC</sub>  | +7                        | V    |
| Operating temperature | T <sub>OPR</sub> | 0~+70                     | °C   |
| Storage temperature   | T <sub>STG</sub> | -55~+125                  | °C   |
| Digital input voltage | V <sub>I</sub>   | -0.5~V <sub>CC</sub> +0.3 | V    |
| RW pin voltage        | VRW              | +15                       | V    |
| LVS output voltage    | VLVS             | V <sub>CC</sub> +0.3      | V    |
| ED pin voltage        | VER              | V <sub>CC</sub> +0.3      | V    |
| Power dissipation     | PD               | 650*                      | mW   |

\* Reduced by 6.5mW for each increase in Ta of 1°C over 25°C.

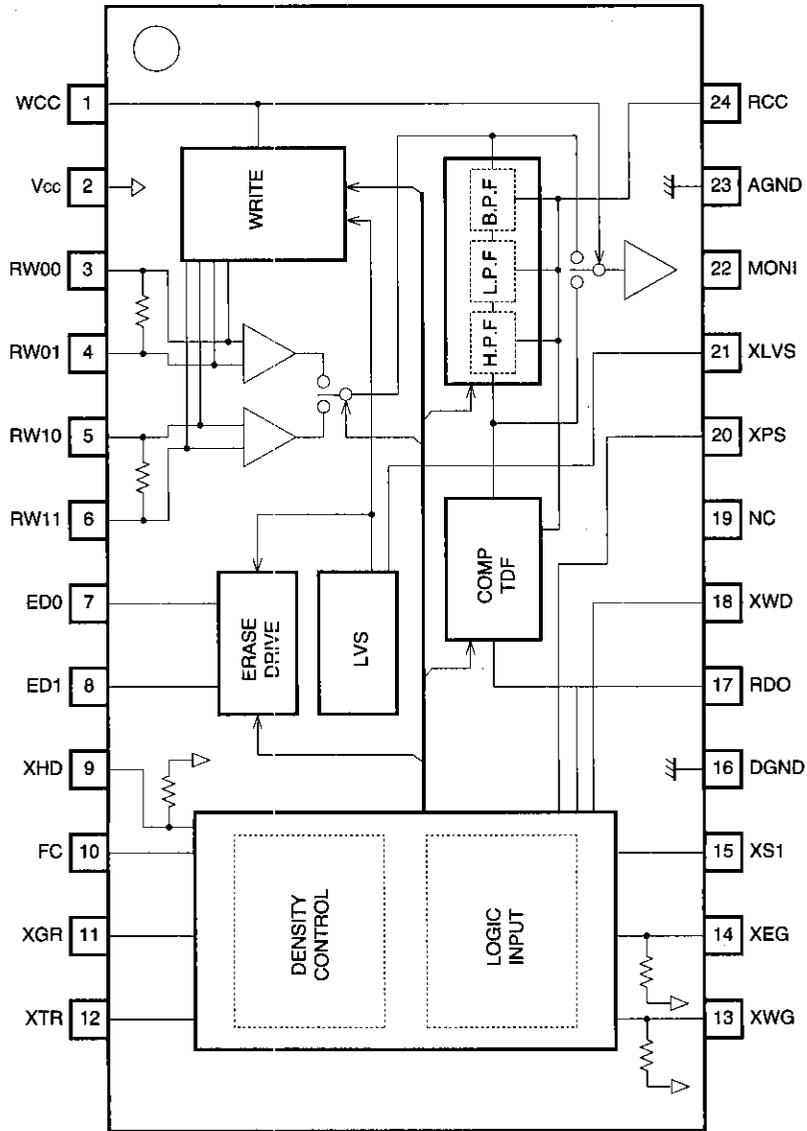
### ●Recommended operating conditions (Ta=25°C)

| Parameter            | Symbol          | Min. | Typ. | Max. | Unit |
|----------------------|-----------------|------|------|------|------|
| Power supply voltage | V <sub>CC</sub> | 4.5  | 5.0  | 5.5  | V    |

FDD read/write amplifier

FDD/HDD

● Block diagram



(Note) Use a short pattern for Vcc, and keep the impedance between Vcc and GND low by inserting a bypass capacitor.

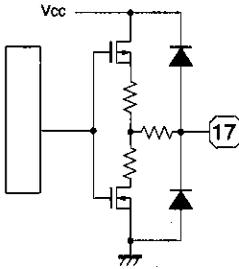
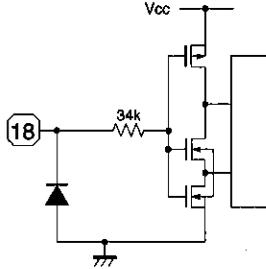
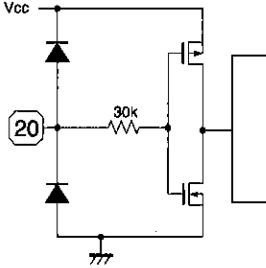
● Pin description

| Pin No | Name | Equivalent circuit | Function   |
|--------|------|--------------------|--|
| 1      | WCC  |                    | <p>For connecting the write current adjustment resistor</p> <p>Connect the write current adjustment resistor between this pin and Vcc.</p> <p>Setting this pin to the low level during reading switches MONI to differentiator output.</p> |
| 2      | Vcc  |                    | Power supply pin   |
| 3      | RW00 |                    | <p>Active when SIDE0 and the read/write head connecting pin (pin 15, XS1) is at the high level (side 0)</p> <p>Starts at RW00 during the start of writing (from reading to writing)</p>  |
| 4      | RW01 |                    | <p>Starts at RW01 during the start of writing (from reading to writing)</p>  |
| 5      | RW10 |                    | <p>Active when the read/write head connecting pin (pin 15, XS1) is at the low level (side 1)</p> <p>Starts at RW10 during the start of writing (from reading to writing)</p>   |
| 6      | RW11 |                    | <p>Starts at RW11 during the start of writing (from reading to writing)</p>  |
| 7      | ED0  |                    | Side 1 erase current sink  |
| 8      | ED1  |                    | Side 1 erase current sink  |

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| Number | Name | Equivalent circuit | Function  |
|--------|------|--------------------|---|
| 9      | XHD  |                    | 1 MB/2 MB selector<br>High=1MB<br>Low=2MB   |
| 10     | FC   |                    | Option 2 selector pin<br>Selector signal high level = active                              |
| 11     | XGR  |                    | Option mode selector pin<br>Controls the write current                                    |
| 12     | XTR  |                    | Inner edge/outer edge position setting<br>Controls the filter and write current           |
| 13     | XWG  |                    | Write enable gate (Schmidt input)<br>Low = active   |
| 14     | XEG  |                    | Erase enable gate (Schmidt input)<br>Low = active   |
| 15     | XS1  |                    | Head/side switching signal<br>Low = active (Schmidt input)<br>High = side 0, low = side 1 |

| Number | Name | Equivalent circuit   | Function  |
|--------|------|--|---|
| 16     | DGND |   | Digital ground  |
| 17     | RDO  |   | Read data output<br>TTL high level = active                     |
| 18     | XWD  |   | Write data input<br>Operates at falling edge<br>(Schmitt input) |
| 19     | NC   |   |   |
| 20     | XPS  |  | Power save selector<br>Low = active                             |

FDD read/write amplifier

FDD/HDD

| Pin No. | Name | Equivalent circuit | Function   |
|---------|------|--------------------|--|
| 21      | XLVS |                    | <p>External low level-voltage detection pin<br/>Open collector output when low level voltage is detected.<br/>Switches to low level when Vcc drops below the specified voltage</p> |
| 22      | MONI |                    | <p>Preamplifier output and differentiator output monitoring<br/>Monitor is switched with pin 1 (WCC)</p>   |
| 23      | AGND |                    | <p>Analog ground</p>   |
| 24      | RCC  |                    | <p>Filter (LPF, BPF) cutoff frequency and TDF first M/M pulse width setting resistor connection</p>  |

● Electrical characteristics (unless otherwise noted, Ta=25°C, Vcc=5V)

## Current consumption

| Parameter                    | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|--------|------|------|------|------|------------|
| Current consumption, Standby | ICCST  | —    | 190  | 400  | μA   | *1         |
| Current consumption, Read    | ICCR   | —    | 28   | 40   | mA   | *1         |
| Current consumption, Write   | ICCW   | —    | 8.5  | 15   | mA   | *2         |

\*1 RRCC=2.0 [kΩ] (XHD=H)

\*2 RWCC=2.4 [kΩ] (When 2MB inner track, XGR = "H", except IWR and IER)

## Low level voltage detection circuit

| Parameter                 | Symbol | Min. | Typ. | Max. | Unit | Conditions  |
|---------------------------|--------|------|------|------|------|---|
| Threshold voltage 1       | VTH1+  | —    | 4.05 | 4.3  | V    | When power supply voltage rises, internal LVS/ write protectect |
|                           | VTH1-  | 3.6  | 3.85 | 4.1  | V    | When power supply voltage falls, internal LVS/ write protectect |
| Threshold voltage 2       | VTH2+  | —    | 3.92 | 4.17 | V    | When supply voltage rises, external LVS                         |
|                           | VTH2-  | 3.47 | 3.72 | 3.97 | V    | When supply voltage falls, external LVS                         |
| Hysteresis voltage        | VH     | 50   | —    | —    | mV   |   |
| Output voltage, low level | VOL    | —    | —    | 0.40 | V    | Vcc=2.5[V] IOL=0.2[mA]  |
| Output leakage current    | IOH    | —    | —    | 10   | μA   |   |

## Recovery time

| Parameter       | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-----------------|--------|------|------|------|------|------------|
| POWER·SAVE→READ | TR2    | —    | —    | 500  | μs   | by XPS     |
| READ→ERASE      | TR3    | —    | —    | 6    | μs   | by XEG     |
| READ→WRITE      | TR4    | —    | —    | 4    | μs   | by XWG     |
| WRITE→READ      | TR5E   | —    | —    | 20   | μs   | by XEG     |
|                 | TR5W   | —    | —    | 160  | μs   | by XWG     |
| SIDE0↔SIDE1     | TR6    | —    | —    | 40   | μs   | by XS1     |
| 1MB↔2MB         | TR7    | —    | —    | 40   | μs   | by XHD     |

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## Preamplifier

| Parameter   | Symbol | Min. | Typ. | Max. | Unit  | Conditions  |
|---|--------|------|------|------|-------|---|
| Voltage gain 1  | GVD1   | 43   | 46   | 49   | dB    | f=125[kHz], VIN=2.5[mVp-p](differential)<br>(OPTION outer edge)                       |
| Voltage gain 2  | GVD2   | 46   | 49   | 52   | dB    | f=125[kHz], VIN=2.5[mVp-p](differential)<br>(1 MB/2 MB outer edge, OPTION inner edge) |
| Voltage gain 3  | GVD3   | 49   | 52   | 56   | dB    | f=125[kHz], VIN=1.5[mVp-p](differential)<br>(1 MB/2 MB inner edge)                    |
| SIDE0↔SIDE1<br>crosstalk                              | GCTLK  | 50   | —    | —    | dB    | f=125[kHz], VIN=100[mVp-p]<br>(differential) *3                                       |
| Differential input resistance                         | RID    | —    | 4    | —    | kΩ    | 8.0 kΩ input resistance //8.0 kΩ<br>damping resistance                                |
| Input conversion noise voltage                        | VN     | —    | 2.5  | 3.7  | μVrms | f=500[Hz] ~1 [MHz]  |
| Input sink current                                    | ISINK  | —    | 180  | —    | μA    |   |
| Differential input voltage<br>amplitude tolerance (1) | VIN    | —    | —    | 5.0  | mVp-p | 5% distortion (sinewave input)<br>(OPTION outer edge)                                 |
| Differential input voltage<br>amplitude tolerance (2) | VIN    | —    | —    | 3.5  | mVp-p | 5% distortion (sine wave input)<br>(1 MB/2 MB outer edge, OPTION inner edge)          |
| Differential input voltage<br>amplitude tolerance (3) | VIN    | —    | —    | 2.0  | mVp-p | 5% distortion (sine wave input)<br>(1 MB/2 MB, inner edge)                            |
| Common mode rejection ratio rejection                 | CMRR   | 50   | —    | —    | dB    | f=125[kHz], VIN=100[mVp-p] *3   |
| Supply voltage ratio<br>rejection                     | PSRR   | 40   | —    | —    | dB    | f=250[kHz], VIN=100[mVp-p] *3   |

## Preamplifier/LPF/differentiator (BPF)

| Parameter  | Symbol | Min. | Typ. | Max. | Unit | Conditions  |
|--|--------|------|------|------|------|---|
| Filter time constant accuracy                            | EFIL   | -10  | —    | +10  | %    | *3  |
| Total gain (preamplifier/<br>LPF/differentiator) (1)     | GVDD1  | 43.0 | 47.0 | 51.0 | dB   | f=250[kHz], VIN=2.5[mVp-p](differential)<br>(2 MB outer edge)     |
| Total gain (preamplifier/<br>LPF/differentiator) (2)     | GVDD2  | 44.0 | 48.0 | 52.0 | dB   | f=250[kHz], VIN=2.5[mVp-p](differential)<br>(2 MB inner edge)     |
| Total gain (preamplifier/<br>LPF/differentiator) (3)     | GVDD3  | 40.5 | 44.5 | 48.5 | dB   | f=250[kHz], VIN=2.5[mVp-p](differential)<br>(OPTION 2 outer edge) |
| Differentiator output peaking<br>frequency setting range | f0     | 0.1  | —    | 0.5  | MHz  | Defined according to typical value<br>in the settings             |

\*3 RRCC=2.0 [kΩ] (XHD=L, XTR=H, FC=L)

## Comparator and waveform shaping

| Parameter                        | Symbol | Min. | Typ. | Max. | Unit | Conditions   |
|----------------------------------|--------|------|------|------|------|--|
| TDF M/M pulse width accuracy (1) | TDF1   | -10  | -    | +10  | %    | 1MB (Typ. : 2545[ns] )<br>f=62.5[kHz]~125[kHz] *4        |
| TDF M/M pulse width accuracy (2) | TDF2   | -10  | -    | +10  | %    | 2MB, OPTION (Typ. : 1280[ns] )<br>f=125[kHz]~250[kHz] *4 |
| RD pulse width                   | TRD    | 270  | 400  | 530  | ns   | Determination level: 1.5 V                               |
| Rise time                        | TTLH   | -    | -    | 70   | ns   | Rise time between 0.4 V and 2.0 V                        |
| Fall time                        | TTHL   | -    | -    | 70   | ns   | Fall time between 2.0 V and 0.4 V                        |
| Peak shift                       | P. S.  | -    | -    | 1.0  | %    | f=250[kHz] , VIN=1[mVp-p] (differ.)                      |
| "L" output voltage               | VOL    | -    | -    | 0.5  | V    |  |
| "H" output voltage               | VOH    | 2.7  | -    | -    | V    | Level after 70 - ns rise from 0.4 V                      |

\*4 RWCC=2.0 [kΩ]

## Write circuit

| Parameter                                     | Symbol | Min.                 | Typ. | Max. | Unit  | Conditions                 |
|---|--------|----------------------|------|------|-------|----------------------------|
| Write current adjustment range                | IWR    | 2.0                  | -    | 20   | mA0-p |                            |
| Write current accuracy                        | ACIW   | -7.0                 | -    | +7.0 | %     | *5                         |
| Write current pairability                     | ΔIWR   | -1.0                 | -    | +1.0 | %     | RWCC=2.4[kΩ]               |
| Write current power supply voltage dependency | PSIW   | -4.0                 | -0.8 | +3.0 | %/V   | RWCC=2.4[kΩ]               |
| Output saturation voltage                     | VSATRW | -                    | 0.4  | 1.0  | V     | IWR=12[mA]                 |
| Off-state leak current                        | ILKRW1 | -                    | -    | 20   | μA    | Unselected side            |
|   | ILKRW2 | -                    | -    | 50   | μA    | Selected side              |
| Minimum write data pulse width                | TWD    | 70                   | -    | -    | ns    |                            |
| Write current switching ratio accuracy        | ACIWTR | ±10× (1 - set ratio) |      |      | %     | *6                         |
| Damping resistance accuracy                   | ACDR   | -25                  | -    | +25  | %     | Write (typically 8.0 [kΩ]) |

\*5 RWCC = 2.4 [kΩ], adapted for desired setting of XTR1/XTR2

\*6 Error in setting ratio (reference: 1 MB outer edge)

## Erase output

| Parameter                   | Symbol | Min. | Typ. | Max. | Unit | Conditions       |
|-----------------------------|--------|------|------|------|------|------------------|
| Erase current setting range | IER    | -    | -    | 40   | mA   |                  |
| Output saturation voltage   | VSATER | -    | 0.2  | 0.6  | V    | IER=40[mA]       |
| Output leakage current      | IOH    | -    | -    | 10   | μA   | Off, ED0=ED1=Vcc |

FDD read/write amplifier

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Logic input

| Parameter                | Symbol           | Min. | Typ. | Max. | Unit | Conditions   |
|--------------------------|------------------|------|------|------|------|--|
| "H" Input voltage        | V <sub>IH</sub>  | 2.0  | —    | —    | V    |  |
| "L" Input voltage        | V <sub>IL</sub>  | —    | —    | 0.8  | V    |  |
| Input voltage hysteresis | V <sub>H</sub>   | 0.15 | —    | —    | V    | Applies to XWD, XWG, XEG, XS1  |
| "L" Input current        | I <sub>IL1</sub> | —    | 50   | 100  | μA   | V <sub>CC</sub> =5[V] V <sub>IL</sub> =GND<br>Applies to XWG, XEG, XHD |

● Mode table

| Mode                          |                        | 1MB                  | 2MB           | OPTION1       | OPTION2       |             |               |               |     |  |
|-------------------------------|------------------------|----------------------|---------------|---------------|---------------|-------------|---------------|---------------|-----|--|
| Transfer rate                 |                        | 250[kbps]            | 500[kbps]     | 500[kbps]     | 500[kbps]     |             |               |               |     |  |
| Input                         | Mode                   | XHD                  | HI            | LOW           | HI            | NO CARE     |               |               |     |  |
|                               |                        | FC                   | LOW           | LOW           | LOW           | HI          |               |               |     |  |
|                               |                        | XGR                  | HI            | NO CARE       | LOW           |             |               |               |     |  |
| track                         | XTR (XSWF)             | Outer track          | Inner track   | Outer track   | Inner track   | Outer track | Inner track   |               |     |  |
|                               |                        | LOW                  | HI            | LOW           | HI            | LOW         | HI            | LOW           | HI  |  |
| Output                        | Preamplifier gain [dB] | 49                   | 52            | 49            | 52            | 46          | 49            | 46            | 49  |  |
|                               | Filter                 | f <sub>0</sub> [kHz] | 187           | 224           | 372           | 376         | 350           | 372           | 350 |  |
|                               |                        | Charac. (Q)          | C             | D             | D             | A           | C             | D             | C   |  |
|                               | TDF                    | [nSEC]               | 2545          |               | 1280          |             | 1280          |               |     |  |
| Write current switching ratio |                        | WCC                  | WCC<br>×0.733 | WCC<br>×0.433 | WCC<br>×0.318 | WCC         | WCC<br>×0.733 | WCC<br>×0.733 |     |  |

Note) \* 1 (A) Butterworth characteristics (C) Option characteristics (D) Refer to low-Q Butterworth characteristics, filter characteristics (However, RRCC=2.0 [kΩ] )

Total filter peak frequency setting

$$f_0 = a / (RRCC [k\Omega] + 0.09) [kHz]$$

- a = 391 1M outer track
- 468 1M inner track
- 777 2M outer track
- 786 2M inner track
- 732 outer track (with OPTION 1), OPTION 2
- 777 inner track (with OPTION 1)

TDF time constant setting

$$250 [kbps] : T = 939 \times RRCC [k\Omega] + 667 [ns]$$

$$500 [kbps] : T = 403 \times RRCC [k\Omega] + 474 [ns]$$

Write current setting

$$I_{wr} = \frac{24.0}{RWCC [k\Omega]} [mA]$$

● Filter characteristic

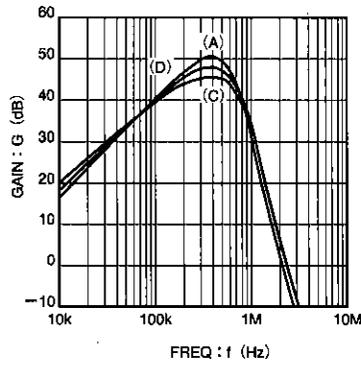
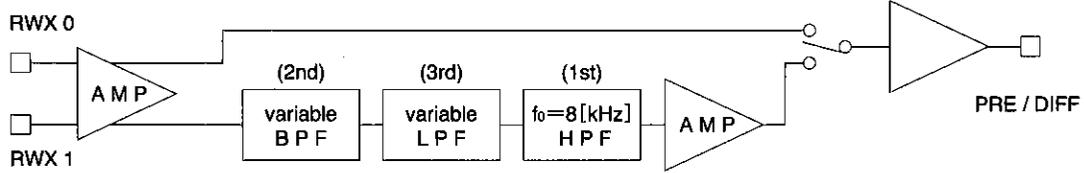
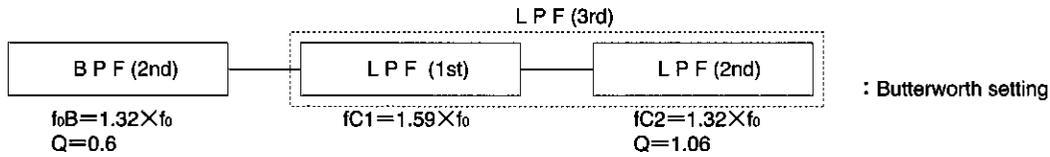


Fig. 1 PRE IN vs. DIFF OUT characteristics

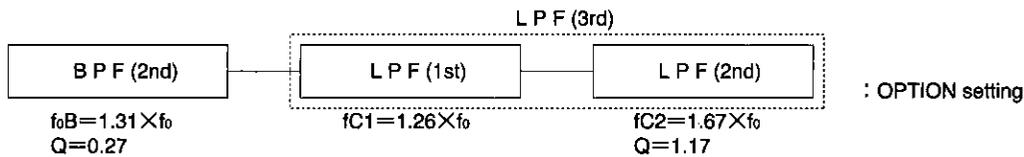
Preampifier — differentiator(B.P.F)— L.P.F



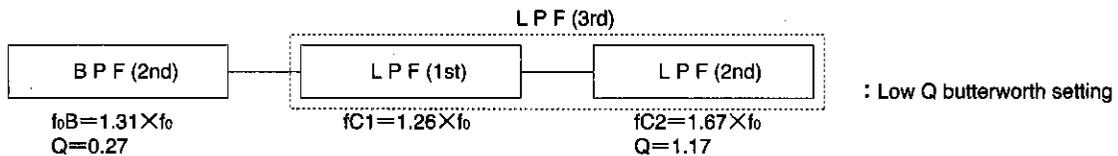
A. Total characteristic peak frequency ( $f_0$ ): 1MB, 2MB inner edge,



C. Total characteristic peak frequency ( $f_0$ ): OPTION1 outer edge, OPTION2



D. Total characteristic peak frequency ( $f_0$ ): 1MB, 2MB outer edge, OPTION1 inner edge



FDD read/write amplifier

FDD/HDD

● Measurement circuit

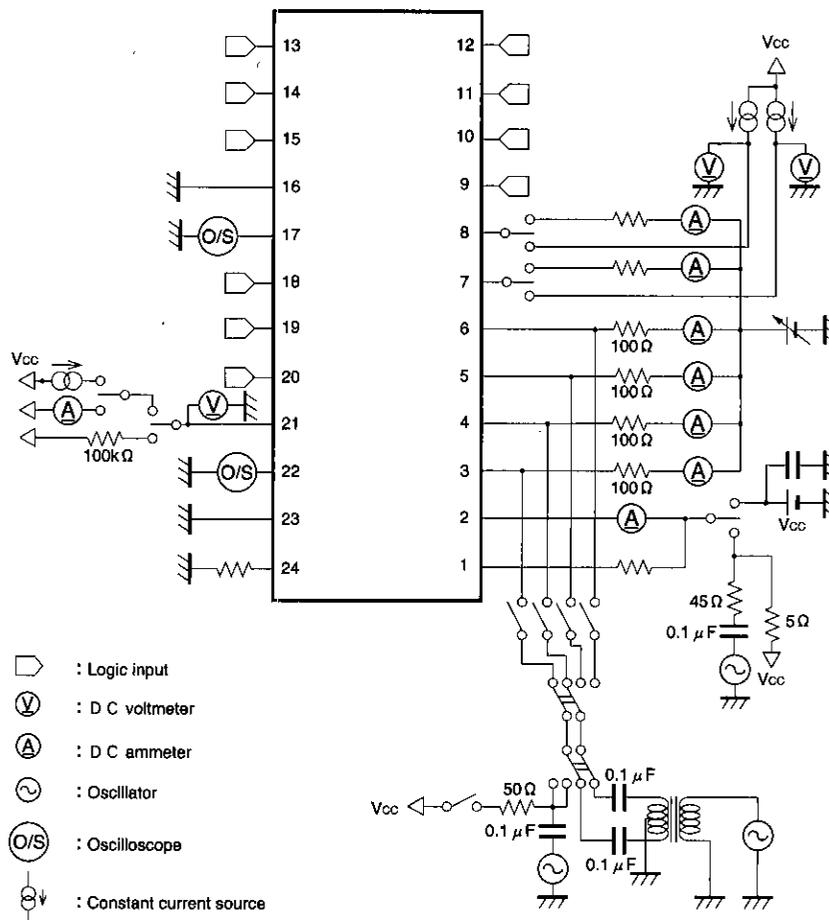


Fig. 2

● Circuit operation

(1) Read

The input signal from the head coils from each side of the disc is amplified by the preamplifier and then differentiated. The filter time constant can be set externally. After differentiation, the differential output is input to the comparator. The time domain filter detects zero cross, and the output is converted to read data. The monostable multivibrator width can be set externally, while the read data pulse width is a constant 400ns.

(2) Write

Input write data are converted to toggle movements by the internal flip-flops, operating the write driver. The

write driver current is supplied by the write current generator, but the externally set current can be controlled according to density and by selecting inner track/outer track.

(3) Erase

An open collector output pin is used, and the erase current is set with a resistor between it and the head.

(4) Power supply

When the low level voltage detector detects a drop in the supply voltage, writing and erasing are prohibited.

● Operation notes

- Use a short pattern for  $V_{CC}$ , and a sufficiently wide AGND and DGND. Keep the impedance between  $V_{CC}$  and GND low by inserting a bypass capacitor.
- Use a pattern that will minimize interference between digital signals and the head.

● Electrical characteristic curves

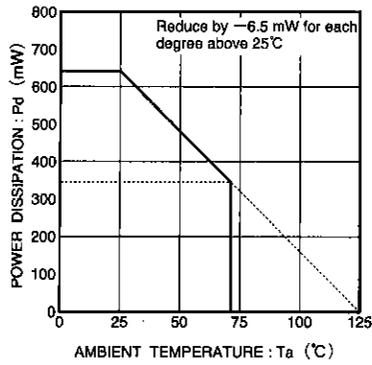


Fig. 3 Thermal derating curve

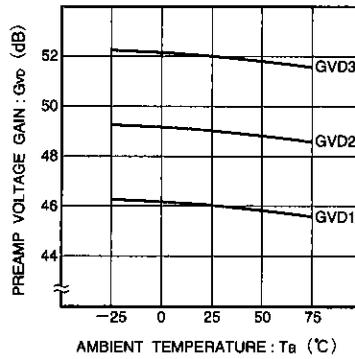


Fig. 4 Preamp voltage gain vs. ambient temperature.

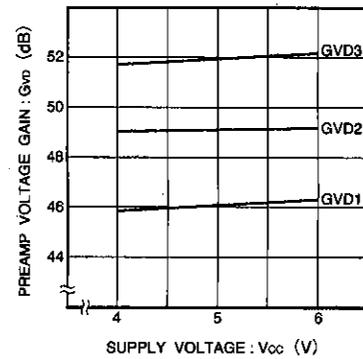


Fig. 5 Preamp voltage gain vs. supply voltage

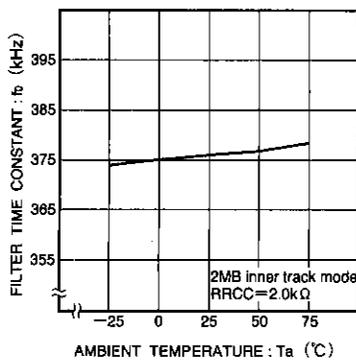


Fig. 6 Filter time constant ( $f_o$ ) vs. ambient temperature

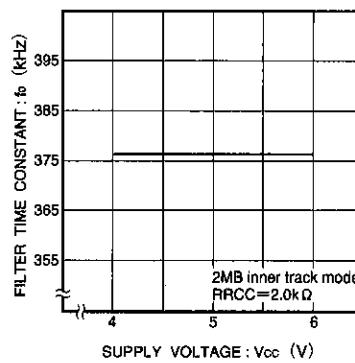


Fig. 7 Filter time constant vs. supply voltage

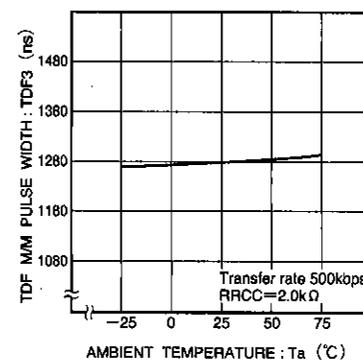


Fig. 8 TDF time constant vs. ambient temperature

FDD read/write amplifier

FDD/HDD

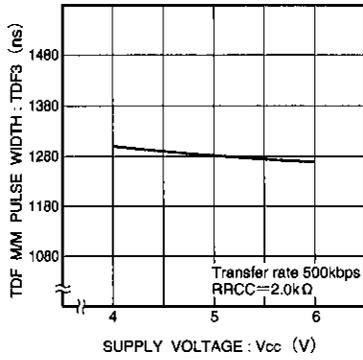


Fig. 9 TDF time constant vs. supply voltage

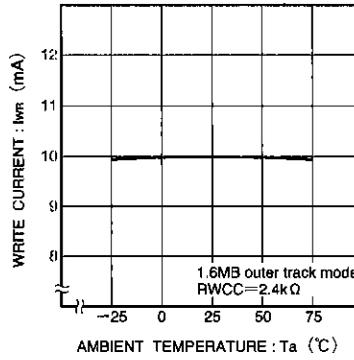


Fig. 10 Write current vs. ambient temperature

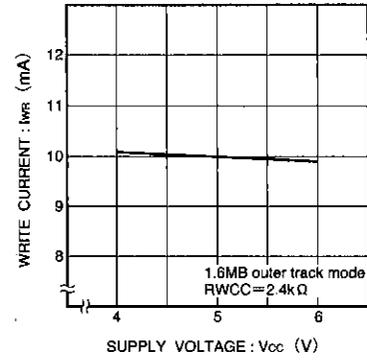


Fig. 11 Write current vs. supply voltage

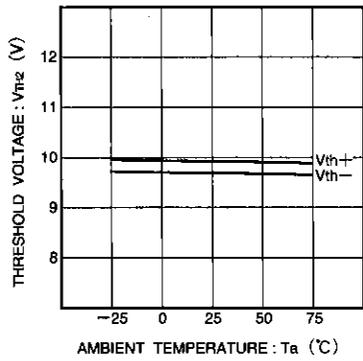


Fig. 12 Low level voltage detection voltage vs. ambient temperature

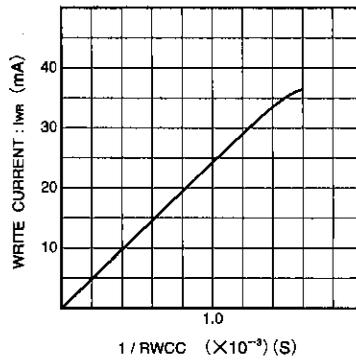
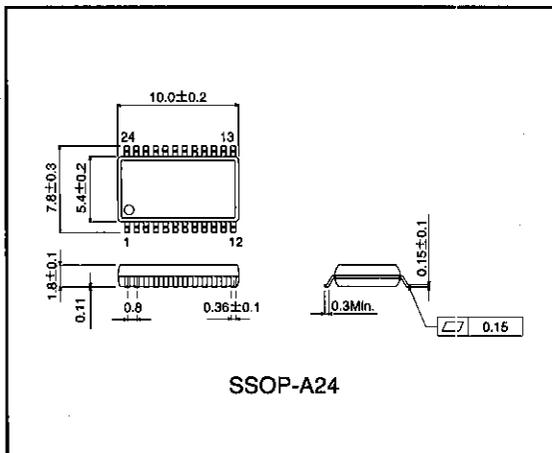


Fig. 13 Write current vs. write current adjustment resistance

● External dimensions (Units: mm)



## Notes

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