8K×8 bit SRAM

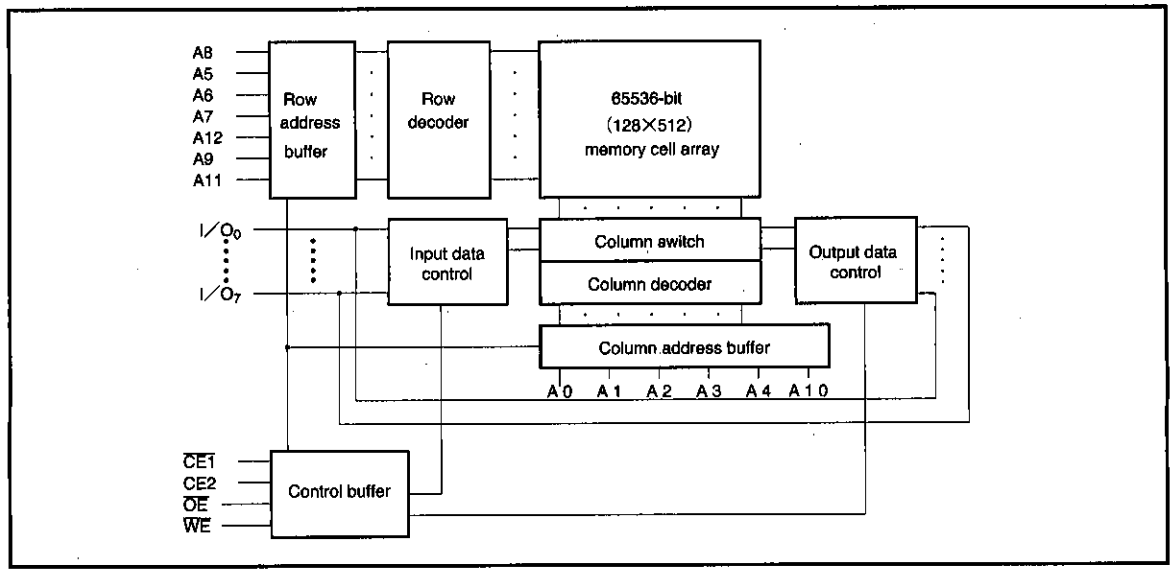
BR6265BF-N10SL

The BR6265BF-N10SL is an 8192 word × 8 bit CMOS static RAM. It runs on a 5V single power supply, and input can be directed coupled with TTL. Current consumption in the non-selected state is extremely low at 20 μA (max.), and memory information can be retained even at a low voltage of 2V, making this product ideal for battery backup operations.
Both the access and cycle timing are 100ns, facilitating timing design.

●Applications
General-purpose

●Features
1) SRAM with an 8192 × 8 bit configuration.
2) 5V single power supply voltage with ±10% fluctuation tolerance.
3) High speed access time of 100ns.
4) TTL compatible input/output.
5) Input and output use the same pin, and there are 3 output states.
6) No clock is necessary (asynchronous static circuit).
7) Input and output data are in the same phase.
8) Low power consumption.

●Block diagram



●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	−0.5 *1 ~7.0	V
Power dissipation	Pd	850*2	mW
Operating temperature range	Topr	0~70	℃
Storage temperature	Tstg	−55~125	℃
I/O voltage	V_I	−0.5~V_{CC}+0.5	V

*1 At pulse width of 50 ns: -3.0 V (min.)

*2 Reduced by 8.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
"H" input voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
"L" input voltage	V_{IL}	−0.3	—	0.8	V
Ambient temperature	Ta	0	—	70	℃

●Pin description

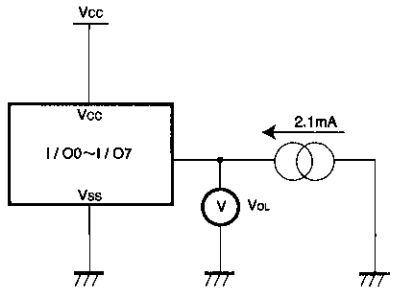
Pin No.	Pin Name	Function
1	NC	Internal chip and not connected
2~10、21、23~25	A0~A12	8192-byte memory address input
11~13、15~19	I/O0~I/O7	8-bit data I/O
20	$\overline{CE1}$	Chip enable control input
26	CE2	Chip enable control input
22	$\overline{OE}$	Output enable control input
27	$\overline{WE}$	Write enable control input
28	V_{CC}	5V±10% power supply
14	V_{SS}	Reference voltage for all input/output, 0 V

●Electrical characteristics (Unless otherwise specified, Ta=0 to 70℃, V_{CC}=5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
"L" input voltage	V_{IL}	−0.3*1	—	0.8	V		—
"H" input voltage	V_{IH}	2.2	—	V_{CC}+0.5	V		—
"L" output voltage	V_{OL}	0	—	0.4	V	I_{OL}=2.1mA	Fig.1
"H" output voltage	V_{OH}	2.4	—	V_{CC}	V	I_{OH}=−1.0mA	Fig.2
		V_{CC}×0.8	—	V_{CC}	V	I_{OH}=−0.1mA	—
Input leakage current	I_{LI}	—	—	±1	μA	V_{IN}=0~V_{CC}	Fig.3
Output leakage current	I_{LO}	—	—	±1	μA	V_{OUT}=0~V_{CC}	Fig.4
Average operating current	I_{CCA1}	—	—	40	mA	$\overline{CE1}$=V_{IL},CE2=V_{IH},I / O : OPEN Minimum cycle time	Fig.5
	I_{CCA2}	—	—	10	mA	$\overline{CE1}$=V_{IL},CE2=V_{IH},I / O : OPEN f=1MHz	Fig.5
Standby current	I_{SB}	—	—	3	mA	$\overline{CE1}$=V_{IH} or CE2=V_{IL}	—
	I_{SB1}	—	—	20	μA	$\overline{CE1}$≧V_{CC}−0.2V, CE2≧V_{CC}−0.2V or CE2≦0.2V	Fig.6
	I_{SB2}	—	—	20	μA	CE2≦0.2V	—

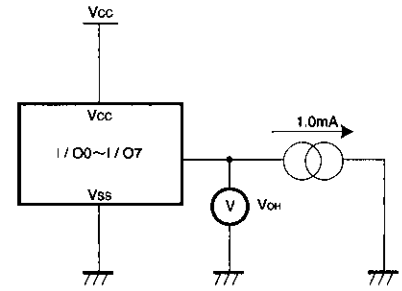
*1 At input voltage pulse width of 50 ns or less : -3.0 V

●Measurement circuit



Data sets all output to LOW (Data 00))

Fig. 1 LOW output voltage measurement circuit



Data sets all output to HIGH (Data FF)

Fig. 2 HIGH output voltage measurement circuit

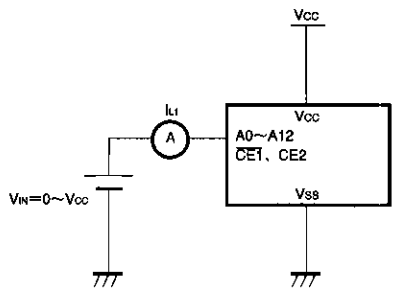


Fig. 3 Input leakage measurement circuit

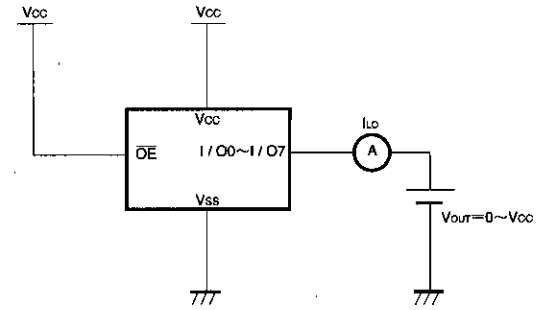
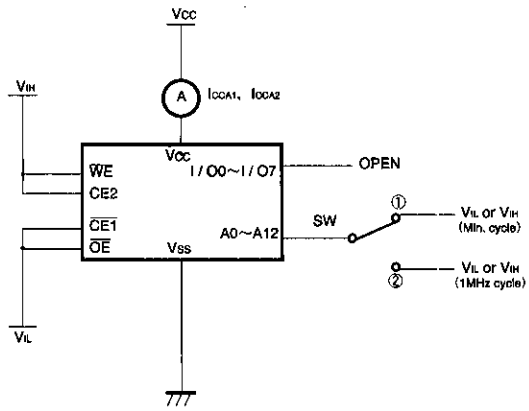


Fig. 4 Output leakage current measurement circuit



①: Average operating current ICCA1

②: Average operating current ICCA2

Fig. 5 Current consumption measurement circuit

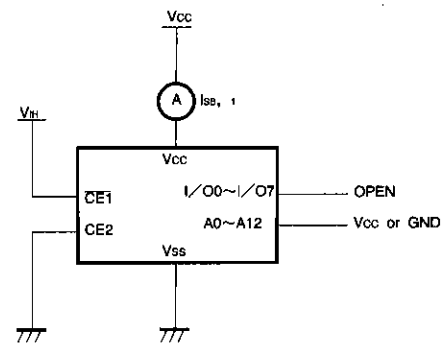


Fig. 6 Standby current measurement circuit

●Operating modes

Control pin				Mode	I / O	Power consumption
$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$			
X	H	X	X	Wait state	High impedance	Standby state
X	X	L	X	Wait state	High impedance	Standby state
H	L	H	H	Output disabled	High impedance	Operating state
L	L	H	H	Read	Data output	Operating state
X	L	H	L	Write	Data output	Operating state

X : Either V_{IL} or V_{IH}

●AC test conditions (Ta=0 to 70℃, 5V±10%)
Input pulse level : 0.8 to 2.4V
Input rise/fall time : 5ns
I/O timing level : 1.5V
Output load : 1 TTL gate and CL = 100pF

●Read cycle

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	t_{RC}	100	—	ns
Address access time	t_{AA}	—	100	ns
$\overline{CE1}$ access time	t_{CO1}	—	100	ns
CE2 access time	t_{CO2}	—	100	ns
$\overline{OE}$ access time	t_{OE}	—	40	ns
Output hold time	t_{OH}	10	—	ns
$\overline{CE1}$ output set time	t_{LZ1}	10	—	ns
CE2 output set time	t_{LZ2}	10	—	ns
$\overline{OE}$ output reset time	t_{OLZ}	5	—	ns
$\overline{OE1}$ deselect output floating	t_{HZ1}	—	35	ns
$\overline{OE2}$ deselect output floating	t_{HZ2}	—	35	ns
$\overline{OE}$ disable output floating	t_{OHZ}	—	35	ns

●Read cycle timing chart 1 ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = $\overline{WE}$ = V_{IH})

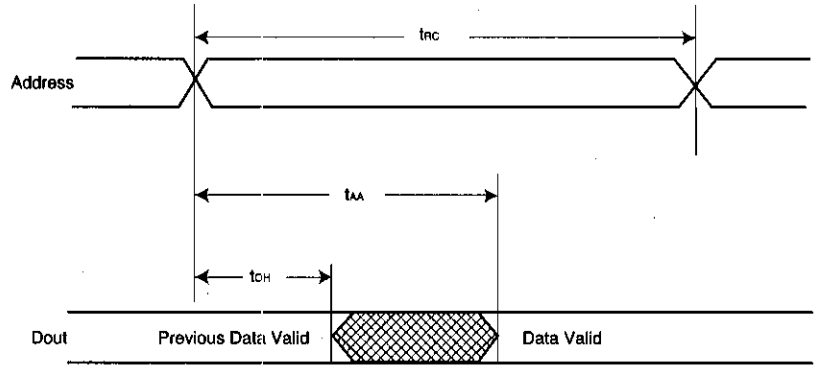
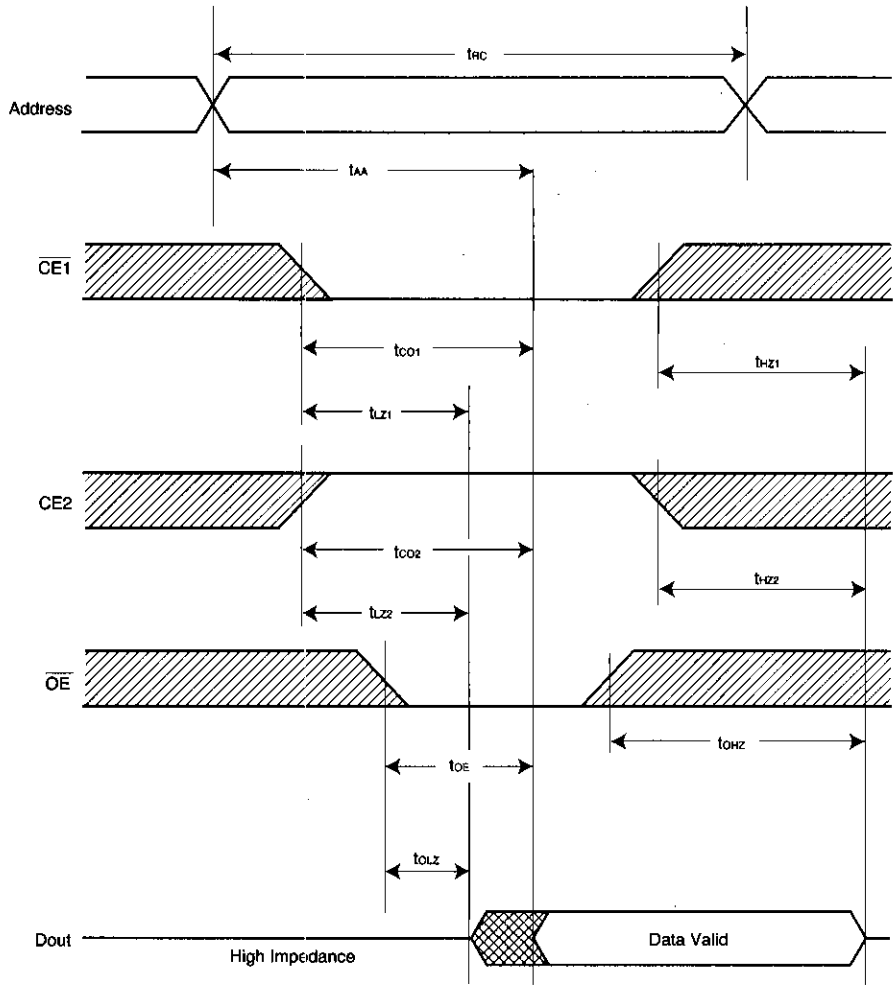


Fig.7

●Read cycle timing chart 2 ($\overline{WE}$ = V_{IH})



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●Write cycle

Parameter	Symbol	Min.	Max.	Unit
Write cycle time	t_{WC}	100	—	ns
Chip select time	t_{CW}	80	—	ns
Address valid time	t_{AW}	80	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	60	—	ns
$\overline{WE}$ output delay time	t_{WR}	0	—	ns
$\overline{CE1}$, CE2 output delay time	t_{WR1}	0	—	ns
$\overline{WE}$ · output floating time	t_{WHZ}	—	35	ns
Input data set time	t_{DW}	40	—	ns
Input data hold time	t_{DH}	0	—	ns
$\overline{WE}$ · output set time	t_{OW}	5	—	ns

●Write cycle timing chart 1 ($\overline{WE}$ control)

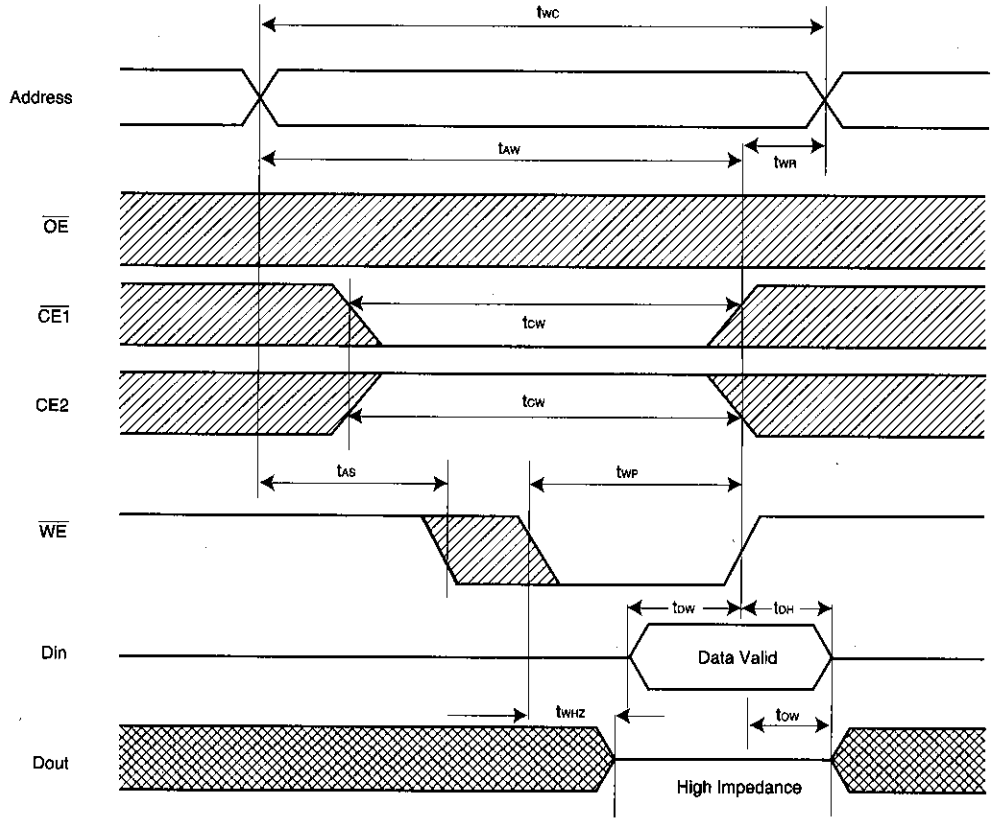

Fig.9

●Write cycle timing chart 2 ($\overline{CE1}$ control)

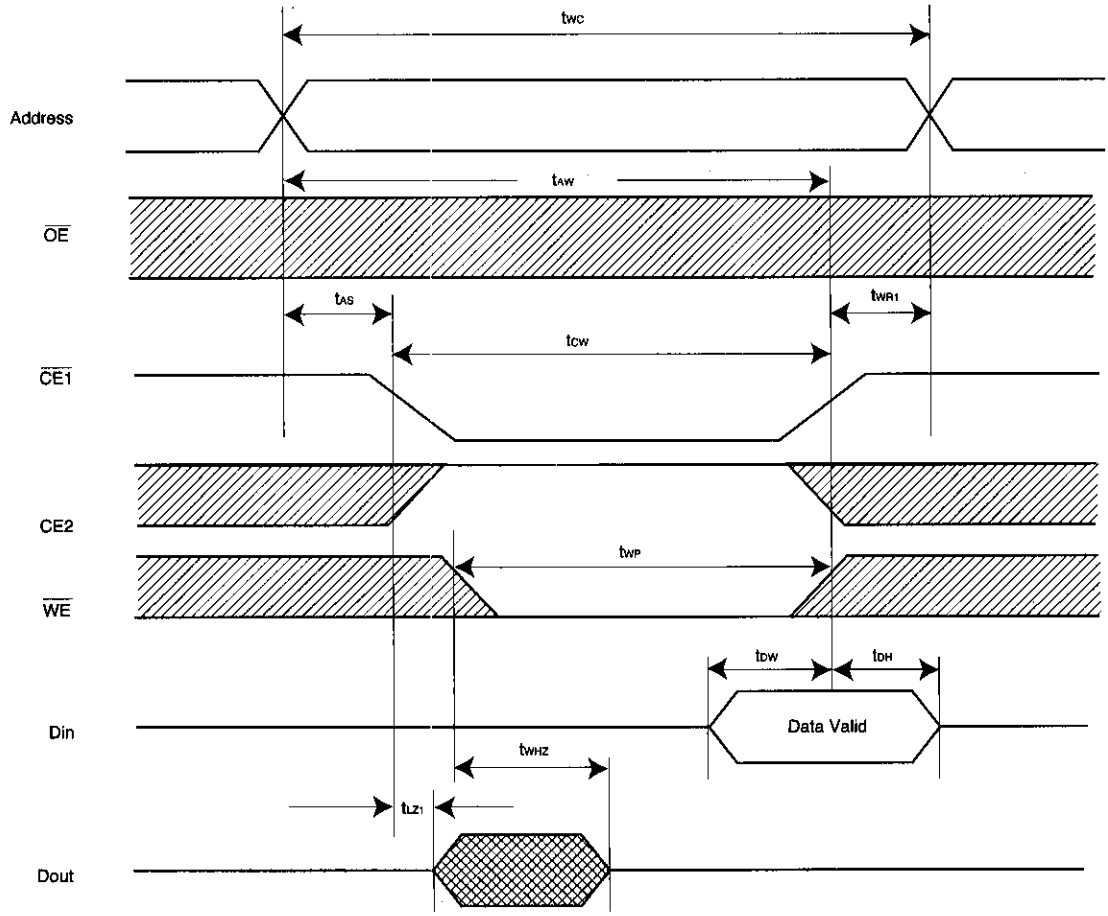

Fig.10

●Write cycle timing chart 3 (CE2 control)

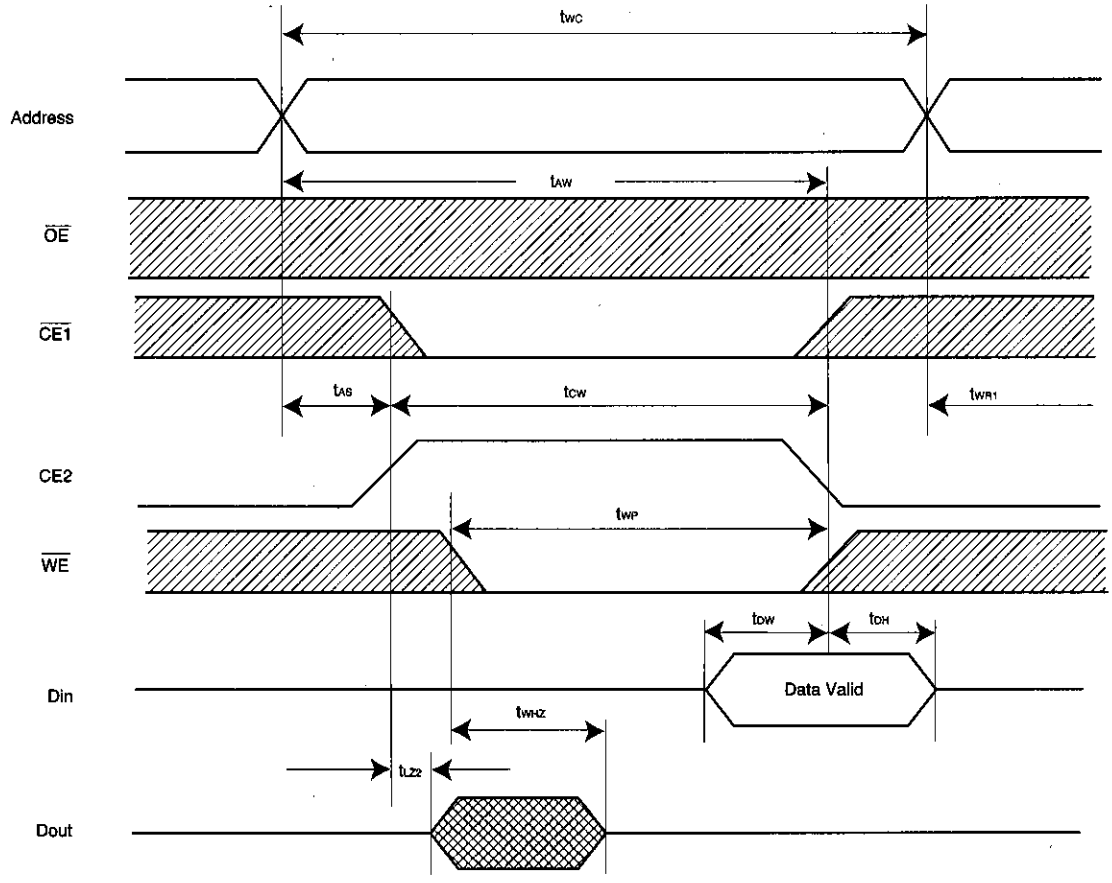

Fig.11

* While the I/O pin is in output state, input signals should not be applied which are in reverse phase to the output.
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●Data retention characteristics at low power supply voltage (Ta = 0 to 70℃) : SL version products

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Data retention power supply voltage	V_{DR}	2.0	—	5.5	V	$\overline{CE1} \geqq V_{CC}-0.2V$, $CE2 \geqq V_{CC}-0.2V$ or $CE2 \leqq 0.2V$
Data retention current	I_{CCDR}*	—	—	10	μA	$\overline{CE1} \geqq V_{CC}-0.2V$, $CE2 \geqq V_{CC}-0.2V$ or $CE2 \leqq 0.2V$, $V_{CC}=3.0V$
CS data retention time	t_{CDR}	0	—	—	ns	
Operating recovery time	t_R	5	—	—	ms	

*1 μA (Max.), when Ta=0~40℃

●Data retention waveform at low power supply voltage

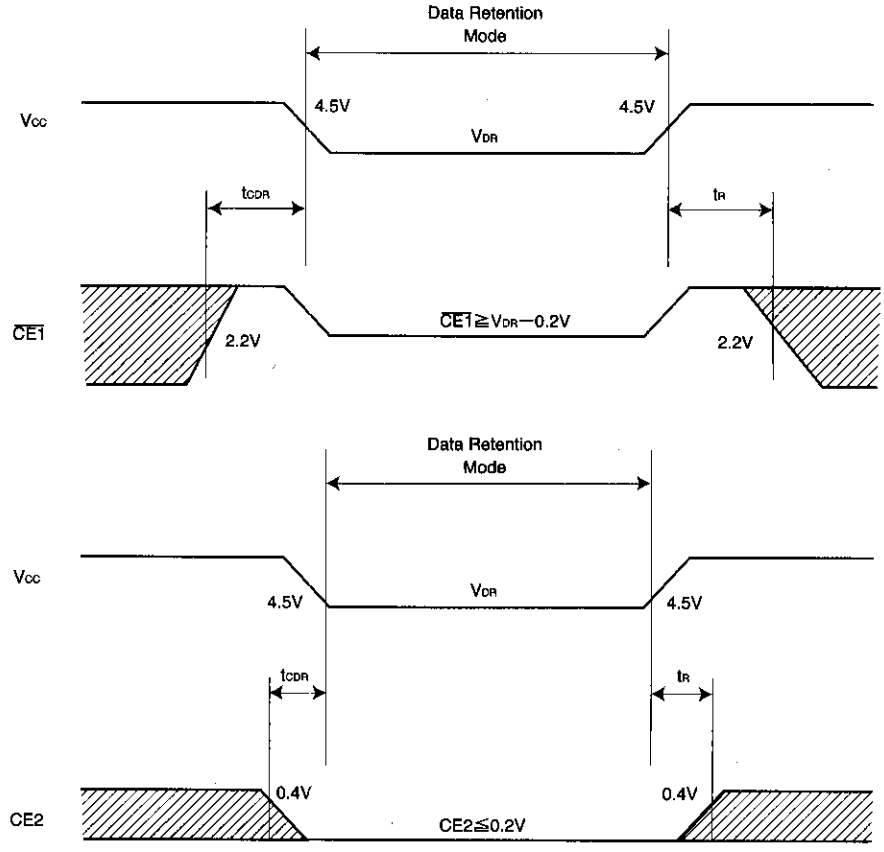
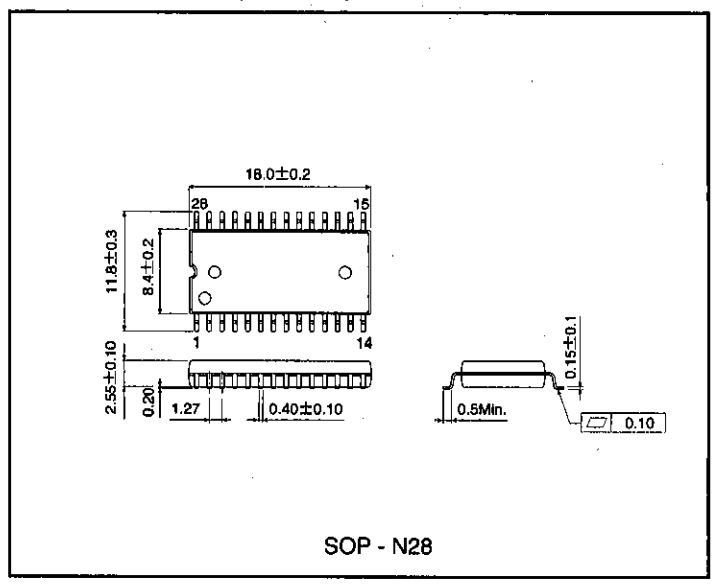


Fig.12

●External dimensions (Units: mm)



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