NTSC Digital Encoder
BU1418K

The BU1418K is an LSI chip that converts RGB input to NTSC analog video signals.

●Applications
Video, CD/CD-G

●Features
1) Supported input clock : 27MHz and 28.636MHz.
2) 24-bit RGB signal input.
3) Synch signal that supports slave systems.
4) NTSC, Y and C signals are output through a high-speed 3-channel, 9-bit DAC (with 75Ω driver)
5) Internal 8-color OSD function.
6) Single 5V power supply.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}, AV_{DD}, DV_{DD}	−0.5~7.0	V
Input voltage	V_{IN}	−0.5~V_{DD}+0.5	V
(Storage temperature)	Tstg	−55~150	℃
Power dissipation	Pd	1375*1	mW

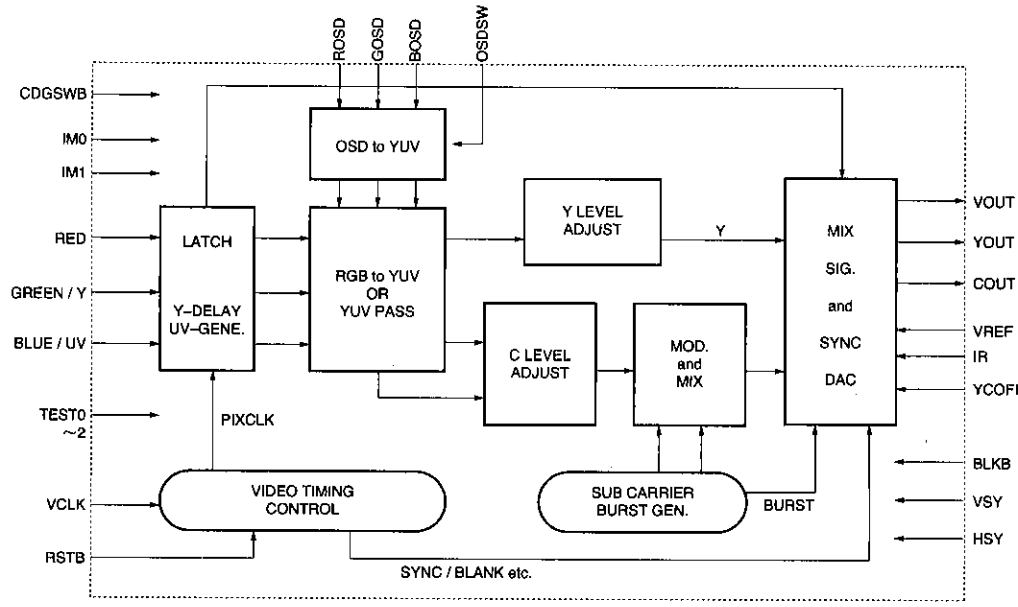
*1 Reduced by 11 mW for each increase in Ta of 1℃ over 25℃.
(When mounted to a 70 × 70 × 1.6 mm glass epoxy board.)
* Does not represent guaranteed performance.
◎ Not designed for radiation resistance.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD},AV_{DD},DV_{DD}*	4.75~5.25	V
Input voltage, high level	V_{IH}	2.1~V_{DD}	V
Input voltage, low level	V_{IL}	0~0.8	V
Analog input voltage	V_{AIN}	0~AV_{DD}	V
Operating temperature	Topr	−25~60	℃

* Use at V_{DD} = AV_{DD} = DV_{DD}

●Block diagram



●Electtic characteristics (unless otherwise noted, Ta=25℃, V_{DD}=AV_{DD}=DV_{DD}=5.0V, GND=AVSS=DVSS=VGND=YGND=CGND=0.0V)

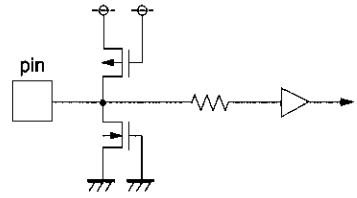
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock frequency 1	fCLK1	—	27.0	—	MHz	Input frequency for the Video-CD mode
Clock frequency 2	fCLK2	—	28.636	—	MHz	Input frequency for the CD-G mode
Burst frequency	fBST	—	3.5795	—	MHz	Subcarrier frequency
Burst cycle	CBST	—	9	—	CYC	
Operational circuit current	IDD	—	120.0	130.0	mA	Color bar output
Output voltage, HIGH	VOH	4.0	4.6	—	V	IOH=−2.0mA
Output voltage, LOW	VOL	—	0.2	1.0	V	IOL=2.0mA
Input voltage, HIGH	VIH	2.1	—	—	V	
Input voltage, LOW	VIL	—	—	0.8	V	
Input current, HIGH	IIH	−10.0	0.0	10.0	μA	VIH=5.0V
Input current, LOW	IIL	−10.0	0.0	10.0	μA	VIL=0.0V
DAC resolution	RES	—	9	—	BITS	
Linearity error	EL	−3.0	±0.5	+3.0	LSB	Measure VOUT in the YCOFF mode
Y current, white level	IYW	—	25.14	—	mA	VREF=1.29V、RIR=1.2kΩ
Y current, black level	IYB	—	7.24	—	mA	VREF=1.29V、RIR=1.2kΩ
Y current, zero level	IYZ	−10.0	0.0	10.0	μA	

●Pin description

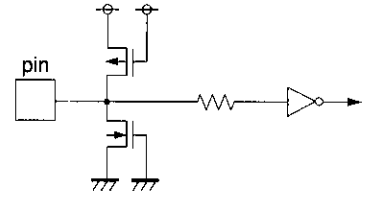
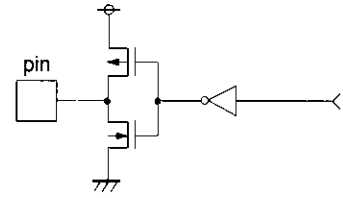
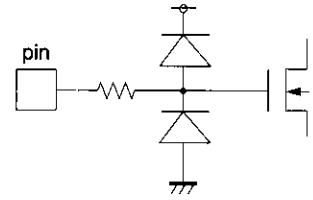
Pin No.	Pin name	Function
1	BOSD	OSD BLUE DATA INPUT
2	GD0 / Y0	GREEN / Y DATA Bit0 (LSB)
3	GD1 / Y1	GREEN / Y DATA Bit1
4	GD2 / Y2	GREEN / Y DATA Bit2
5	GD3 / Y3	GREEN / Y DATA Bit3
6	GD4 / Y4	GREEN / Y DATA Bit4
7	GD5 / Y5	GREEN / Y DATA Bit5
8	GD6 / Y6	GREEN / Y DATA Bit6
9	GND	DIGITAL GROUND
10	GD7 / Y7	GREEN / Y DATA Bit7 (MSB)
11	BD0 / UV0	BLUE/UV DATA Bit0 (LSB)
12	BD1 / UV1	BLUE/UV DATA Bit1
13	BD2 / UV2	BLUE/UV DATA Bit2
14	BD3 / UV3	BLUE/UV DATA Bit3
15	OSDSW	OSD INPUT ENABLE
16	CDGSWB	SELECT Video—CD/$\overline{\text{CD-G}}$
17	BD4 / UV4	BLUE / UV DATA Bit4
18	BD5 / UV5	BLUE / UV DATA Bit5
19	BD6 / UV6	BLUE / UV DATA Bit6
20	BD7 / UV7	BLUE / UV DATA Bit7 (MSB)
21	GND	DIGITAL GROUND
22	NC	—
23	IM0	INPUT MODE SET Bit0
24	IM1	INPUT MODE SET Bit1
25	TEST1	NORMALLY PULLDOWN TO GND
26	TEST2	NORMALLY PULLDOWN TO GND
27	VSY	V - SYNC INPUT FROM DECODER
28	HSY	H - SYNC INPUT FROM DECODER
29	PIXCLK	PIXEL CLOCK MONITOR
30	BLKB	DATA BLANKING $\overline{\text{ENABLE}}$
31	V_{DD}	DIGITAL VDD
32	NC	—

Pin No.	Pin name	Function
33	NC	—
34	NC	—
35	VREF	REFERENCE VOLTAGE (1.29V)
36	CGND	CHROMA OUTPUT GROUND
37	COUT	CHROMA OUTPUT
38	VGND	COMPOSITE OUTPUT GROUND
39	VOUT	COMPOSITE OUTPUT
40	AVSS	ANALOG (DAC, VREF) GROUND
41	NC	—
42	IR	REFERENCE RESISTOR (1.2K)
43	AVDD	ANALOG (DAC, REF) VDD
44	YGND	LUMINANCE OUTPUT GROUND
45	YOUT	LUMINANCE OUTPUT
46	NC	—
47	NC	—
48	YCOFF	DAC (YOUT, COUT) OFF
49	DVSS	DIGITAL (DAC_CTRL) GROUND
50	DVDD	DIGITAL (DAC_CTRL) VDD
51	VCLK	CLOCK INPUT
52	RSTB	LOGIC PART INITIAL $\overline{\text{RESET}}$
53	TEST0	NORMALLY PULLDOWN TO GND
54	RD0	RED DATA Bit0 (LSB)
55	RD1	RED DATA Bit1
56	RD2	RED DATA Bit2
57	ROSD	OSD RED DATA INPUT
58	RD3	RED DATA Bit3
59	RD4	RED DATA Bit4
60	RD5	RED DATA Bit5
61	V_{DD}	DIGITAL VDD
62	RD6	RED DATA Bit6
63	RD7	RED DATA Bit7
64	GOSD	OSD GREEN DATA INPUT

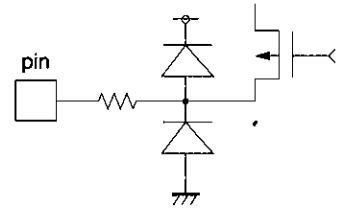
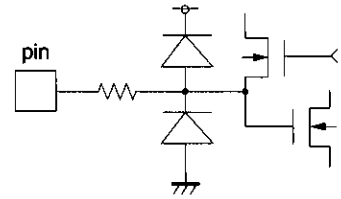
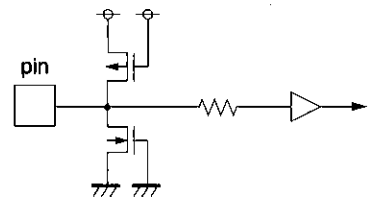
●Input/output circuit

Pin No.	Pin name	In/output	Equivalent circuit	Pin descriptions
2~8 10	GD [0 : 7] / Y [0 : 7]	Input		For G data input during 24-bit RGB input. The input timing is set to match that of VCLK/2 synchronized to the fall of HSY
11~14 17~20	BD [0 : 7] / UV [0 : 7]	Input		For B data input during 24-bit RGB input. The input timing is set to match that of VCLK/2 synchronized to the fall of HSY
54~56 58~60 62,63	RD [0 : 7]	Input		For R data input during 24-bit RGB input. The input timing is set to match that of VCLK/2 synchronized to the fall of HSY
57 64 1 15	ROSD GOSD BOSD OSDSW	Input		For OSD data input when using the OSD function. When OSDSW is HIGH, inputs from ROSD, GOSD and BOSD have priority. When using the OSD function outputs color according to date from ROSD, GOSD, and BOSD when H is input at this pin.
16	CDGSWB	Input		Input for switch between the Video-CD (H) mode and CD-G (L) mode.
23 24	IM0 IM1	Input		Control pin for selecting the input mode from RGB / DAC through.

●Input/output circuit

Pin No.	Pin name	In/output	Equivalent circuit	Pin descriptions
28	HSY	Input		For horizontal synch signal input. Inputs the negative HSYNC signal. Also used for the synch signal generated by halving the VCLK clock frequency.
27	VSY	Input		For vertical synch signal input. Inputs the negative VSYNC signal.
30	BLKB	Input		Enables (LOW level) data output immediately after end of equivalent pulse.
29	PIXCLK	Output		Monitor pin for the VCLK/2 internal clock. RGB data is processed internally upon startup.
31,61 43 50	V_{DD} AVDD DVDD	—	—	Power supply pin for the digital and analog blocks.
9,21 36 38 40 44 49	GND CGND VGND AVSS YGND DVSS	—	—	Ground pin for digital and analog blocks, composite output, Y output and C output.
35	VREF	Input		Reference voltage that determines the DAC output amplitude (1LSB output current). Normally applied 1.29V. (output 1.0V_{P-P})

●Input/output circuit

Pin No.	Pin name	In/output	Equivalent circuit	Pin descriptions
37	COUT	Output		S pin chroma output. CGND pin is the reference ground.
39	VOUT	Output		Composite output. VGND is the reference ground.
45	YOUT	Output		S pin luminance output. YGND is the reference ground.
42	IR	Input		Set by connecting the reference resistance to the DAC output amplitude (1LSB output current). A voltage roughly equal to 1V_{P-P} can be output by connecting 1.2 kΩ when pin 35 is 1.29 V.
48	YCOFF	Input		Input of the low power mode switching signal. AT HIGH, the DAC output of YOUT and COUT are turned off.
51	VCLK	Input		For system clock signal input that operates the digital block. MPEG1 and CD-G input a 27.0 MHz or 28.6 MHz 50% duty clock signal.
52	RSTB	Input		For reset input that initializes the IC.
25 26 53	TEST1 TEST2 TEST0	Input		Normally connected to GND

●Circuit operation

(1) General

The BU1418K converts 8-bit digital image data to NTSC composite signals (V), luminance signals (Y), and color signals (C) and outputs them through a 9-bit high-speed DAC as television signals.

Digital image data can be adapted for Video-CD and CD-G decoded output, and is switched according to the CDGSWB input voltage. Input data is received and processed by the pixel clock, which halves the doubled pixel clock signal from VCLK and synchronizes it with the fall of the horizontal synchronization signal (from HSY). The internal pixel clock and be monitored with PIXCLK.

The input clock frequency is calculated as follows.

Video-CD (CDGSWB = HIGH) : 27.000MHz

CD-G (CDGSWB = LOW) : 28.636MHz

Input data are input via RD0 through RD7, GD0 through GD7, and BD0 through BD7 in the format RGB (4 : 4 : 4), YUV (4 : 2 : 2) or YUV (4 : 1 : 1).

RD7, GD7 and BD7 are each MSB. However, the YUV input mode cannot be used in the CD-G mode. Select the format with inputs to IM0 and IM1.

Enabling OSDSW validates input data from ROSD, GOSD and BOSD, allowing for the input of 7-color (8 including black) data.

Input data is internally converted to YUV in the case of the RGB format or OSD input. Internal Y, U and V data are adjusted to the NTSC 100 IRE level, after which U and V data are phase-modulated by an internally ordered 3.58 MHz subcarrier, generating modulated color signals.

Finally, the needed synchronization levels, color blank level and burst signals, etc., are mixed, and NTSC composite signals, luminance signals and color signals are output through the 9-bit DAC.

NTSC composite : VOUT

Luminance signal (Y) : YOUT

Color signal (C) : YOUT

Television signal field sequences are interlaced in the Video-CD mode and non-interlaced in the CD-G mode.

As setting BLKB to HIGH enables data output immediately after the equivalent pulse (9H) zone, this IC is adaptable for closed-caption and teletext broadcasting.

When a 75Ω load is connected externally and video input pins (75Ω termination) are also connected, the luminance component of DAC output has a roughly 1.0 Vpp output range at the white level. For details concerning DAC output voltage levels, refer to Section 4, "DAC output level adjustment" As the YOUT and COUT DAC output pins can be turned off by setting YCOFF to HIGH, the BU1418K allows for a low power mode.

Table 1. YCOFF low power consumption mode

Pin No.	Pin name	Output mode and power consumption			
	YCOFF	VOUT	YOUT	COUT	Power consumption (Typ.)
48	LOW	Composite signal	Luminance signal	Color signal	0.65W
	HIGH	Composite signal	No output (0V)	No output (0V)	0.35W

*1 When AVDD=5.0V.

(2) Input format

The input format for digital data is set with IM1 and IM0 as shown in the table below. In addition to RGB, input in YUV formats (4 : 2 : 2 and 4 : 1 : 1) is also possible.

Also, digital RGB input can be converted to analog RGB output (in the RGB through mode). The YUV format can only be input in the Video-CD mode (CDGSWB is HIGH).

Table 2. Input format setting

IM1	IM0	Input format	Output signal
0	0	R (8 bits), G (8 bits), B (8 bits)	Television signals (9-bit resolution)
0	1	YUV (4:2:2) format	Television signals (9-bit resolution)
1	0	YUV (4:1:1) format	Television signals (9-bit resolution)
1	1	RGB input expanded to ROSD, GOSD, BOSD (see table below)	RGB analog signal (9 bits)

RGB through mode bit assignment is shown in the table below.

Table 3. RGB through mode bit assignment

Output pin	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VOUT (39)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	ROSD
YOUT (45)	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	GOSD
COUT (37)	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	BOSD

The BU1418K also has internal OSD switches and a color data generation function, making it easily adaptable for combined use with an OSD-IC that outputs blank and RGB signals. Inputs to ROSD, GOSD and BOSD are valid while OSDSW input is at the HIGH level. The relationship between OSD data and color data output is shown in the table below.

Table 4. OSD function : Input data/color output correlation

OSDSW	ROSD	GOSD	BOSD	Output color signal
H	L	L	L	BLACK (BLANKING)
H	L	L	H	BLUE
H	L	H	L	GREEN
H	L	H	H	CYAN
H	H	L	L	RED
H	H	L	H	MAGENTA
H	H	H	L	YELLOW
H	H	H	H	WHITE
L	X	X	X	Depends on RGB input

(3) Output level

Figs. 1 through 3 show pin output voltage level and the digital values of DAC output.

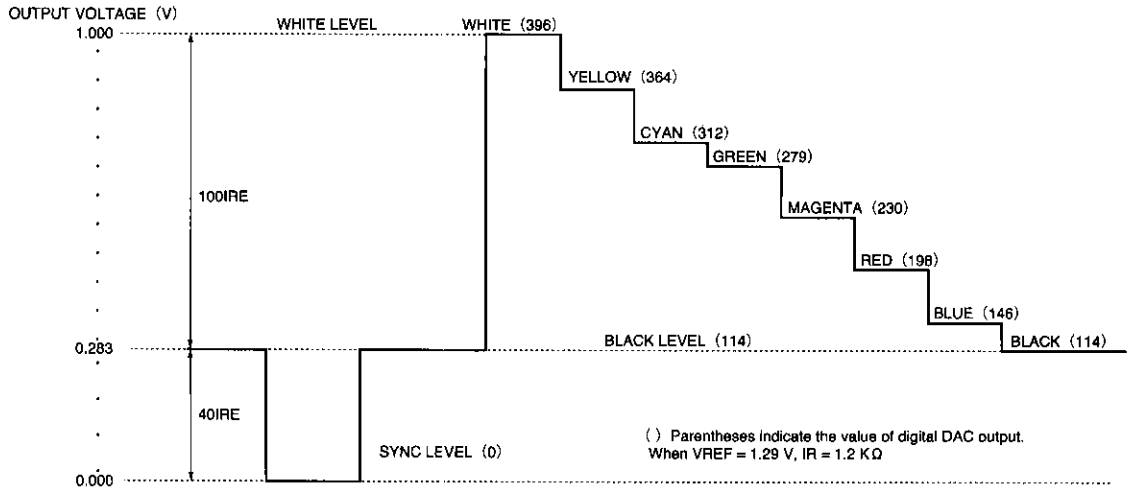


Fig. 1 NTSC Y (luminosity) signal output level

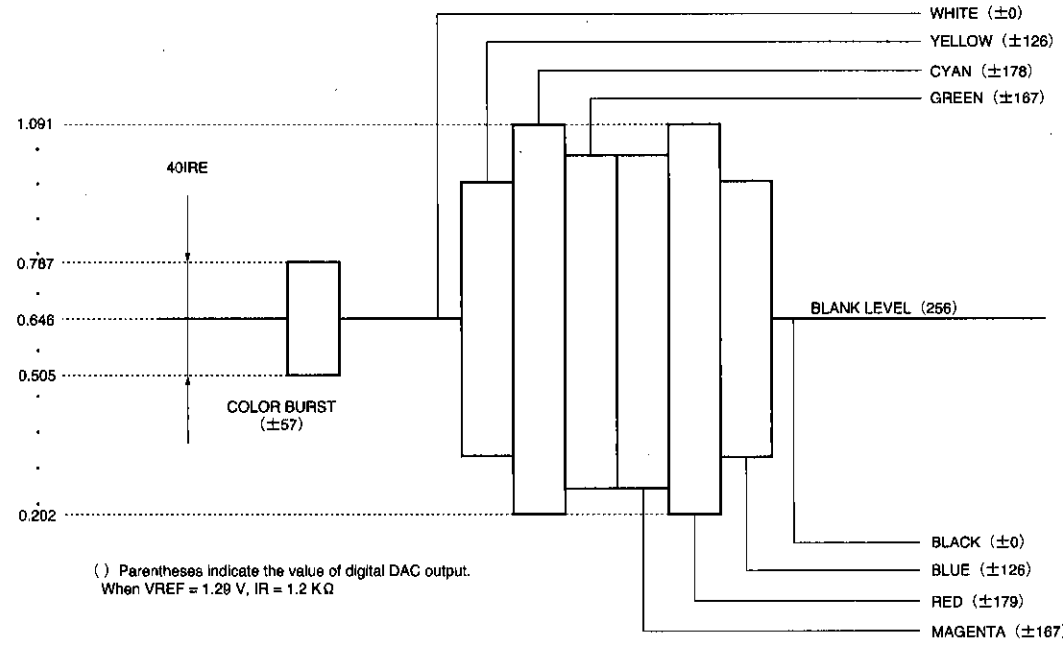


Fig. 2 NTSC C (chroma) signal output level

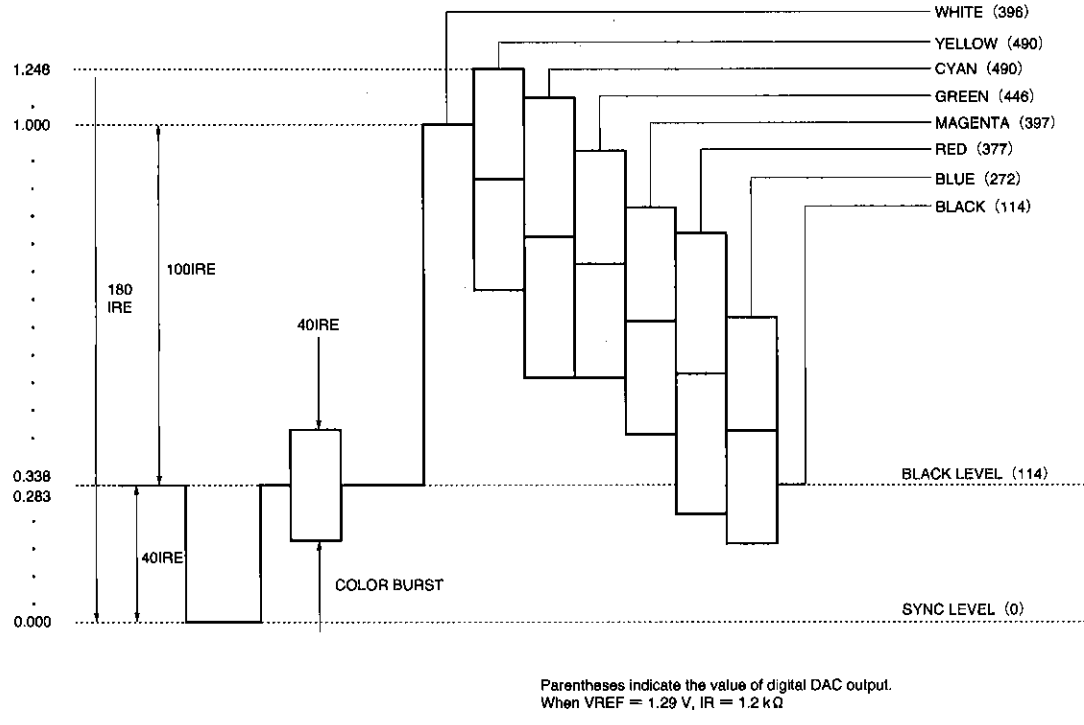


Fig. 3 NTSC V (composite) signal output level

(4) Timing

The BU1418K outputs NTSC television signals based on inputs to VCLK, HSY and VSY. The table below shows the input and output of timing pins.

Table 5. Timing input/output (BU1418K)

No	Pin	Name	Input/output	Function
1	51	VCLK	Input	Doubled pixel clock input
2	29	PIXCLK	Output	Pixel clock output (1/2 VCLK)
3	52	RSTB	Input	System reset input
4	27	VSY	Input	Vertical synchronization signal input
5	25	HSY	Input	Horizontal synchronization signal input
6	30	BLKB	Input	Enables ("H") data output after equivalent pulse (9H)
7	16	CDGSWB	Input	Switching between Video-CD/$\overline{\text{CD-G}}$ modes

Timing of internal clock (monitored with PIXCLK) generation and relationship between input data and VCLK/PIXCLK :

Clock generation and data input timing

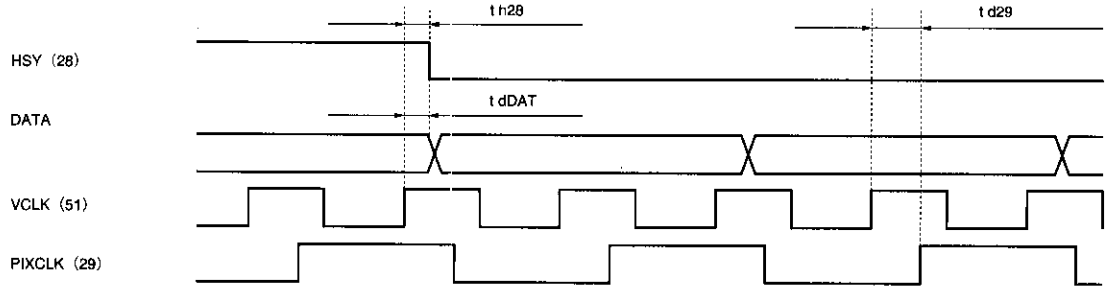


Fig. 4

Paramenter	Symbol	Unit	Min.	Typ.	Max.
HSY input hold time	t h28	nS	—	5.0	—
Data input delay time	t dDAT	nS	—	5.0	—
PIXCLK delay time	t d29	nS	—	25.0	—

Input of YUV should be timed using input to HSY as a reference, as shown in the illustration below.

4 : 1 : 1 format

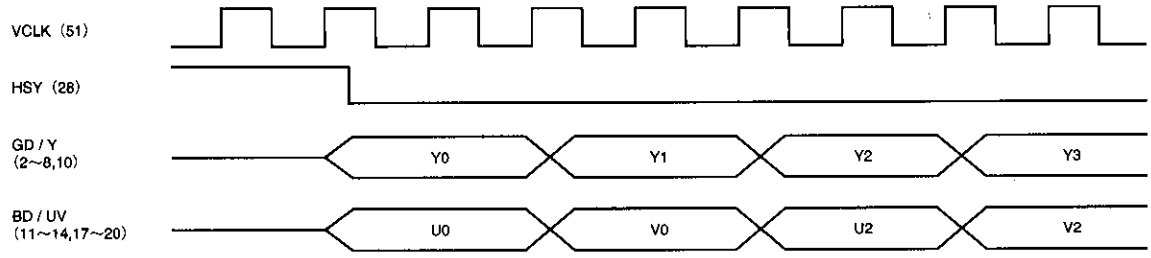


Fig. 5

4 : 2 : 2 format

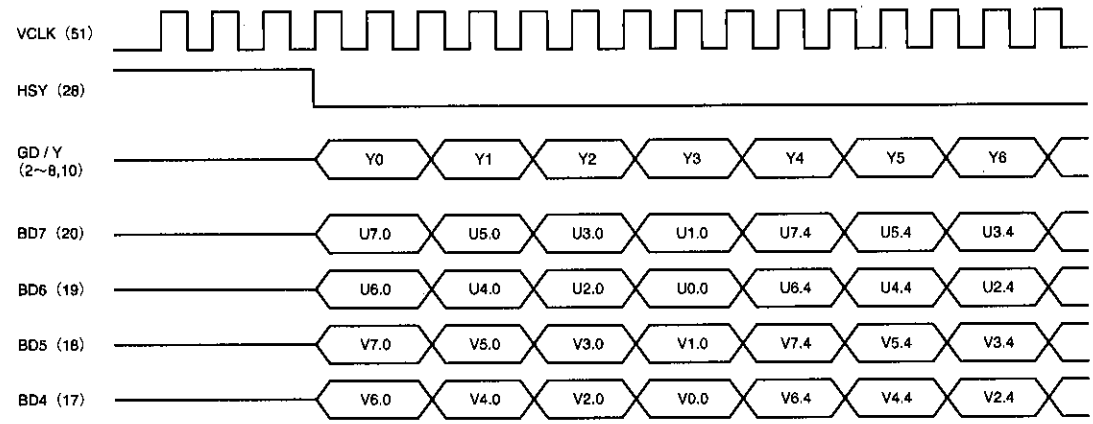


Fig. 6

* Numbers immediately following UV data indicate the bit. Numbers after the period (.) indicate the time relationship to Y data.

Timing for ODD/EVEN discrimination

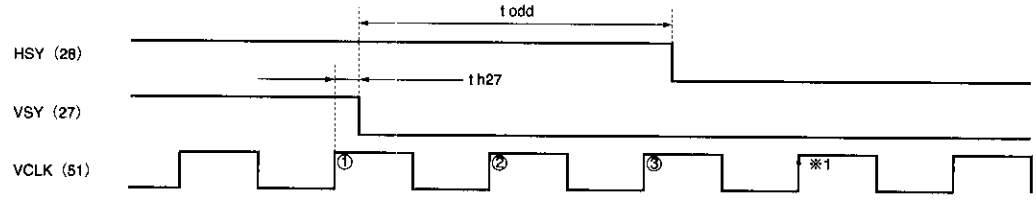


Fig. 7

Paramenter	Symbol	Unit	Min.	Typ.	Max.
VSY input holding time	t h27	nS	—	5.0	—
ODD field identification delay time	t odd	VCLK	—	2	—

※1 The field is identified as ODD when HSY starts before the clock startup (①②③), and as EVEN if HSY does not shut down. Design so that in the CD-G mode, HSY and VSY inputs always result in the ODD field (the rising signal is input to HSY with timing ①②③).

Frame timing in the Video-CD mode

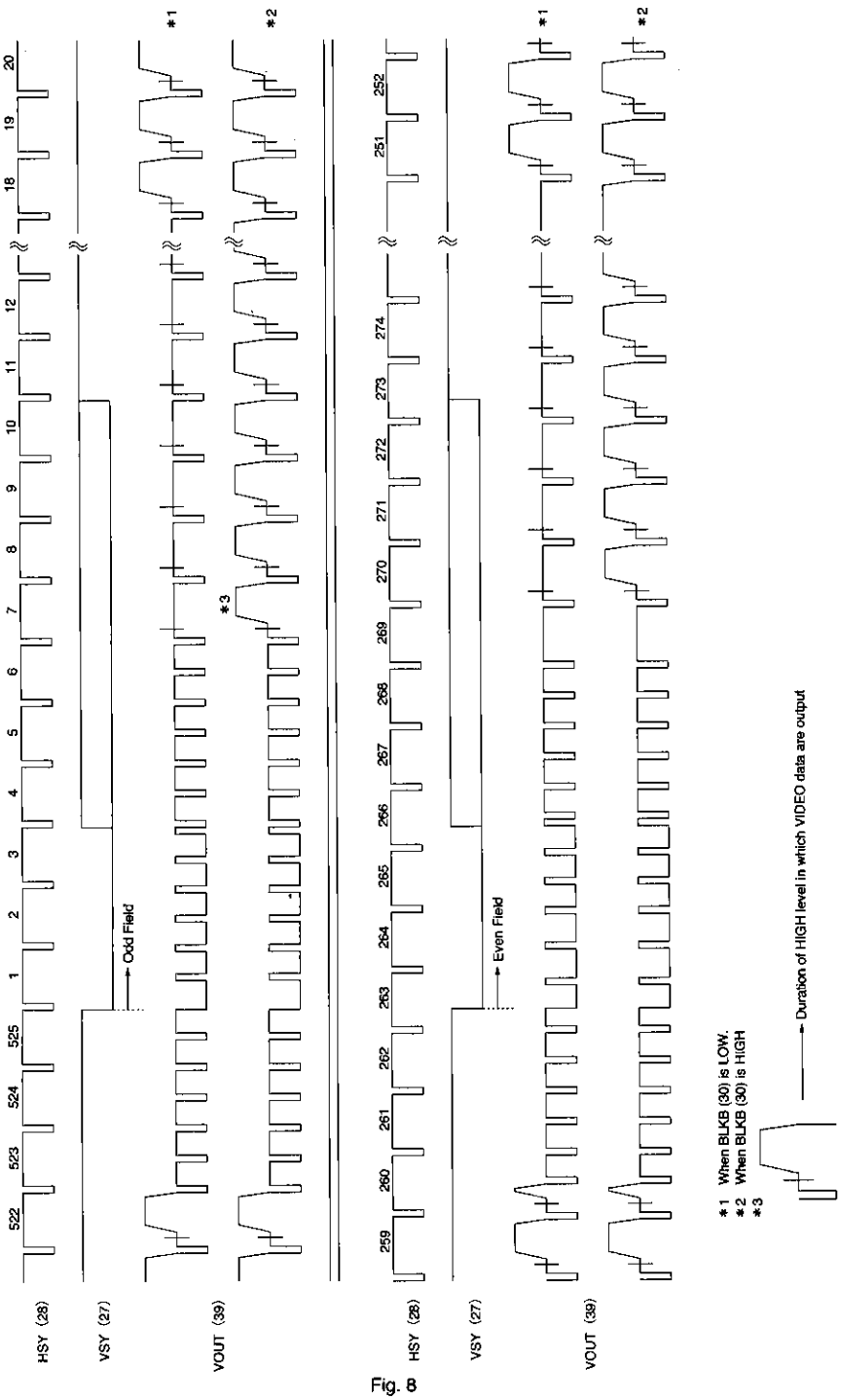


Fig. 8

Frame timing in the CD-G mode

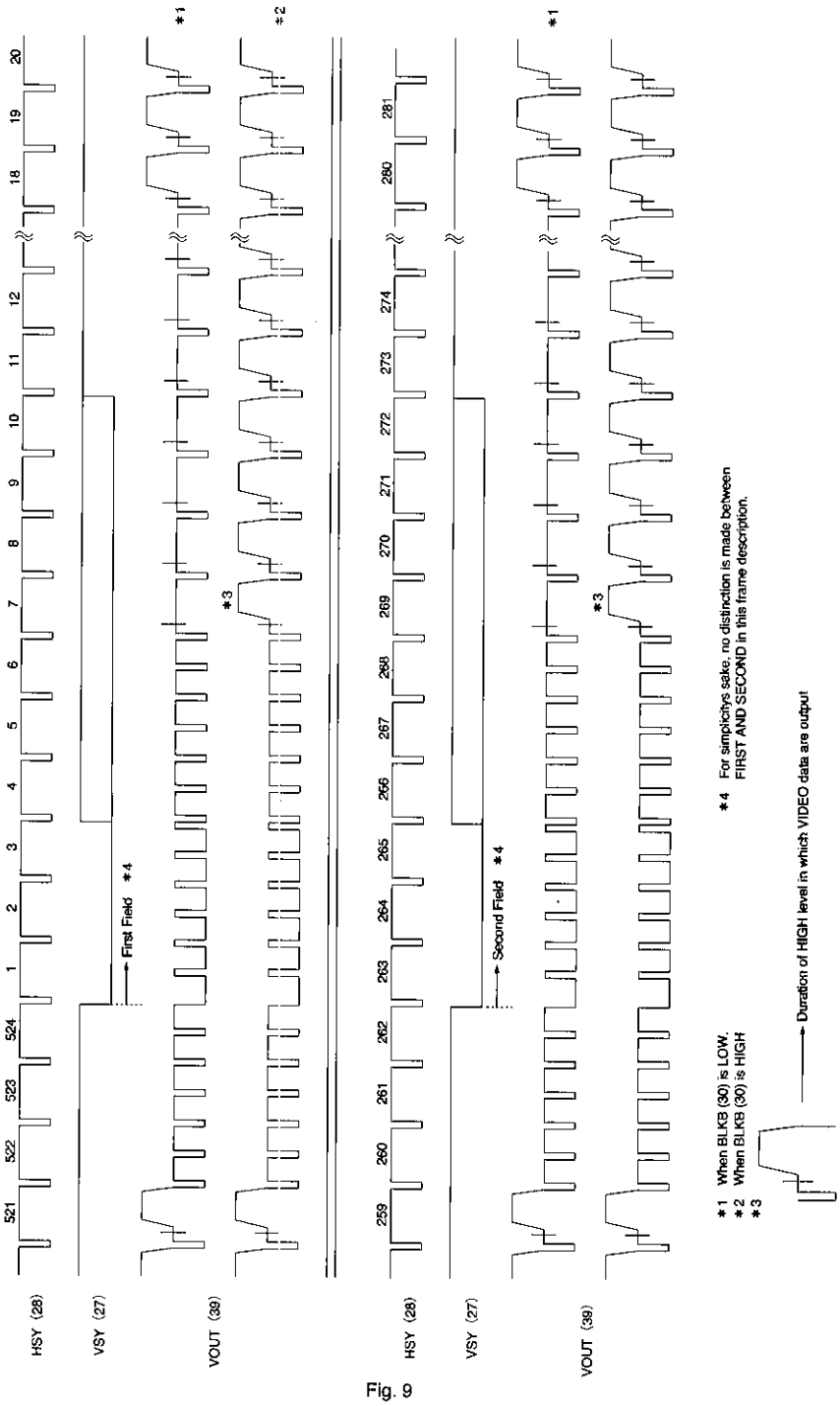


Fig. 9

Television signal timing diagram

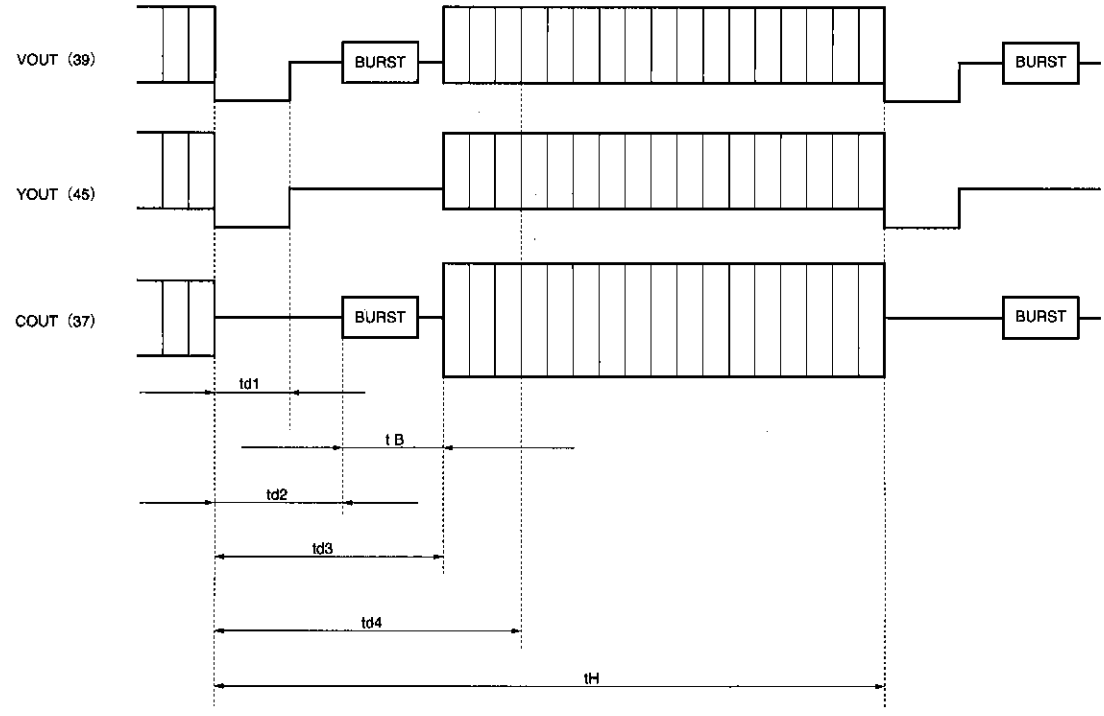


Fig. 10

Parameter	Symbol	Unit	Video - CD	CD - G	Note
SYNC rise	td1	VCLK	128	134	Generated automatically by BU1418K
Burst start	td2	VCLK	142	152	Generated automatically by BU1418K
Burst end	td3	VCLK	212	224	Generated automatically by BU1418K
Data validity	td4	VCLK	254	270	Blank data input in this interval
During of 1 line	tH	VCLK	1716	1820	Input Hsync input during this interval
Burst cycle	tB	fsc	9	9	Generated automatically by BU1418K

(4) DAC output level adjustment

The DAC output voltage level is determined by the internal DAC output current and the attached DAC output resistor. The output current of each DAC bit is determined by the VREF pin (pin 35) voltage and by the resistor attached to the IR pin (pin 42) (see below).

I (1LSB) = VVREF / (RIR + R0) * 1 / 16 [A] (equation 4-1)

VVREF : voltage impressed on VREF [V]
RIR : resistor attached to IR [Ω]
R0 : Internal parasitic resistance of IC [Ω]

Thus, when VVREF = 1.29V and RIR = 1.2kΩ, the current output for each LSB is 63.48 μA. The white level of Y has a digital value of 396 (decimal) and therefore is calculated as follows :

V (Y white) = 0.06348 * 396 = 25.14 [mA]

If a 37.5Ω resistor is attached to DAC output, amplitude is 0.943 [V_{P-P}].

The DAC output level can be fine-tuned according to equation 4-1 above. Please contact ROHM when using constants that differ significantly from the following: output level=1 V_{P-P}, VVREF=1.29V, RIR=1.2kΩ and attached DAC output resistor=37.5Ω.

●Application example
RGB input mode

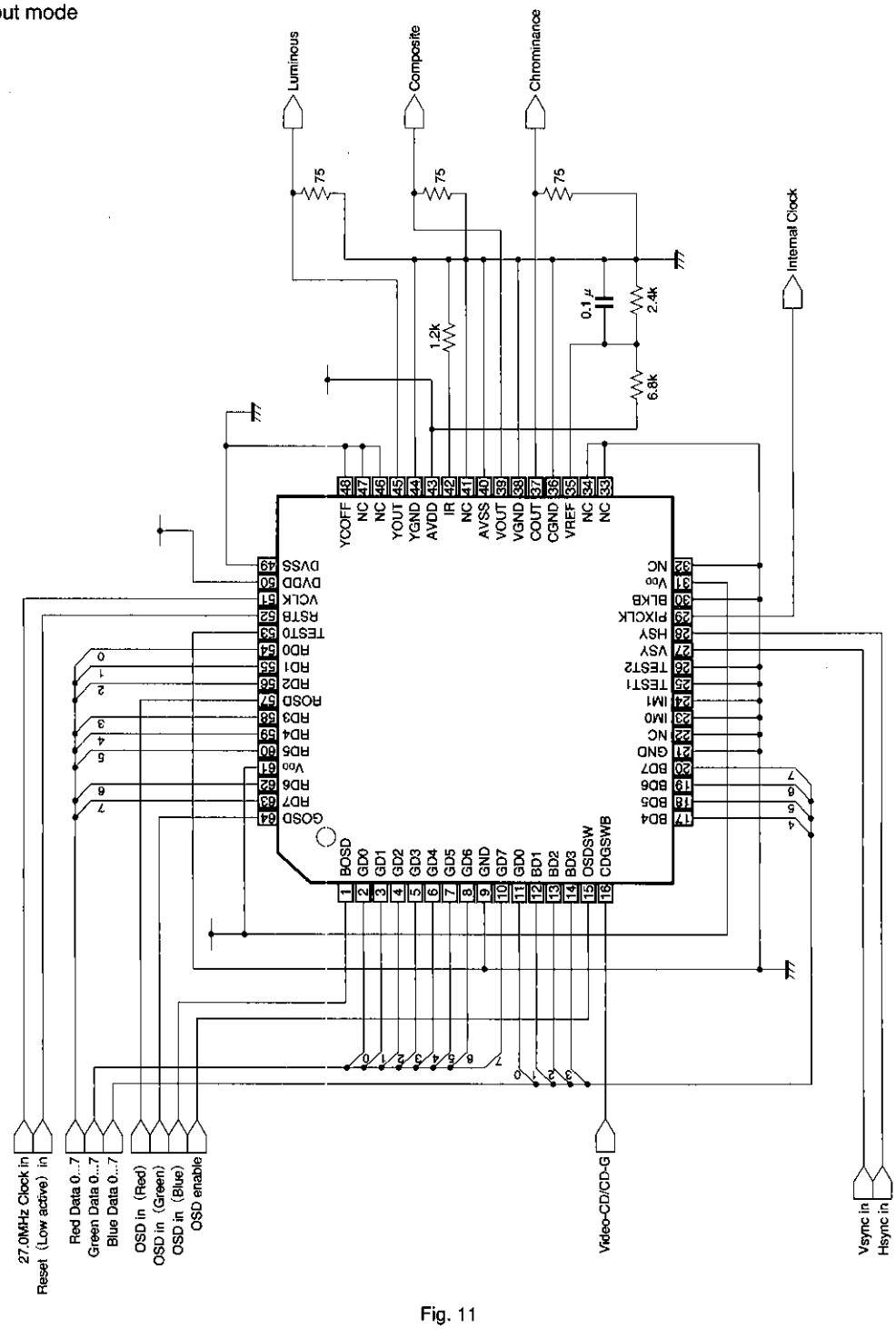
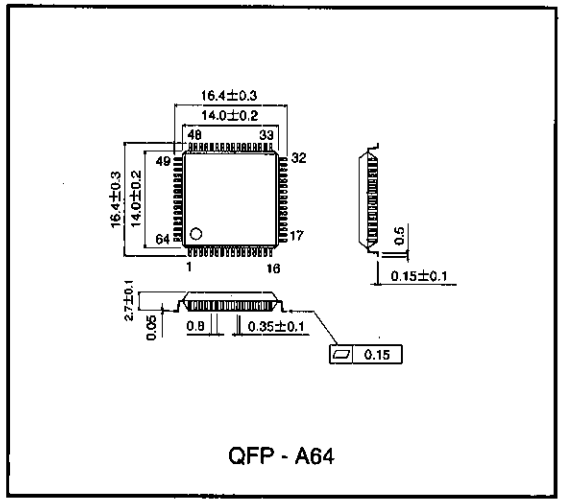


Fig. 11

●External dimensions (Units: mm)



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