# 8-bit shift register and latch driver BU2114/BU2114F

The BU2114 and BU2114F are CMOS ICs with low power consumption, and are equipped with an 8-bit shift register latch. Data in the shift register can be latched asynchronously. The outputs (O1 to O8) are open drain outputs (because there is no protection diode, a maximum voltage above  $V_{DD}$ , of up to 7V, can be applied), and one output can drive 36mA. A total output of up to 150mA can be driven (when using static operation).

#### Applications

Features

sumption.

Logic diagram

2) Open drain output.

These are designed for a wide range of applications in microcomputer peripheral circuits, such as in industrial

1) The CMOS configuration enables low power con-

equipment, office telephones, audio visual equipment, and expansion input and output boards.

- 3) Latch to 8-bit shift register provided, enabling drive of up to 150mA. (IsiNK = 36mA)
- 4) Cascade connections possible.

## ËΝ 009 <u>P</u> CQB R CQB R XQB R LATCH SIN SOUT CQB ÒQB COR CQB cat COE cas СК RST

Serial IN/parallel OUT drivers

**NOHW** 

# BU2114/BU2114F

## Pin layout



## ●Absolute maximum ratings (unless otherwise noted, Ta=25℃)

Parameter		Symbol	Limits	Unit
Applied voltage		VDD	-0.3~7.0	v
Input voltage		Vin	-0.3~Vpd0.3	v
Operating temperature		Topr	-25~75	<u>с</u>
Storage temperature		Tstg	-55~150	°C
Input protection diode current		ID	±20	mA
Power dissipation	BU2114		1100*1	
	BU2114F	- Pd -	400*2	– mW

\*1 Reduced by 8.8 mW for each increase in Ta of 1°C over 25°C.

\*2 Reduced by 3.2 mW for each increase In Ta of 1°C over 25°C.

## ●Recommended operating conditions (unless otherwise noted, Ta=25℃)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Recommend voltage	VDD	4.5	5.0	5.5	v	
Input voltage	Vin	0	—	Vod	v	SIN, CK, LATCH, EN, RST
Output voltage	νουτ	0	_	VDD	v	SOUT

 $\ensuremath{\mathbb{O}}$  Not designed for radiation resistance.

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# BU2114/BU2114F

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
"L" input voltage	V⊫	0	_	1.5	V	SIN, LATCH, EN
"H" input voltage	Vн	3.5		5.0	V	SIN, LATCH, EN
"L" output current	ls∟	_		6	mA	SOUT (VL=0.4)
"H" output current	lsн	_	-	-6	mA	SOUT (VL=VDD-0.4)
Schmitt trigger "H" threshold value	VP	2.31	-	3.28	V	CK, RST
Schmitt trigger "L" threshold value	VN	1.5	· -	2.58	v	CK, RST
Schmitt trigger hysteresis width	Vн	0.35	0.75	-	v	CK, RST
"L" output voltage	Vol Vol	_		0.15 0.4	V V	01~08lp=12mA 01~08lp=36mA
Output leakage current	L	_		±10	μA	
Current consumption	Ισο	_	1	100	μA	Vod or GND
Pull-up resistance	Rup	35	50	68	ΚΩ	
Pull-down resistance	RDN	35	50	68	ΚΩ	

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Pins descriptions

Pin No.	Symbol	1/0	Function
1	SIN	In	Serial data input pin
2	СК	In	Shift clock for shift register
3	LATCH	In	Setting this pin to "L" holds the latch output. While it is "H", latch output changes simultaneously when the shift register output changes.
4	SOUT	Out	This is the output for the final-stage shift register.
5	EN	İn	This is the Enable pin for O1 to O8. When this pin is "L", the latch output appears as is. When the output is "H", however, output QN is "L", and when the latch output is "L", Qn becomes "High- Z"
6	RST	In	Resets the shift register and latch.
7	GND	_	0 V power supply
8	GND	_	0 V power supply
9	GND	_	0 V power supply
10	O8	Out	Latch output for 8th stage of shift register
11	07	Out	Latch output for 7th stage of shift register
12	O6	Out	Latch output for 6th stage of shift register
13	O5	Out	Latch output for 5th stage of shift register
14	O4	Out	Latch output for 4th stage of shift register
15	O3	Out	Latch output for 3rd stage of shift register
16	O2	Out	Latch output for 2nd stage of shift register
17	01	Out	Latch output for 1st stage of shift register
18	Vdd	—	+Vob power supply

Note 1) O1 to O8 are open drain output, and when the shift register output is "H", the output level goes "L".

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# BU2114/BU2114F

●Timing chart (unless otherwise noted, Ta=25℃, VDD=5.0V)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Clock frequency	f	Input duty 50%			5	MHz
Clock pulse width	tow		100	_	_	nsec
Latch pulse width	trw	· · · · ·	100			nsec
Data setup time	tsu	CK → SIN	100	_		nsec
Data hold time	th	CK → SIN	100	_	_	nsec
Clock latch time	tau		100	-	-	nsec



Fig.2 Timing conditions

Serial IN/paraltel OUT drivers

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## BU2114/BU2114F

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Output "L - H" propagation time Input CK to output SOUT	tslн		_	_	100	nsec
Output "H - L" propagation time Input CK to output SOUT	tsplh		_		100	nsec
Output "L - H" propagation time Input CK to output ON	tolh	V⊮=5∨	<u> </u>	_	200	nsec
Output "H - L" propagation time Input CK to output ON	tонL	V⊫=0v	_	_	200	nsec
Output "L - H" propagation time Input EN to output ON	telH		_	_	100	nsec
Output "H - L" propagation time Input EN to output ON	ten.		_	_	100	nsec



Note) Measured with pull-up resistance of 1.0  $k\Omega$  and load of 20 pF applied to terminals O1 to O8.

Fig.3 Switching characteristic

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# BU2114/BU2114F

## •Timing chart

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Fig.4

## ●I/O circuit diagram





Pull-down input

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Serial IN/paratlel OUT drivers

# BU2114/BU2114F

# •External dimensions (Units: mm)



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