Picture cell driver for STN (LCD driver) for low voltage power supplies

BU9718KV

The BU9718KV is a driver IC designed for the character-type STN liquid crystal panels which are ideal for applications such as portable devices. The number of display segments includes 32 output segments and 3 common outputs, enabling drive of up to 96 segments. A compact 48-pin QFP package with a pitch of 0.5 mm is used, enabling compact size for the set as a whole.

●Applications

Portable terminals (POS, ECR, PDA, and others), movie projectors, cameras, telephones (cordless hand-held telephone units), and others Low-voltage power supply sets

●Features

1) Operates on 3V power supply.
2) Low current dissipation. (0.1μA in low power mode (actual value))
3) Compact package. (molded section is 7.0 mm□)
4) Up to 32 segment output pins and 3 common output pins are provided, enabling a total display of up to 96 segments.
5) 1 / 3 duty display.
6) Either 1 / 2 or 1 / 3 bias can be selected for power supply for LCD display.

●Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Pin	Limits	Unit
Power supply voltage*1	V_{DD}	V_{DD}	– 0.3 ~ + 7.0	V
Input voltage*1	V_{IN}	OSC, CS, CK, DI, RES	– 0.3 ~ V_{DD} + 0.3	V
Output voltage*1	V_{OUT}	OSC	– 0.3 ~ V_{DD} + 0.3	V
Output current	I_{SO}	S_1 ~ S_{32}	300	μA
	I_{CO}	COM_1 ~ COM_3	3	mA
Power dissipation	Pd	—	400 *2	mW
Storage temperature	Tstg	—	– 55 ~ + 125	°C

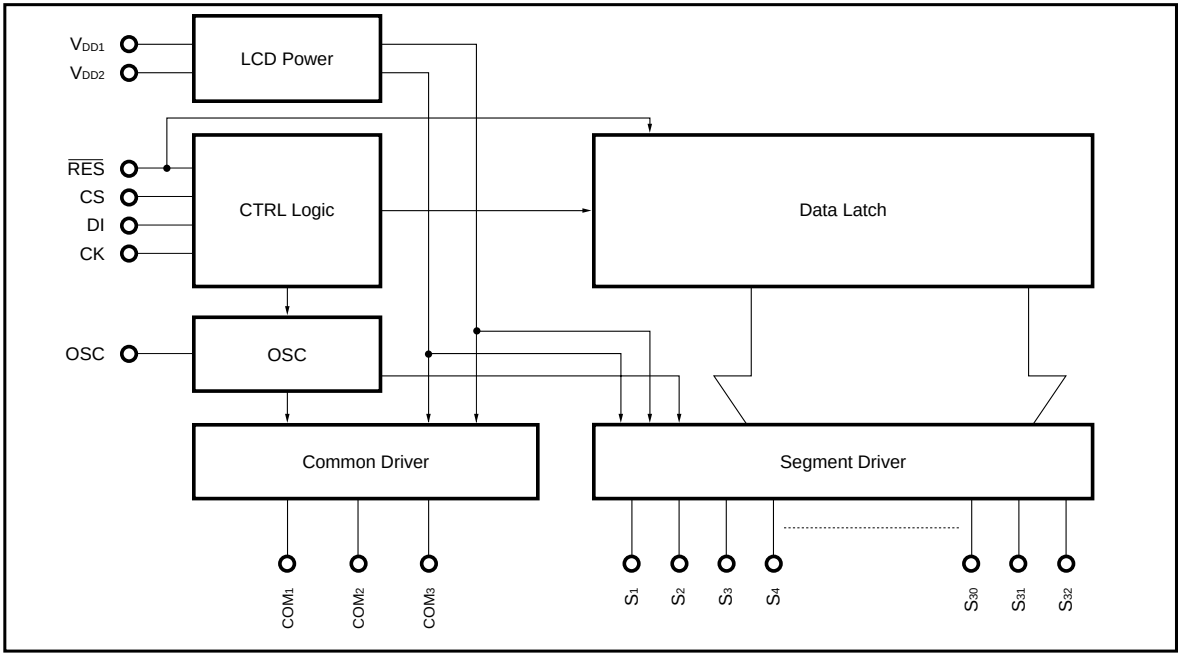
∗1 Max. voltage that can be applied with a V_{SS} pin
∗2 Reduced by 4.0mW for each increase in Ta 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C, V_{SS} = 0V)

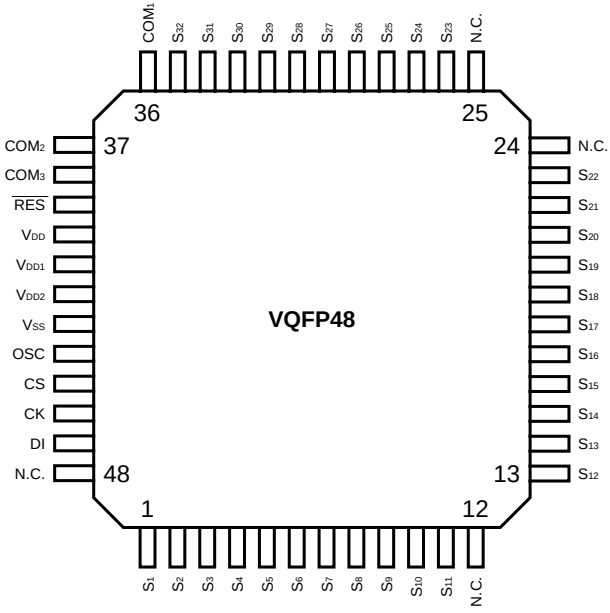
Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit
Power supply voltage*	V_{DD}	V_{DD}	2.7	—	3.5	V
Input voltage*	V_{DD1}	V_{DD1}	0	2 / 3 V_{DD}	V_{DD}	V
	V_{DD2}	V_{DD2}	0	1 / 3 V_{DD}	V_{DD}	V
Oscillation freq., with external input	f_{OSC}	OSC	—	38	100	kHz
External resistance	R	OSC	—	47	—	kΩ
External capacitance	C	OSC	—	1000	—	pF
Operating temperature	Topr	—	– 40	—	85	°C

∗ Indicates the max. voltage that can be applied with a V_{SS} pin.

●Block diagram



●Pin assignments



●Pin descriptions

Pin No.	Pin name	I / O	Function	Processing when not in use
1—11 13—23 26—35	S_1—S_{11} S_{12}—S_{22} S_{23}—S_{32}	O	Segment data output pin; outputs LCD drive voltage that matches COM_1 - COM_3 compatible data	OPEN
36 37 38	COM_1 COM_2 COM_3	O	Common drive output; frame freq. $f_C = (f_{OSC} / 384)$ Hz	V_{SS}
39	$\overline{RES}$	I	Reset input; when $\overline{RES}$ = L, resets internal data (include. control data)	V_{DD}
44	OSC	—	Oscillation pin (for common, segment alternation waves)	V_{SS}
45	CS	I	Chip segment input; when CS = H, data can be transferred	V_{SS}
46	CK	I	Synchronous clock input for serial data transfer	V_{SS}
47	DI	I	Serial data input	V_{SS}
41	V_{DD1}	—	Internal standard voltage for liquid-crystal drive; when using 1 / 2 bias mode, connects to V_{DD2}	OPEN
42	V_{DD2}	—	Internal standard voltage for liquid-crystal drive; when using 1 / 2 bias mode, connects to V_{DD1}	OPEN

● Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 2.7V to 3.5V, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
Input high level voltage	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	—	CS, CK, DI, $\overline{RES}$
Input low level voltage	V_{IL}	0	—	0.2 V_{DD}	V	—	CS, CK, DI, $\overline{RES}$
Input high level current	I_{IH}	0	—	6.0	µA	$V_I = V_{DD}$	CS, CK, DI, $\overline{RES}$
Input low level current	I_{IL}	0	—	6.0	µA	$V_I = V_{SS}$	CS, CK, DI, $\overline{RES}$
Output high level voltage	V_{SOH}	—	V_{DD} – 1.0	—	V	I_O = – 20µA	S_1 ~ S_{32}
	V_{COH}	—	V_{DD} – 1.0	—	V	I_O = – 100µA	COM_1 ~ COM_3
Output low level voltage	V_{SOL}	—	1.0	—	V	I_O = 20µA	S_1 ~ S_{32}
	V_{COL}	—	1.0	—	V	I_O = 100µA	COM_1 ~ COM_3
Output medium level voltage	V_{CM1}	—	1 / 2 V_{DD} ± 1.0	—	V	1 / 2bias	COM_1 ~ COM_3
	V_{SM1}	—	2 / 3 V_{DD} ± 1.0	—	V	1 / 3bias	S_1 ~ S_{32}
	V_{CM2}	—	2 / 3 V_{DD} ± 1.0	—	V	1 / 3bias	COM_1 ~ COM_3
	V_{SM2}	—	1 / 3 V_{DD} ± 1.0	—	V	1 / 3bias	S_1 ~ S_{32}
	V_{CM3}	—	1 / 3 V_{DD} ± 1.0	—	V	1 / 3bias	COM_1 ~ COM_3
Power supply current	I_Q	—	0.1	30	µA	Low-power mode	—
	I_{DD}	—	100	300	µA	f_{OSC} = 38kHz	—

●AC characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 2.7V to 3.5V, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
Guaranteed oscillation range	f_{OSC}	10	38	80	kHz	C = 1000pF R = 47kΩ	OSC
Operating frequency	f_{OSC}	—	—	100	kHz	External input	OSC
Data set-up time	t_{DS}	200	—	—	ns	—	CK, DI
Data hold time	t_{DH}	200	—	—	ns	—	CK, DI
CS set-up time	t_{CS}	200	—	—	ns	—	CS, CK
CS hold time	t_{CH}	200	—	—	ns	—	CS, CK
CK "H" level pulse width	t_{CKH}	200	—	—	ns	—	CK
CK "L" level pulse width	t_{CKL}	200	—	—	ns	—	CK
Rise time	tr	—	—	100	ns	—	CS, CK, DI
Fall time	tf	—	—	100	ns	—	CS, CK, DI

AC timing waveform

(1) When CK is stopped at “L”

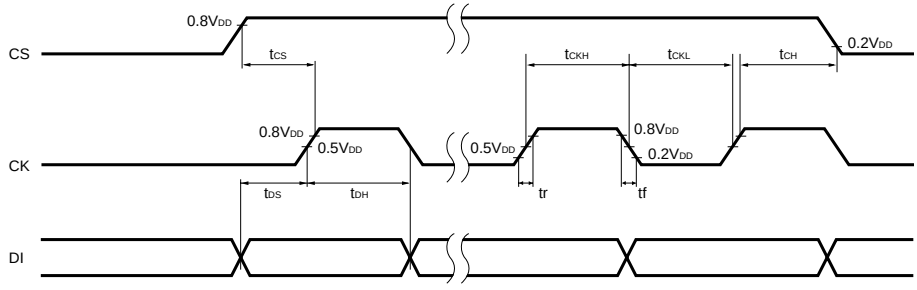


Fig.1

(2) When CK is stopped at “H”

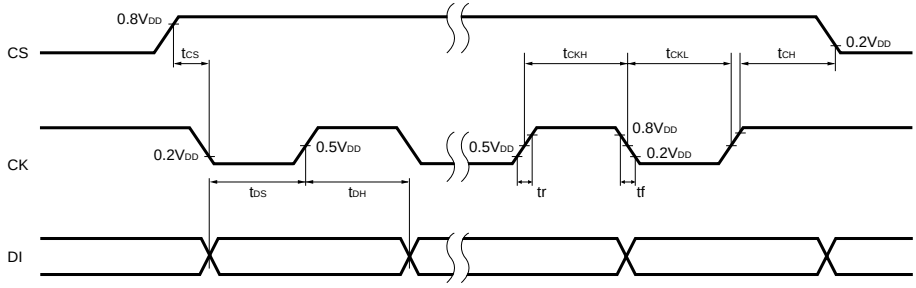


Fig.2

Timing charts

(1) When CK is stopped at “L”

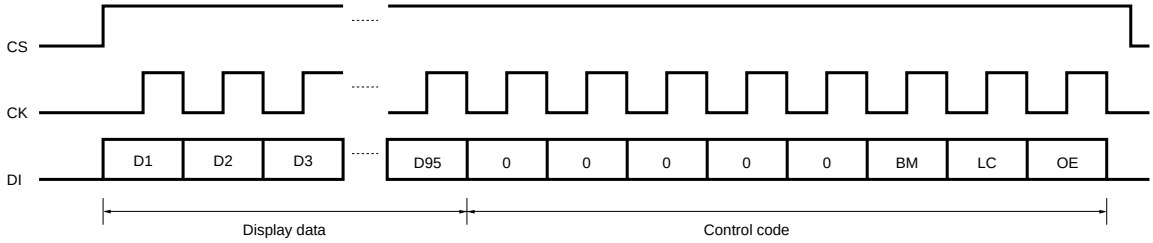


Fig.3

When CS is HIGH, data can be transferred. Data is sent to the shift register at the rising edge of CK. After all of the DI data has been transferred, CS should be set to LOW. The voltage corresponding to the display data transferred at the falling edge of CS is output.

(2) When CK is stopped at “H”

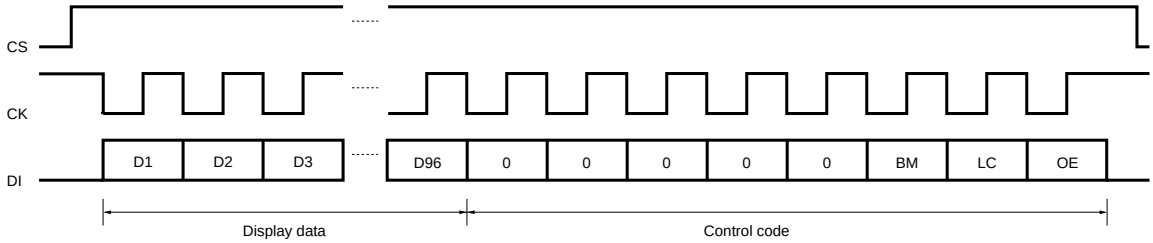


Fig.4

Control code table

OE	Output enable control
0	Normal operation
1	No display; all display data = 0 (internal oscillation circuit is operating)

LC	Low-power mode control
0	Normal operation
1	Low-power mode = internal oscillation circuit has stopped; segment and common output = 0

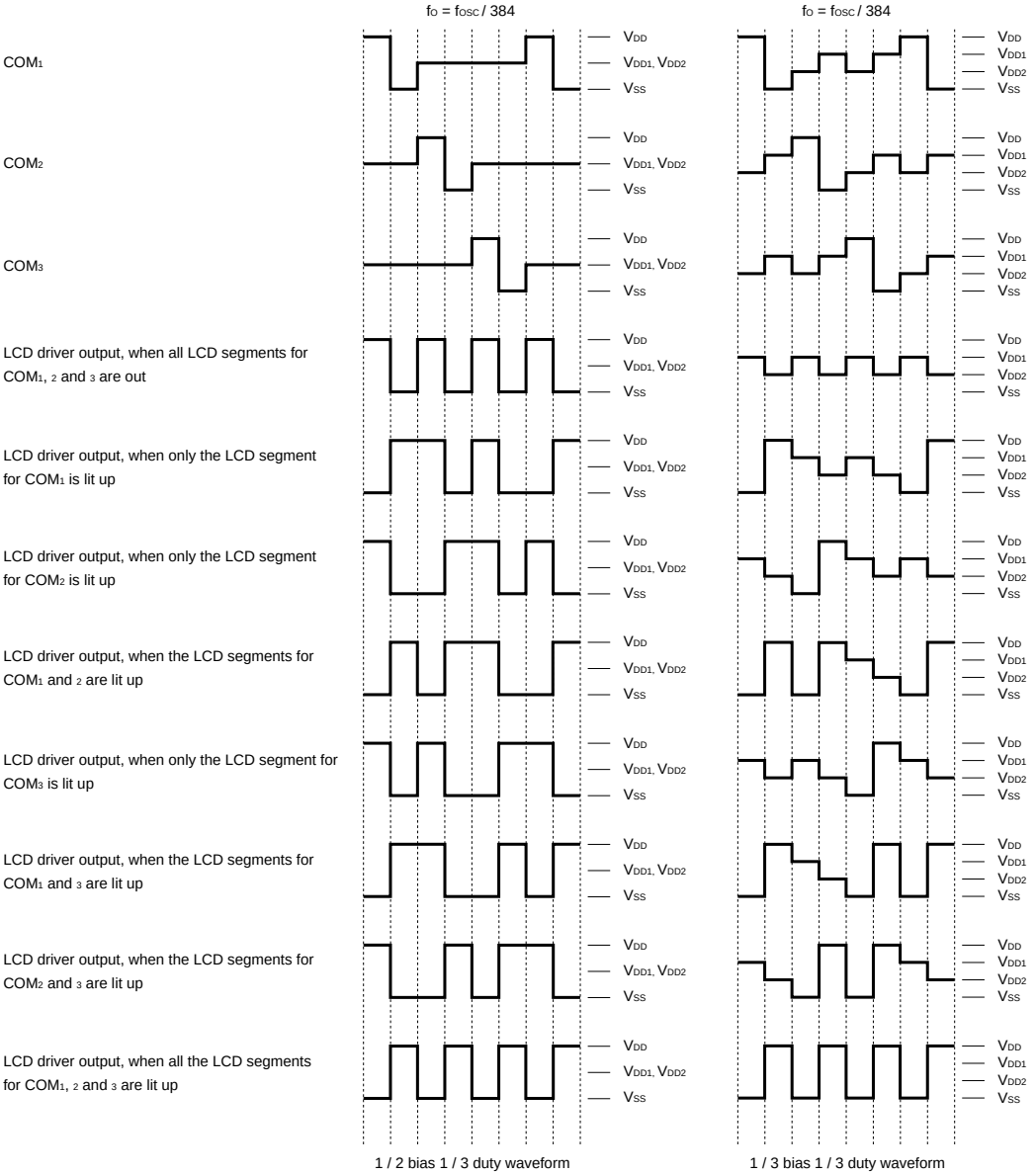
BM	Bias mode control
0	1 / 3 bias
1	1 / 2 bias

Correspondence between display data input and segments

Segment	COM3	COM2	COM1
S1	D1	D2	D3
S2	D4	D5	D6
S3	D7	D8	D9
S4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48

Segment	COM3	COM2	COM1
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96

●Output waveforms



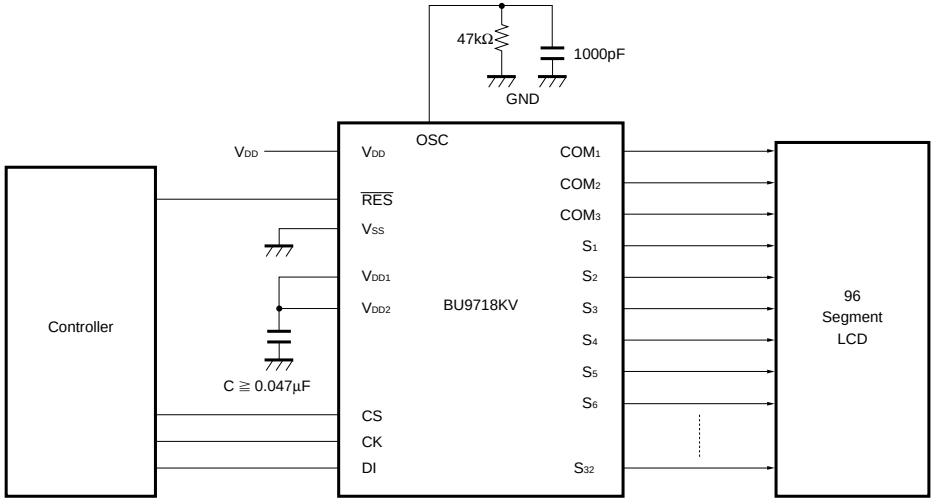
1 / 2 bias 1 / 3 duty waveform

Fig.5

1 / 3 bias 1 / 3 duty waveform

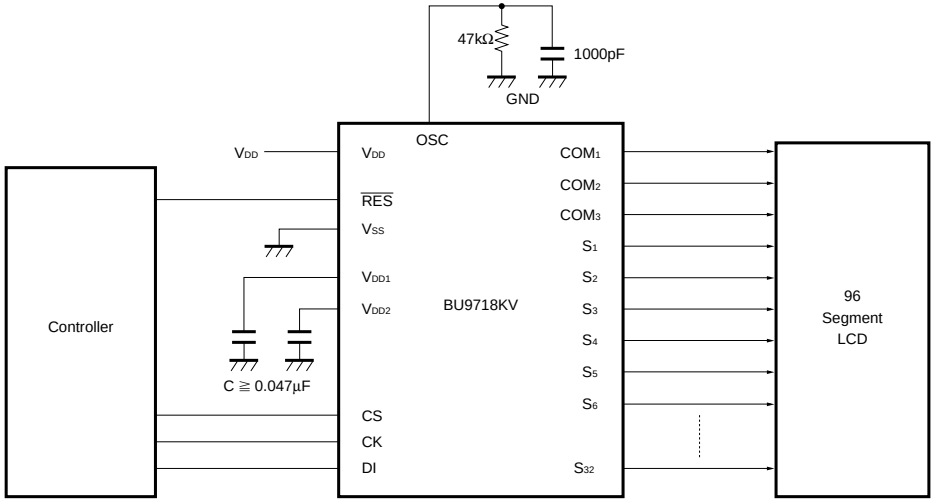
Fig.6

●Application example 1



1 / 2 bias mode

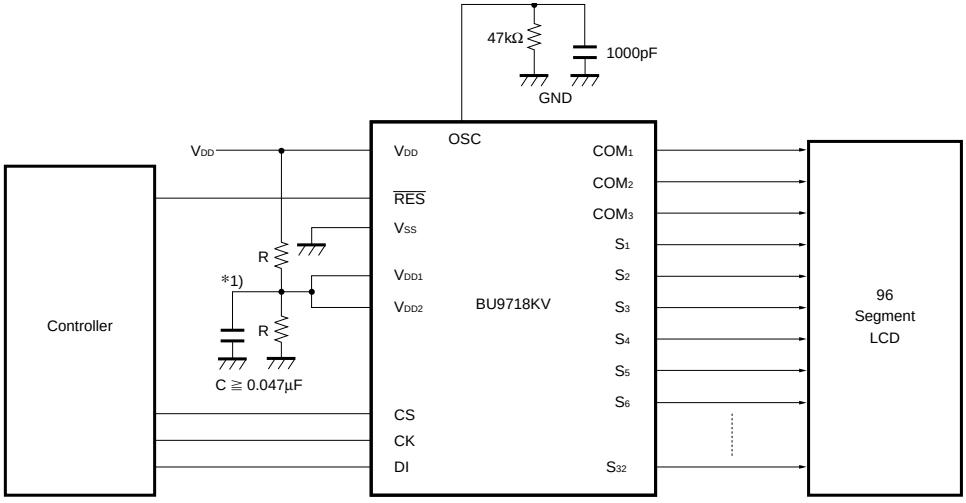
Fig.7



1 / 3 bias mode

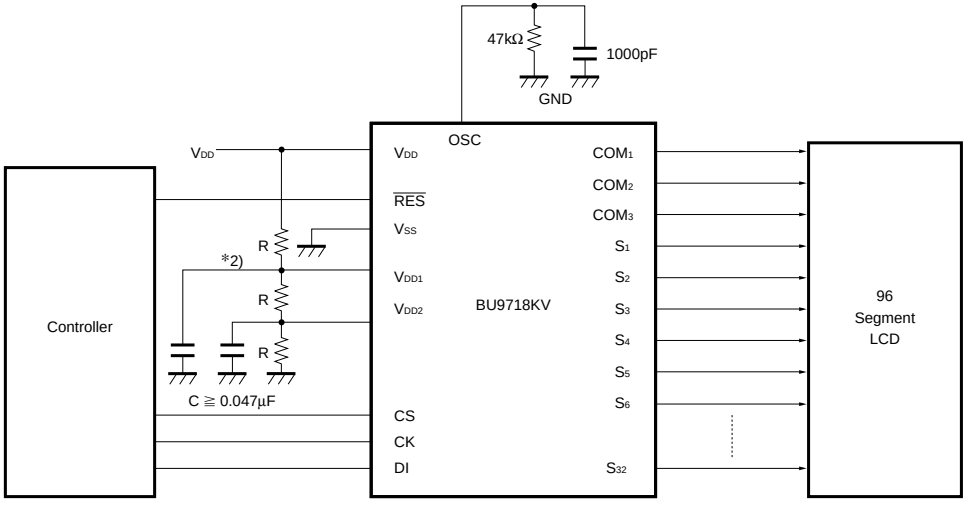
Fig.8

●Application example 2



1 / 2 bias mode

Fig.9



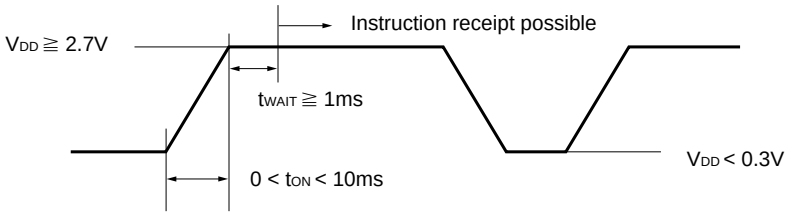
1 / 3 bias mode

Fig.10

Note: The resistance values and capacitance for ∗1 and ∗2 should be set to match the LCD panel, and should be checked using test operation.

Make sure of the following when resetting when the power is on.

- When using the external reset terminal, make $\overline{RST}$ = “L” at 1 ms or more with V_{DD} at 2.7V or more.
- When not using the external reset terminal,V_{DD} has to satisfy the following conditions.



●External dimensions (Units: mm)