CAT8836

NanoPower Supervisory Circuit

Description

The CAT8836 is a voltage supervisory circuit intended to provide circuit initialization and start−up timing for DSPs and other processor−based systems.

When system power comes on, CAT8836's output once the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the output active as long as V_{DD} remains below the threshold voltage of V_{TH}. After V_{DD} exceeds the monitoring threshold an internal timer delays the return of the output to the inactive state (high) to ensure proper system reset.

The duration of this reset delay is controlled by the CT input. When CT is connected to GND the reset delay is 10 ms, typical, in duration and when connected to V_{DD}, the delay time is typically 200 ms. Whenever the supply voltage drops below the monitoring threshold voltage V_{TH}, the output becomes active (low) again.

Features

- Supply Current: 220 nA (typical)
- Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3.0 V, and 3.3 V
- Power−On Reset Generator with Selectable Delay Time: 10 ms or 200 ms
- Push/Pull $\overline{\text{RESET}}$ (active low) Output
- Manual Reset Input
- Pin−for−Pin Replacement for TPS3836
- TSOT23−5 Package
- Temperature Range: −40°C to +85°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Applications Using Low−Power DSPs, Microcontrollers, or Microprocessors
- Portable− and Battery−Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Automotive Systems
- Notebook Computers

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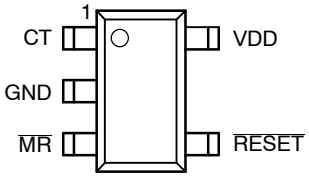
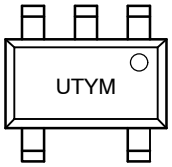
TSOT−23
TD SUFFIX
CASE 419AE

PIN CONNECTIONS



(Top View)

MARKING DIAGRAM



UT = Device Code
Y = Production Year (Last Digit)
M = Production Month: 1−9 (Jan − Sep), O, N, D (Oct − Dec)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

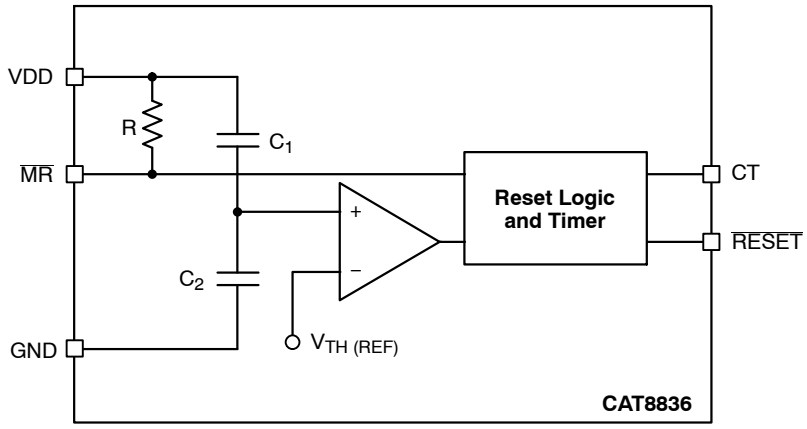


Figure 1. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Description
1	CT	Delay select pin for a fixed value of 10 ms or 200 ms.
2	GND	Ground
3	$\overline{MR}$	Manual Reset
4	$\overline{RESET}$	Active low Reset. Reset is asserted either if VDD falls below reset threshold or if MR is activated.
5	VDD	Supply Voltage which is monitored

Table 2. ABSOLUTE MAXIMUM RATINGS (Over operating free−air temperature range, unless otherwise noted.)

Parameter	Symbol	Value	Unit
Supply voltage (Note 1)	V_{DD}	7	V
All other pins (Note 1)		−0.3 to 6	V
Maximum low output current	I_{OL}	5	mA
Maximum high output current	I_{OH}	−5	mA
Input clamp current, ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	±10	mA
Output clamp current, ($V_O < 0$ or $V_O > V_{DD}$)	I_{OK}	±10	mA
Storage temperature range	T_{STG}	−65 to +150	°C
Soldering temperature		+260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. All voltages are with respect to GND.

Table 3. RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	1.6	5.5	V
Voltage range, CT, $\overline{MR}$ and $\overline{RESET}$ pins		0	V_{DD} + 0.3	V
High−level input voltage	V_{IH}	$0.7 \times V_{DD}$		V
Low−level input voltage	V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\overline{MR}$	$\Delta t/\Delta V$		100	ns/V
Operating temperature range	T_A	−40	+85	°C

2. Refer to Electrical Characteristics and Application Information for Safe Operating Area.

Table 4. ELECTRICAL CHARACTERISTICS (Over recommended operating conditions, unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ high−level output voltage		V_{OH}	V_{DD} = 3.3 V, I_{OH} = −2 mA	0.8 × V_{DD}			V
$\overline{\text{RESET}}$ Low−level output voltage		V_{OL}	V_{DD} = 1.8 V, I_{OL} = 1 mA			0.4	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA				
$\overline{\text{RESET}}$ power−up voltage (Note 3)			$V_{DD} \geq$ 1.1 V, I_{OL} = 50 μA			0.2	V
Negative−going input threshold voltage (Note 4)	CAT8836E18	V_{TH}	T_A = −40°C to +85°C	1.66	1.71	1.74	V
	CAT8836J25			2.18	2.25	2.29	V
	CAT8836H30			2.70	2.79	2.85	V
	CAT8836L30			2.56	2.64	2.69	V
	CAT8836K33			2.84	2.93	2.99	V
Hysteresis at V_{DD} input		V_{HYS}	1.7 V < V_{IT} < 2.5 V		30		mV
			2.5 V < V_{IT} < 3.5 V		40		
Input high−level current	$\overline{\text{MR}}$ (Note 5)	I_{IH}	$\overline{\text{MR}}$ = 0.7 × V_{DD}, V_{DD} = 5.5 V	−40	−60	−100	μA
	CT		CT = V_{DD} = 5.5 V	−25		+25	nA
Input low−level current	$\overline{\text{MR}}$ (Note 5)	I_{IL}	$\overline{\text{MR}}$ = 0 V, V_{DD} = 5.5 V	−130	−200	−340	μA
	CT		CT = 0 V, V_{DD} = 5.5 V	−25		+25	nA
Supply current		I_{DD}	V_{DD} > V_{TH}, V_{DD} < 3 V		220	400	nA
			V_{DD} > V_{TH}, V_{DD} > 3 V		250	450	
			V_{DD} < V_{TH}		10	15	μA
Internal pull−up resistor at $\overline{\text{MR}}$		R_{IN}			30		kΩ
Input capacitance at $\overline{\text{MR}}$ and CT		C_I	V_I = 0 V to V_{DD}		5		pF

3. The lowest voltage at which the $\overline{\text{RESET}}$ output becomes active. t_R, $V_{DD} \geq$ 15 μs/V.
4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminal.
5. If manual reset is unused, $\overline{\text{MR}}$ should be connected to V_{DD} to minimize current consumption.

Table 5. SWITCHING CHARACTERISTICS (At T_A = +25°C, R_L = 1 MΩ, and C_L = 50 pF, unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Delay time		t_{PD}	$V_{DD} \geq V_{TH}$ + 0.2 V, $\overline{\text{MR}}$ = 0.7 × V_{DD}, CT = GND	5	10	15	ms
			$V_{DD} \geq V_{TH}$ + 0.2 V, $\overline{\text{MR}}$ = 0.7 × V_{DD}, CT = V_{DD}	100	200	300	
Propagation (delay) time, high−to−low−level output	V_{DD} to $\overline{\text{RESET}}$ delay	t_{PHL}	V_{IL} = V_{TH} − 0.2 V, V_{IH} = V_{TH} + 0.2 V			10	μs
			V_{IL} = 1.6 V			50	
Propagation (delay) time, high−to−low−level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay	t_{MHL}	$V_{DD} \geq V_{TH}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}			100	ns

Table 6. TIMING REQUIREMENTS (At T_A = +25°C, R_L = 1 MΩ, and C_L = 50 pF, unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse width	at V_{DD}	t_W	V_{IH} = V_{TH} + 0.2 V, V_{IL} = V_{TH} − 0.2 V	6			μs
	at $\overline{\text{MR}}$	t_{WR}	$V_{DD} \geq V_{TH}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			

Table 7. FUNCTION TABLE

$\overline{MR}$	$V_{DD} > V_{TH}$	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

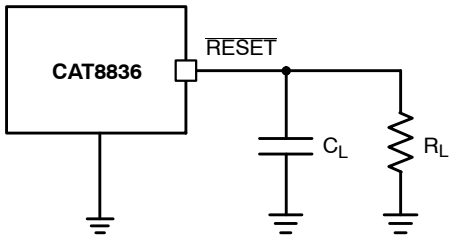


Figure 2. Test Circuit

TIMING DIAGRAM

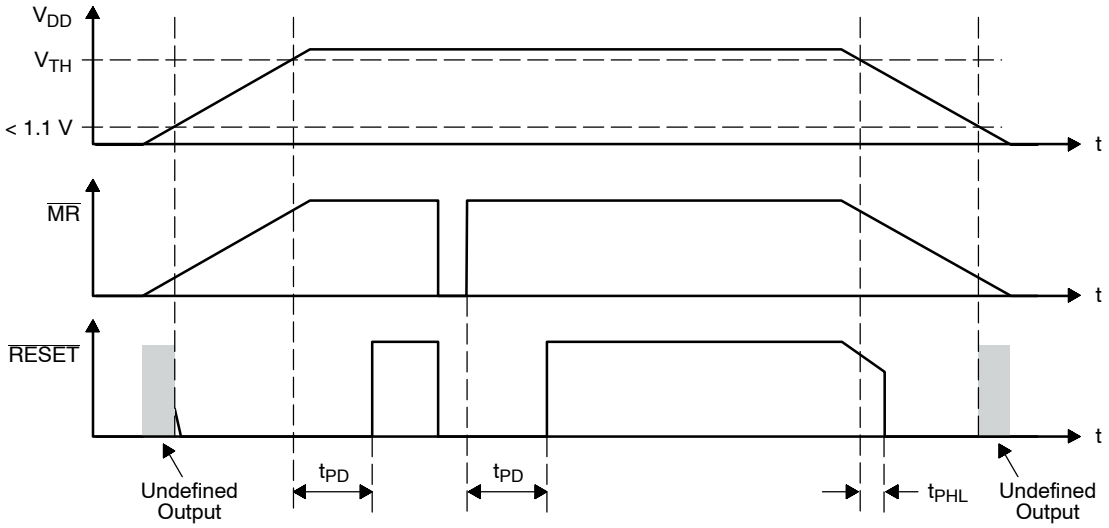


Figure 3. Timing Diagram

TYPICAL CHARACTERISTICS

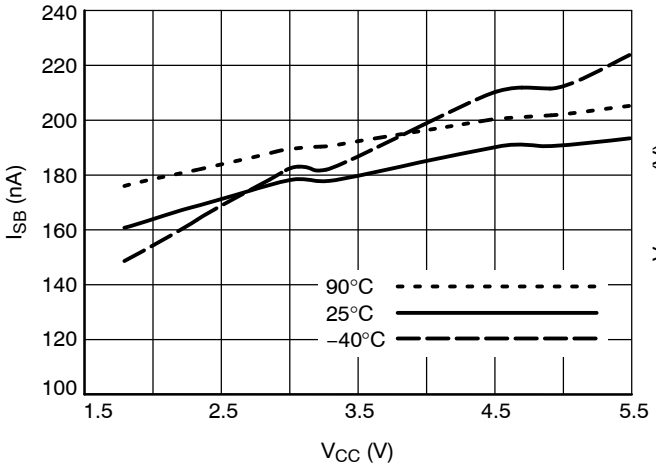


Figure 4. Supply Current vs. Supply Voltage

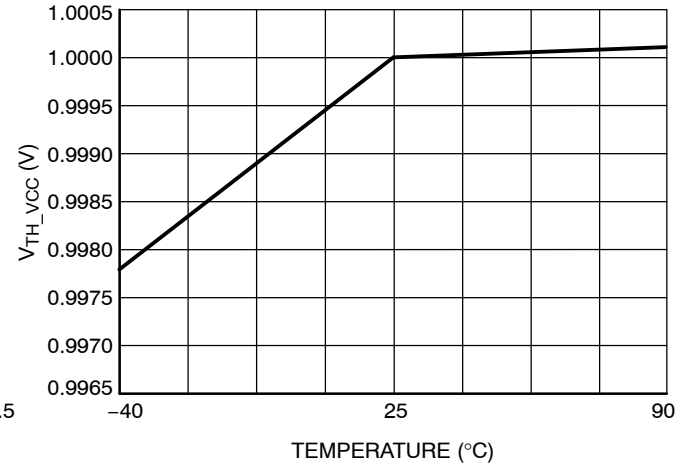


Figure 5. Normalized Reset Threshold Voltage vs. Temperature

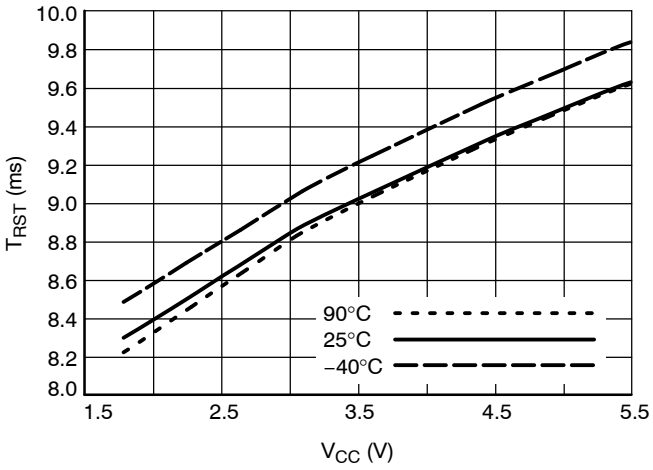


Figure 6. Reset Time Out vs. V_{CC} (CT = 0 V)

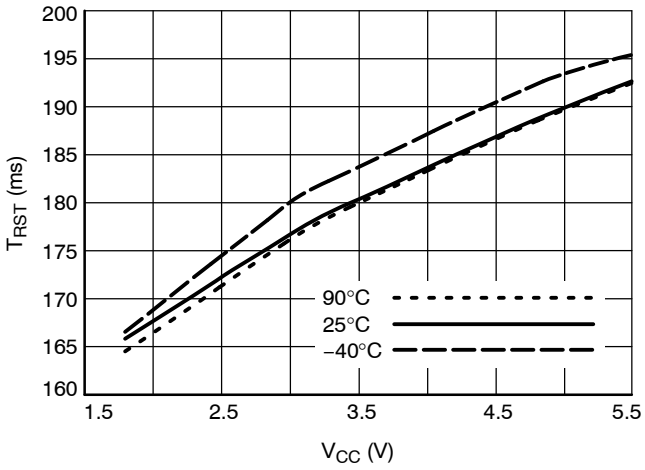


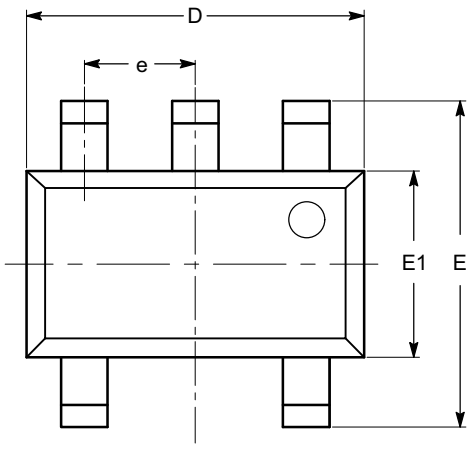
Figure 7. Reset Time Out vs. V_{CC} (CT = 5 V)

Detailed Description

The supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage of V_{TH}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold.

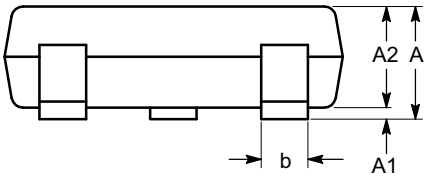
PACKAGE DIMENSIONS

TSOT−23, 5 LEAD
CASE 419AE−01
ISSUE O

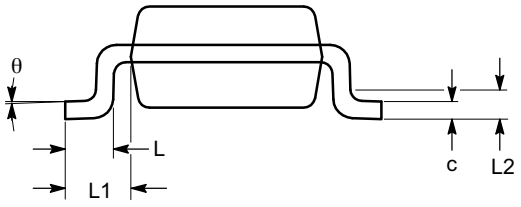


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
θ	0°		8°



SIDE VIEW



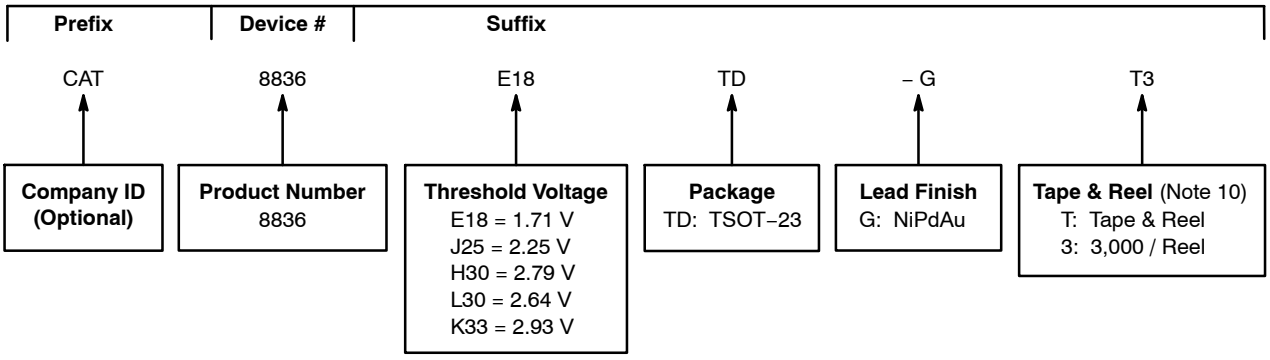
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

Table 8. ORDERING INFORMATION

Device	Nominal Supply Voltage	Threshold Level	Marking	Package	Shipping
CAT8836E18TD−GT3	1.8 V	1.71	UTYM	TSOT−23 (Pb−Free)	3000 / Tape & Reel
CAT8836J25TD−GT3	2.5 V	2.25			
CAT8836H30TD−GT3	3.0 V	2.79			
CAT8836L30TD−GT3	3.0 V	2.64			
CAT8836K33TD−GT3	3.3 V	2.93			

Example of Ordering Information (Notes 6 – 9)



6. All packages are RoHS−compliant (Lead−free, Halogen−free).
7. The standard finish is NiPdAu.
8. The device used in the above example is a CAT8836E18TD−GT3 (CAT8836, 1.71 threshold voltage, TSOT−23, NiPdAu, Tape & Reel, 3,000/Reel).
9. For additional detection voltage, package and temperature options, please contact your nearest ON Semiconductor Sales office.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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