CAT9557

8-Bit I²C-Bus and SMBus I/O Port with Reset

Description

The CAT9557 is a device which provides parallel input/output port expansion for SMBus and I²C−bus applications. The CAT9557 consists of an 8−bit input port register, 8−bit output port register, and an I²C−bus/SMBus interface. It has low current consumption and a high−impedance open−drain output pin, IO0.

The system master can enable the CAT9557's I/O as either input or output by writing to the configuration register. The system master can also invert the CAT9557 inputs by writing to the active HIGH polarity inversion register. Finally, the system master can reset the CAT9557 in the event of a time−out by asserting a LOW in the reset input.

The power−on reset puts the registers in their default state and initializes the I²C−bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without turning off the power to the part.

Features

- Operating Power Supply Voltage Range of 2.3 V to 5.5 V
- 5 V Tolerant Inputs/Outputs
- 400 kHz I²C Bus Compatible
- Low Stand−by Current
- 8 General Purpose Input/Output Expander/Collector
- Input/Output Configuration Register
- Active High Polarity Inversion Register
- Internal Power−on Reset
- Noise Filter on SCL/SDA Inputs
- Active Low $\overline{\text{RESET}}$ Input
- 3 Address Pins Allowing up to 8 Devices on the I²C−bus/SMBus
- High−impedance Open−drain on IO0
- Power−up with All Channels Configured as Inputs
- 16−lead SOIC and TSSOP, and 16−pad TQFN (4 x 4 mm) Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- White Goods (Dishwashers, Washing Machines)
- Handheld Devices (Cell Phones, PDAs, Digital Cameras)
- Data Communications (Routers, Hubs and Servers)

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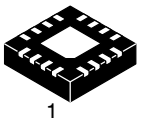
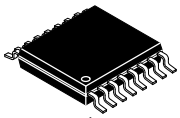
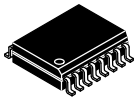


TQFN−16
HV4 SUFFIX
CASE 510AE



TSSOP−16
Y SUFFIX
CASE 948AN



SOIC−16
W SUFFIX
CASE 751BG

MARKING DIAGRAMS

See detailed marking information on page 2 of this data sheet.

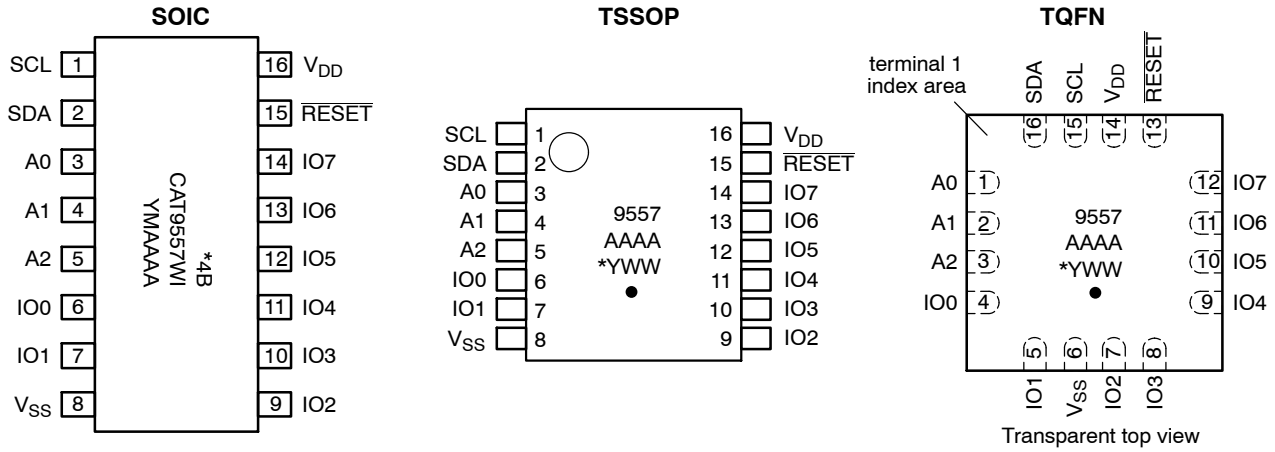
PIN CONNECTIONS

See detailed pin connections information on page 2 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping†
CAT9557WI−GT2	SOIC−16 (Pb−Free)	2,000 / Tape & Reel
CAT9557YI−GT2	TSSOP−16 (Pb−Free)	2,000 / Tape & Reel
CAT9557HV4I−GT2	TQFN−16 (Pb−Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



Special Marking Notes

*: Assembly Location Code
4: NiPdAu Lead Finish
B: Product Revision fixed as “B”
CAT9557W: Product Code
I: Temperature Range (Industrial)
Y: Production Year (Last Digit)
M: Production Month (One Digit):
1−9, (Jan−Sep), O, N, D (Oct−Dec)
AAAA: Last 4 Characters of Assembly Lot Number

Special Marking Notes

9557: Product Code
AAAA: Last 4 Characters of Assembly Lot Number
*: Assembly Location Code
Y: Production Year (Last Digit)
WW: Production Week (Two Digits)
● Pb−free Microdot

Figure 1. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No (SO16, TSSOP16)	Pin No (TQFN16)	Pin Name	Description
1	15	SCL	Serial Clock Line
2	16	SDA	Serial Data Line
3	1	A0	Address Input 0
4	2	A1	Address Input 1
5	3	A2	Address Input 2
6	4	IO0	Input/Output 0 (open−drain)
7	5	IO1	Input/Output 1
8	6 (Note 1)	VSS	Supply Ground
9	7	IO2	Input/Output 2
10	8	IO3	Input/Output 3
11	9	IO4	Input/Output 4
12	10	IO5	Input/Output 5
13	11	IO6	Input/Output 6
14	12	IO7	Input/Output 7
15	13	$\overline{\text{RESET}}$	Active LOW Reset Input
16	14	V_{DD}	Supply Voltage

1. TQFN package die supply ground is connected to both the VSS pin and the exposed center pad. The VSS pin must be connected to the supply ground for proper device operation. For enhanced thermal, electrical, and board−level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

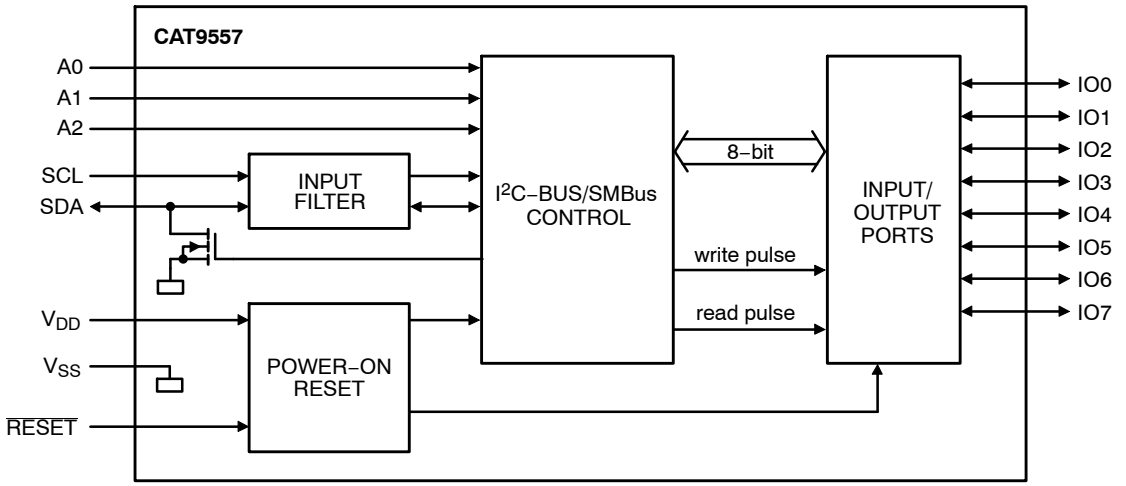
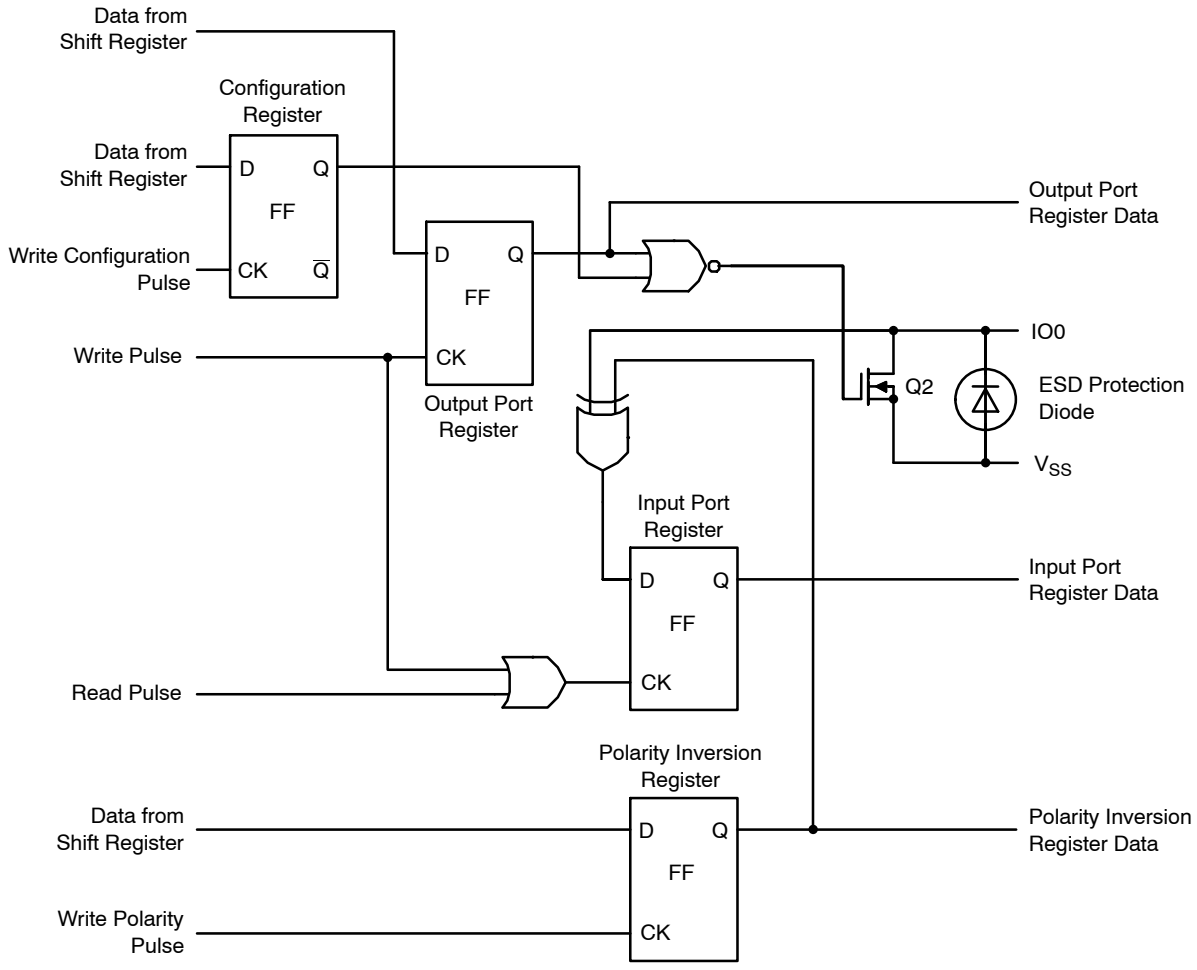
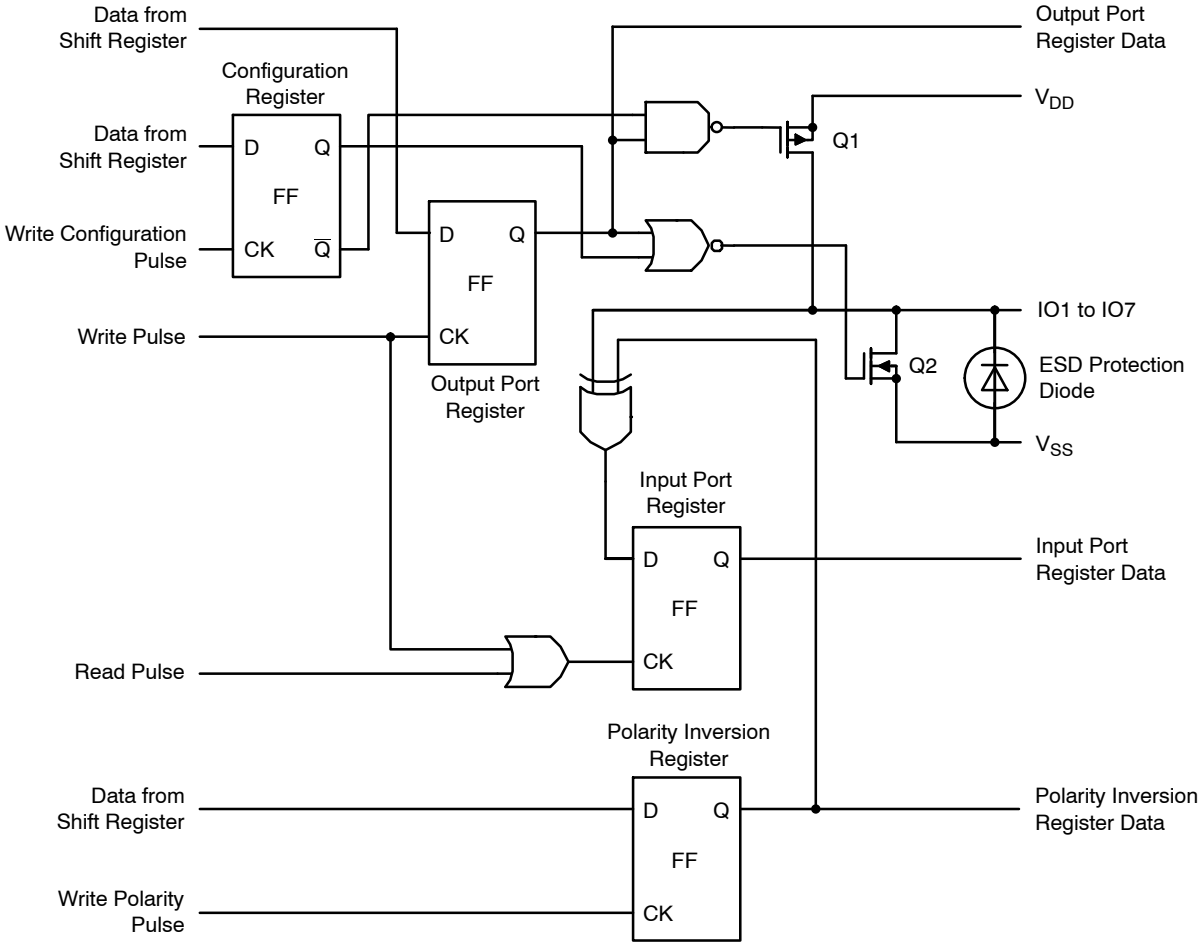


Figure 2. Block Diagram of CAT9557



On power−up or reset, all registers return to default values.

Figure 3. Simplified Schematic of IO0



On power−up or reset, all registers return to default values.

Figure 4. Simplified Schematic of IO1 to IO7

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{DD} with Respect to Ground	−0.5 to +6	V
Voltage on Any Input Pin with Respect to Ground	−0.5 to +5.5	V
DC Output Current on I/O_1 to I/O_7 pins (V_o = 0 to V_{DD})	±50	mA
DC Output Current on I/O_0 pin (V_o = 0 to V_{DD})	+50	mA
DC Output Current on I/O_0 to I/O_7 pins (VI < 0)	−20	mA
DC Input Current (VI < 0)	−20	mA
DC Input Current on I/O_1 to I/O_7 pins (VI < 0 or VI > V_{DD})	±20	mA
DC Input Current on I/O_0 pin (VI < 0)	−20	mA
V_{DD} Supply Current	85	mA
V_{SS} Supply Current	100	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Parameter	Symbol	Reference Test Method	Min	Units
ESD Susceptibility	V_{ZAP} (Note 2)	JEDEC Standard JESD 22	2000	V
Latch−up	I_{LTH} (Notes 2, 3)	JEDEC Standard 17	100	mA

2. This parameter is tested initially and after a design or process change that affects the parameter.
3. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to VDD +1 V.

Table 4. D.C. OPERATING CHARACTERISTICS

(V_{DD} = 2.3 V to 5.5 V; V_{SS} =0 V; T_A = -40°C to +85 °C; unless otherwise specified.)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLIES						
Supply voltage	V_{DD}		2.3	−	5.5	V
Supply current	I_{DD}	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz	−	19	25	μA
LOW−level standby current	I_{stbL}	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs	−	0.25	3	μA
HIGH−level standby current	I_{stbH}	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs	−	0.25	1	μA
Additional standby current	ΔI_{stb}	Standby mode; V_{DD} = 5.5 V; every LED I/O at V_I = 4.3 V; f_{SCL} = 0 kHz	−	0.8	1	mA
Power−on reset voltage (Note 4)	V_{POR}	No load; V_I = V_{DD} or V_{SS}	−	1.65	2.1	V
INPUT SCL, $\overline{\text{RESET}}$; INPUT/OUTPUT SDA						
LOW−level input voltage	V_{IL}		−0.5	−	+0.3V_{DD}	V
HIGH−level input voltage	V_{IH}		0.7V_{DD}	−	V_{DD}	V
LOW−level output current	I_{OL}	V_{OL} = 0.4 V; V_{DD} = 2.3 V	3	−	−	mA
Leakage current	I_L	V_I = V_{DD} or V_{SS}	−1	−	+1	μA
Input capacitance (Note 5)	C_i	V_I = V_{SS}	−	6	10	pF
I/Os						
LOW−level input voltage	V_{IL}		−0.5	−	+0.8	V
HIGH−level input voltage	V_{IH}		2.0	−	5.5	V
LOW−level output current (Note 6)	I_{OL}	V_{OL} = 0.5 V, V_{DD} = 2.3 V	8	10	−	mA
HIGH−level output current (Note 7)	I_{OH}	Except pin I_{O0}; V_{OH} = 2.4 V; V_{DD} = 3 V	−4	−	−	mA
		Pin I_{O0}; V_{OH} = 4.6 V	−	−	1	μA
Input leakage current	I_{LI}	V_{DD} = 5.5 V; V_I = V_{SS}	−	−	−100	μA
Input capacitance (Note 5)	C_i		−	−	5	pF
Output capacitance (Note 5)	C_o		−	−	5	pF
SELECT INPUTS A0, A1, A2						
LOW−level input voltage	V_{ILA}		−0.5	−	+0.8	V
HIGH−level input voltage	V_{IHA}		2.0	−	5.5	V
Input leakage current	I_{LIA}		−1	−	+1	μA

4. V_{DD} must be lowered to 0.2 V in order to reset part.
5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. The total amount sunk by all I/Os must be limited to 100 mA and 25 mA per bit.
7. The total current sourced by all I/Os must be limited to 85 mA and 20 mA per bit.

Table 5. A.C. CHARACTERISTICS (V_{DD} = 2.3 V to 5.5 V; T_A = −40°C to +85°C, unless otherwise specified.) (Note 8)

Parameter	Symbol	Conditions	Standard−mode I²C−bus		Fast−mode I²C−bus		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		0	100	0	400	kHz
Bus free time between a STOP and START condition (Note 9)	t_{BUF}		4.7	–	1.3	–	μs
Hold time (repeated) START condition	$t_{HD;STA}$		4.0	–	0.6	–	μs
Set−up time for a repeated START condition	$t_{SU;STA}$		4.7	–	0.6	–	μs
Set−up time for STOP condition	$t_{SU;STO}$		4.0	–	0.6	–	μs
Data hold time	$t_{HD;DAT}$		0	–	0	–	ns
Data valid acknowledge time (Note 10)	$t_{VD;ACK}$		–	1	–	0.9	μs
Data valid time (Note 11)	$t_{VD;DAT}$		–	1	–	0.9	μs
Data set−up time	$t_{SU;DAT}$		250	–	100	–	ns
LOW period of the SCL clock	t_{LOW}		4.7	–	1.3	–	μs
HIGH period of the SCL clock	t_{HIGH}		4.0	–	0.6	–	μs
Fall time of both SDA and SCL signals (Notes 9 and 12)	t_f		–	300	–	300	ns
Rise time of both SDA and SCL signals (Notes 9 and 12)	t_r		–	1000	–	300	ns
Noise pulse width suppressed at the SCL and SDA inputs (Note 9)	t_{SP}		–	50	–	50	ns
PORT TIMING							
Data output valid time	$t_{v(Q)}$	pin IO0	–	250	–	250	ns
		pins IO1 to IO7	–	200	–	200	ns
Data input set−up time	$t_{su(D)}$		0	–	0	–	ns
Data input hold time	$t_{h(D)}$		200	–	200	–	ns
RESET TIMING							
Reset pulse width	$t_{w(rst)}$		6	–	6	–	ns
Reset recovery time	$t_{rec(rst)}$		0	–	0	–	ns
Reset time	t_{rst}		400	–	400	–	ns

8. Test conditions according to “AC Test Conditions” table.
9. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
10. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
11. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
12. C_b = total capacitance of one bus line in pF.

Table 6. A.C. TEST CONDITIONS

Input Rise and Fall time	≤ 10 ns
CMOS Input Voltages	0.2 V_{DD} to 0.8 V_{DD}
CMOS Input Reference Voltages	0.3 V_{DD} to 0.7 V_{DD}
TTL Input Voltages	0.4 V to 2.4 V
TTL Input Reference Voltages	0.8 V, 2.0 V
Output Reference Voltages	0.5 V_{DD}
Output Load: SDA, $\overline{INT}$	Current Souce I_{OL} = 3 mA; C_L = 100 pF
Output Load: I/Os	Current Source: I_{OL}/I_{OH} = 10 mA; C_L = 50 pF

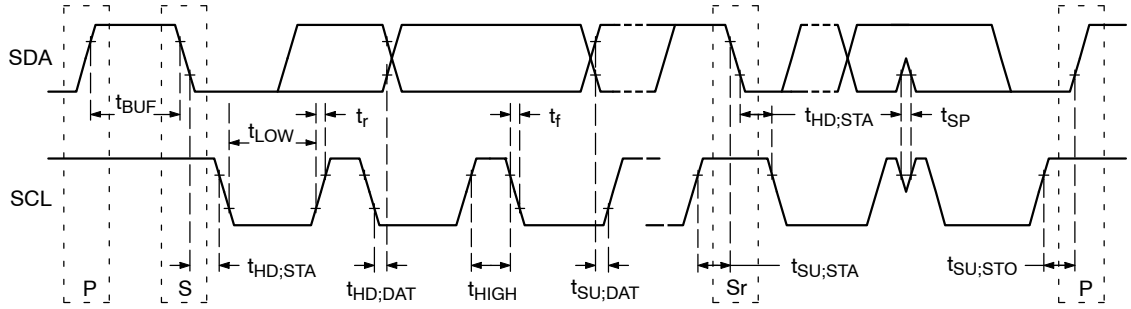


Figure 5. Definition of Timing on the I²C−bus

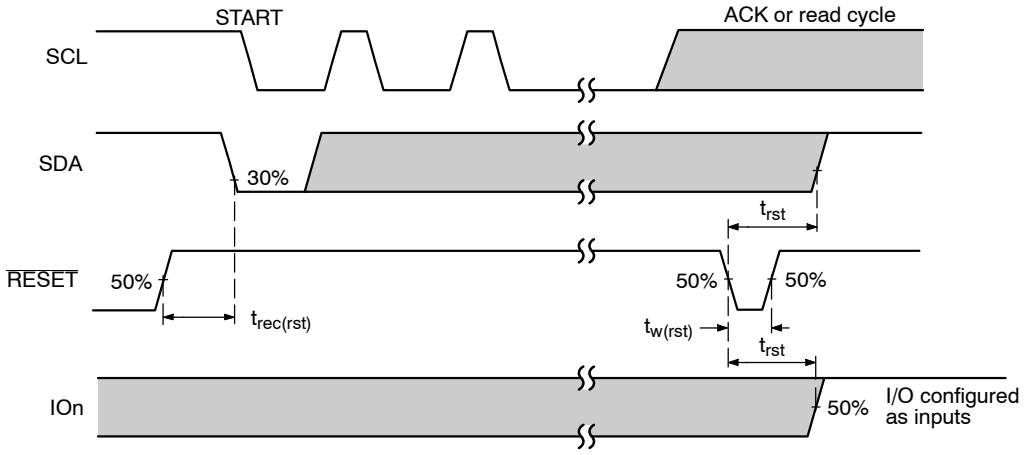


Figure 6. Definition of $\overline{\text{RESET}}$ Timing

PIN DESCRIPTION

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull−up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs. A pull−up resistor must be connected from SDA line to V_{DD}. The value of the pull−up resistor, R_P, can be calculated based on minimum and maximum values from Figures 7 and 8 (see Note 13).

$\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of tw(rst). The CAT9557 registers and SMBus/I^2C−bus state machine will be held in their default state until the RESET input is once again HIGH. This input requires a pull−up resistor to V_{DD} if no active connection is used.

A0, A1, A2: Device Address Inputs

These inputs are used for extended addressing capability. The A0, A1, A2 pins should be hardwired to V_{DD} or V_{SS}. When hardwired, up to eight CAT9557s may be addressed on a single bus system. The levels on these inputs are compared with corresponding bits, A2, A1, A0, from the slave address byte.

I/O_0 to I/O_7: Input / Output Ports

Any of these pins may be configured as input or output. The simplified schematic of I/O_0 is shown in Figure 3 and the simplified schematic of I/O_1 to I/O_7 is shown in Figure 4. When an I/O is configured as an input, the output transistor Q2 from I/O_0 or the output transistors Q1 and Q2 from any of the I/O_1 to I/O_7 are off for that particular I/O. If the I/O pin is configured as an output, the open drain output stage of I/O_0 or the push−pull output stage of I/O_1 to I/O_7 is enabled. Care should be taken if an external voltage is applied to an I/O pin configured as an output due to the low impedance paths that exist between the pin and either V_{DD} or V_{SS}.

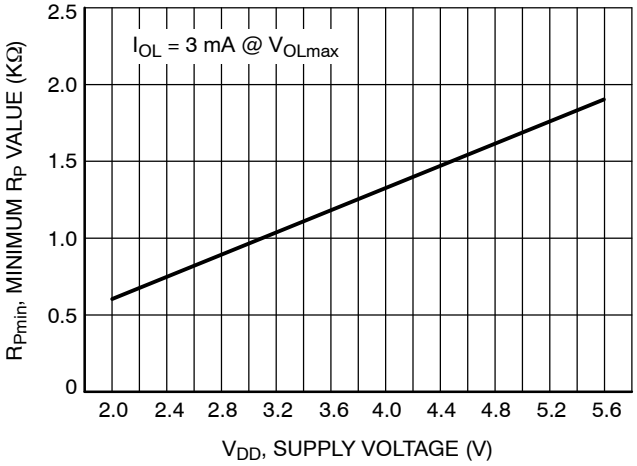


Figure 7. Minimum R_P Value vs. Supply Voltage

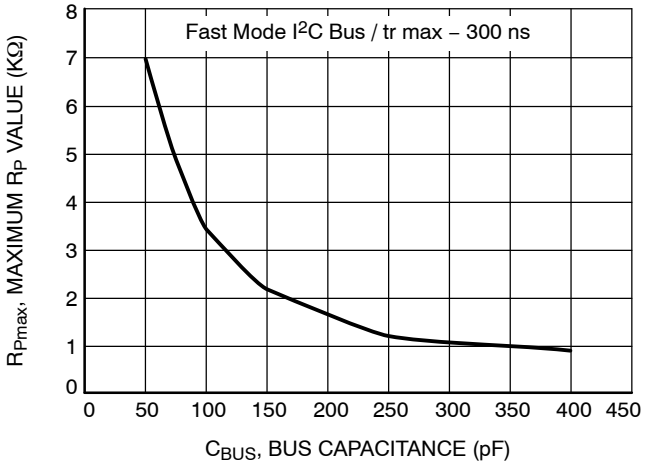


Figure 8. Maximum R_P Value vs. Bus Capacitance

13. According to the Fast Mode I^2C bus specification, for bus capacitance up to 200 pF, the pull up device can be a resistor. For bus loads between 200 pF and 400 pF, the pull−up device can be a current source (I_{max} = 3 mA) or a switched resistor circuit.

FUNCTIONAL DESCRIPTION

The CAT9557 general purpose input / output (GPIO) peripherals provide up to eight I/O ports, controlled through an I^2C compatible serial interface.

The CAT9557 supports the I^2C Bus data transmission protocol. This I^2C Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9557 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 9).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The device monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9557 for a read or write operation. The four most significant bits of the slave address are fixed as binary 0011 (Figure 10). The device uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7−bit slave address is the R/$\overline{W}$ bit that specifies whether a read or write operation is to be performed. When this bit is set to “1”, a read operation is initiated, and when set to “0”, a write operation is selected.

Following the START condition and the slave address byte, the CAT9557 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9557 then performs a read or a write operation depending on the state of the R/$\overline{W}$ bit.

To conserve power, no internal pull−up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

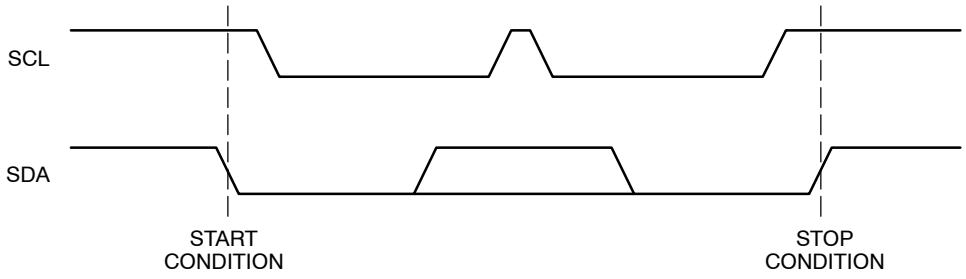


Figure 9. START/STOP Condition

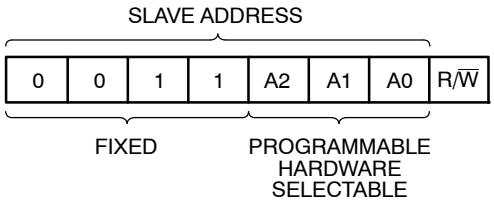


Figure 10. CAT9557 Slave Address

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 9).

The CAT9557 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8–bit byte.

When the CAT9557 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9557 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a STOP condition to return the CAT9557 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

Refer to Figure 2. Block Diagram of CAT9557.

The CAT9557 consists of an input port register, an output port register, a polarity inversion register and a configuration register. Table 7 shows the register address table. Tables 8 to 11 list Register 0 through Register 3 information.

Table 7. REGISTER COMMAND BYTE

Command (hex)	Protocol	Function
0x00	Read byte	Input port register
0x01	Read/write byte	Output port register
0x02	Read/write byte	Polarity inversion register
0x03	Read/write byte	Configuration register

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored. The default value, X, is determined by the externally applied logic level.

Table 8. REGISTER 0 –
Input Port Register Bit Allocation

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	x	x	x	x	x	x	x	x

Table 9. REGISTER 1 –
Output Port Register Bit Allocation

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	0	0	0	0	0	0	0	0

Table 10. REGISTER 2 –
Polarity Inversion Register Bit Allocation

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	1	1	1	1	0	0	0	0

Table 11. REGISTER 3 –
Configuration Register Bit Allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip−flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set (“1”) the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared (“0”), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit to “1” in the configuration register to enable the corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared (“0”), the corresponding port pin is enabled as an output. At power−up, the I/Os are configured as inputs.

Data is transmitted to the CAT9557 registers using the write mode shown in Figure 11 and Figure 12.

The CAT9557 registers are read according to the timing diagrams shown in Figure 13 and Figure 14. Once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte will be sent.

Power−On Reset Operation

When power is applied to V_{DD}, an internal Power−On Reset (POR) holds the CAT9557 in a reset condition until V_{DD} has reached VPOR. At that point, the reset condition is released and the CAT9557 registers and I^2C−bus/SMBus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

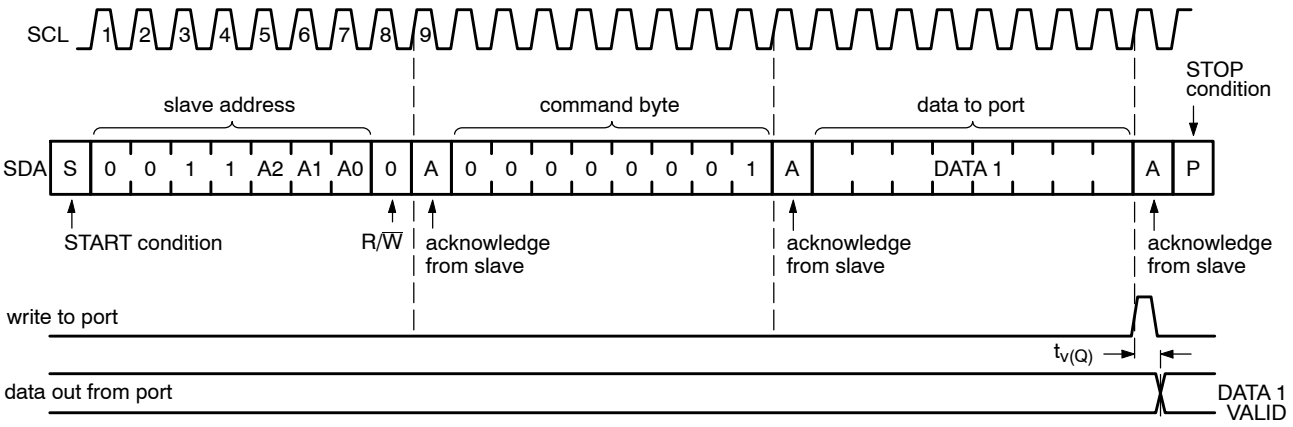


Figure 11. Write to Output Port Register

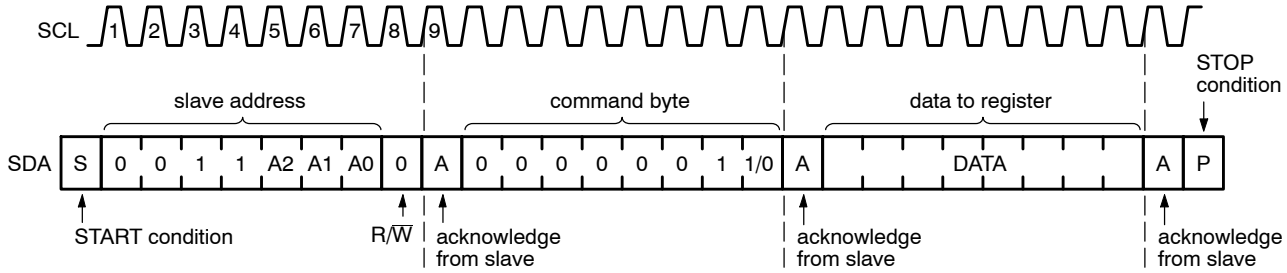


Figure 12. Write to I/O Configuration or Polarity Inversion Registers

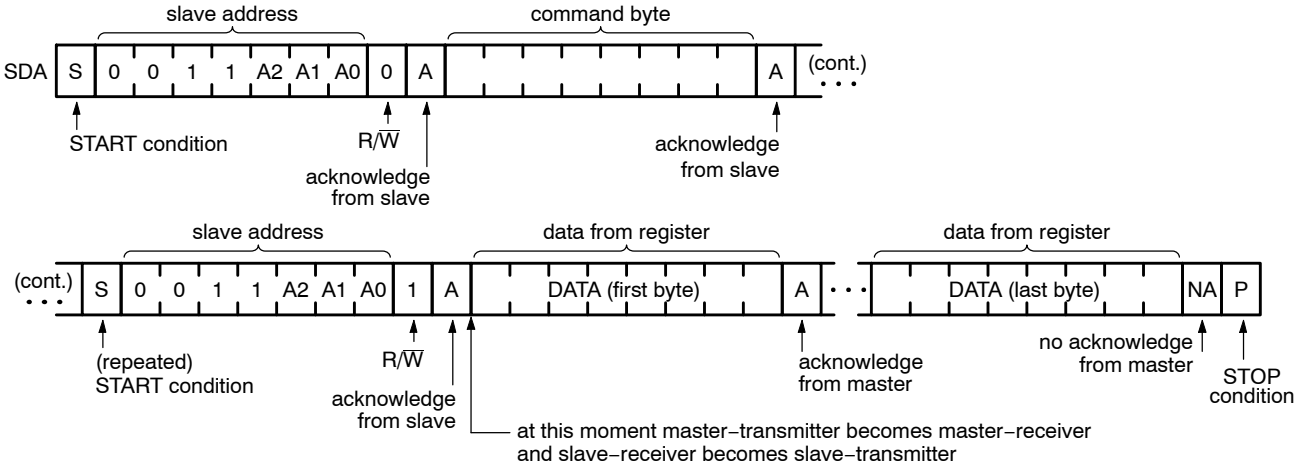
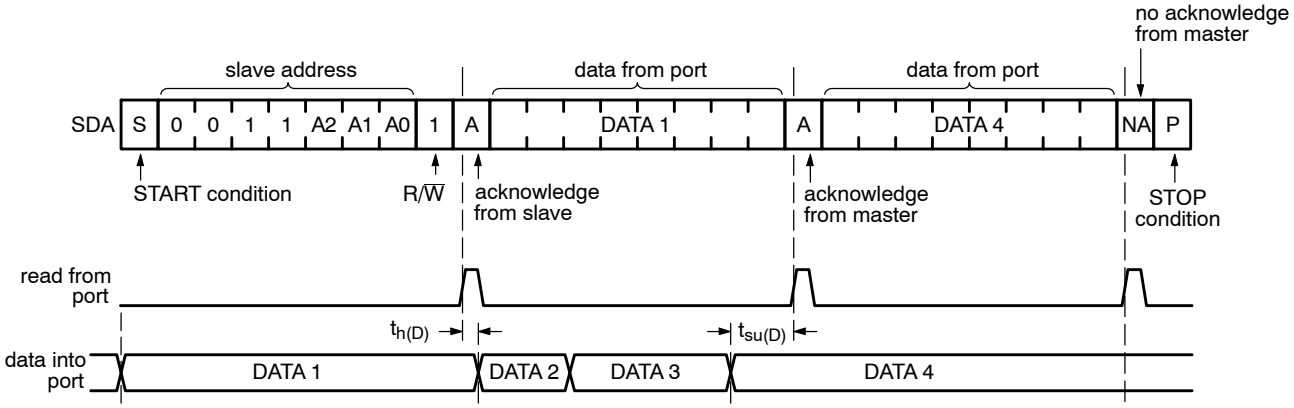


Figure 13. Read from Register

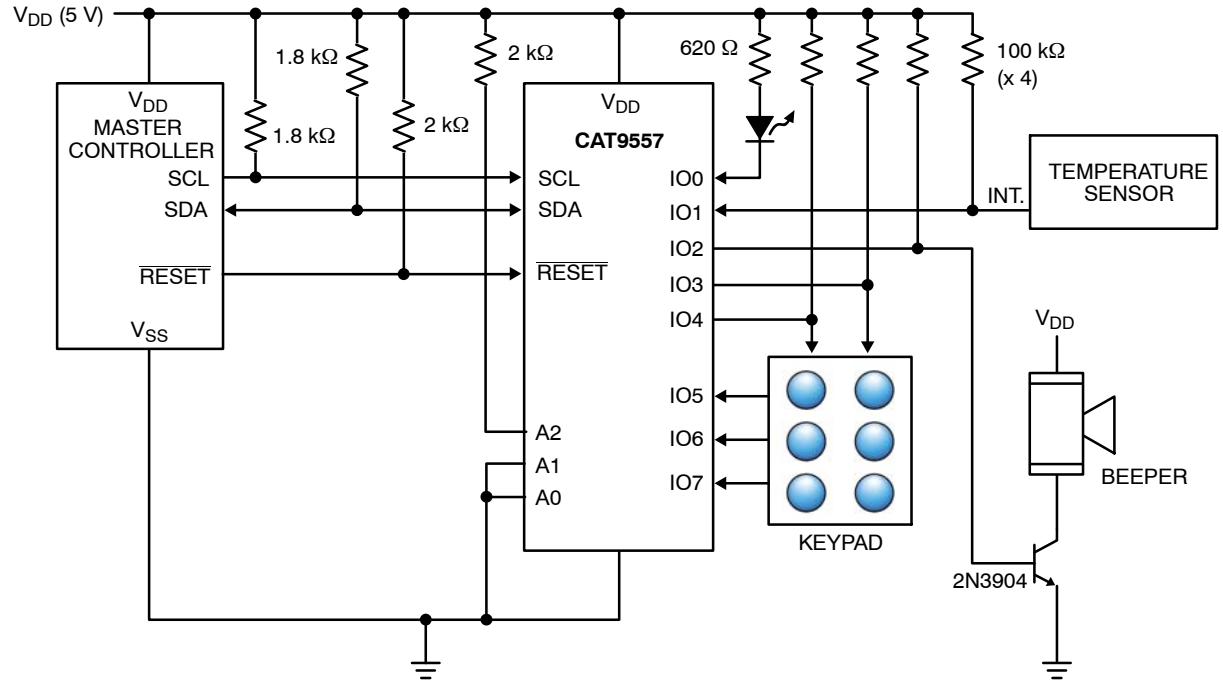


Remark: This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Figure 14. Read Input Port Register

APPLICATIONS INFORMATION



Device address configured as 0011 100x for this example.

IO0, IO2, IO3 configured as outputs.

IO1, IO4, IO5 configured as inputs.

IO6, IO7 are not used.

Figure 15. Typical Application

Minimizing I_{DD} when the I/Os are Used to Control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 15. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 16 shows a high value resistor in parallel with the LED. Figure 17 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.

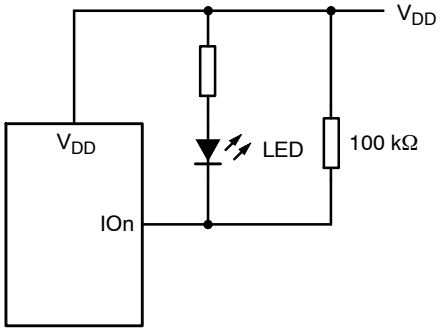


Figure 16. High Value Resistor in Parallel with the LED

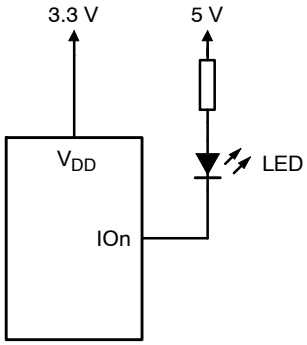
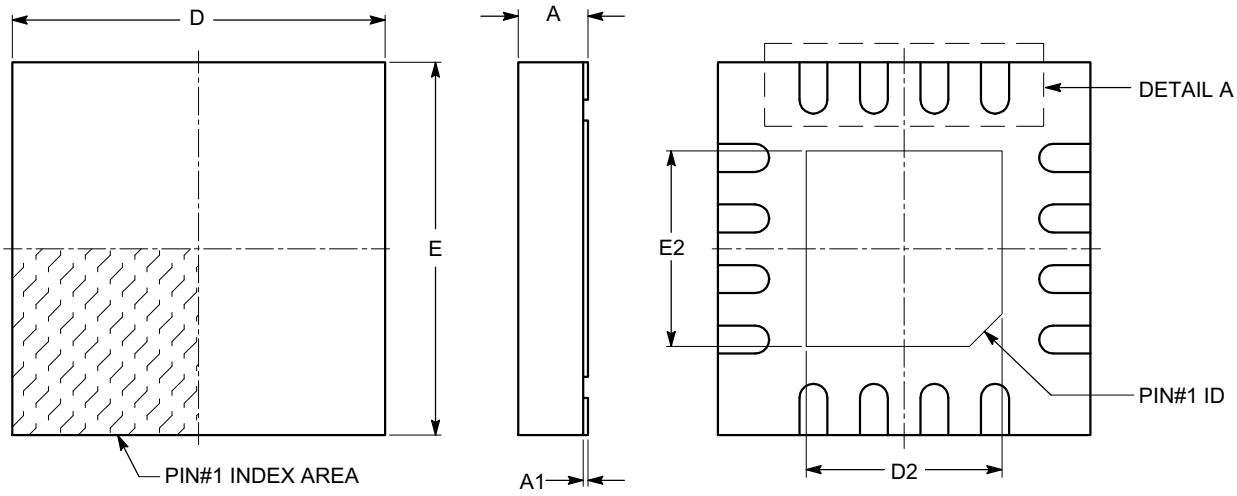


Figure 17. Device Supplied by a Lower Vol

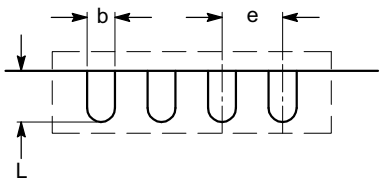
PACKAGE DIMENSIONS

TQFN16, 4x4
CASE 510AE−01
ISSUE A

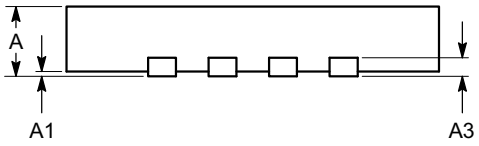


TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	2.00	−−−	2.25
E	3.90	4.00	4.10
E2	2.00	−−−	2.25
e		0.65 BSC	
L	0.45	−−−	0.65



DETAIL A

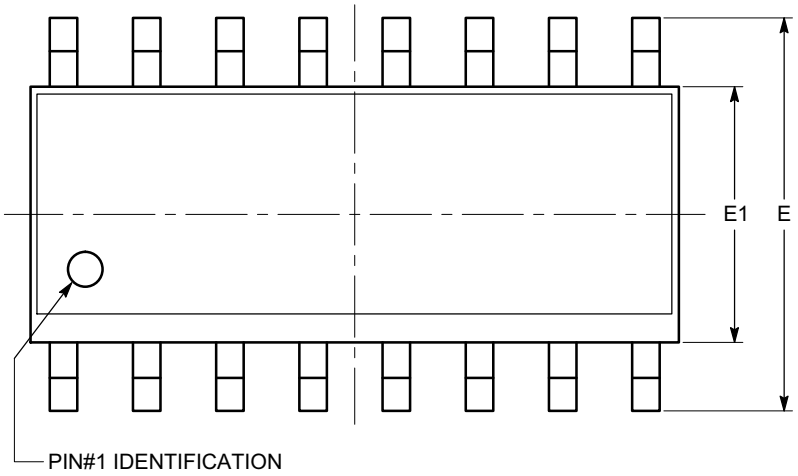


FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-220.

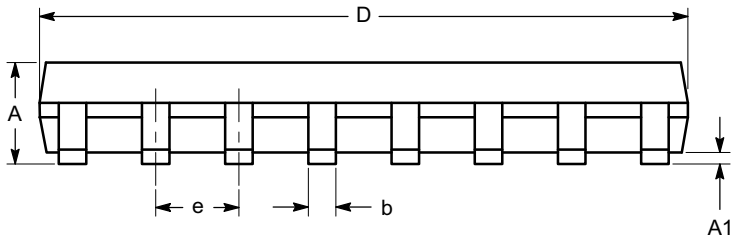
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

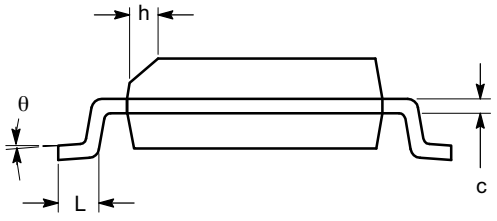


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

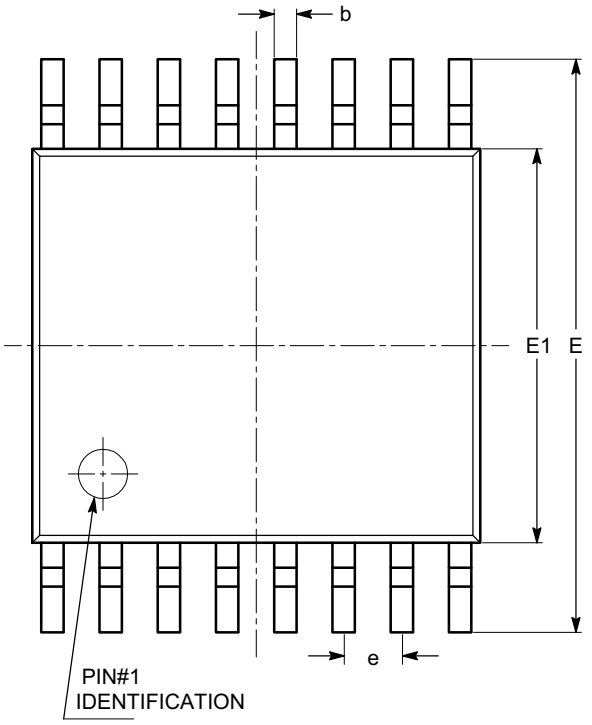


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

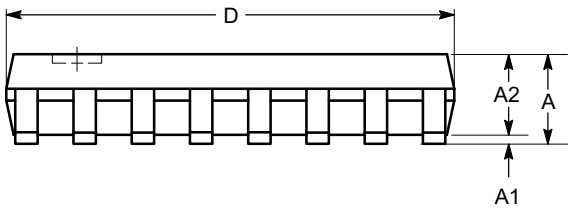
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

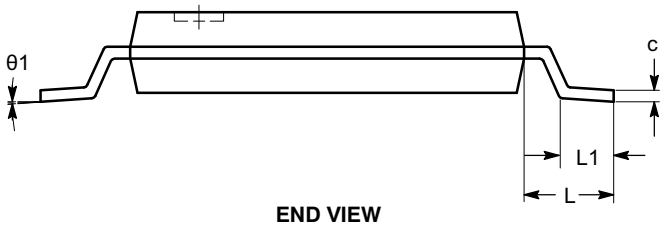


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0º		8º



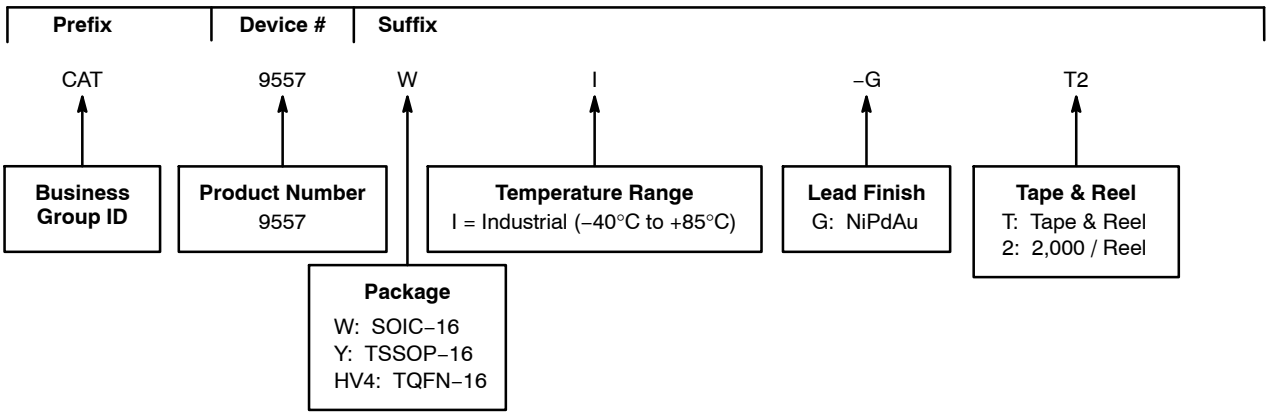
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information (Notes 14 to 17)



14. All packages are RoHS–compliant (Lead–free, Halogen–free).
15. The standard finish is NiPdAu.
16. The device used in the above example is a CAT9557WI–GT2 (CAT9557, SOIC–16, Industrial Temperature, NiPdAu, Tape & Reel, 2,000/Reel).
17. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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