National Semiconductor

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

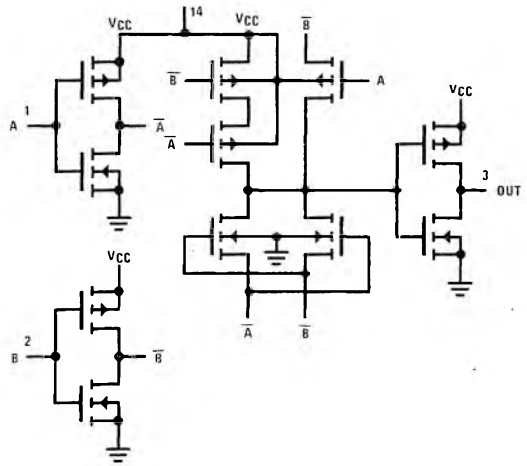
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Low power	100 nW (typ.)
■ Medium speed operation	$t_{PHL} = t_{PLH} = 40$ ns (typ.) at $C_L = 15$ pF, 10 V supply
■ High noise immunity	0.45 V_{CC} (typ.)

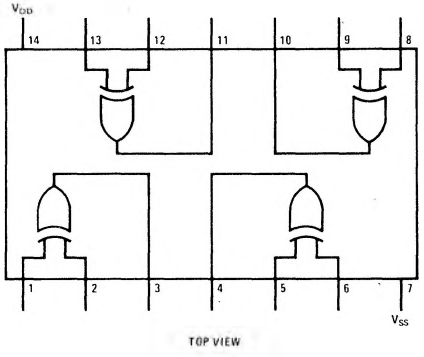
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

Schematic Diagram



Connection Diagram



TOP VIEW

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4030M	−55°C to +125°C
CD4030C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			2.5		0.025	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
	V_{DD} = 10V			0.05		0	0.05			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	V_{DD} = 10V	9.95			9.95	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
	V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.45			−0.3	−0.6		−0.21			mA
	V_{DD} = 10V	−0.95			−0.65	−1.3		−0.45			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

DC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.05	5.0			70	μA
	V_{DD} = 10V			10		0.1	10			140	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		0.25	25			350	μW
	V_{DD} = 10V			100		1.0	100			1,400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
	V_{DD} = 10V			0.05		0	0.05			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	V_{DD} = 10V	9.95			9.95	10		9.95			V
Noise Immunity (All Inputs)(V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0	0.35			0.3	1.2		0.25			mA
	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
	V_{DD} = 10V	−0.45			−0.32	−1.3		−0.25			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		100	200	ns
	V_{DD} = 10V		40	100	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 5.0V		100	200	ns
	V_{DD} = 10V		40	100	ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5.0V		70	150	ns
	V_{DD} = 10V		25	75	ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5.0V		80	150	ns
	V_{DD} = 10V		30	75	ns
Input Capacitance (C_I)	V_I = 0V or V_I = V_{DD}		5.0		pF

AC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		100	300	ns
	V_{DD} = 10V		40	150	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 5.0V		100	300	ns
	V_{DD} = 10V		40	150	ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5.0V		70	300	ns
	V_{DD} = 10V		25	150	ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5.0V		80	300	ns
	V_{DD} = 10V		30	150	ns
Input Capacitance (C_I)	V_I = 0V or V_I = V_{DD}		5.0		pF

Truth Table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level