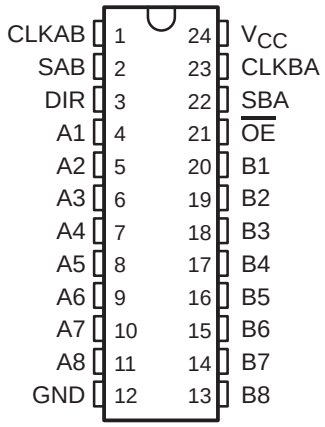
- **BiCMOS Technology With Low Quiescent Power**
- **Buffered Inputs**
- **Noninverted Outputs**
- **Input/Output Isolation From V_{CC}**
- **Controlled Output Edge Rates**
- **64-mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7 V**
- **SCR Latch-Up-Resistant BiCMOS Process and Circuit Design**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (EN) DIP**

EN, M, OR SM PACKAGE
(TOP VIEW)



description

The CD74FCT646 is an octal bus transceiver with 3-state outputs. It consists of D-type flip-flops and control circuitry, arranged for multiplexed transmission of data directly from the input bus or from the internal registers. The device uses a small-geometry BiCMOS technology. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input.

The D-type flip-flops act as internal storage registers on the low-to-high transition of either CLKAB or CLKBA. Output-enable ($\overline{OE}$) and DIR inputs control the transceiver functions. Data present at the high impedance output can be stored in either register, or both; however, only one of the two buses can be enabled as outputs at any one time. The select-control (SAB and SBA) inputs can multiplex stored and transparent (real time) data. The direction control (DIR) determines which data bus receives data when $\overline{OE}$ is low. In the high-impedance state ($\overline{OE}$ high), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the DIR and $\overline{OE}$ terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

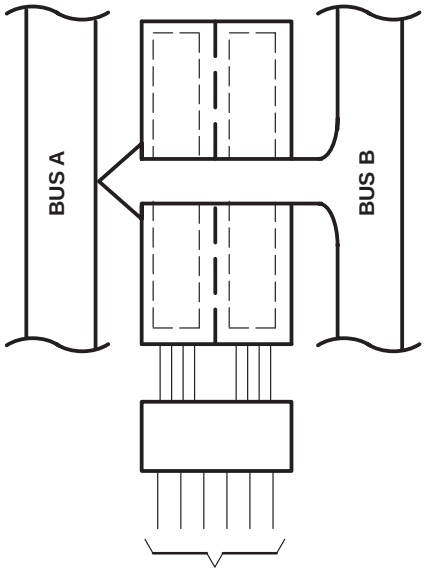
The outputs are a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC}. This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

$\overline{OE}$ and DIR control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either or both registers.

SAB and $\overline{SBA}$ can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

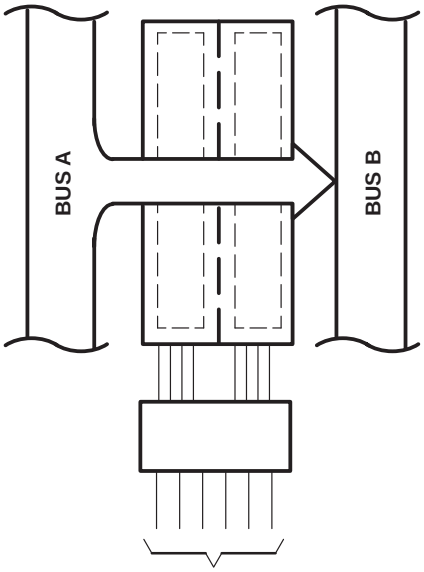
When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

The CD74FCT646 is characterized for operation from 0°C to 70°C.



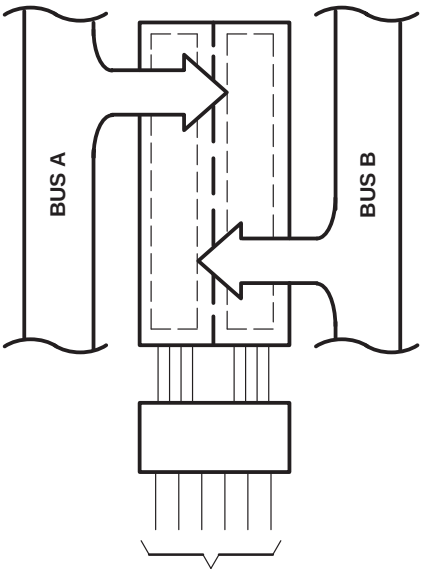
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



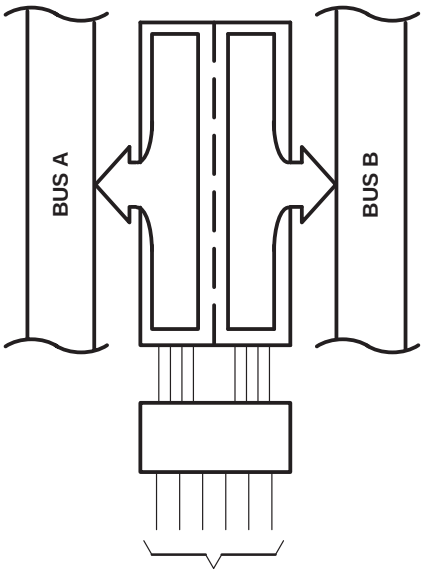
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

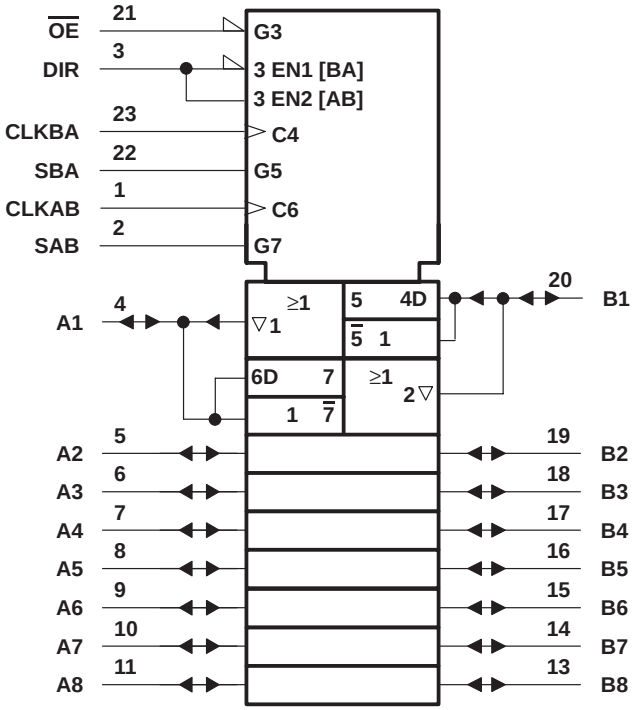
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

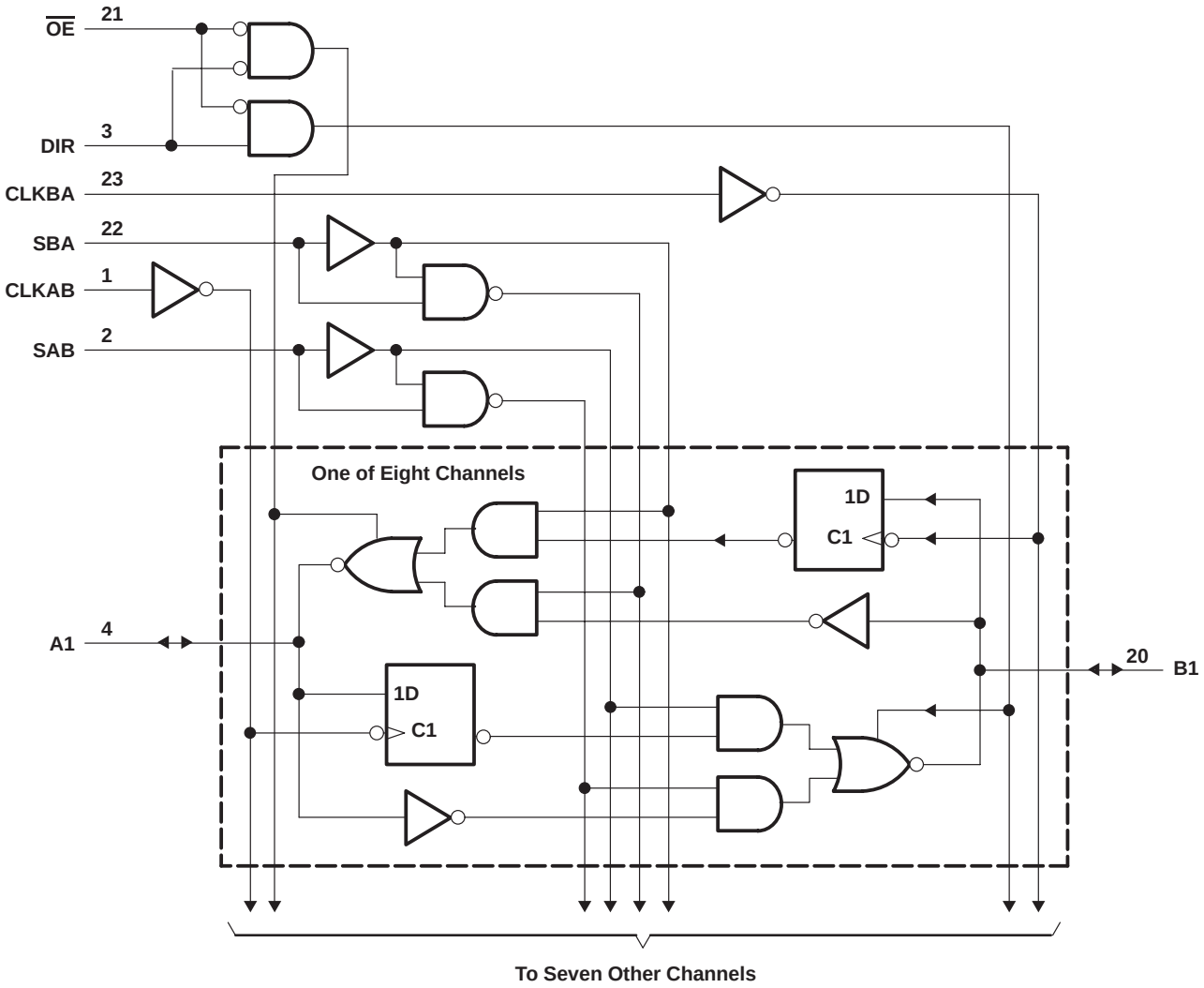
† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
DC input clamp current, I_{IK} (V_I < –0.5 V) . . . . . –20 mA
DC output clamp current, I_{OK} (V_O < –0.5 V) . . . . . –50 mA
DC output sink current per output pin, I_{OL} . . . . . 70 mA
DC output source current per output pin, I_{OH} . . . . . –30 mA
Continuous current through V_{CC}, I_{CC} . . . . . 140 mA
Continuous current through GND . . . . . 528 mA
Package thermal impedance, θ_{JA} (see Note 1): EN package . . . . . 67°C/W
M package . . . . . 46°C/W
SM package . . . . . 61°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
V_{IK}	I_I = –18 mA		4.75 V		–1.2		–1.2	V
V_{OH}	I_{OH} = –15 mA		4.75 V	2.4		2.4		V
V_{OL}	I_{OL} = 64 mA		4.75 V		0.55		0.55	V
I_I	$V_I = V_{CC}$ or GND		5.25 V		±0.1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND		5.25 V		±0.5		±10	µA
I_{OS}‡	$V_I = V_{CC}$ or GND,	V_O = 0	5.25 V	–60		–60		mA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.25 V		8		80	µA
ΔI_{CC}§	One input at 3.4 V, Other inputs at V_{CC} or GND		5.25 V		1.6		1.6	mA
C_i	$V_I = V_{CC}$ or GND				10		10	pF
C_o	$V_O = V_{CC}$ or GND				15		15	pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

§ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			85	MHz
t_w	Pulse duration	CLKBA or CLKAB high or low	6		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	2		ns

switching characteristics over recommended operating temperature conditions (unless otherwise noted) (see Figure 2)

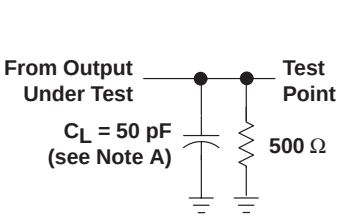
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C TYP	MIN	MAX	UNIT
f_{max}				85		MHz
t_{pd}	CLKBA or CLKAB	A or B	6.8	2	9	ns
	A or B	B or A	6.8	2	9	
	SBA or SAB†	A or B	8.3	2	11	
t_{en}	$\overline{OE}$	A or B	10.5	2	14	ns
t_{dis}	$\overline{OE}$	A or B	6.8	2	9	ns

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

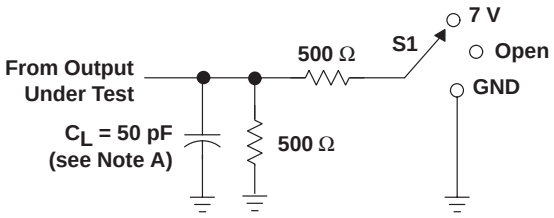
noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		0.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

PARAMETER MEASUREMENT INFORMATION

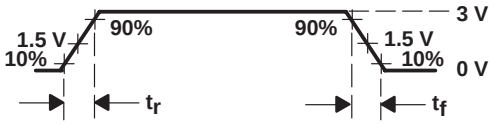


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

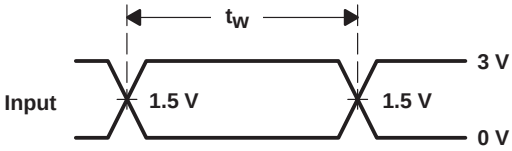


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

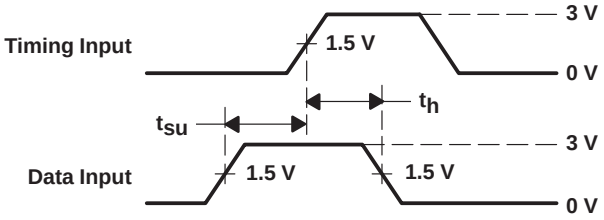
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Drain	7 V



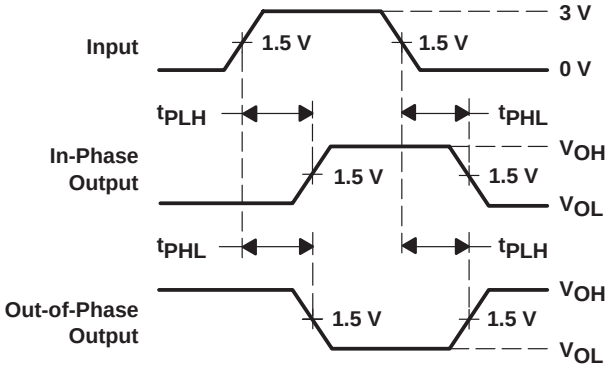
VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



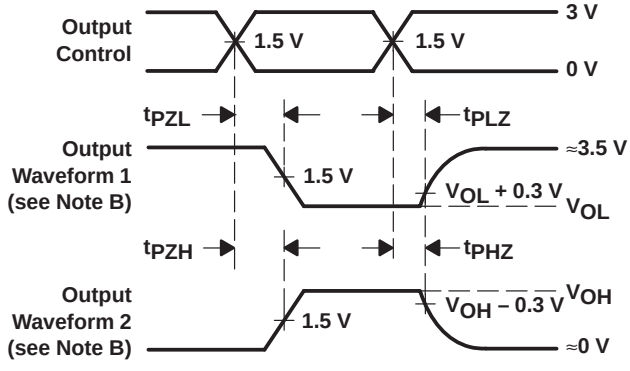
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r and t_f = 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CD74FCT646EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available
CD74FCT646M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
CD74FCT646M96	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
CD74FCT646SM	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	Samples Not Available

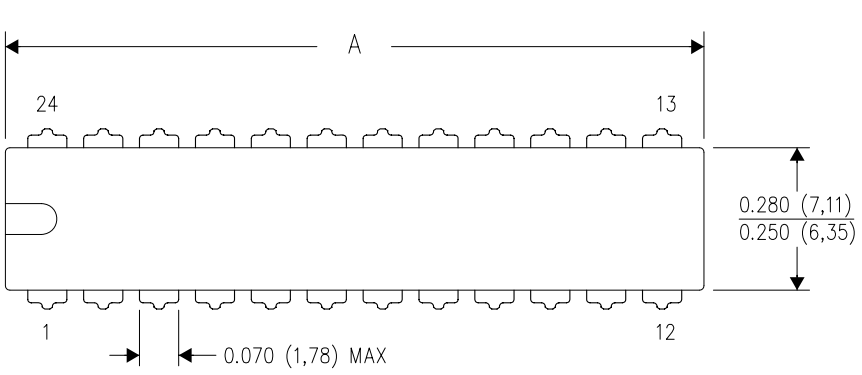
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

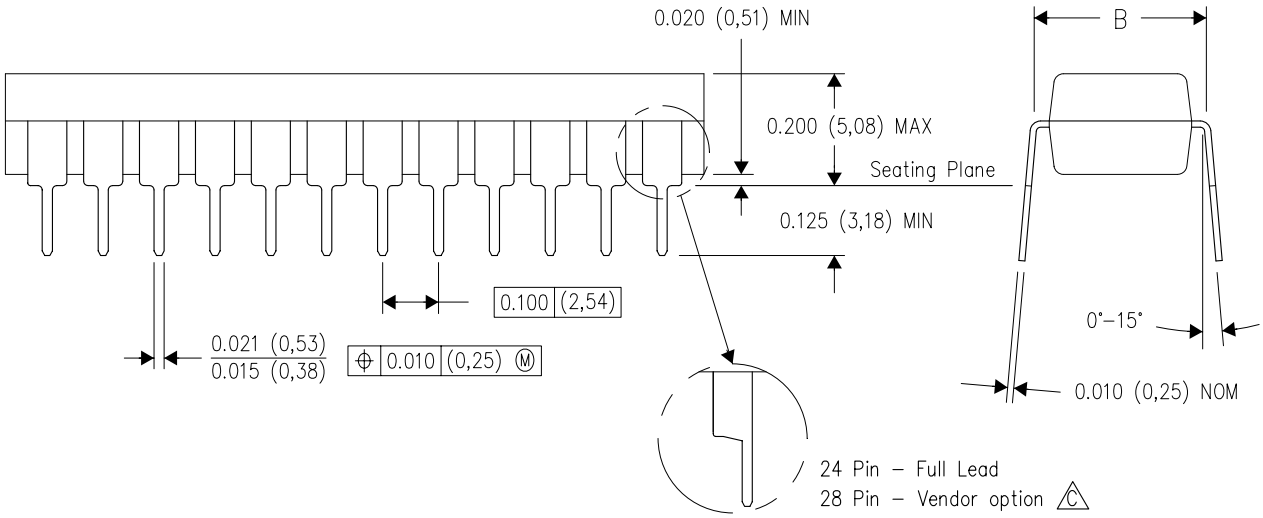
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



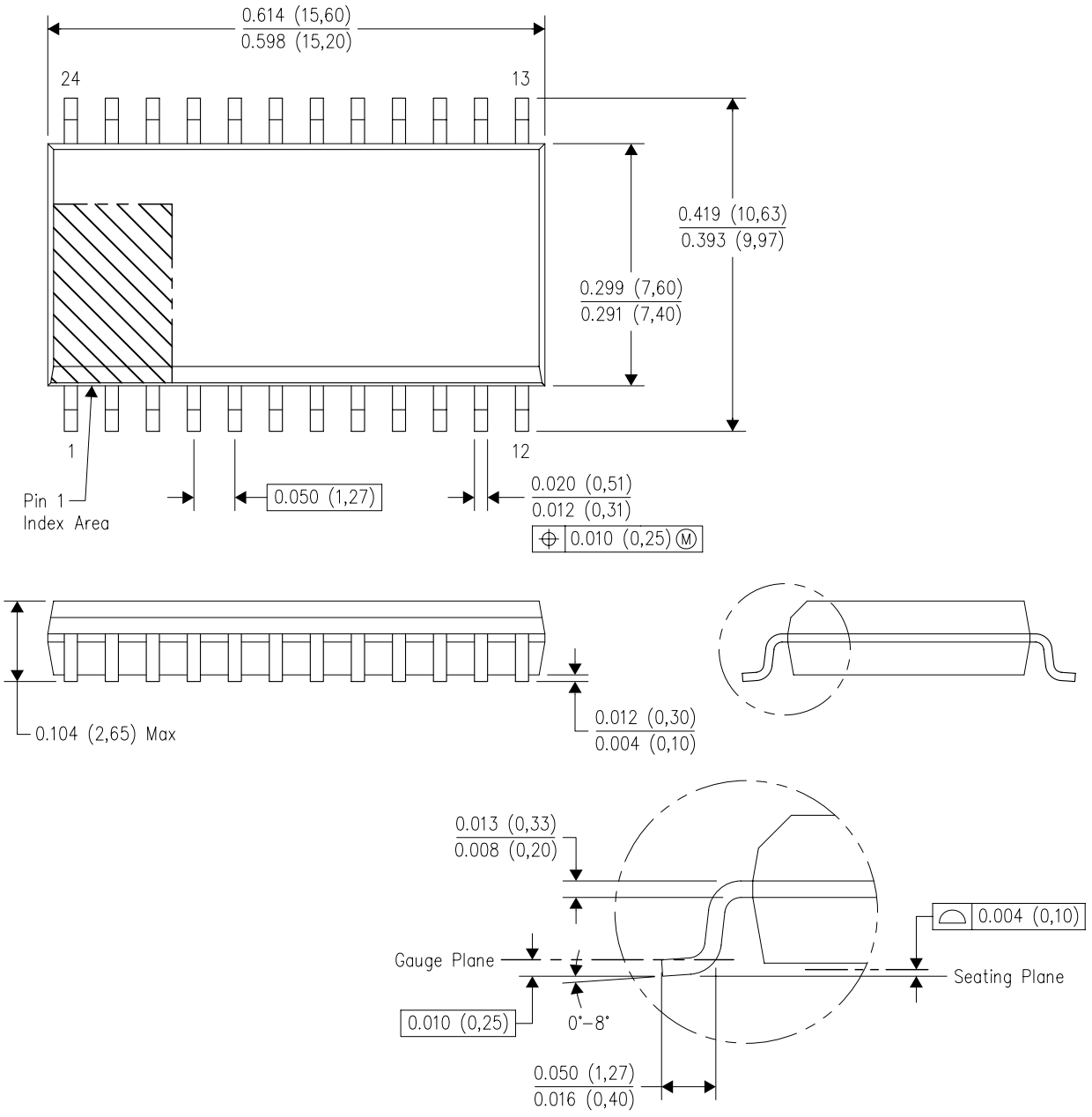
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

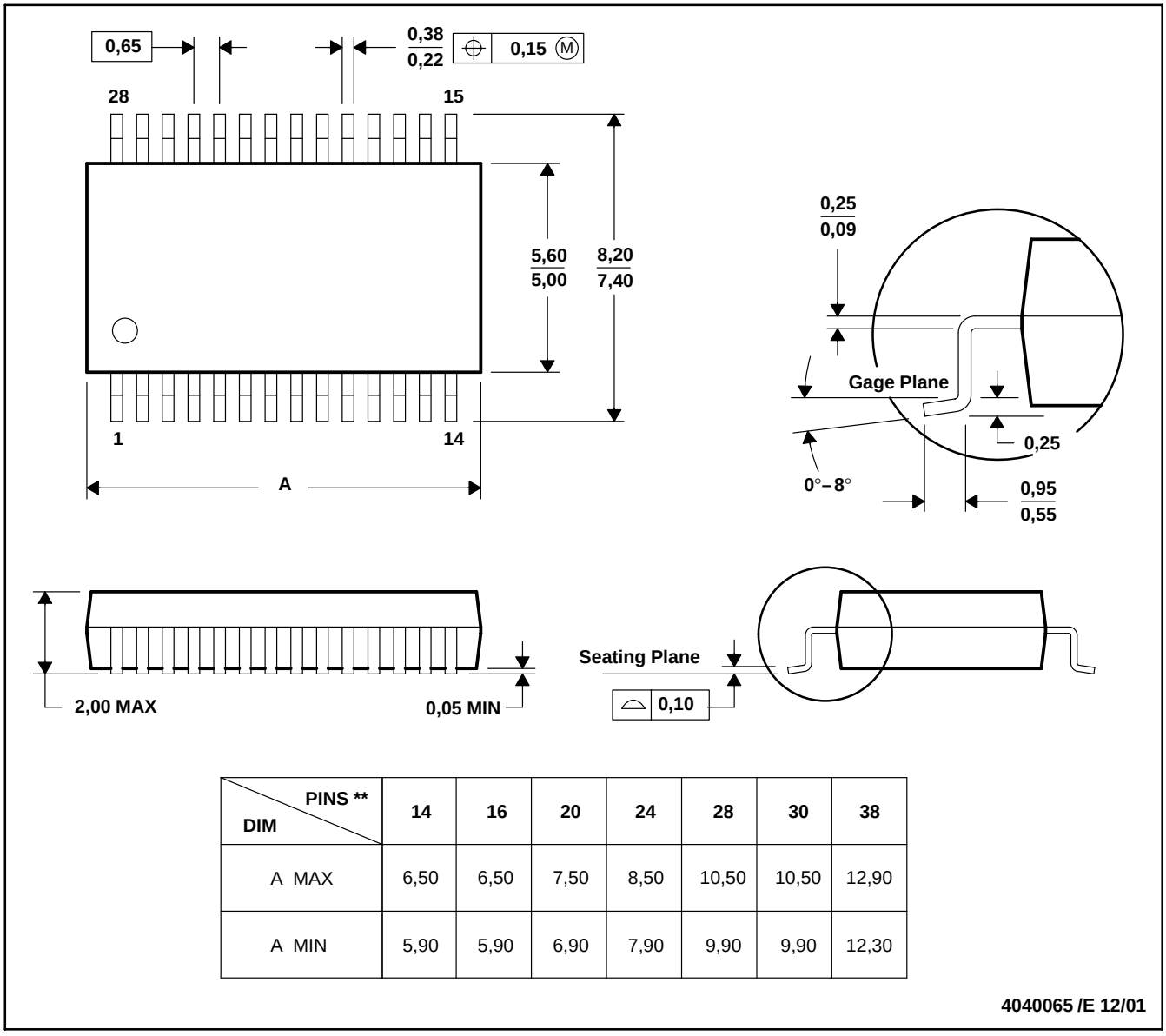


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265