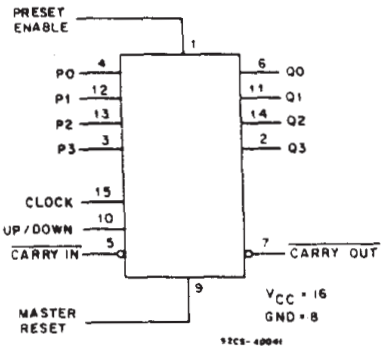
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS302

August 2000

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Up/Down Counters

CD54/74HC/HCT4510 BCD Decade Counter, Asynchronous Reset
CD54/74HC/HCT4516 4-Bit Binary Counter, Asynchronous Reset

Type Features:

- *Synchronous counting and asynchronous loading*
- *Look-ahead carry for high-speed counting*

The CD54/74HC/HCT4510 presettable BCD up/down counter and the CD54/74HC/HCT4516 presettable binary up/down counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the Master Reset line, and can be preset to any binary number present on the preset inputs by a high level on the Preset Enable line. The 4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

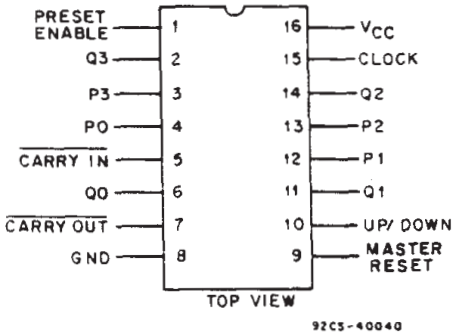
If the Carry-In input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the Carry-Out of a less significant stage to the Carry-In of a more significant stage.

The 4510 and 4516 can be cascaded in the ripple mode by connecting the Carry-Out to the clock of the next stage. If the Up/Down input changes during a terminal count, the Carry-Out must be gated with the clock, and the Up/Down input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 5.)

The CD54HC/HCT4510 and the CD54HC/HCT4516 are supplied in 16-lead ceramic dual-in-line frit-seal packages (F suffix). The CD74HC/HCT4510 and the CD74HC/HCT-4516 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

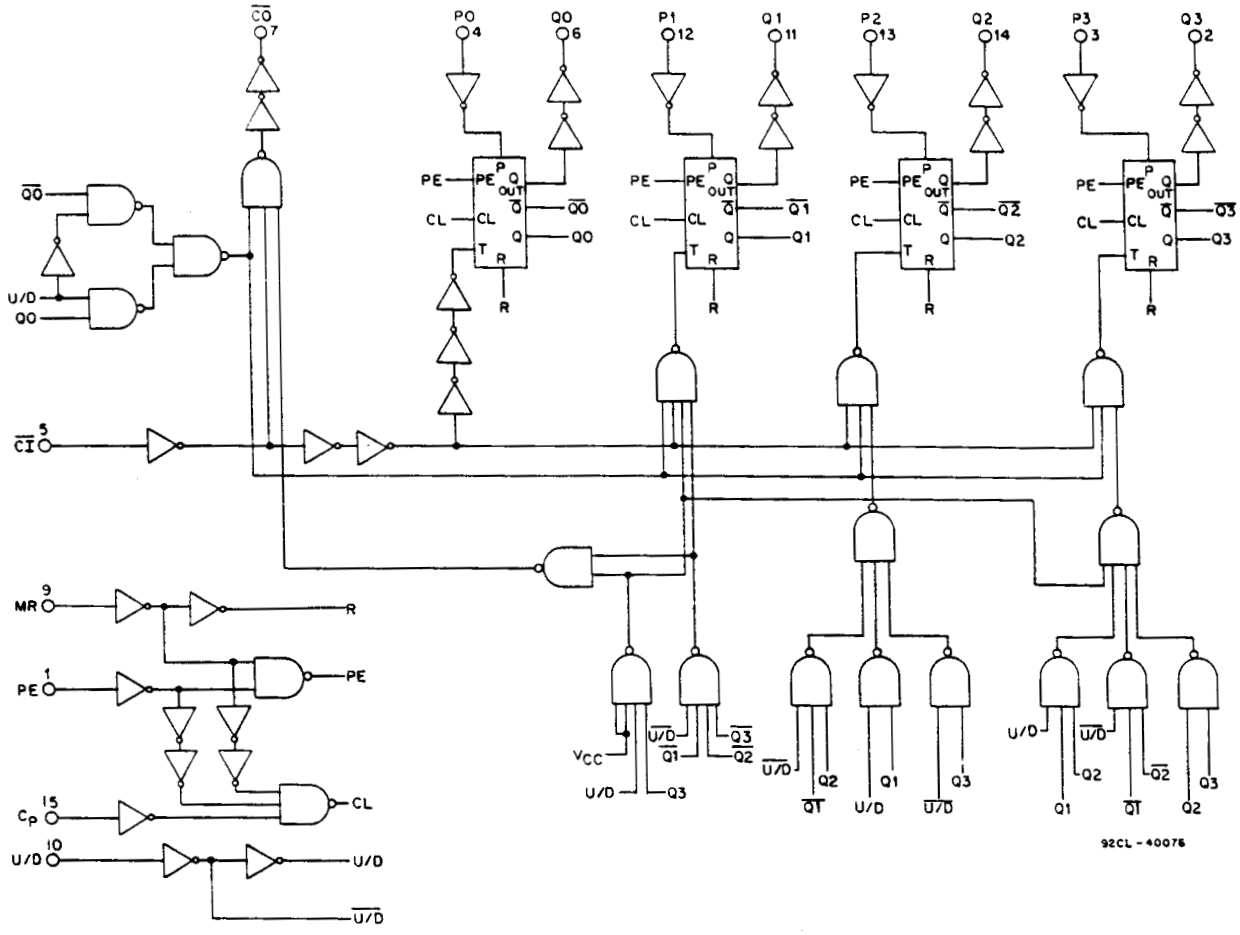


Fig. 1 - Logic diagram for HC/HCT4510.

TRUTH TABLE

CL	$\overline{CI}$	U/D	PE	MR	ACTION
X	H	X	L	L	NO COUNT
⎍	L	H	L	L	COUNT UP
⎍	L	L	L	L	COUNT DOWN
X	X	X	H	L	PRESET
X	X	X	X	H	RESET

X = Don't Care H = High Voltage Level
L = Low Voltage Level

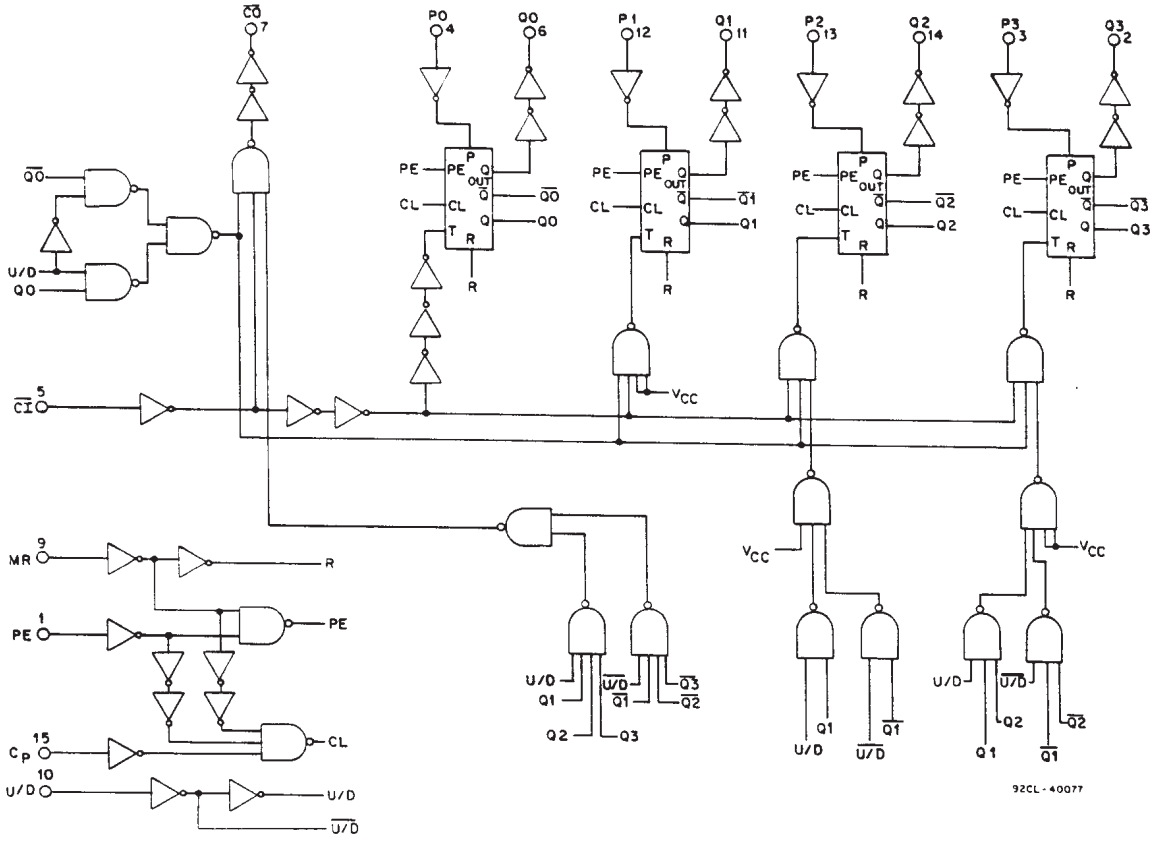


Fig. 2 - Logic diagram for HC/HCT4516.

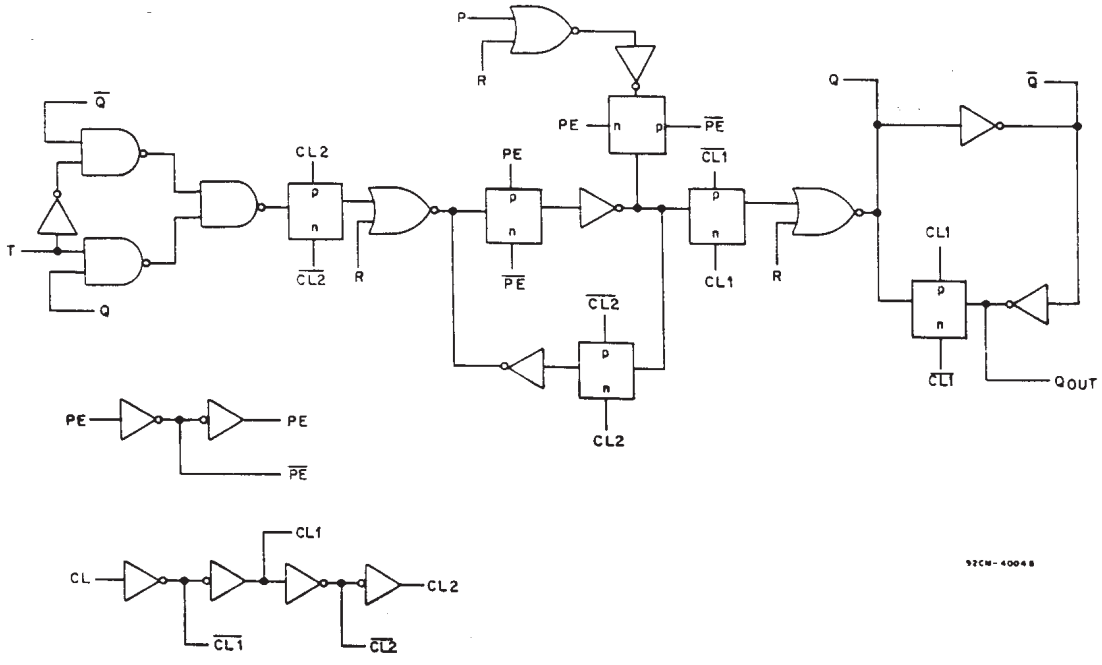


Fig. 3 - Logic diagram of flip-flops for HC/HCT4510/4516.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = −55 to +100°C (PACKAGE TYPE F,H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = −40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H ..... −55 to +125°C
PACKAGE TYPE E,M ..... −40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	−40	+85	°C
CD54 Types	−55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4510/4516/CD54HC4510/4516										CD74HCT4510/4516/CD54HCT4510/4516									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
P0-P3	0.75
MR	1.5
U/D, PE, $\overline{CI}$	1
CP	1.25

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES				UNITS
			4510		4516		
			HC	HCT	HC	HCT	
Propagation Delay:							
CP to Qn	t_{PLH}, t_{PHL}	15	18	21	18	21	ns
CP to $\overline{CO}$	t_{PLH}, t_{PHL}	15	22	24	22	24	
PE to Qn	t_{PLH}, t_{PHL}	15	21	22	21	22	
PE to $\overline{CO}$	t_{PLH}, t_{PHL}	15	25	28	25	28	
MR to Qn	t_{PHL}	15	18	18	18	18	
MR to $\overline{CO}$	t_{PLH}	15	20	20	20	20	
$\overline{CI}$ to $\overline{CO}$	t_{PLH}, t_{PHL}	15	10	13	10	13	
Power Dissipation Capacitance	C_{PD}*		59	65	68	72	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

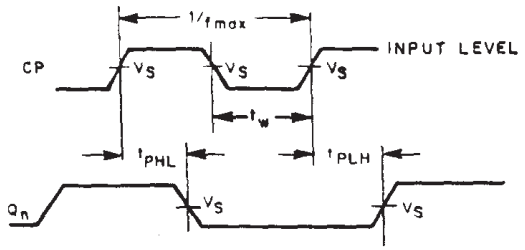
V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

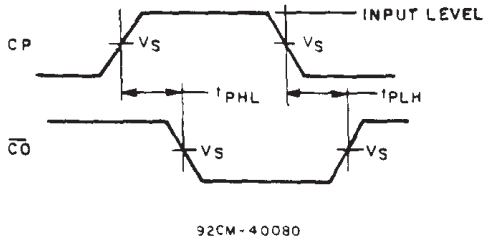
CHARACTERISTIC		TEST CONDITIONS	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width:		2	80	—	—	—	100	—	—	—	120	—	—	—	ns
CP	t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	100	—	—	—	125	—	—	—	150	—	—	—	
MR	t_W	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
PE	t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time,	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	
Pn to PE,		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
$\overline{CI}$ to CP		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time,	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
Pn to PE		4.5	3	—	3	—	3	—	3	—	3	—	3	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
		2	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{CI}$ to CP	t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
		2	0	—	—	—	0	—	—	—	0	—	—	—	
U/D to CP	t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Removal Time:		2	80	—	—	—	100	—	—	—	120	—	—	—	
MR to CP	t_{REM}	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Maximum Frequency		2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
CP	f_{MAX}	4.5	30	—	30	—	24	—	24	—	20	—	20	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

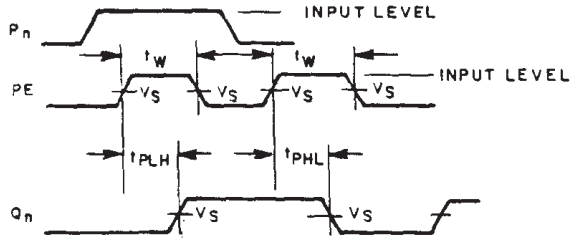
CHARACTERISTIC		V_{CC} (V)	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay:	t_{PLH}	2	—	220	—	—	—	275	—	—	—	330	—	—	ns
CP to Qn	t_{PHL}	4.5	—	44	—	50	—	55	—	63	—	66	—	75	
		6	—	37	—	—	—	47	—	—	—	56	—	—	
	t_{PLH}	2	—	260	—	—	—	325	—	—	—	390	—	—	
CP to $\overline{CO}$	t_{PHL}	4.5	—	52	—	58	—	65	—	73	—	78	—	87	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	
PE to Qn	t_{PHL}	4.5	—	50	—	53	—	63	—	66	—	75	—	80	
		6		43	—	—	—	54	—	—	—	64	—	—	
	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	
PE to $\overline{CO}$	t_{PHL}	4.5	—	60	—	68	—	75	—	85	—	90	—	102	
		6	—	51	—	—	—	64	—	—	—	76	—	—	
		2	—	210	—	—	—	265	—	—	—	315	—	—	
MR to Qn	t_{PHL}	4.5	—	42	—	42	—	53	—	53	—	63	—	63	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
		2	—	235	—	—	—	295	—	—	—	355	—	—	
MR to $\overline{CO}$	t_{PLH}	4.5	—	47	—	47	—	59	—	59	—	71	—	71	
		6	—	40	—	—	—	50	—	—	—	60	—	—	
	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
$\overline{CI}$ to $\overline{CO}$	t_{PHL}	4.5	—	25	—	31	—	31	—	39	—	38	—	47	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Transition Time:	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Qn, $\overline{CO}$	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



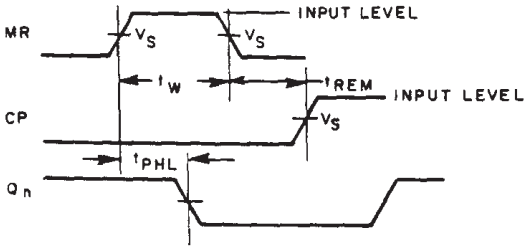
(a) *Clock to output delays and clock pulse width.*



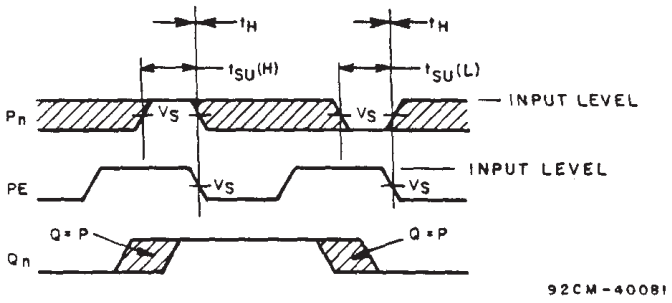
(b) *Clock to carry out delays.*



(c) *Preset Enable pulse width and Preset Enable to output delays.*



(d) *Master reset pulse width, master reset to output delay and master reset to clock removal time.*



(e) *Setup and hold times data to Preset Enable (PE).*

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 4 - AC waveforms.

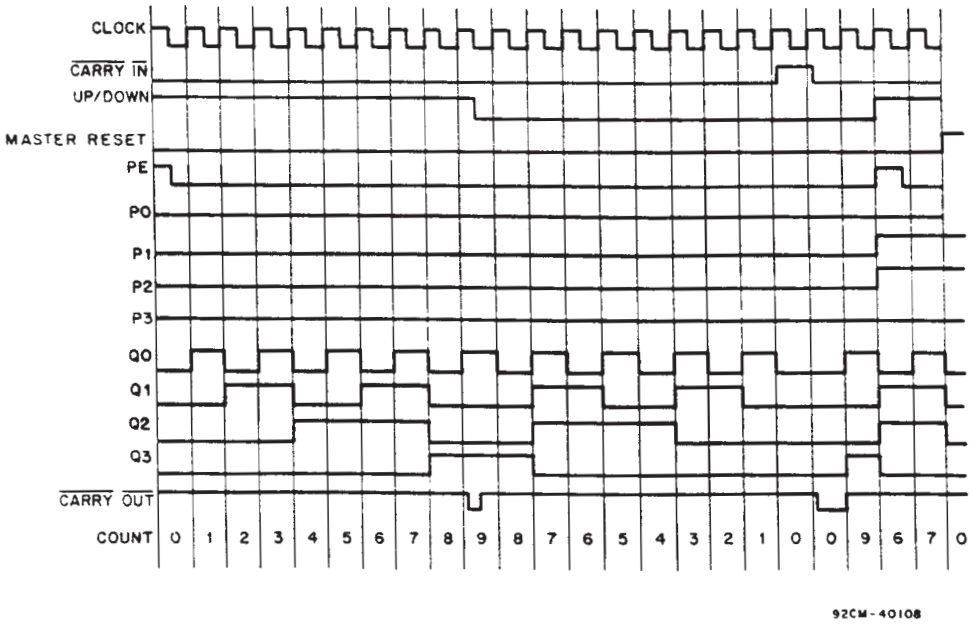


Fig. 5 - Timing diagram for CD54/74HC/HCT4510.

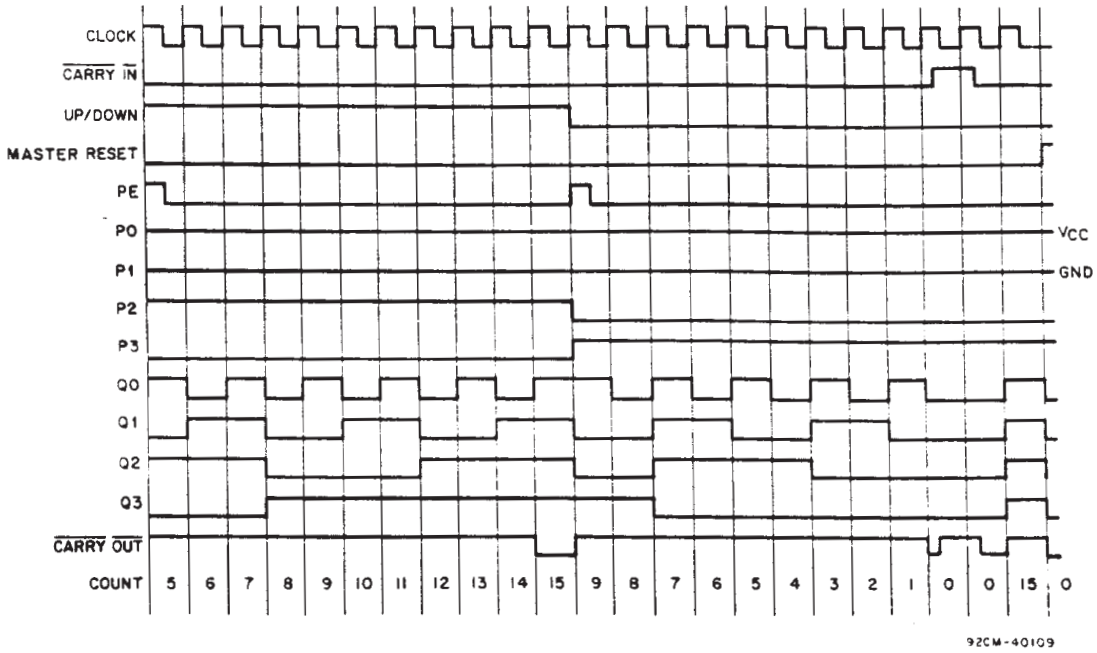
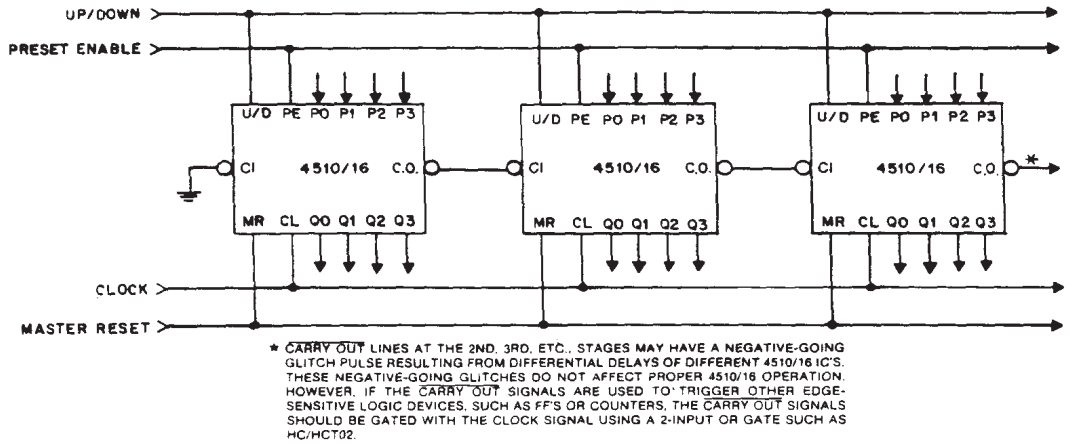
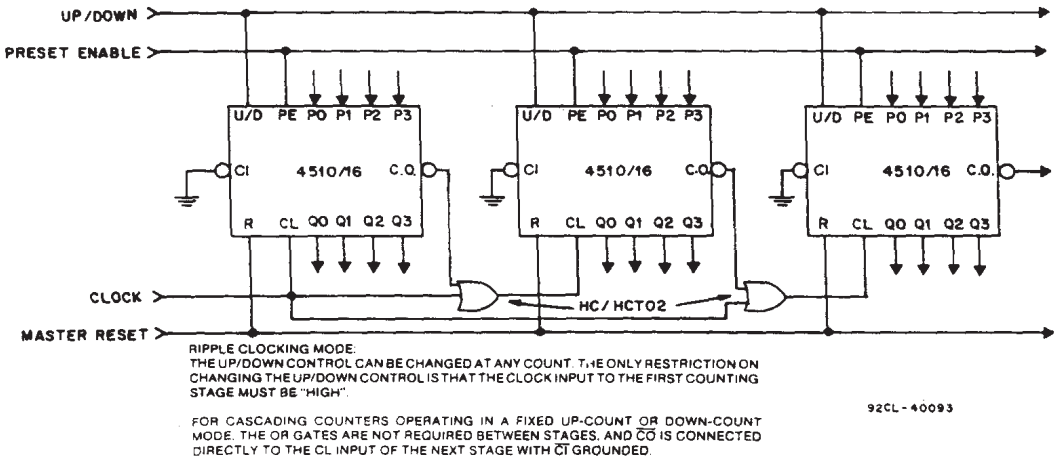


Fig. 6 - Timing diagram for CD54/74HC/HCT4516.



(a) Parallel clocking.



(b) Ripple clocking.

Fig. 7 - Cascading counter packages.

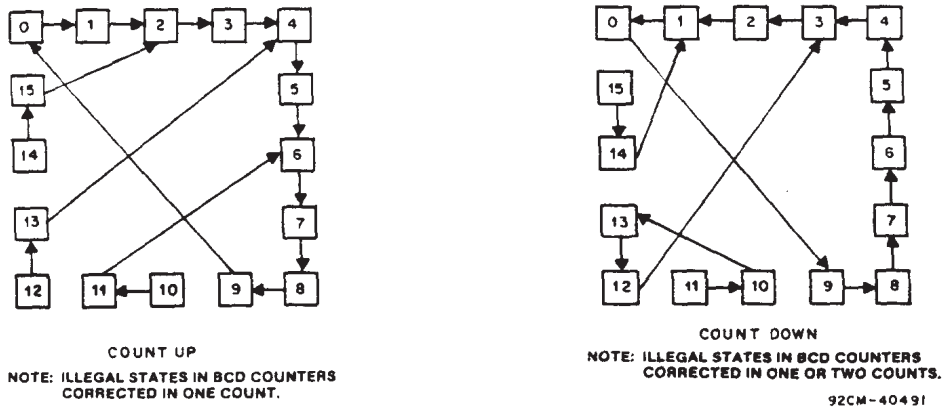


Fig. 8 - HC/HCT4510 State Diagrams.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD54HC4516F3A	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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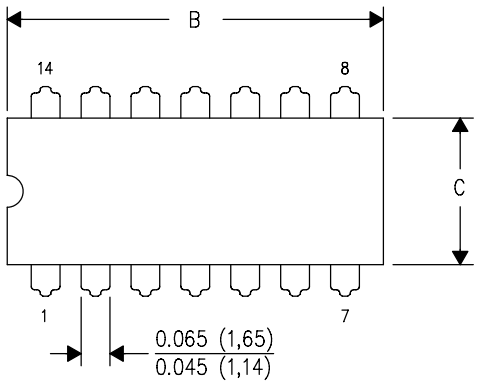
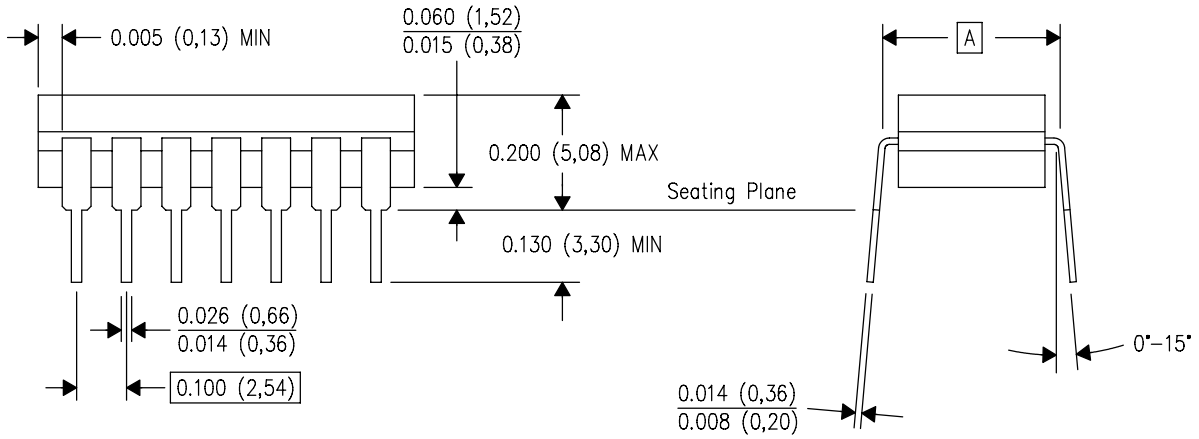
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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