Low-Noise Two-Channel 100-MHz Clock Generator

Check for Samples: CDCM9102

FEATURES

- **Integrated Low-Noise Clock Generator Including PLL, VCO, and Loop Filter**
- **Two Low-Noise 100-MHz Clocks (LVPECL, LVDS, or pair of LVCMOS)**
  - **Support for HCSL Signaling Levels (AC-Coupled)**
  - **Typical Period Jitter: 21 ps pk-pk**
  - **Typical Random Jitter: 510 fs**
  - **Output Type Set by Pins**
- **Bonus Single-ended 25-MHz Output**
- **Integrated Crystal Oscillator Input Accepts 25-MHz Crystal**
- **Output Enable Pin Shuts Off Device and Outputs.**
- **5-mm × 5-mm QFN-32 Package**
- **ESD Protection Exceeds 2 kV HBM, 500 V CDM**
- **Industrial Temperature Range (–40°C to 85°C)**
- **3.3-V Power Supply**

APPLICATIONS

- **Reference Clock Generation for PCI Express Gen 1, Gen2, and Gen3**
- **General-Purpose Clocking**

DESCRIPTION

The CDCM9102 is a low-jitter clock generator designed to provide reference clocks for communications standards such as PCI Express™. The device is easy to configure and use. The CDCM9102 provides two 100-MHz differential clock ports. The output types supported for these ports include LVPECL, LVDS, or a pair of LVCMOS buffers. HCSL signaling is supported using an ac-coupled network. The user configures the output buffer type desired by strapping device pins. Additionally, a single-ended 25-MHz clock output port is provided. Uses for this port include general-purpose clocking, clocking Ethernet PHYs, or providing a reference clock for additional clock generators. All clocks generated are derived from a single external 25-MHz crystal.

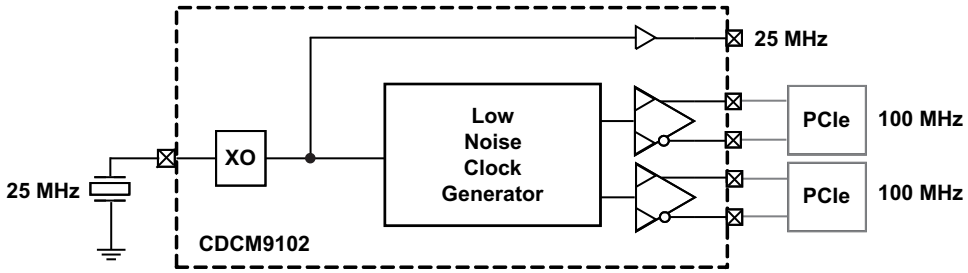


Figure 1. CDCM9102 Typical Application Example

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

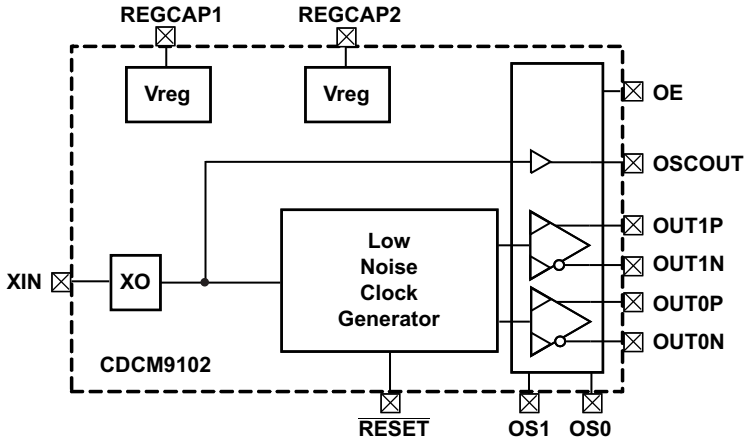


Figure 2. CDCM9102 Block Diagram

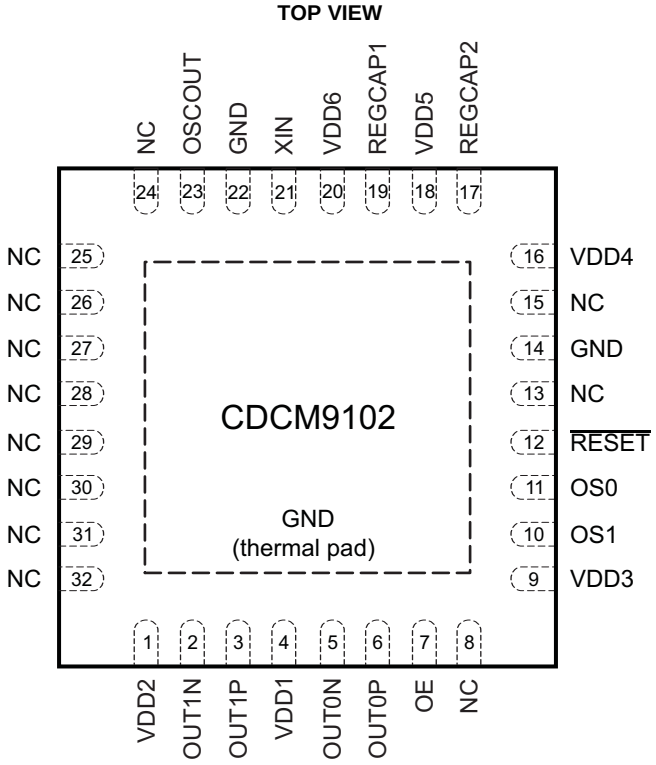


Figure 3. Pin Diagram

PIN FUNCTIONS

NAME	QFN32 PIN NO.	DESCRIPTION
POWER SUPPLIES		
GND	Thermal pad, 14, 22	Power supply ground and thermal relief
VDD2	1	Power Supply, OUT1 clock port
VDD1	4	Power Supply, OUT0 clock port
VDD3	9	Power supply, low-noise clock generator
VDD4	16	Power supply, low-noise clock generator
VDD5	18	Power supply, low-noise clock generator
VDD6	20	Power supply, crystal oscillator input
REGCAP1	19	Capacitor for internal regulator, connect 10-µF Y5V capacitor to GND
REGCAP2	17	Capacitor for internal regulator, connect 10-µF Y5V capacitor to GND
DEVICE CONFIGURATION AND CONTROL		
NC	8, 13, 15, 24–32	No connection permitted
OE	7	Output enable/shutdown control input (see Table 1)
OS1	10	Output format select control inputs (see Table 2)
OS0	11	
RESET	12	Device reset input (active-low) (see Table 3)(1)
CRYSTAL OSCILLATOR		
XIN	21	Parallel resonant crystal input (25 MHz)
DEVICE OUTPUTS		
OUT0P	6	Output 0 – positive terminal (100 MHz)
OUT0N	5	Output 0 – negative terminal (100 MHz)
OUT1P	3	Output 1 – positive terminal (100 MHz)
OUT1N	2	Output 1 – negative terminal (100 MHz)
OSCOUT	23	Oscillator output port (25 MHz)

(1) For proper device startup, it is recommended that a capacitor be installed from pin 12 to GND. See *STARTUP TIME ESTIMATION* section for more details.

ORDERING INFORMATION

T_A	PACKAGED DEVICES	FEATURES
–40°C to 85°C	CDCM9102RHBT	32-pin QFN (RHB) package, small tape and reel
	CDCM9102RHBR	32-pin QFN (RHB) package, tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
VDDx	Supply voltage range(2)	–0.5		4.6	V
V_{IN}	Input voltage range (3)	–0.5		V_{DDx} + 0.5	V
V_{OUT}	Output voltage range(3)	–0.5		V_{DDx} + 0.5	V
I_{IN}	Input current			20	mA
I_{OUT}	Output current			50	mA
T_{stg}	Storage temperature range	–65		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Supply voltages must be applied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp–current ratings are observed

DISSIPATION RATINGS(1)(2)

PARAMETER		TEST CONDITIONS	VALUE, 4 × 4 Vias on Pad	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	0 LFM	35	ºC/W
θ_{JP}(3)	Junction-to-thermal pad (top) thermal resistance		4	ºC/W

(1) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC 2S2P (high-K board).
(2) Connected to GND with sixteen thermal vias (0.3 mm in diameter)
(3) θ_{JP} (junction-to-pad) is used for the QFN package, because the primary heat flow is from the junction to the GND pad of the QFN package.

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
POWER SUPPLIES					
V_{DDX}	DC power-supply voltage	3	3.3	3.6	V
TEMPERATURE					
T_A	Ambient temperature	–40		85	°C

DEVICE CURRENT CONSUMPTION

T_A = –40°C to 85°C, VDDx = 3.3 V, OE = 1, values represent cumulative current/power on all VDDx pins.

BLOCK	CONDITION	CURRENT (mA)	DEVICE POWER (mW)	EXTERNAL RESISTOR POWER (mW)
Entire device, core current		85	280	
Output Buffers	LVPECL	28	42.4	50
	LVDS	20	66	
	LVCMOS	$V \times f_{out} \times (C_L + 20 \times 10^{-12}) \times 10^3$	$V^2 \times f_{out} \times (C_L + 20 \times 10^{-12}) \times 10^3$	

DIGITAL INPUT CHARACTERISTICS – RESET, OE, OS1, OS0

T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS INPUTS						
V_{IH}	Input high voltage		0.6 V_{DD}			V
V_{IL}	Input low voltage				0.4 V_{DD}	V
I_{IH}	Input high current	V_{DD} = 3.6 V, V_{IL} = 0 V			200	µA
I_{IL}	Input low current	V_{DD} = 3 V, V_{IH} = 3.6 V			–200	µA
C_{IN}	Input capacitance			8	10	pF
R_{PU}	Input pullup resistor			150		kΩ

CRYSTAL-OSCILLATOR INPUT-PORT CHARACTERISTICS (XIN)

V_{DD} = 3.3 V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CRYSTAL CHARACTERISTICS (External 25 MHz Crystal)						
f_{XTAL}	Crystal input frequency	Fundamental mode		25		MHz
ESR	Effective series resistance of crystal				50	Ω
C_{IN}	On-chip load capacitance			8	10	pF
$XTAL_{DL}$	Maximum drive level - XTAL		0.1		1	mW
C_{SHUNT}	Maximum shunt capacitance				7	pF

CLOCK OUTPUT BUFFER CHARACTERISTICS (OUTPUT MODE = LVPECL)

VDD1, VDD2 = 3.3 V; T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage		V_{DD} – 1.18		V_{DD} – 0.73	V
V_{OL}	Output low voltage		V_{DD} – 2		V_{DD} – 1.55	V
$\|V_{OD}\|$	Differential output voltage		0.6		1.23	V
t_R/t_F	Output rise/fall time	20% to 80%			175	ps
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				20	ps

CLOCK OUTPUT BUFFER CHARACTERISTICS (OUTPUT MODE = LVDS)

VDD1, VDD2 = 3.3V; T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage		0.247		0.454	V
ΔV_{OD}	V_{OD} magnitude change				50	mV
V_{OS}	Common-mode voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} magnitude change				50	mV
t_R/t_F	Output rise/fall time	20% to 80%			255	ps
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				30	ps

CLOCK OUTPUT BUFFER CHARACTERISTICS (OUTPUT MODE = LVCMOS)

VDD1, VDD2 = 3.3V; T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage	V_{CC} = 3 V to 3.6 V, I_{OH} = –100 µA	V_{DD} – 0.5			V
V_{OL}	Output low voltage	V_{CC} = 3 V to 3.6 V, I_{OH} = 100 µA			0.3	V
t_{SLEW}	Output rise/fall slew rate	20% to 80%	2.4			V/ns
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				50	ps

OUTPUT JITTER PERFORMANCE

f_{OUT} = 100 MHz, V_{DD} = 3.3 V, T_A = 25°C, jitter integration bandwidth 10 kHz–20 MHz

LVCMOS OUTPUT MODE		LVPECL OUTPUT MODE		LVDS OUTPUT MODE	
Random jitter (fs)	Period jitter (ps pk-pk)	Random jitter (fs)	Period jitter (ps pk-pk)	Random jitter (fs)	Period jitter (ps pk-pk)
507	24.5	510	20.7	533	26.5

TEST CONFIGURATIONS

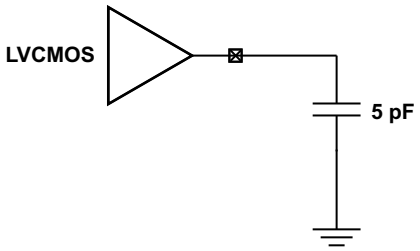


Figure 4. LVCMOS Output Test Load

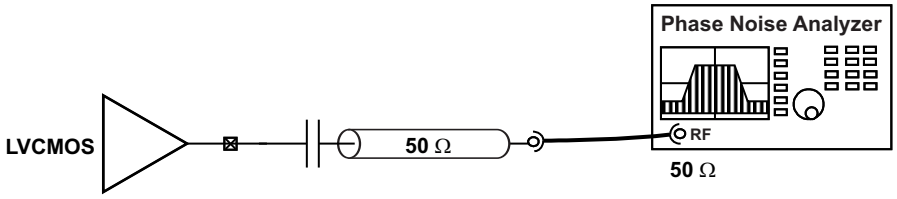


Figure 5. LVCMOS AC Configuration for Device Test

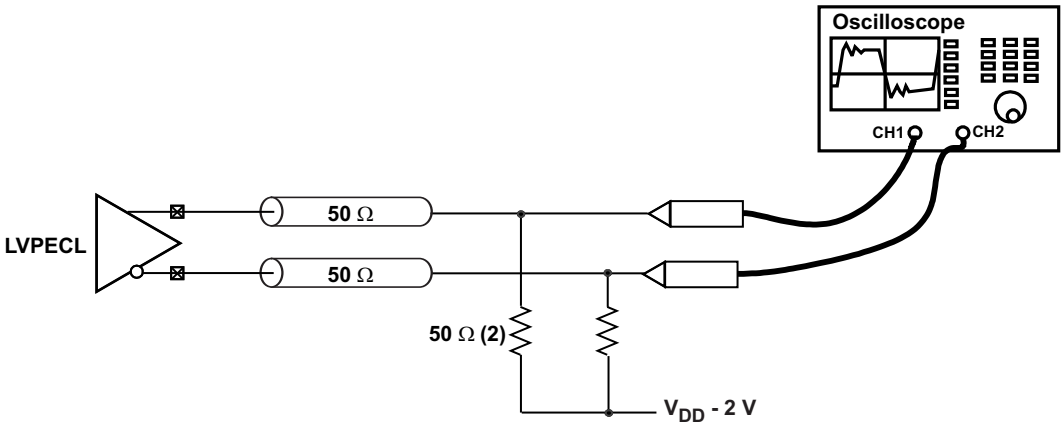


Figure 6. LVPECL DC Configuration for Device Test

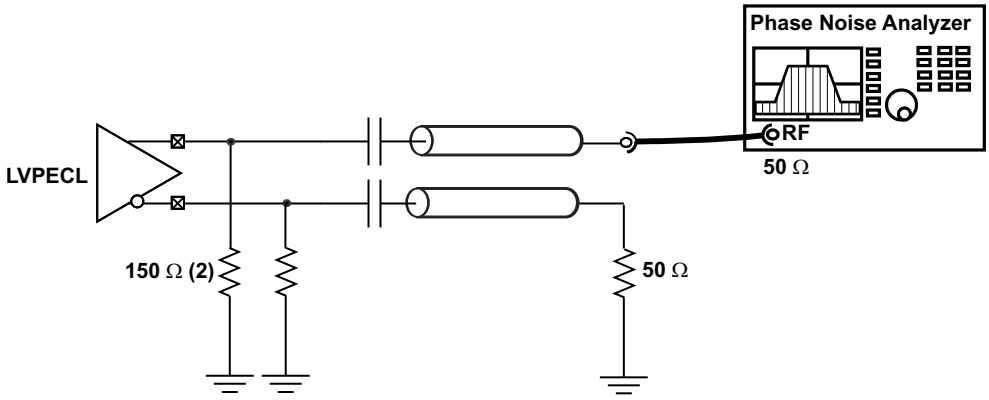


Figure 7. LVPECL AC Configuration for Device Test

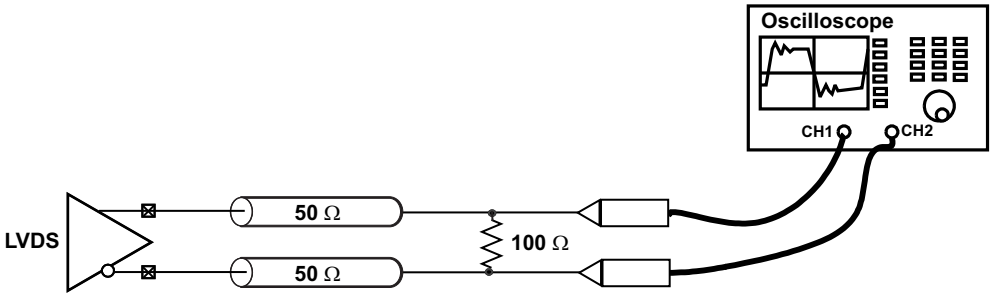


Figure 8. LVDS DC Configuration for Device Test

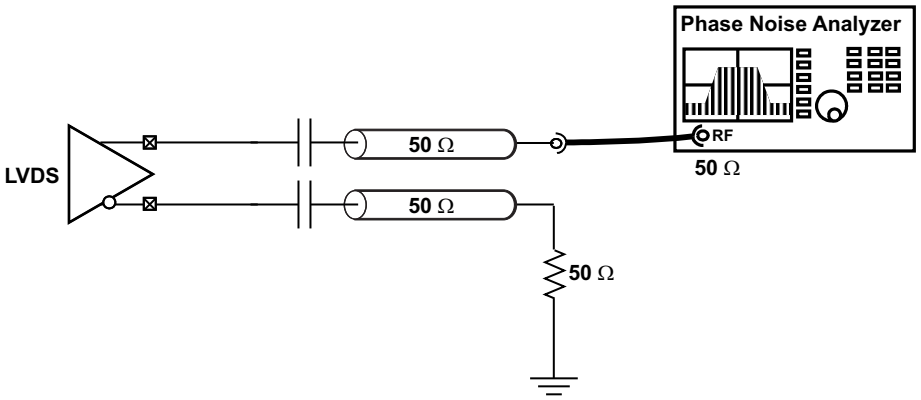


Figure 9. LVDS AC Configuration for Device Test

PERFORMANCE CHARACTERISTICS

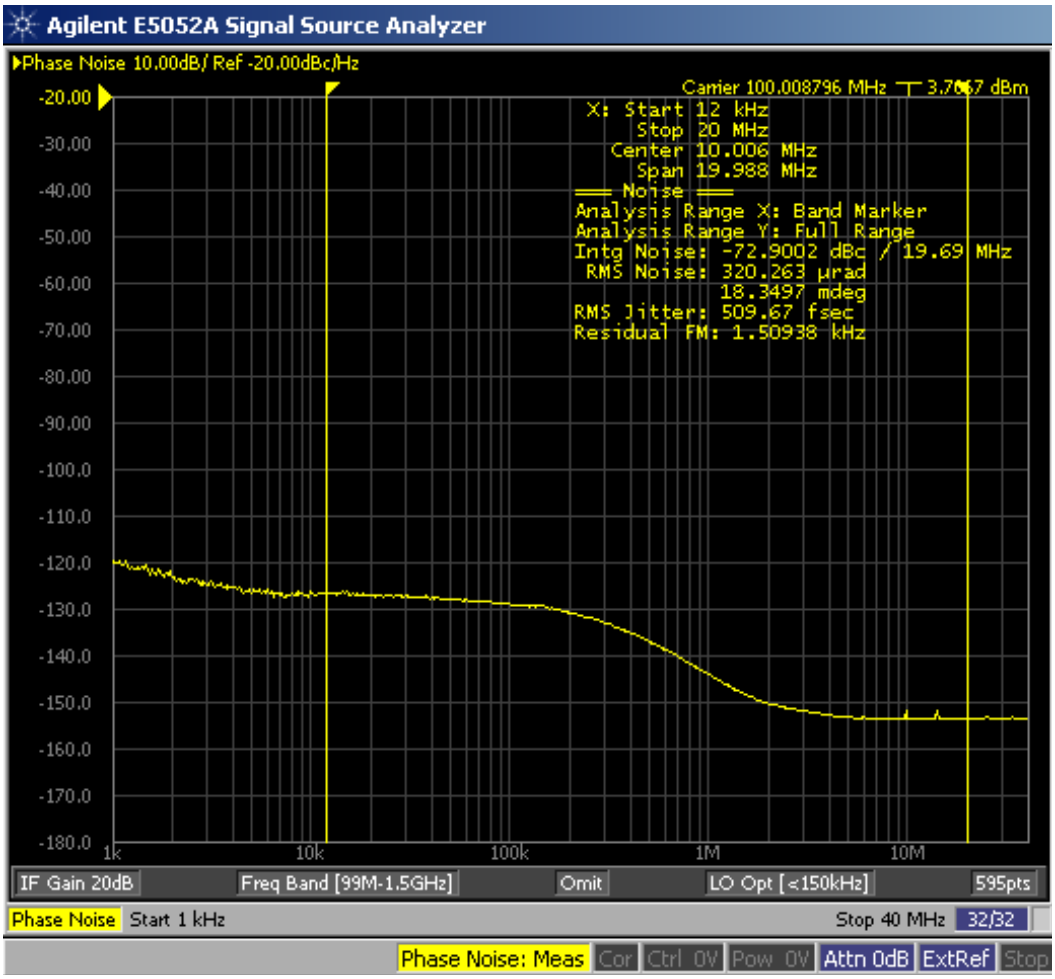


Figure 10. CDCM9102 Typical Phase Noise Performance (LVPECL Mode)

FUNCTIONAL DESCRIPTION

DEVICE CONFIGURATION

Table 1. CDCM9102 Pin Control of Output Enable

OE (Pin 7)	MODE	DEVICE CORE	OUTPUT
0	Power down	Power down	Hi-Z
1	Normal	Active	Active

Table 2. CDCM9102 Pin Configuration of Output Type

CONTROL PINS		OUTPUT MODE
OS1 (Pin 10)	OS0 (Pin 11)	
0	0	LVCMOS, OSCOUT = OFF
0	1	LVDS, OSCOUT = OFF
1	0	LVPECL, OSCOUT = OFF
1	1	LVPECL, OSCOUT = ON

Table 3. CDCM9102 Device Reset

RESET (Pin 12)	OPERATING MODE	DEVICE OUTPUTS
0	Device reset	Hi-Z
0 → 1	Clock generator calibration	Hi-Z
1	Normal	Active

APPLICATION INFORMATION

CRYSTAL INPUT (XIN) INTERFACE

The CDCM9102 implements a *Colpitts oscillator*; therefore, one side of the crystal connects to the XIN pin and the other crystal terminal connects to ground. The device requires the use of a fundamental-mode crystal, and the oscillator operates in parallel resonance mode. The correct load capacitance is necessary to ensure that the circuit oscillates properly. The load capacitance comprises all capacitances in the oscillator feedback loop (the capacitances seen between the terminals of the crystal in the circuit). It is important to account for all sources of capacitance when calculating the correct value for the external discrete load capacitance shown in Figure 11.

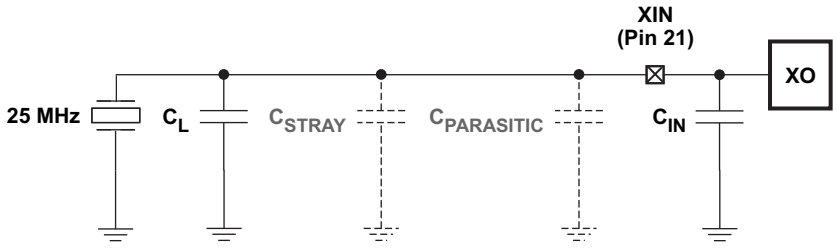


Figure 11. Configuration of Circuit for CDCM9102 XIN Oscillator

The CDCM9102 has been characterized with 10-pF parallel-resonant crystals. The input stage of the crystal oscillator in the CDCM9102 is designed to oscillate at the correct frequency for all parallel-resonant crystals with low-pull capability and rated with a load capacitance that is equal to the sum of the on-chip load capacitance at the XIN pin (C_{IN} = 10 pF maximum), crystal stray capacitance, and board parasitic capacitance between the crystal and XIN pin. To minimize stray and parasitic capacitances, minimize the trace distance routed from the crystal to the XIN pin and avoid other active traces and/or active circuitry in the area of the crystal oscillator circuit. Table 4 lists crystal types that have been evaluated with the CDCM9102.

Table 4. CDCM9102 Crystal Recommendations

MANUFACTURER	PART NUMBER
Vectron	VXC1-1133
Fox	218-3
Saronix	FP2650002

A mismatch of the load capacitance results in a frequency error according to Equation 1:

$$\frac{\Delta f}{f} = \frac{C_S}{2\left(C_{Lr} + C_O\right)} - \frac{C_S}{2\left(C_{La} + C_O\right)} \quad (1)$$

where:

- Δf is the frequency error required by the application.
- f is the fundamental frequency of the crystal.
- C_S is the motional capacitance of the crystal. This is a parameter in the data sheet of the crystal.
- C_0 is the shunt capacitance of the crystal. This is a parameter in the data sheet of the crystal.
- C_{Lr} is the rated load capacitance of the crystal. This is a parameter in the data sheet of the crystal.
- C_{La} is the actual load capacitance implemented on the PCB (C_{IN} + stray capacitance + parasitic capacitance + C_L).

The difference between the rated load capacitance (from the crystal datasheet) and the actual load capacitance (C_{La} = C_{IN} + C_L + C_{STRAY} + $C_{PARASITIC}$) should be minimized. A crystal with a low pull-ability rating (low C_S) is ideal.

Design Example:

Desired frequency tolerance Δf ≤ ±80 ppm

Crystal Vendor Parameters:

Intrinsic Frequency Tolerance = ±30 ppm

C_0 = 7 pF (shunt capacitance)
C_S = 10 fF (motional capacitance)
C_{Lr} = 12 pF (load capacitance)

Substituting these parameters into Equation 1 yields a maximum value of C_{La} = 17 pF in order to achieve the desired Δf (±50 ppm). Recall that $C_{La} = C_{IN} + C_L + C_{STRAY} + C_{PARASITIC}$ = 8 pF + ($C_L + C_{STRAY} + C_{PARASITIC}$)(1) . Ideally, the load presented to this crystal should be 12 pF; therefore the sum of ($C_L + C_{STRAY} + C_{PARASITIC}$) must be less than 9 pF. Stray and parasitic capacitance must be controlled. This is because the Colpitts oscillator is particularly sensitive to capacitance in parallel with the crystal; therefore, good layout practice is essential. It is recommended that the designer extract the stray and parasitic capacitance from the printed circuit board design tool and adjust C_L accordingly to achieve $C_{Lr} = C_{La}$. In common scenarios, the external load capacitor is often unnecessary; however, it is recommended that pads be implemented to accommodate an external load capacitor so that the ppm error can be minimized.

STARTUP TIME ESTIMATION

The CDCM9102 contains a low-noise clock generator that calibrates to an optimal operating point at device power up. In order to ensure proper device operation, the oscillator must be stable prior to the low-noise clock generator calibration procedure. Quartz-based oscillators can take up to 2 ms to stabilize; therefore it is recommended that the application ensure that the RESET pin is de-asserted at least 5 ms after the power supply has finished ramping. This can be accomplished by controlling the RESET pin directly, or by applying a 47-nF capacitor to ground on the RESET pin (this provides a delay because the RESET pin includes a 150-kΩ pullup resistor.

The CDCM9102 startup time can be estimated based on parameters defined in Table 5 and graphically shown in Figure 12.

Table 5. CDCM9102 Startup Time Dependencies

Parameter	Definition	Description	Formula / Method of Determination
t_{REF}	Reference clock period	The reciprocal of the applied reference frequency in seconds	$t_{REF} = \frac{1}{f_{REF}} = 0.04\ \mu s$
t_{pul}	Power-up time (low limit)	Power-supply rise time to low limit of power-on-reset trip point	Time required for power supply to ramp to 2.27 V
t_{puh}	Power-up time (high limit)	Power supply rise time to high limit of power-on-reset trip point	Time required for power supply to ramp to 2.64 V
t_{rsu}	Reference start-up time	After POR releases, the Colpitts oscillator is enabled. This start-up time is required for the oscillator to generate the requisite signal levels for the delay block to be clocked by the reference input.	500 µs best case and 800 µs worst case (for a crystal input)
t_{delay}	Delay time	Internal delay time generated from the reference clock. This delay provides time for the reference oscillator to stabilize.	$t_{delay} = 16{,}384 \times t_{REF} = 655\ \mu s$
t_{VCO_CAL}	VCO calibration time	VCO calibration time generated from the reference clock. This process selects the operating point for the VCO based on the PLL settings.	$t_{VCO\_CAL} = 550 \times t_{REF} = 22\ \mu s$
t_{PLL_LOCK}	PLL lock time	Time requried for PLL to lock within ±10 ppm of f_{REF}	The PLL settles in 12.5 µs

(1) C_{IN} = 8 pF (typical), 10 pF (maximum). See the *Crystal Oscillator Input Port Characteristics* (XIN) table.

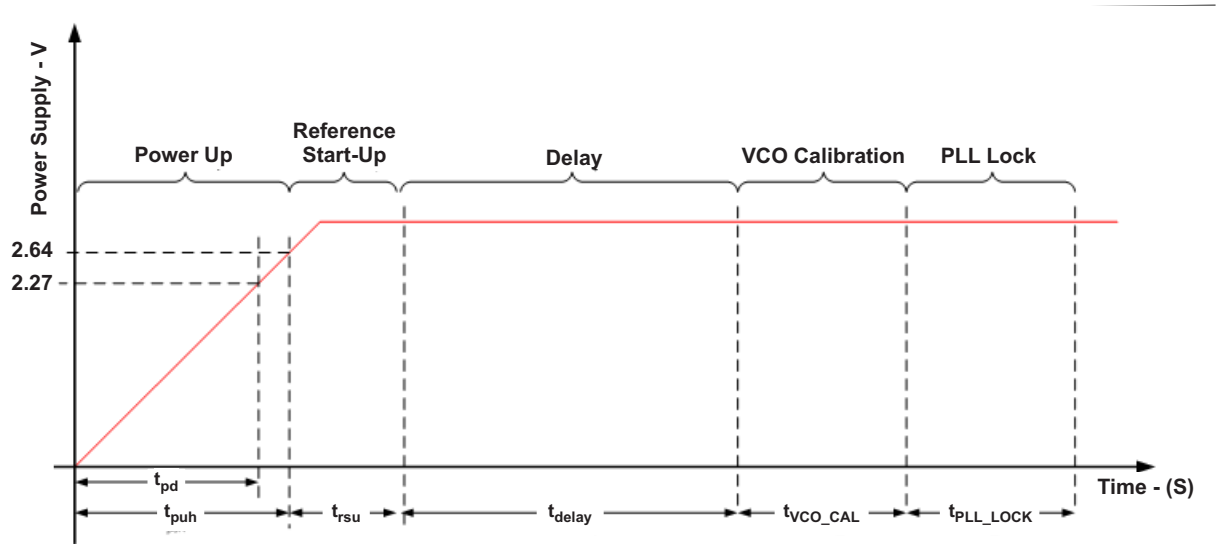


Figure 12. CDCM9102 Start-Up Time Dependencies

The CDCM9102 startup time limits, t_{MAX} and t_{MIN}, can now be calculated as follows

$$t_{MAX} = t_{puh} + t_{rsu} + t_{delay} + t_{VCO\_CAL} + t_{PLL\_LOCK}$$

$$t_{MIN} = t_{pul} + t_{rsu} + t_{delay} + t_{VCO\_CAL} + t_{PLL\_LOCK}$$

THERMAL MANAGEMENT

To ensure optimal performance and reliability, good thermal design practices are important when using the CDCM9102. Die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

The device package has an exposed pad that provides the primary heat removal path as well as an electrical grounding to the printed circuit board (PCB). To maximize the removal of heat from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in Figure 13.

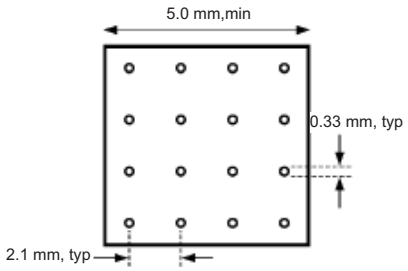


Figure 13. Recommended PCB Layout for CDCM9102

POWER SUPPLY FILTERING

PLL-based frequency synthesizers are very sensitive to noise on the power supply, which can dramatically increase the jitter of the PLL. This is especially true for analog-based PLLs. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL has attenuated jitter due to power supply noise at frequencies beyond the PLL bandwidth due to attenuation by the loop response.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass

capacitors provide the very low-impedance path for high-frequency noise and guard the power supply system against induced fluctuations. The bypass capacitors also provide a source of instantaneous current as required by the device output stages. Therefore, bypass capacitors must have low ESR. To properly use the bypass capacitors, they must be placed very close to the power supply pins and must be laid out with short loops to minimize inductance.

Figure 14 shows a general recommendation for decoupling the power supply. The CDCXM9102 power supplies fall into one of two categories: analog supplies (VDD3, VDD4, and VDD5), and input/output supplies (VDD1, VDD2, and VDD6). Short the analog supplies together to form the analog supply node; likewise, short the input/output supplies together to form the I/O supply node. Isolate the analog node from the PCB power supply and I/O node by inserting a ferrite bead. This helps isolate the high-frequency switching noises generated by the clock drivers and I/O from the sensitive analog supply node. Choosing an appropriate ferrite bead with low dc resistance is important, as it is imperative to maintain a voltage at the power-supply pin of the CDCM9102 that is over the minimum voltage needed for its proper operation.

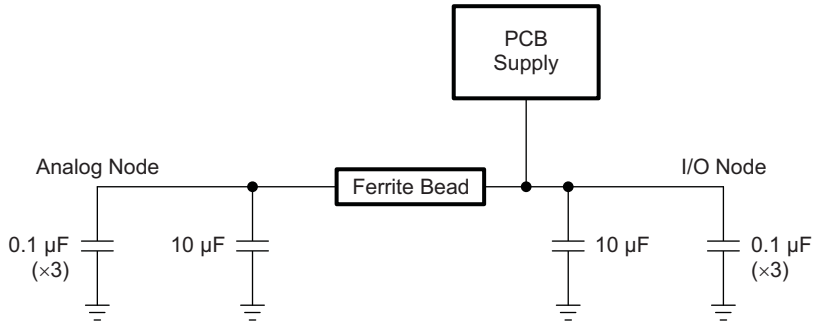


Figure 14. CDCM9102 Power Supply Decoupling – Power Pin Bypass Concept

OUTPUT TERMINATION

The CDCM9102 is a 3.3-V clock driver which has the following options for the output type: LVPECL, LVDS, and LVCMOS.

LVPECL TERMINATION

The CDCM9102 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination is required to ensure correct operation of the device and to optimize signal integrity. The proper termination for LVPECL is 50 Ω to (Vcc-2) V but this dc voltage is not readily available on a board. Thus a Thevenin's equivalent circuit is worked out for the LVPECL termination in both direct-coupled (dc) and ac-coupled cases, as shown in Figure 15 and Figure 16. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac coupling is required.

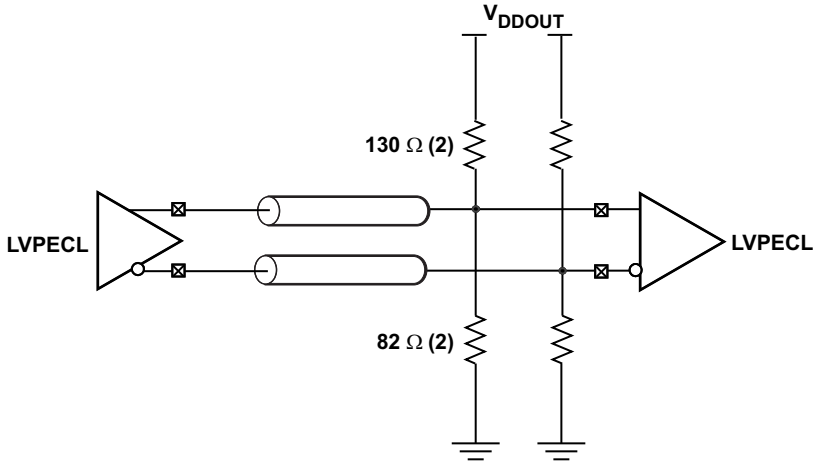


Figure 15. LVPECL Output Termination (DC-Coupled)

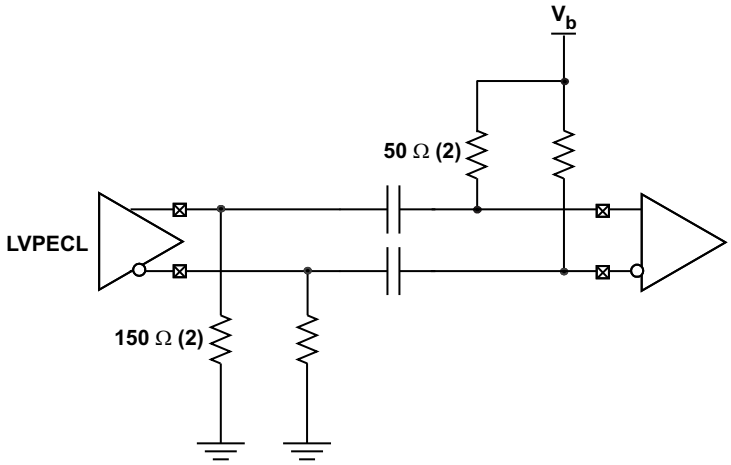


Figure 16. LVPECL Output Termination (AC-Coupled)

LVDS TERMINATION

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either a direct-coupled (dc) termination or ac-coupled termination can be used for LVDS outputs, as shown in Figure 17 and Figure 18. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac coupling is required.

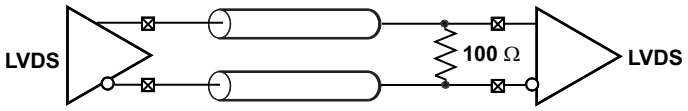


Figure 17. LVDS Output Termination (DC Coupled)

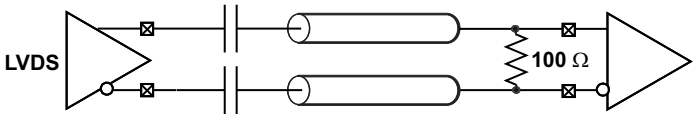


Figure 18. LVDS Output Termination (AC Coupling)

LVCMOS TERMINATION

Series termination is a common method to maintain the signal integrity for LVCMOS drivers, if connected to a receiver with a high-impedance input. For series termination, a series resistor, Rs, is placed close to the driver, as shown in Figure 19. The sum of the driver impedance and Rs should be close to the transmission-line impedance, which is usually 50 Ω. Because the LVCMOS driver in the CDCM9102 has an impedance of 30 Ω, Rs is recommended to be 22 Ω to maintain proper signal integrity.

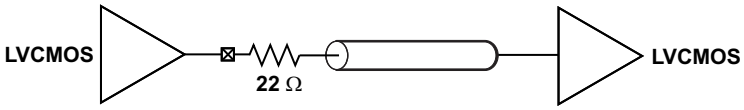


Figure 19. LVCMOS Output Termination

INTERFACING BETWEEN LVPECL and HCSL (PCI Express)

Certain PCI Express applications require HCSL signaling. Because the common-mode voltage for LVPECL and HCSL are different, applications requiring HCSL signaling must use ac coupling as shown in Figure 20. The 150-Ω resistors ensure proper biasing of the CDCM9102 LVPECL output stage. The 471-Ω and 56-Ω resistor network biases the HCSL receiver input stage.

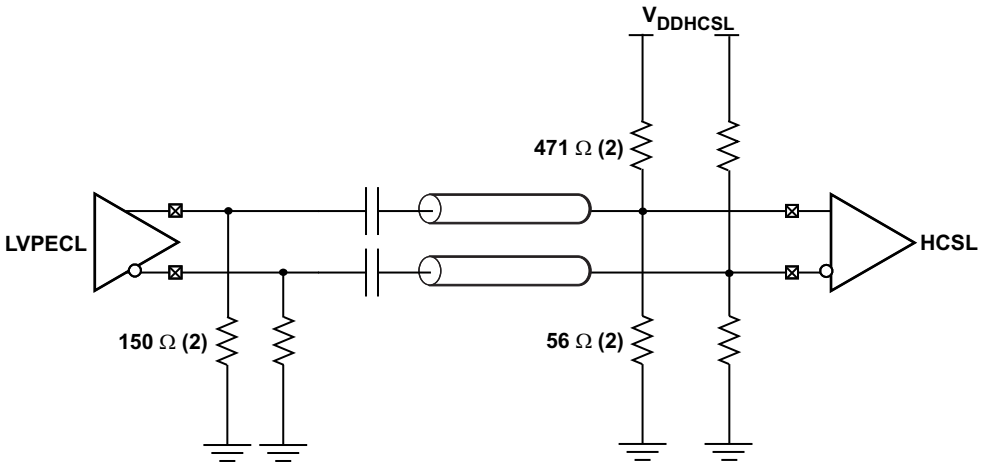


Figure 20. Interfacing Between LVPECL and HCSL

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CDCM9102RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CDCM9102RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

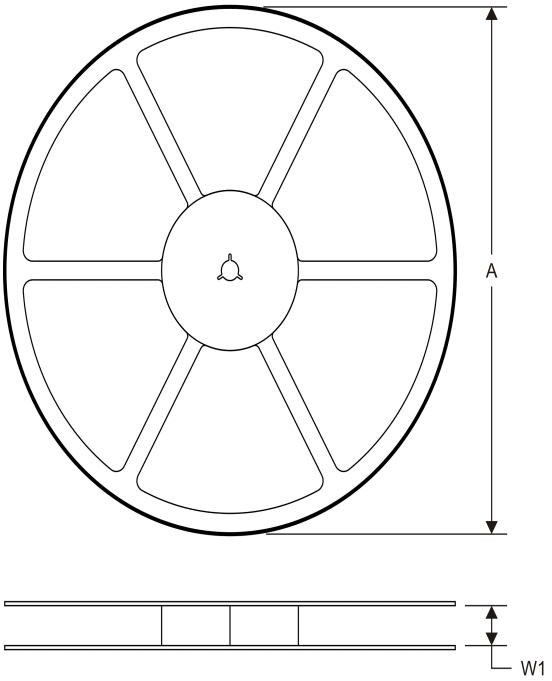
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

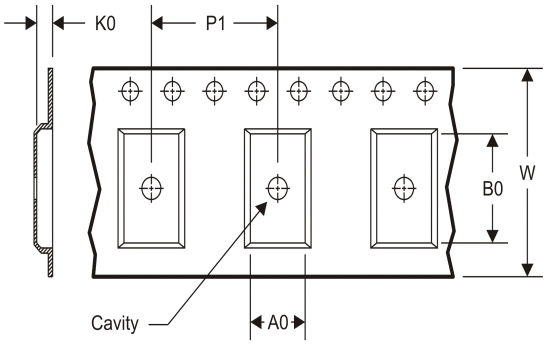
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



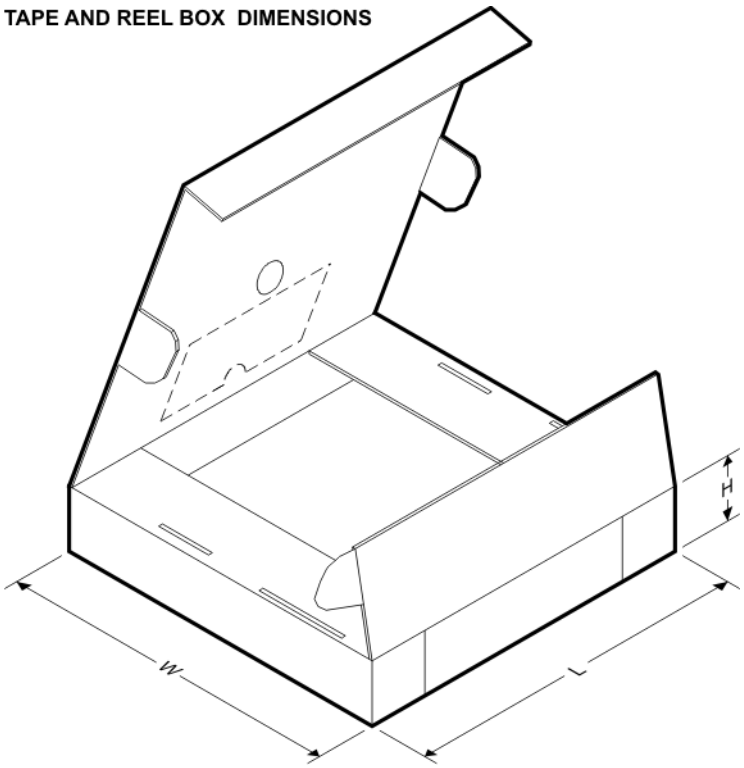
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM9102RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCM9102RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

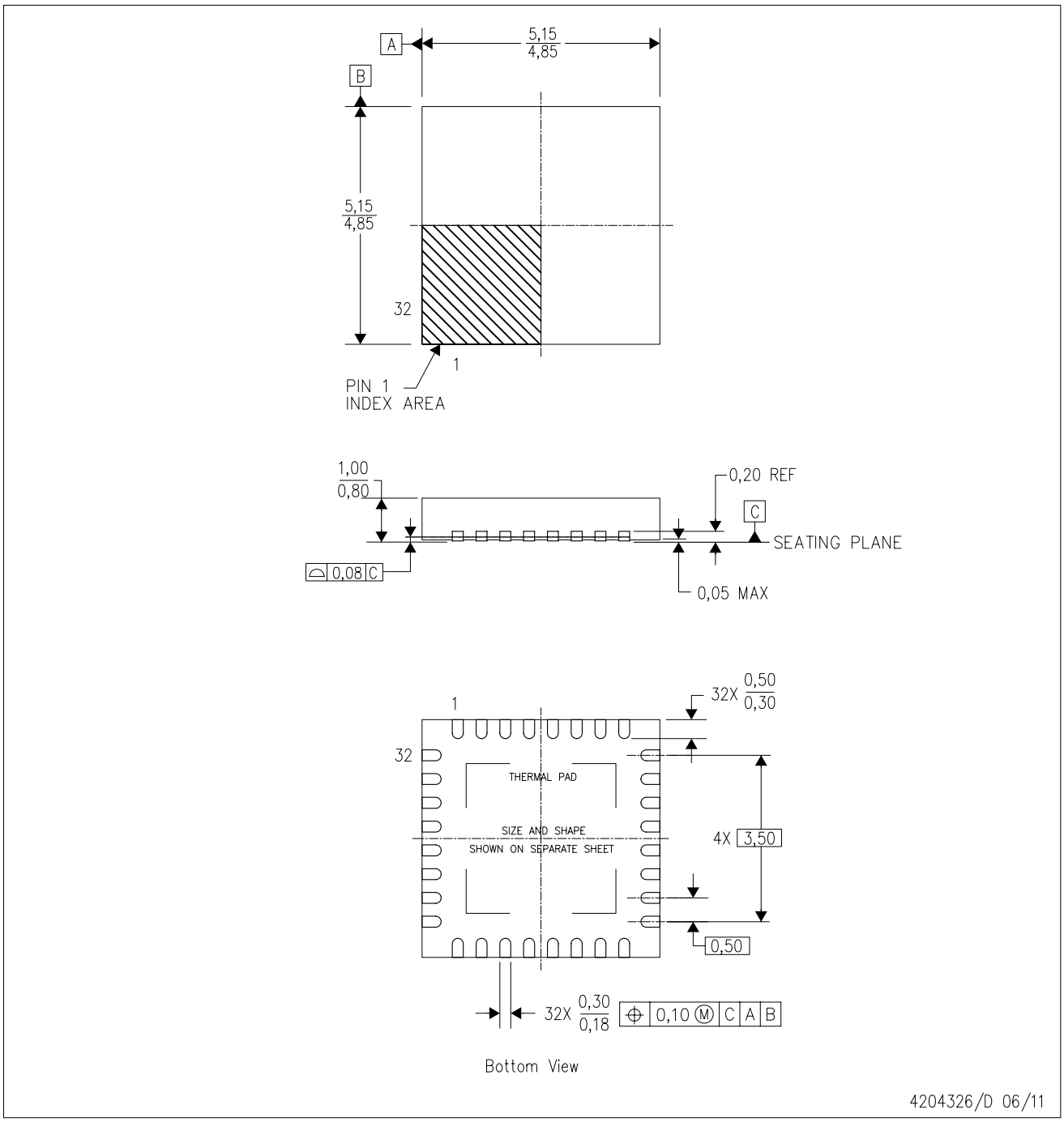
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM9102RHBR	QFN	RHB	32	3000	367.0	367.0	35.0
CDCM9102RHBT	QFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

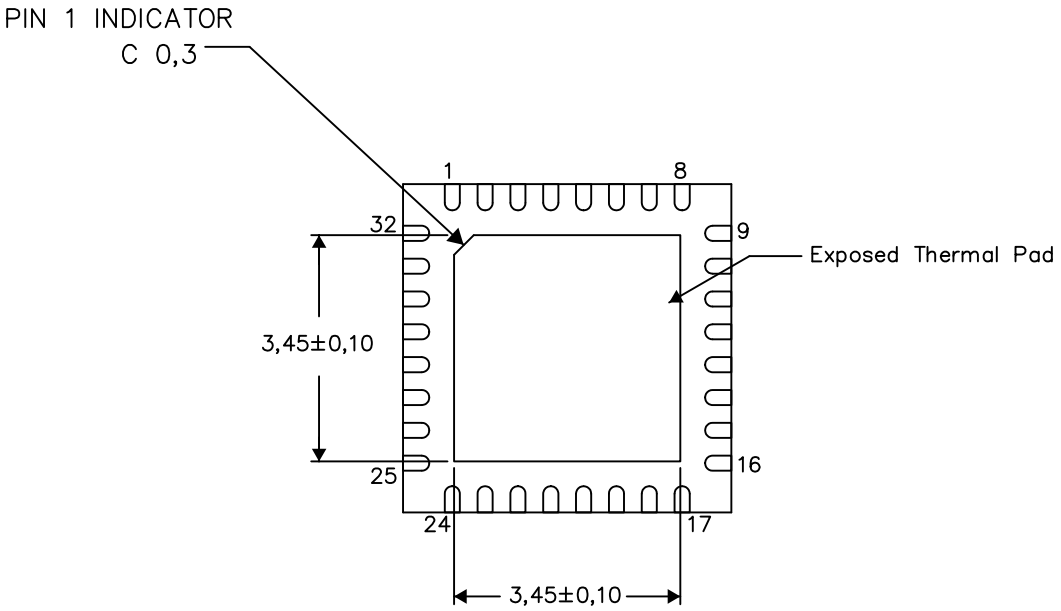
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



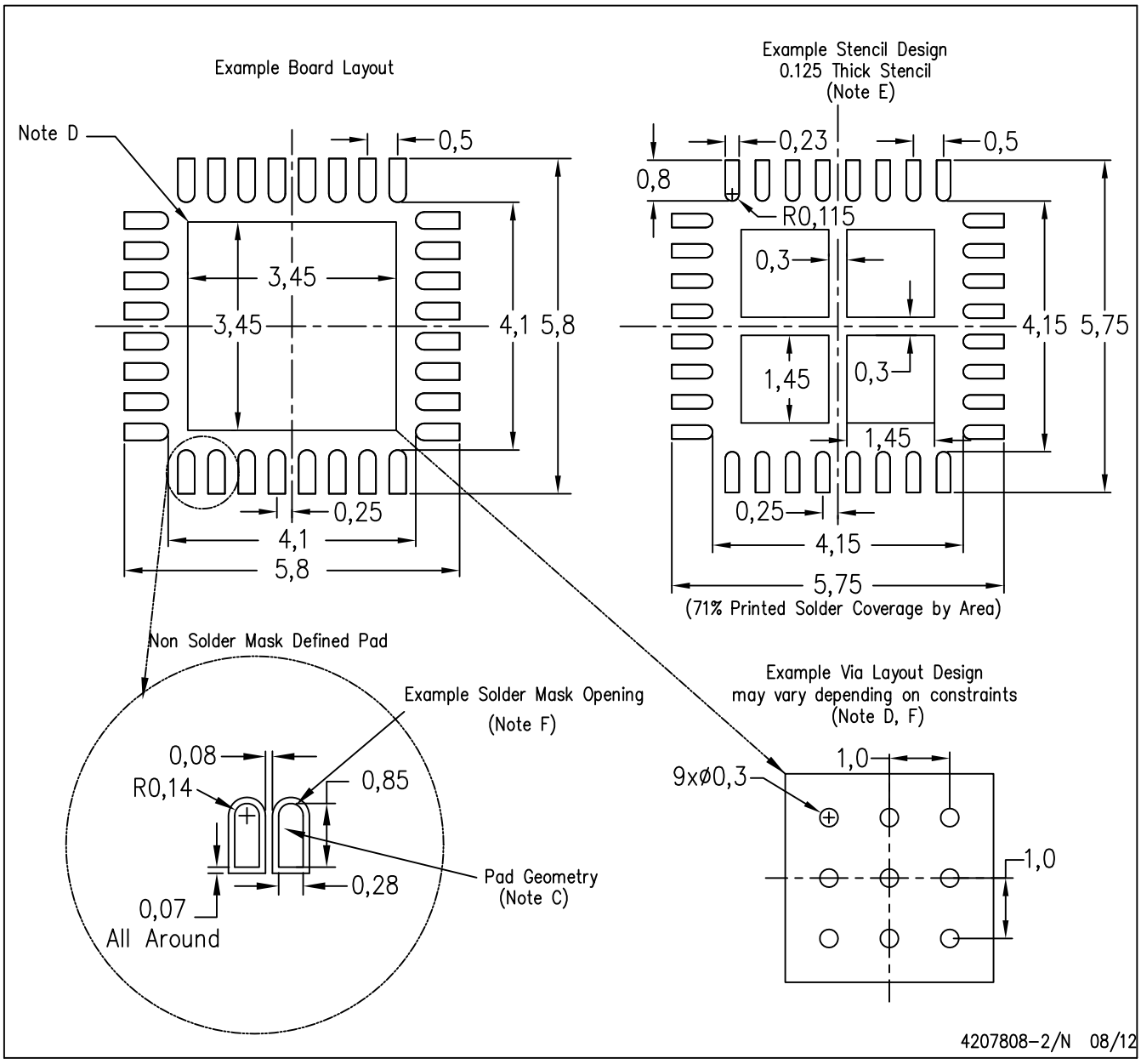
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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