Preliminary Information

PROCESSOR
Data Sheet

This is **Version 0.9** of the IDT WinChip 3 Processor data sheet.

The latest versions of this data sheet may be obtained from

www.winchip.com

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as components in life support or other medical devices or systems (hereinafter life support devices) unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices are devices which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **This policy covers any component of a life support device or system whose failure to perform can cause the failure of the life support device or system, or to affect its safety or effectiveness.**

REVISION HISTORY

DATE	*VERSION*	*REVISION*
4/1999	0.9	Initial internal use release

CONTENTS

1 INTRODUCTION

The IDT WinChip 3™ processor family, designed by Centaur Technology Inc., is a plug-compatible alternative to the Intel® Pentium® processor with MMX™ technology (also known informally as the *P55C* processor). In addition to the Intel Pentium family, the IDT WinChip 3 processor family also directly competes with other "Socket 7"-compatible processors such as the AMD K6™, the AMD K6-2™, and the Cyrix® 6x86MX/MII™ processors.

The IDT WinChip 3 processor family is based on a unique Centaur-developed design approach and is manufactured with the IDT 0.25-micron CMOS technology. This technology provides high-performance, low-cost, and low-power solutions to the desktop personal computer market.

When considered individually, the function, performance, and cost of the IDT WinChip 3 processor family are all very competitive. When considered as a whole, the IDT WinChip 3 processor family offers a breakthrough level of *value*.

1.1 BASIC FEATURES

The IDT WinChip 3 processor family comprises several versions. All family versions share the following common features:

Notable Features

- Plug-compatible with the Intel Pentium processor—bus, electrical interface, and physical package ("Socket 7").
- Software-compatible with Intel Pentium processors and the thousands of X86 software applications available.
- Software-compatible with Intel MMX technology.
- Two large (64-KB each) on-chip caches.
- Two large TLBs (128 entries each).
- Sophisticated branch prediction mechanism.
- Two MMX units with superscalar execution.
- Bus speeds up to 100 MHz (Super7™ bus).
- Very small die (76 mm^2 in IDT 0.25-micron technology).

1.2 PROCESSOR VERSIONS

The IDT WinChip 3 processor is ideally suited for desktop applications. These basic versions are offered in several internal speed ranges and several different voltage settings.

WinChip 3

- 3DNow!™ instructions. These new instructions are compatible with the 3DNow! instructions included in the AMD K6-2 processor. These instructions provide significant performance improvements for 3D geometry and lighting calculations.
- 3DNow! instructions are directly utilized by Microsoft's Direct3D version 6 as well as by many games.

Speed Versions

- The IDT WinChip 3 processor is initially available in several speed grades:

  233 (3x66-MHz),

  266 (3.5x66-MHz),

  300 (2.33x100-MHz),

  300 (4x66-MHz),

  333 (2.5x100-MHz),

  333 (2.66x100-MHz).
- Future versions of the WinChip 3 processor will provide other speed grades and bus speed combinations.

Voltage Versions

- IDT WinChip 3 processors initially support one of two voltage ranges:

  Desktop 2.8V (2.7V–2.9V)

  Mobile 2.2V (2.1V–2.9V)

1.3 COMPETITIVE COMPARISONS

The following tables summarize the major features of the IDT WinChip 3 processor and its primary competitors. The competitive information is as specified in the competitive processor's data sheets and is accurate only as of the time this datasheet was written. The features are those that characterize the primary capabilities of an x86 processor. Additional specifics on the WinChip 3 processor design are found in Chapter 2.

The major themes of this summary are:

- The IDT WinChip 3 processor has equivalent or better cache and TLB capabilities. These are critical to system performance for modern PC operating systems and applications. (See Table 1-1)
- The IDT WinChip 3 processor has a generally simpler internal architecture than its competitors. However, the IDT WinChip 3 selectively implements advanced features like superscalar execution and branch prediction. This design approach results in good performance and a very efficient design (See Table 1-2).
- The IDT WinChip 3 processor has a much smaller die than its competitors (See Table 1-3).

Table 1-1. Cache and TLB Characteristics.

MAJOR FEATURES		*WINCHIP 3*	*INTEL P55*	*AMD K6*	*CYRIX 6x86MX/MII*
I-Cache	Size	64 KB	16 KB	32 KB	256
	Data Ways	2	4	2	assoc
D-Cache	Size	64 KB	16 KB	32 KB	64 KB unified I & D cache
	Data Ways	4	4	2	4
TLB	Size (I / D)	128 / 128	32 / 64	64 /128	16
	Ways	8	assoc	?	direct
	L2 TLB	N	N	N	64 x 6
Page Dir Cache		8 entries	N	N	N

Table 1-2. Microarchitecture Characteristics.

MAJOR FEATURES		WINCHIP 3	INTEL P55	AMD K6	CYRIX 6x86MX/MII
Decode	General	1 Inst In-order	2 Insts In-order	3 Insts In-order	2 Insts In-order
	MMX/3D	2 Insts In-order			
Issue & Execute		Single In-order	2 Insts In-order	3 insts Out-order	2 Insts Out-order
	MMX/3D	2 Insts In-order			
Branch Prediction		Y	Y	Y	Y
Call/Return Stack		8 entries	Y	16 entries	N

Table 1-3. Technology & Die Size

MAJOR FEATURES	WINCHIP 3	INTEL P55	AMD K6-2	CYRIX 6x86MX/MII
Technology	0.25µ	0.25µ	0.25µ	0.25µ
Metal Layers	5LM	4LM	5LM+LI	4LM
Die Size	76 mm^2	98 mm^2	81 mm^2	88 mm^2

1.4 COMPATIBILITY

The IDT WinChip 3 processor is compatible with the Intel Pentium processor with MMX technology.

An IDT WinChip 3 processor can plug into existing Pentium processor-based desktop and portable system boards and can operate without requiring changes to the system hardware. In some cases, a special BIOS may be needed (due to possible use by the BIOS of Pentium processor-unique machine specific registers). Currently, BIOS support for the IDT WinChip 3 processor is available from Award, AMI, Phoenix, and Insyde.

The IDT WinChip 3 processor does not provide Pentium-compatible dual processing (neither do the mobile Pentium processor, the AMD K6 and AMD K6-2 processors, nor the Cyrix 6x86MX/MII processor).

Note that *all* processors developed for use in PCs ("x86" processors) have some differences in low-level functions. (These include differences between the various Intel processors and between Intel processors and the equivalent Cyrix and the AMD processors.) The IDT WinChip 3 processor has similar differences.

IDT has performed extensive testing of hundreds of PC boards, peripherals, software applications, and operating systems to confirm the IDT WinChip 3 processor's compatibility.

Indicative of this compatibility, the IDT WinChip 3 processor has XXCAL Inc. Platinum Certification (their highest compatibility rating) and will soon obtain Windows 98 and Windows NT certification.

Designed for Microsoft® Windows®98

PLATINUM XXCAL, INC. TESTING LABORATORIES CERTIFIED

1.5 DATA SHEET ASSUMPTIONS

The IDT WinChip 3 processor specifications are directly based upon the Pentium processor's external specifications as defined by: (1) publicly available Intel publications, and (2) by the actual behavior (derived from testing) of the Pentium processor. This data sheet book provides only minimal descriptions of these Pentium-compatible functions. The major emphasis in this document is to describe differences from the explicit and implicit (behavioral) Pentium specifications.

The intent of these specifications is to make it easy for a board designer, system designer, or BIOS developer to utilize the IDT WinChip 3 processor in place of the Pentium processor or the Pentium processor with MMX technology. (This, of course, makes it trivially easy for the end-user to be able to exploit the advantages of the IDT WinChip 3 processor.) We assume that the reader is a potential direct user of the IDT WinChip 3 processor and is thus familiar with the specifications of the Pentium processor.

Table 1-4 lists some relevant documents that define the reference x86 architecture.

Table 1-4. x86 Architecture Specification Documents

DOCUMENT TITLE	*INTEL ORDER #*	*VERSION*
Intel Architecture Software Developer's Manual, Vol. 1	243190	001
Intel Architecture Software Developer's Manual, Vol. 2	243191	001
Intel Architecture Software Developer's Manual, Vol. 3	243192	001
Pentium Processor Family Developer's Manual	241428	005
Pentium Processor with MMX Technology	243185	004
Pentium Processor Specification Update	242480	027

2 WINCHIP 3 ARCHITECTURE

2.1 INTRODUCTION

The IDT WinChip 3 processor is externally (bus and software) compatible with the Intel Pentium processor with MMX Technology. However, the internal architecture and design of the IDT WinChip 3 processor is very different from that of the Pentium processor and other contemporary x86 processors such as the AMD K6 and Cyrix 6x86MX/MII processors. The IDT WinChip 3 processor uses a unique design approach that provides significant benefits to the end-user.

This design approach provides high performance at low cost and low power using a unique architecture that includes large on-chip caches and is extensively optimized for the target PC environment. The resulting IDT WinChip 3 processor is smaller (die size is only 58 mm^2 in 0.25µ geometry technology) than any other x86 processor yet has comparable performance to the most recent processors.

Philosophically, the IDT WinChip 3 processor's internal design is a return to the same basic concepts of RISC design that allowed microprocessor performance breakthroughs in the 1980s. Recently, however, contemporary x86 processors have followed a different path using very complex internal designs employing advanced architecture concepts such as superscalar execution, out-of-order instruction execution, reorder buffers, non-blocking caches, and so forth (these terms are all found in the datasheets of competitive products).

Unfortunately, while these advanced technical concepts make for good technical reading, the real bottom-line benefit that they provide to the end-user has been limited; especially when considering the resultant large chip sizes (resulting in high costs) and high power consumption. No such advanced technical hocus-pocus is to be found on an IDT WinChip 3 processor — it merely offers compatibility with good performance, low cost, and low power consumption.

2.2 KEY CONCEPTS

The key concepts underlying the IDT WinChip 3 processor design are:

- *Simple instructions (load, store, branch, ALU) dominate instruction execution time.* This is the basic RISC design concept, which is also true in the x86 architecture: over 90% of instructions executed come from these basic categories. Of course, "simple" x86 instructions are more complex than corresponding RISC architecture instructions.

  The IDT WinChip 3 processor optimizes the performance of these types of basic x86 instructions while minimizing the hardware provided for other little-used x86 functions. The little-used instructions are primarily implemented in microcode with minimal hardware support.

- *Memory performance is the limiting CPI performance factor.* Due to the high ratio of internal clock speed versus the relatively limited PC processor-bus speed, off-chip memory-access performance is the primary factor in processor CPI performance (as opposed to internal instruction execution performance).

  The IDT WinChip 3 processor addresses this phenomenon by providing very large on-chip caches and TLBs that run at the high internal processor clock frequency. In addition, sophisticated TLB and cache management algorithms are included to further reduce bus activity.

- *Optimize the design for the target user environment.* The IDT WinChip 3 processor implements very specific and detailed design tradeoffs to provide high performance with low cost. Minimal hardware is provided for functions that are not heavily used or that are not critical to performance in the target environments (low-end desktop and mobile systems). These design optimizations are based on extensive and detailed analysis of the actual behavior of Windows operating systems and applications

- *Small is beautiful.* The IDT WinChip 3 processor is highly optimized for small physical size and fewer logic transistors. In addition to the obvious cost benefits, this small size provides secondary benefits of low power consumption and improved reliability.

2.3 COMPONENT SUMMARY

2.3.1 General Architecture

Figure 2-1 illustrates the basic components of the IDT WinChip 3 processor.

Fundamentally, the IDT WinChip 3 processor's internal design is a classic five-stage integer pipeline execution core with an additional instruction translation stage to translate x86 instructions coming from the fetch stage into the internal micro-instruction format.

Fetching and translating x86 instructions is asynchronous to the internal execution pipeline. Integer and floating-point instructions are issued and executed one at a time in program order. MMX and 3DNow! instructions can be paired and issued and executed two at a time. All instructions are executed and retired in order. Cache and TLB misses stall the pipeline until the data is available for the requesting instruction.

In spite of this basic micro-architecture, the IDT WinChip 3 processor achieves high performance through several mechanisms:

- Good CPI on highly used instructions. The IDT WinChip 3 processor implements specific design features to reduce the number of cycles for heavily used instructions — including complex functions such as protect-mode segment-register loads and string instructions.
- Very large and fast on-chip caches and TLBs. These reduce the bus wait component of system performance, which can be equal to the processor-running component.
- Lots of fine-tuning and low-level optimizations. This includes such items as fast unaligned data access and fewer pipeline interlocks than the Pentium processor.
- Issue and execution pairing on instructions that benefit significantly from dual execution. This feature, like all others, is highly tuned for x86 application code.

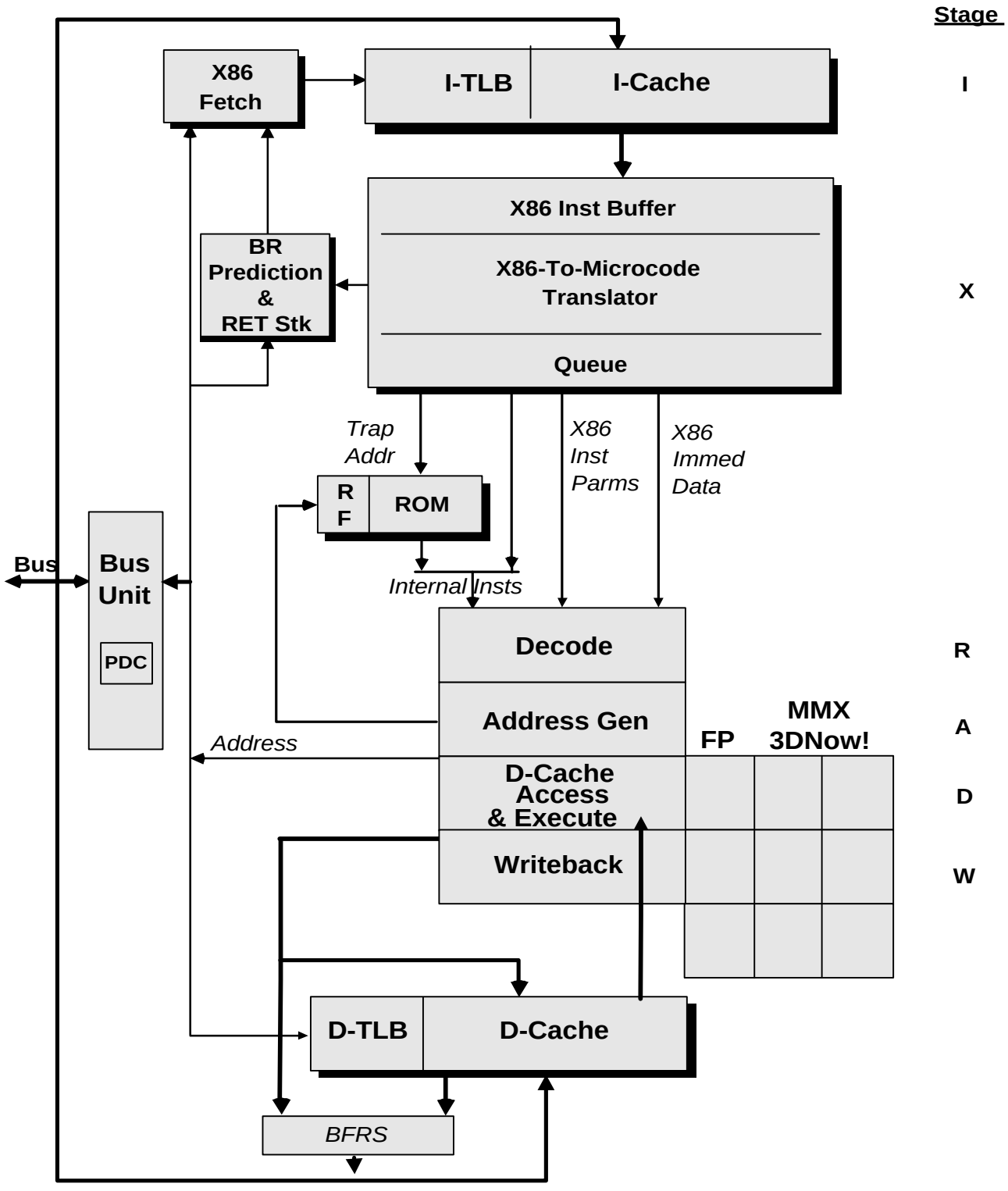


Figure 2-1. IDT WinChip 3 Processor Data Flow

2.3.2 I-Cache

The I-cache contains 64KB organized as two-way set associative with 32-byte lines. An LRU replacement algorithm is used. The associated I-TLB contains 128 entries organized as 8-way set associative with a 7-bit pseudo-LRU replacement algorithm. This large cache and TLB has a one-clock access time and operates at the high clock frequencies of the IDT WinChip 3 processor.

The I-TLB utilizes an 8-entry unified page directory cache that significantly reduces the TLB miss penalty. In addition, the I-cache control logic includes several innovative features that minimize cache invalidates and unnecessary bus fetches.

As opposed to many other contemporary x86 processors, the data in the I-cache is exactly what came from the bus; that is, there are no “hidden” pre-decode bits. This facilitates the provision of large cache capacity in a small physical size.

The I-cache is dynamically turned off when not used to reduce power requirements.

2.3.3 Translator Unit

The I-cache or bus unit delivers up to 16 bytes per clock to an x86 instruction buffer in the translator unit. The translator converts x86 instructions to internal instruction and data forms. Assuming that the instruction is in the x86 instruction buffer at the start of the cycle, the translator translates an entire x86 instruction in one clock. Instruction prefixes other than 0F require an additional translator cycle for each prefix. However, due to the asynchronous fetch and “lookahead” capability of the translator, these extra cycles for prefixes rarely result in a bubble in the execution pipeline.

The translator can also translate two MMX or two 3DNow! instructions each clock. The “pairing” rules for allowed combinations are similar to those for MMX on the Pentium processor and for 3DNow! on the AMD K6-2 processor.

The output of the translator is: (1) the internal micro-instruction stream to perform the x86 instruction function, (2) the immediate data fields from the x86 instruction, and (3) various x86 state information used to control execution (for example, operand size). The internal instruction stream for an x86 instruction can consist of micro-instructions directly generated by the translator, or micro-instructions from the on-chip ROM (microcode), or both. For performance-sensitive instructions, there is no delay due to access of micro-code from ROM.

The microcode ROM capacity is larger than most x86 microcode ROMs to allow more unimportant (relative to performance) functions to be performed in microcode (versus in hardware), to allow extensive self-test microcode, and to allow extensive built-in debugging aids (for processor design debug).

Instruction fetch and translator operation is made asynchronous from micro-instruction execution via a three-entry translated-instruction queue between the translator and the execution unit. Each entry contains up to three internal instructions for the corresponding x86 instruction. Most performance-critical x86 instructions can be represented by these three generated instructions. This queue allows the translator to “look-ahead” and continue translating x86 instructions even though the execution unit is stalled or is busy with a microcode sequence. The translator can also overlap generation of multiple internal instructions with translating prefixes on the subsequent instruction.

2.3.4 Branch Prediction Unit

The IDT WinChip 3 has two advanced branch prediction mechanisms. These predict the branch target address and whether the branch is to be taken during the translator stage (X).

The branch target address for displacement branches is directly calculated while the branch instruction is the X- stage. The target address is fetched from the I-cache during the next cycle. This direct calculation of the target address eliminates the need for a large branch target buffer (BTB) such as found in the Pentium processor.

The prediction of the direction of conditional branches is performed by a state-of-the-art mechanism. A 12-bit global branch history is combined with the branch address to index a dynamically updated branch history table (BHT) with 4K entries. The BHT entry predicts whether the conditional branch direction will agree with a default direction guess by the translator. The translator guess is 70% accurate leading to an overall BHT prediction accuracy of over 90%.

In addition, x86 Return instructions are accurately predicted by an 8-entry Return-address stack.

2.3.5 Execution Unit

Internal micro-instructions are executed in a tightly coupled four-stage pipeline that is very similar in structure to a basic RISC pipeline:

- **Decode stage (R)**: Micro-instructions are decoded, integer register files are accessed, resource dependencies evaluated, and so forth.
- **Addressing stage (A)**: Memory addresses are calculated and sent to the cache units. The IDT WinChip 3 processor is capable of calculating most x86 instruction address forms in one clock; a few forms containing two registers or a shifted index register require two clocks.

  Branches (x86 and microcode) are also resolved in the A-stage. A fast forwarding mechanism allows the EFLAGS result of the instruction in front of a conditional branch (in the D-stage) to resolve conditional branches in the A-stage. Resolving branches in the A-stage means that a mispredicted, or not predicted, branch causes only a three clock stall.

- **The Execute stage (D):** Integer ALU operations or load accesses to the D-cache are performed. All basic register-register ALU functions take one clock except multiply and divide. Load-ALU and Load-ALU-store sequences require only two clocks; the ALU operation and the store are combined.

  During this stage the floating-point, MMX and 3DNow! execution units access their registers. These execution units "hang off" the end of the main execution unit so that load-ALU operations for these units can be pipelined in one clock.

- **Write-back stage (W)**: The results of operations are committed to the registers and store data is written to the D-cache or external write buffers.

Although the pipeline structure is similar to non-x86 processors, the micro-instructions and associated execution units are highly tuned to the x86 architecture. The micro-instructions closely resemble the corresponding x86 instructions. Examples of specialized hardware features supporting the x86 architecture are: hardware handling of the x86 condition codes, segment descriptor decode and manipulation instructions, hardware to automatically save the x86 floating-point environment, and so forth.

2.3.6 D-Cache

The D-cache is very similar to the I-cache (except for set-associativity): 64 KB organized as four-way set associative with 32-byte lines. A 3-bit pseudo-LRU replacement algorithm is used. The associated D-TLB contains 128 entries organized as 8-way set associative with a 7-bit pseudo-LRU replacement algorithm. This large cache has a one-clock access time and is designed to operate at the high clock frequencies of the IDT WinChip 3 processor. The D-TLB shares the 8-entry unified page directory cache that reduces the TLB miss penalty. The D-cache is dynamically turned off when not used to reduce power requirements.

2.3.7 X86 Fetch Unit

The x86 instruction fetch unit manages fetching instructions and I-TLB entries from the bus and delivering instructions from the I-cache. It implements a "smart" instruction prefetch mechanism to minimize wasted bus cycles.

2.3.8 FP Unit

In addition to the integer execution unit, the IDT WinChip 3 processor has a separate 80-bit floating-point execution unit that can execute x86 floating-point instructions in parallel with integer instructions.

The floating-point unit is designed to maximize clock frequency and to minimize chip size while providing good floating-point performance for typical desktop use. The unit is fully pipelined and can start a floating-point add or multiply each clock.

The IDT WinChip 3 processor issues only one instruction per clock into the main instruction pipeline. However, once a hardwired floating point instruction (load, store, add, multiply, divide, square root, etc.) reaches the FP unit, following integer instructions can execute in parallel with the floating-point instruction. Certain little-used and complex floating point instructions (sin, atan, etc.) use the integer instruction pipeline and thus cannot be overlapped with integer execution.

The floating-point unit is dynamically turned off when not used to reduce power requirements.

2.3.9 MMX Units

The IDT WinChip 3 processor contains two separate execution units for the MMX-compatible instructions. Up to two MMX instructions are issued and executed each clock (using the same pairing rules as for the Pentium processor).

Each MMX unit contains an adder and logic functions. One MMX unit has a multiplier-adder and the other has a shifter/packer. The multiplier(-adder) is fully pipelined and can start one MMX multiply[-add] instruction (which consists of up to four separate multiplies) every clock. The MMX units share hardware with the 3DNow! units such that in any clock only two MMX or 3DNow! instructions can be executed.

Architecturally, the MMX registers are the same as the floating-point registers. However, there are actually two different register files (one in the FP-unit and one in the MMX units) that are kept synchronized by hardware.

The MMX unit is dynamically turned off when not used to reduce power requirements.

2.3.10 3DNow! Units

The IDT WinChip 3 processor contains two separate execution units for the new 3DNow! instructions. These instructions are compatible with the AMD K6-2 processor 3DNow! instructions and provide performance assists for graphics transformations via new SIMD single-precision floating-point capabilities. Up to two 3DNow! instructions are issued and executed each clock. Each instruction operates on two single precision floating-point numbers.

One 3DNow! unit has two single-precision floating-point multipliers. The other unit has two single-precision floating-point adders. Other functions such as conversions, reciprocal, and reciprocal square root are provided by the appropriate unit.

The multiplier and adder are fully pipelined and can start one 3DNow! multiply instruction (which consists of two separate multiplies) and one 3DNow! add instruction (which consists of two separate adds) every clock.

2.3.11 Bus Unit

The IDT WinChip 3 processor bus unit provides an external bus interface compatible with the Pentium processor. In addition to the expected bus control functions, the bus unit implements an eight-entry page-directory cache to reduce the impact of TLB misses. Four 64-bit write buffers allow internal execution to proceed overlapped with waiting for external stores to complete.

The IDT WinChip 3 processor bus unit contains many special features designed to reduce bus traffic and cache disruption. Examples include store byte-combining function (optional), cache cast-out snarfing, “smart lock” management mechanisms, weak-read ordering (optional), and so forth. The optional features are controlled by memory range registers that allow different address-space regions to have different characteristics.

The IDT WinChip 3 supports bus speeds of 60, 66, 75, 83, 95 and 100 MHz. The 100 MHz bus is compatible with the AMD Super7 bus architecture. The IDT WinChip 3 supports integer and fractional ratios of the bus frequency to core frequency.

3 PROGRAMMING INTERFACE

3.1 GENERAL

In general, the IDT WinChip 3 processor is compatible with both the bus and software-visible architecture of the Intel Pentium processor with MMX technology. That is, a program that executes on a Pentium processor should generally execute on an IDT WinChip 3 processor and produce the same results (with the exceptions as noted in this datasheet).

The IDT WinChip 3 processor's Pentium-compatible functions include:

- All basic X86 instructions, registers, and functions
- All floating-point (numeric processor) instructions, registers and functions
- All new Pentium processor instructions and registers (CMPXCHG8B, RDMSR, WRMSR, RDTSC, CPUID, RSM, MOV CR4)
- All basic operating modes: real mode, protect mode, virtual-8086 mode
- System Management Interrupt (SMI) and the associated System Management Mode (SMM)
- All interrupt and exception functions
- All debug functions (including the new I/O breakpoint function)
- All input/output functions
- All tasking functions (TSS, task switch, etc.)
- Processor initialization behavior

The IDT WinChip 3 processor, in addition to the MMX instructions, also includes 3Dnow! instructions to boost the performance of 3D graphics.

However, there are some differences between the IDT WinChip 3 processor and the Pentium processor. These differences fall into four groups:

- **Additional IDT WinChip 3 processor functions**. Examples are memory range registers that allow different attributes for each range. These additional functions are provided through Machine Specific Registers such that compatibility is not affected.
- **Implementation-specific differences**. Examples are cache and TLB testing features, and performance monitoring features that expose the internal implementation features. These types of functions are incompatible among *all* different x86 implementations.—including the Intel486, the Pentium, and the Pentium Pro processors.
- **Omitted functions**. Some Pentium processor functions are not provided on the IDT WinChip 3 processor because they aren't used or aren't needed in the targeted PC systems. Examples are some specific bus functions such as functional redundancy checking and performance monitoring.

  These types of differences are similar to those among various versions of the Pentium processor (for example, the mobile Pentium processor also omits the same bus functions as omitted by the IDT WinChip 3 processor), and among the AMD-K6 and Cyrix 6x86MX/MII processors.
- **Low-level behavioral differences**. A few low-level IDT WinChip 3 processor functions are different from the Pentium because the results are (1) documented in the Intel documentation as *undefined*, and (2) known to be different for different x86 implementations (in particular, different among the Intel i486, the Pentium, and the Pentium Pro processors). That is, compatibility with the Pentium processor for these functions is clearly not needed for software compatibility (or they wouldn't be different across different implementations). Where the Pentium and Pentium Pro processor results differ, the IDT WinChip 3 processor often provides the Pentium Pro result.

This chapter summarizes the first three types of differences: additional functions, implementation-specific functions, and omitted functions. *Appendix A* contains more details on machine-specific functions. *Appendix B* contains details on low-level differences.

In some areas, we also include comparative information about the Pentium Pro, AMD-K6, and Cyrix 6x86MX/MII processors. This information is taken from the data sheets of these products and has not been verified by IDT. Our Pentium processor information, however, is based on detailed testing.

3.2 ADDITIONAL FUNCTIONS

The IDT WinChip 3 processor provides some memory range management functions. These are similar in concept, but different in specifics, to memory range registers in the Pentium Pro, AMD-K6, and Cyrix 6x86MX/MII processors (all of which are different from each other). These functions are provided via Machine Specific Registers. *Appendix A* provides specifics on the IDT WinChip 3 Machine Specific Registers. Note that there are differences in the specifics of memory range management between the IDT WinChip 3 and its predecessor, the *IDT WinChip C6*. The IDT WinChip 3 processor supports extended CPUID functions, as defined by AMD. The IDT WinChip 3 processor also includes instructions to boost the performance of 3D graphics compatible with the AMD-3D Now! technology

3.3 MACHINE-SPECIFIC FUNCTIONS

3.3.1 General

All x86 processor implementations provide a variety of *machine-specific functions*. Examples are cache and TLB testing features, and performance monitoring features that expose the internal implementation features. These types of functions are different and incompatible among all different x86 implementations—including the Intel i486, the Pentium, and the Pentium Pro processors, and between these processors and competitive processors from Cyrix and AMD. The Intel documentation clearly identifies these types of functions as machine-specific and warns of possible changes in new implementations.

This section describes the IDT WinChip 3 processor machine-specific functions that are most likely used by software and compares them to related processors where applicable. *Appendix A* describes the IDT WinChip 3 processor machine-specific registers (*MSR*s).

This section covers those features of Pentium-compatible processors that are used to commonly identify and control processor features. All Pentium-compatible processors have the same mechanisms, but the bit-specific data values often differ.

3.3.2 Standard CPUID Instruction Functions

The CPUID instruction is available on all contemporary x86 processors. The CPUID instruction has two standard functions requested via the EAX register. The first function returns a vendor identification string in registers EBX, ECX and EDX. The second CPUID function returns an assortment of bits in EAX and EDX that identify the chip version and describe the specific features available.

The EAX:EBX:ECX:EDX return values of the CPUID instruction executed with EAX=0 are:

Table 3-1

REGISTER[BITS] – MEANING	*WINCHIP 3*	*P54*	*P55*	*K6*	*M2*
EAX (highest EAX input value understood by CPUID)	1	1	1	1	1
EBX:EDX:ECX (vendor ID string)	“Centaur Hauls”	“Genuine Intel”	“Genuine Intel”	“Authentic AMD”	“Cyrix Instead”

The EAX return values of the CPUID instruction executed with EAX == 1 are:

Table 3-2

EAX BITS - MEANING	*WINCHIP 3*	*P54*	*P55*	*K6*	*M2*
3:0 - Stepping ID					
7:4 - Model ID	Same as the return value in EDX after Reset (see next section)				
11:8 - Family ID					
13:12 - Type ID					

The EDX return values of the CPUID instruction with EAX=1 are:

Table 3-3

EAX BITS - MEANING	WINCHIP 3	P54	P55	K6	M2	NOTES
0 - FP present	1	1	1	1	1	
1 - VM86 Extensions (VME)	0	1	1	1	0	1
2 - Debugging Extensions	1	1	1	1	1	
3 - Page Size Extensions (4MB)	0	1	1	1	0	1
4 - Time Stamp Counter (TSC) supported	1	1	1	1	1	2
5 - Model Specific Registers present	1	1	1	1	1	3
6 - PAE supported (P6 Function)	0	0	0	0	0	4
7 - Machine Check Exception	1/0	1	1	1	0	5
8 - CMPXCHG8B instruction	0/1	1	1	1	1	6
9 - APIC supported	0	1	1	0	0	7
10:11 -Reserved						
12- Memory Range Registers	0	0	0	0	0	8
13 - PTE Global Bit supported	0	0	0	0	1	4
14- Machine Check Architecture supported	0	0	0	0	0	4
15- Conditional Move supported	0	0	0	0	1	4
16:22 - Reserved						
23 - MMX supported	1/0	0	1	1	1	9
24:31 - Reserved						

Notes On CPUID Feature Flags

General: an "x/y" entry means that the default setting of this bit is x but the bit (and the underlying function) can be set to y using the FCR MSR.

1. These "Appendix H" functions are not provided on the IDT WinChip 3 processor since they are not used by the target operating systems. They are also not provided on the Cyrix 6x86MX/MII processor.
2. The IDT WinChip 3 processor implementation varies slightly from that of the Pentium processor in a way that should have no practical impact.
3. Every system has different MSRs—addresses and contents.
4. This is a function introduced with the Pentium Pro processor and is generally not provided on Pentium-compatible processors.
5. The Machine Check exception is defined by Intel documentation as machine-specific. The IDT WinChip 3 processor's Machine Check has slightly different specifics than the Pentium processor's Machine Check function. The Machine Check support can be enabled or disabled by a bit in the FCR MSR. The CPUID bit reports the current setting of this enable control.
6. The Pentium processor-compatible CMPXCHG8B instruction is provided and always enabled. However, the default for the corresponding CPUID function bit is 0 (due to a bug found in Windows NT). This default can be changed via a bit in the FCR MSR.
7. This is an Intel-specific multiprocessing function. None of the other Pentium-compatible processors provide this function since it has no utility in the target system environment.
8. The IDT WinChip 3 and Cyrix 6x86MX/MII processors have memory range registers, but the specifics are not compatible with the P6 MRRs. The Pentium processor has no memory range registers.

9. The IDT WinChip 3 processor's MMX-technology compatible instruction support can be enabled or disabled by a bit in the FCR. The CPUID bit reports the current setting of this enable control.

3.3.3 Extended CPUID Instruction Functions

The IDT WinChip 3 processor supports extended CPUID functions similar to those provided by the AMD-K6 and Cyrix 6x86MX/MII™. These functions provide additional information about the IDT WinChip 3.

Extended CPUID functions are requested by executing CPUID with EAX set to any value in the range 0x80000000 through 0x80000005.

The IDT WinChip 3 CPUID instruction aliases EAX values in the range 0xC0000000 through 0xC0000005 to the extended functions in the range 0x80000000 through 0x80000005 (there is no guarantee that this will be true in future processors. The following table summarizes the extended CPUID functions.

EAX	*TITLE*	*OUTPUT*
80000000	Largest Extended Function Input Value	EAX=80000005 EBX,ECX,EDX=Reserved
80000001	Processor Signature and Feature Flags	EAX=Processor Signature EBX,ECX=Reserved EDX=Extended Feature Flags
80000002	Processor Name String	EAX,EBX,ECX,EDX
80000003	Processor Name String	EAX,EBX,ECX,EDX
80000004	Processor Name String	EAX,EBX,ECX,EDX
80000005	TLB and Cache Information	EAX = Reserved EBX = TLB Information ECX = L1 Data Cache Information EDX = L1 Instruction Cache Information

Largest Extended Function Input Value (EAX=0x80000000)

Returns 0x80000005 in EAX, the largest extended function input value.

would be returned by extended function EAX=0x80000002 as follows:

EAX = 0x20544449

EBX = 0x436E6957

ECX = 0x20706968

EDX = 0x44332D32

Since the string is exactly 16 bytes, the extended functions EAX=0x80000003 and EAX=0x80000004 return zero in EAX, EBX, ECX, and EDX.

Note that FCR[20] is always '1' since the AMD-3Dnow! instructions are always supported on the WinChip 3.

Cache Information (EAX=0x80000005)

Returns information about the implementation of the TLBs and caches.

REGISTER	DESCRIPTION	VALUE
EAX	Reserved	
EBX	TLB Information	
EBX[31:24]	D-TLB associativity	8
EBX[23:16]	D-TLB # entries	128
EBX[15: 8]	I-TLB associativity	8
EBX[7: 0]	I-TLB # entries	128
ECX	L1 Data Cache Information	
ECX[31:24]	Size (Kbytes)	64
ECX[23:16]	Associativity	4
ECX[15: 8]	Lines per Tag	1
ECX[7: 0]	Line Size (bytes)	32
EDX	L1 Instruction Cache Information	
EDX[31:24]	Size (Kbytes)	64
EDX[23:16]	Associativity	2
EDX[15: 8]	Lines per Tag	1
EDX[7: 0]	Line Size (bytes)	32

3.3.4 Processor Identification

The IDT WinChip 3 processor provides several machine-specific features. Some of these features are compatible with those provided by P55 and are identified by the standard CPUID function EAX=1.

Other machine-specific features described in this datasheet have no P55 equivalent. These features are controlled by IDT WinChip 3 MSRs. Some of these features are not backward-compatible with the predecessor IDT WinChip C6.

System software must not assume that all future processors in the IDT WinChip family will implement all of the same machine-specific features or even that these features will be implemented in a backward-compatible manner. In order to determine if the processor supports particular machine-specific features, system software should follow the following procedure.

Identify the processor as a member of the IDT WinChip family by checking for a Vendor Identification String of "CentaurHauls" using CPUID with EAX=0. Once this has been verified, system software must determine the processor version in order to properly configure the machine-specific registers. In particular some of the control fields of the memory configuration registers were redefined for the IDT WinChip 3.

There are two ways of distinguishing between the IDT WinChip 3 and its predecessors, the IDT WinChip C6 and WinChip 2.

If system software is only concerned with programming the memory configuration registers, then it can read the MCR_CTRL register and inspect the Trait Mode Key field (MCR_CTRL[19:17]). In the IDT WinChip 3 and later versions of the processor family the Trait Mode Key must be written to the Trait Mode control field (MCR_CTRL[8:6]) in order to activate the memory configuration registers.

In general system software can determine the processor version by comparing the Family and Model Identification fields returned by the CPUID standard function EAX=1.

If the processor version is not recognized then system software must not attempt to activate any machine-specific feature.

The following table indicates how to interpret the results of both methods.

FAMILY	*MODEL*	*TRAIT MODE KEY MCR_CTRL[19:17]*	*PROCESSOR VERSION*
5	4	0	IDT WinChip C6, use appropriate datasheet.
5	8 & 9	1	IDT WinChip 2 & 3, use this datasheet

3.3.5 EDX Value After Reset.

As for other x86 processors, after reset the EDX register holds a component identification number as follows:

	31:14	13:12	11:8	7:4	3:0
EDX	Reserved	Type ID	Family ID	Model ID	Stepping ID
	18	2	4	4	4

The specific values for the various *IDT WinChip* processor types are:

PROCESSOR	TYPE ID	FAMILY ID	MODEL ID	STEPPING ID
WinChip C6	0	5	4	Varies
WinChip 2	0	5	8	Varies
WinChip 3	0	5	9	Varies

For comparison, following are the values for other X86 processors:

PROCESSOR	TYPE ID	FAMILY ID	MODEL ID	STEPPING ID
P54C	0	5	2	Varies
P55	0	5	4	Varies
Cyrix 6x86MX/MII	0	6	0	Varies
AMD-K6	0	5	6-9	Varies

3.3.6 CR4

Control register 4 (CR4) is a new feature of the Pentium processor that controls some of its advanced features. The *IDT WinChip 3* processor provides a CR4 with the following specifics:

CR4 BITS - MEANING	WIN CHIP 2	P54	P55	K6	M2	NOTES
0: VME: Enables VME feature	0	0/1	0/1	0/1	0	1
1: PVI: Enables PVI feature	0	0/1	0/1	0/1	0	1
2: TSD: Makes RDTSC inst privileged	0/1	0/1	0/1	0/1	0/1	
3: DE: Enables I/O breakpoints	0/1	0/1	0/1	0/1	0/1	
4: PSE: Enables 4-MB pages	0	0/1	0/1	0/1	0	1
5: PAE: Enables addr extensions	r	r	r	r	r	2
6: MCE: Enables machine check exception	0/1	0/1	0/1	0/1	0	3
7: PGE: Enables global page feature	r	r	r	r	0/1	2
8: PCE: Enables RDPMC for all levels	0/1	r	0/1	r	0/1	

31:9 - reserved	r	r	r	r	r	

Notes On CR4

General: a “0/1” means that the default setting of this bit is 0 but the bit can be set to (1). A “0” means that the bit is always 0; it cannot be set. An “r” means that this bit is reserved. It appears as a 0 when read, and a GP exception is signaled if an attempt is made to write a 1 to this bit.

1. The IDT WinChip 3 processor does not provide this “Appendix H” function and this CR4 bit cannot be set. However, no GP exception occurs if an attempt is made to set this bit. The Cyrix 6x86MX/MII processor also does not provide this function.
2. This is a Pentium-Pro processor function that is typically not provided on P55-compatible processor.
3. The IDT WinChip 3 processor Machine Check has slightly different specifics than the P54C Machine Check function

3.3.7 Machine-Specific Registers

The IDT WinChip 3 processor implements the Pentium family concept of Machine Specific Registers (MSRs). RDMSR and WRMSR instructions are provided and the CPUID instruction identifies that the IDT WinChip 3 processor supports MSRs. However, the IDT WinChip 3 processor MSRs are different from the Pentium and Pentium Pro processors (which are different from each other, and from the Cyrix 6x86MX/MII and AMD-K6 processors).

In general, the MSRs have no usefulness to application or operating system software and are not used. (This is to be expected since the MSRs are different on each processor). *Appendix A* contains a detailed description of the *IDT WinChip 3* processor’s MSRs.

3.4 OMITTED FUNCTIONS

This section summarizes those functions that are included in some Pentium processor versions, but are not in the IDT WinChip 3 processor.

3.4.1 Pentium Appendix H Enhancements

The infamous *Appendix H* functions are those Pentium functions that are documented in Appendix H (Advanced Functions) of Volume 3 of *the Pentium Processor Family Developer's Manual*.

Unfortunately, Appendix H is only available to those with the "appropriate non-disclosure agreements in place". However, most of these functions are now publicly documented in the Pentium Pro processor documentation.

The Appendix H features are identified as "optional in future *are specifically identified as being supported or not by the CPUID instruction*.

Due to the limited utility of these advanced functions (they are complex operating system functions), there are few programs that utilize these features. In particular, these functions are either not used at all, or are conditionally used if present, by Microsoft desktop operating systems.

The IDT WinChip 3 processor does not provide the following Appendix H functions.

Virtual Memory Enhancements (4-MB Pages).

These Pentium processor enhancements provide the ability to optionally define 4-MB virtual memory pages in addition to the usual 4-KB page size. A bit in the feature identification return from the CPUID instruction indicates whether this feature is present or not. This enhancement is not provided on the IDT WinChip 3 processor since it is not used by the target operating systems: Windows 95 and Windows 98. Note that this function is also not provided on the Cyrix 6x86MX/MII processor.

Virtual-8086 Mode Enhancements (VME)

These Pentium processor enhancements provide potential performance improvements to mode-switching operations while operating in VM86 mode. A bit in the feature identification return from the CPUID instruction indicates whether this feature is present or not. This enhancement is not provided on the IDT WinChip 3 processor since it is not used by the target Microsoft operating systems. Note that this function is also not provided on the Cyrix 6x86MX processor.

3.4.2 Other Functions

The IDT WinChip 3 processor also omits the software interface to the Intel-proprietary symmetric multiprocessing support: *APIC*. This bus function is omitted since the target market for the IDT WinChip 3 processor is typical desktop systems (which do not support APIC multiprocessing).

A bit in the feature identification return from the CPUID instruction indicates whether this feature is present or not. This enhancement is not provided on the IDT WinChip 3 processor (as it is not on the mobile Pentium processor and on the AMD-K6 and Cyrix 6x86MX/MII processors).

4 HARDWARE INTERFACE

4.1 BUS INTERFACE

The IDT WinChip 3 processor bus interface is compatible with the Pentium processor and the Pentium processor with MMX technology. This behavior is specified in *Pentium Processor Family Developer's Manual*.

The majority of the pins within the bus interface are involved with the physical memory and I/O interface. These pins and this interface perform the same functions as in the Pentium processor. The remaining pins are power and ground pins, test and debug support pins and various ancillary control functions. Most of these pins are identical to the Pentium processor. Others are associated with functions that behave slightly differently from the Pentium processor on the IDT WinChip 3 processor. Still others behave differently among the various versions of the Pentium processor, and thus require clarification on the IDT WinChip 3 processor. Lastly there are several Pentium processor functions which are completely omitted on the IDT WinChip 3.

4.1.1 Differences

The areas where the IDT WinChip 3 processor differs from the Pentium processor are not anticipated to cause operational compatibility issues. These differences are:

- Bus Frequency Control
- Machine Check Exceptions on BUSCHK# and PEN#
- Drive Strengths
- Probe Mode / JTAG / TAP Port (see *Test and Debug Section*)

Bus Frequency Control

Like other Socket 7 processors, the IDT WinChip 3 processor derives its internal clock frequency by multiplying the external bus clock based on the levels of the BF pins at the deassertion of RESET. Supported clock ratios are shown in Table 4-1.

Table 4-1. Bus Frequency Ratios

BF2	BF1	BF0	IDT WINCHIP 3 CLOCK RATIO	K6 CLOCK RATIO
1	0	0	2.5x	5/2x
1	0	1	3x	3x
1	1	0	3.33x	2x
1	1	1	3.5x	7/2x
0	0	0	4.5x	9/2x
0	0	1	2.33x	5x
0	1	0	4x	4x
0	1	1	2.66x	11/2x

Note: Not all motherboards document a multiplier setting of 2.33 or 2.66. If your motherboard does not have these multipliers documented, then use 5 for the 2.33 multiplier and 5.5 for the 2.66 multiplier.

Machine Check Exceptions on BUSCHK# & PEN#

As in the Pentium processor, the BUSCHK# interrupt causes a Machine Check exception or is ignored based on CR4.MCE. The difference is that the semantics of Machine Check exception are slightly different on a IDT WinChip 3 processor from a Pentium processor (a IDT WinChip 3 processor doesn't save and report the bus address and cycle data). See section 4.4 for further description of Machine Check.

Drive Strength

Desktop Pentium processors have three driver strengths that can be selected at Reset for certain pins (for example ADS#). The driver strength is selected by the BRDYC# and BUSCHK# pins when sampled at RESET deassertion.

The IDT WinChip 3 processor has only two driver strengths:

Table 4-2. Drive Strengths

BUSCHK#	BRDYC#	IDT WINCHIP 3 DRIVER	P54C DRIVER
0	0	Medium	Strong
0	1	Medium	Medium
1	0	Typical	Typical
1	1	Typical	Typical

Only ADS#, A[20:3], HITM# and W/R# are configurable. All other drivers are typical strength. The AC characteristics of both drive strengths are described in Chapter 5, Electrical Specifications.

4.1.2 Clarifications

Power Supply Voltage

The IDT WinChip 3 processor operates with a split power plane. Depending on the version, the processor requires either 2.8 Volts or 2.2 Volts at its Vcore inputs.

5V Tolerance

Like the P55, the IDT WinChip 3 processor's CLK input is not 5 Volt tolerant. It should be driven by a 3.3 Volt device.

4.1.3 Omissions

Advanced Peripheral Interrupt Controller (APIC)

The APIC is not supported by the IDT WinChip 3. The APIC pins (PICCLK, PICD0, and PICD1) are classified as reserved, and should not be connected on the motherboard.

(The APIC is also not supported in the mobile Pentium processor, the Cyrix 6x86MX/MII and AMD-K6 processors.)

Dual Processor Interface

The IDT WinChip 3 processors do not support the dual processor interface. The associated pins (D/P#, PBGNT#, PBREQ#, PHIT#, and PHITM#) are classified as reserved, and should not be connected on the motherboard.

(The DP interface is also not supported in the mobile Pentium processor, the Cyrix 6x86MX/MII and AMD K6.)

Functional Redundancy Checking Mode

The IDT WinChip 3 processors do not support the functional redundancy checking mode. The FRCMC# pin is classified as reserved, and should not be connected on the motherboard

(The functional redundancy checking mode is also not supported in the mobile Pentium processors, the Pentium processors with MMX technology, and the Cyrix 6x86MX/MII.)

Breakpoint and Performance Monitoring Signals

The IDT WinChip 3 processors internally support instruction and data breakpoints. However, the IDT WinChip 3 does not support the Pentium processor's external indication of breakpoint matches via the BP3-BP0 pins. Similarly, the IDT WinChip 3 contains performance monitoring hooks internally, but it does not support the Pentium processor's external indication of performance monitoring events on PM1-PM0. The associated pins are unconnected on the IDT WinChip 3 package.

4.2 SIGNAL SUMMARY

Table 4-3 summarizes the bus interface signals of a Pentium and which signals are provided on a IDT WinChip 3 processor: an '•' in each processor's column indicates that the pin is supported by that processor.

Table 4-3. Signal Summary

SIGNAL	TYPE	P55 (TCP)	P55 (PPGA)	P54C (TCP)	P54C (PPGA)	WINCHIP 3 (CPGA)
A20M#	I	•	•	•	•	•
A31-A3	I/O	•	•	•	•	•
ADS#	O	•	•	•	•	•
ADSC#	O		•		•	•
AHOLD	I	•	•	•	•	•
AP	I/O	•	•	•	•	•
APCHK#	I	•	•	•	•	•
APICEN/PICD1	I/O		•		•	
BE7#-BE0#	O	•	•	•	•	•
APICID[3:0]	-	•	•		•	
BF[2:0]	I	•	•	•	•	•
BOFF#	I	•	•	•	•	•
BP[3:2] PM/BP[1:0]	O	•	•	•	•	
BRDY#	I	•	•	•	•	•
BRDYC#	I		•		•	•
BREQ	O	•	•	•	•	•
BUSCHK#	I	•	•	•	•	•
CACHE#	O	•	•	•	•	•
CLK	I	•	•	•	•	•
CPUTYP	I		•		•	
D/C#	O	•	•	•	•	•
D63-D0	I/O	•	•	•	•	•
D/P#	-		•		•	
DP7-DP0	I/O	•	•	•	•	•
DPEN# - PICD0	-		•		•	
EADS#	I	•	•	•	•	•
EWBE#	I	•	•	•	•	•
FERR#	O	•	•	•	•	•
FLUSH#	I	•	•	•	•	•
FRCMC#	-			•	•	
HIT#	I	•	•	•	•	•
HITM#	I	•	•	•	•	•
HLDA	O	•	•	•	•	•
HOLD	I	•	•	•	•	•

SIGNAL	TYPE	P55 (TCP)	P55 (PPGA)	P54C (TCP)	P54C (PPGA)	WINCHIP 3 (CPGA)
IERR#	O	•	•	•	•	•
IGNNE#	I	•	•	•	•	•
INIT	I	•	•	•	•	•
INV	I	•	•	•	•	•
KEN#	O	•	•	•	•	•
INTR	I	•	•	•	•	•
NMI	I	•	•	•	•	•
LOCK#	O	•	•	•	•	•
M/IO#	O	•	•	•	•	•
NA#	I	•	•	•	•	•
PBGNT#	-		•		•	
PBREQ#	-		•		•	
PCD	O	•	•	•	•	•
PCHK#	O	•	•	•	•	•
PEN#	I	•	•	•	•	•
PHIT#	-		•		•	
PHITM#	-		•		•	
PICCLK	-		•		•	
PRDY	O	•	•	•	•	•
PWT	O	•	•	•	•	•
R/S#	I	•	•	•	•	•
RESET	I	•	•	•	•	•
SCYC	O	•	•	•	•	•
SMI#	I	•	•	•	•	•
SMIACT#	O	•	•	•	•	•
STPCLK#	I	•	•	•	•	•
TCK	I	•	•	•	•	•
TDI	I	•	•	•	•	•
TDO	O	•	•	•	•	•
TMS	I	•	•	•	•	•
TRST#	I	•	•	•	•	•
VCC2DET#	-		•		•	•
W/R#	O	•	•	•	•	•
WB/WT#	O	•	•	•	•	•

4.3 POWER MANAGEMENT

The IDT WinChip 3 processor provides both static and dynamic power management.

4.3.1 Static Power Management

The IDT WinChip 3 processor supports the five power management modes of the Pentium processor: NORMAL state, STOP CLOCK state, STOP GRANT state, STOP CLOCK SNOOP state, and AUTOHALT state. These are described in the *Pentium Family Developer's Manual.*

4.3.2 Dynamic Power Management

The IDT WinChip 3 processor uses dynamic power management techniques to reduce power consumption in the NORMAL state. In NORMAL state, the on-chip arrays, selected datapaths, and the associated control logic are powered down when not in use.

4.4 TEST & DEBUG

4.4.1 Machine Check

IDT WinChip 3 Processors provide a Machine Check exception function (INT 18) that is slightly different than the Pentium processor or Pentium Pro processor Machine Check function (which are different from each other, of course). These differences are reasonable and expected since Intel documentation specifies that the Machine Check architecture is processor-specific.

In both the Pentium processor and IDT WinChip 3 processor, the Machine Check exception must be enabled by setting the MCE bit in CR4. If not enabled, the conditions (below) causing a Machine Check are ignored and no processor action is taken.

Both the IDT WinChip 3 processor and Pentium processor cause a Machine Check, if enabled, when:

- BUSCHK# is asserted
- PEN# is asserted and a data parity error is detected (PCHK# is asserted)

The differences between the IDT WinChip 3 processor and the Pentium processor are:

- The Pentium processor reports specifics about the bus cycle in MSRs 0 and 1. The IDT WinChip 3 processor does not provide this bus-cycle data.
- The IDT WinChip 3 processor default behavior for internally detected processor errors is (like the Pentium processor) to assert IERR# and (normally) perform to a Shutdown bus cycle. However, if the EMCIE bit in the FCR is set, then internal errors on an IDT WinChip 3 processor cause a Machine Check exception.

4.4.2 BIST

A Built-in Self-Test (BIST) can be requested as part of the IDT WinChip 3 processor reset sequence using exactly the same mechanism as used on the Pentium processor (INIT asserted as RESET deasserted).

The IDT WinChip 3 processor BIST performs the following general functions:

- A hardware-implemented exhaustive test of (1) all internal microcode ROM, and (2) the X86 instruction decode, instruction generation and entry point generation logic.
- An extensive microcode test of all internal registers and datapaths.
- An extensive microcode test of data and instruction caches, their tags, and associated TLBs.

BIST requires about two million internal clocks.

EAX Value After Reset

The result of a BIST is indicated by a code in EAX. Normally EAX is zero after reset. If a BIST is requested as part of the Reset sequence, EAX contains the BIST results. A 0 in EAX after BIST Reset means that no failures were detected. Any value other than zero indicates an error has occurred during BIST.

4.4.3 Internal Error Detection

During normal execution, the IDT WinChip 3 processor detects parity errors in both caches. In addition, certain “impossible” internal states are detected by microcode. These errors are normally reported via the same mechanism as in the Pentium processor: the IERR# bus signal is asserted and (normally) a Shutdown occurs. (The Shutdown can be suppressed on both processors via a control bit in the TR1 MSR.)

Alternatively, an optional feature (a control bit in the FCR MSR) allows internal errors to be reported as Machine Check exceptions.

4.4.4 JTAG

The IDT WinChip 3 processor has a JTAG scan interface that is used for test functions and the proprietary Debug Port. However, unlike the Pentium processor, the IDT WinChip 3 processor does not provide a fully compatible IEEE 1149.1 JTAG function.

From a practical user viewpoint, JTAG does not exist and the associated pins (TCK, and so forth) should not be used.

4.4.5 Debug Port

The Pentium processor (and other processors such as the AMD-K6) have a proprietary Debug Port which uses the JTAG scan mechanism to control internal debug features (“probe mode”). These interfaces are not documented and are available (if at all) only under a non-disclosure agreement.

Similarly, the IDT WinChip 3 processor has an undocumented and proprietary debug interface.

5 ELECTRICAL SPECIFICATIONS

5.1 AC TIMING TABLES FOR 100-MHZ BUS

Table 5-1. Clock Switching Characteristics for 100-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f	CLK Frequency	50	100	MHz		
t_1	CLK Period	10	20	ns		
t_2	CLK High Time	3.0		ns		2V
t_3	CLK Low Time	3.0		ns		0.8V
t_4	CLK Fall Time	0.15	1.5	ns		2V-0.8V
t_5	CLK Rise Time	0.15	1.5	ns		2V-0.8V
	CLK Period Stability		±250	ps		

Table 5-2. Output Delay Timings for 100-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_6	A[31:3] Valid Delay	1.1	4.0	ns		(1,2)
t_7	A[31:3] Float Delay		7.0	ns		(1,2)
t_8	ADS# Valid Delay	1.0	4.0	ns		(1,2)
t_9	ADS# Float Delay		7.0	ns		(1,2)
t_{10}	ADSC# Valid Delay	1.0	4.0	ns		(1,2)
t_{11}	ADSC# Float Delay		7.0	ns		(1,2)
t_{12}	AP Valid Delay	1.0	5.5	ns		(1,2)
t_{13}	AP Float Delay		7.0	ns		(1,2)
t_{14}	APCHK# Valid Delay	1.0	4.5	ns		(1,2)
t_{15}	BE#[7:0] Valid Delay	1.0	4.0	ns		(1,2)
t_{16}	BE#[7:0] Float Delay		7.0	ns		(1,2)
t_{17}	BREQ Valid Delay		4.0	ns		(1,2)
t_{18}	CACHE# Valid Delay	1.0	4.0	ns		(1,2)
t_{18}	CACHE# Float Delay		7.0	ns		(1,2)
t_{20}	D/C# Valid Delay	1.0	4.0	ns		(1,2)
t_{21}	D/C# Float Delay		7.0	ns		(1,2)
t_{22}	D[63:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{23}	D[63:0] Valid Delay		7.0	ns		(1,2)
t_{24}	DP[7:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{25}	DP[7:0] Float Delay		7.0	ns		(1,2)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{26}	FERR# Valid Delay	1.0	4.5	ns		(1,2)
t_{27}	HIT# Valid Time	1.0	4.0	ns		(1,2)
t_{28}	HITM# Valid Time	1.1	4.0	ns		(1,2)
t_{29}	HLDA Valid Time	1.0	4.0	ns		(1,2)
t_{30}	LOCK# Valid Time	1.1	4.0	ns		(1,2)
t_{31}	LOCK# Float Time		7.0	ns		(1,2)
t_{32}	M/IO# Valid Time	1.0	4.0	ns		(1,2)
t_{33}	M/IO# Float Time		7.0	ns		(1,2)
t_{34}	PCD Valid Time	1.0	4.0	ns		(1,2)
t_{35}	PCD Float Time		7.0	ns		(1,2)
t_{36}	PCHK# Valid Time	1.0	4.5	ns		(1,2)
t_{37}	PWT Valid Time	1.0	4.0	ns		(1,2)
t_{38}	PWT Float Time		7.0	ns		(1,2)
t_{39}	SCYC Valid Time	1.0	4.0	ns		(1,2)
t_{40}	SCYC Float Time		7.0	ns		(1,2)
t_{41}	SMIACT# Valid Time	1.0	4.0	ns		(1,2)
t_{42}	W/R# Valid Time	1.0	4.0	ns		(1,2)
t_{43}	W/R# Float Time		7.0	ns		(1,2)

Notes:

1. *C_L = 0 pF*
2. *All outputs are glitch free signals, guaranteed to rise and fall monotonically when driven into capacitive loads. Most system loads must be treated as transmission lines. Depending on the length of the transmission line, loading and impedance mismatches, the signal may not rise or fall monotonically at a given point along the transmission line.*

Table 5-3. Input Setup and Hold Timings for 100-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{44}	A[31:5] Setup Time	3.0		ns		
t_{45}	A[31:5] Hold Time	1.0		ns		
t_{46}	A20M# Setup Time	3.0		ns		(1)
t_{47}	A20M# Hold Time	1.0		ns		(1)
t_{48}	AHOLD Setup Time	3.5		ns		
t_{49}	AHOLD Hold Time	1.0		ns		
t_{50}	AP Setup Time	1.7		ns		
t_{51}	AP Hold Time	1.0		ns		
t_{52}	BOFF# Setup Time	3.5		ns		
t_{53}	BOFF# Hold Time	1.0		ns		

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{54}	BRDY# Setup Time	3.0		ns		
t_{55}	BRDY# Hold Time	1.0		ns		
t_{56}	BRDYC# Setup Time	3.0		ns		
t_{57}	BRDYC# Hold Time	1.0		ns		
t_{58}	D[63:0] Read Data Setup Time	1.7		ns		
t_{59}	D[63:0] Read Data Hold Time	1.5		ns		
t_{60}	DP[7:0] Read Data Setup Time	1.7		ns		
t_{61}	DP[7:0] Read Data Hold Time	1.5		ns		
t_{62}	EADS# Setup Time	3.0		ns		
t_{63}	EADS# Hold Time	1.0		ns		
t_{64}	EWBE# Setup Time	1.7		ns		
t_{65}	EWBE# Hold Time	1.0		ns		
t_{66}	FLUSH# Setup Time	1.7		ns		(2)
t_{67}	FLUSH# Hold Time	1.0		ns		(2)
t_{68}	HOLD Setup Time	1.7		ns		
t_{69}	HOLD Hold Time	1.5		ns		
t_{70}	IGNNE# Setup Time	1.7		ns		
t_{71}	IGNNE# Hold Time	1.0		ns		
t_{72}	INIT Setup Time	1.7		ns		
t_{73}	INIT Hold Time	1.0		ns		
t_{74}	INTR Setup Time	1.7		ns		
t_{75}	INTR Hold Time	1.0		ns		
t_{76}	INV Setup Time	1.7		ns		
t_{77}	INV Hold Time	1.0		ns		
t_{78}	KEN# Setup Time	3.0		ns		
t_{79}	KEN# Hold Time	1.0		ns		
t_{80}	NA# Setup Time	1.7		ns		
t_{81}	NA# Hold Time	1.0		ns		
t_{82}	NMI Setup Time	1.7		ns		
t_{83}	NMI Hold Time	1.0		ns		
t_{84}	SMI Setup Time	1.7		ns		
t_{85}	SMI Hold Time	1.0		ns		
t_{86}	STPCLK# Setup Time	1.7		ns		
t_{87}	STPCLK# Hold Time	1.0		ns		
t_{88}	WB/WT# Setup Time	1.7		ns		
t_{89}	WB/WT# Hold Time	1.0		ns		

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 5-4. RESET & Configuration Signals for 100-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{90}	RESET Setup Time	1.7		ns		
t_{91}	RESET Hold Time	1.0		ns		Power Up
t_{92}	RESET Pulse Width, VCC and CLK Stable	15		CLKs		
t_{93}	RESET Active After VCC and CLK Stable	1.0		ms		
t_{94}	BF0, BF1, BF2 Setup Time	1.0		ms		(3)
t_{95}	BF0, BF1, BF2 Hold Time	2		CLKs		(1)
t_{96}	BRDYC# Hold Time	1.0		ns		(4)
t_{97}	BRDYC# Setup Time	2		CLKs		(2)
t_{98}	BRDYC# Hold Time	2		CLKs		(2)
t_{99}	FLUSH# Setup Time	1.7		ns		(1)
t_{100}	FLUSH# Hold Time	1.0		ms		(1)
t_{101}	FLUSH# Setup Time	2		CLKs		(2)
t_{102}	FLUSH# Hold Time	2		CLKs		(2)

Notes:

1. *To be sampled on a specific clock edge, setup and hold times must be met relative to the clock edge on which the RESET signal is first sampled negated.*
2. *To be sampled asynchronously, signals must be stable two cycles before and remain so until two cycles after the deassertion of RESET.*
3. *The BF[2:0] pins must remain stable for at least 1 ms before the negation of RESET.*
4. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*

5.2 AC TIMING TABLES FOR 95-MHZ BUS

Table 5-5. Clock Switching Characteristics for 83-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f	CLK Frequency	47 1/2	95	MHz		
t_1	CLK Period	10 1/2	21	ns		
t_2	CLK High Time	3.0		ns		2V
t_3	CLK Low Time	3.0		ns		0.8V
t_4	CLK Fall Time	0.15	1.5	ns		2V-0.8V
t_5	CLK Rise Time	0.15	1.5	ns		2V-0.8V
	CLK Period Stability		±250	ps		

Table 5-6. Output Delay Timings for 95-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_6	A[31:3] Valid Delay	1.1	4.0	ns		(1,2)
t_7	A[31:3] Float Delay		7.0	ns		(1,2)
t_8	ADS# Valid Delay	1.0	4.0	ns		(1,2)
t_9	ADS# Float Delay		7.0	ns		(1,2)
t_{10}	ADSC# Valid Delay	1.0	4.0	ns		(1,2)
t_{11}	ADSC# Float Delay		7.0	ns		(1,2)
t_{12}	AP Valid Delay	1.0	5.5	ns		(1,2)
t_{13}	AP Float Delay		7.0	ns		(1,2)
t_{14}	APCHK# Valid Delay	1.0	4.5	ns		(1,2)
t_{15}	BE#[7:0] Valid Delay	1.0	4.0	ns		(1,2)
t_{16}	BE#[7:0] Float Delay		7.0	ns		(1,2)
t_{17}	BREQ Valid Delay		4.0	ns		(1,2)
t_{18}	CACHE# Valid Delay	1.0	4.0	ns		(1,2)
t_{18}	CACHE# Float Delay		7.0	ns		(1,2)
t_{20}	D/C# Valid Delay	1.0	4.0	ns		(1,2)
t_{21}	D/C# Float Delay		7.0	ns		(1,2)
t_{22}	D[63:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{23}	D[63:0] Valid Delay		7.0	ns		(1,2)
t_{24}	DP[7:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{25}	DP[7:0] Float Delay		7.0	ns		(1,2)
t_{26}	FERR# Valid Delay	1.0	4.5	ns		(1,2)
t_{27}	HIT# Valid Time	1.0	4.0	ns		(1,2)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{28}	HITM# Valid Time	1.1	4.0	ns		(1,2)
t_{29}	HLDA Valid Time	1.0	4.0	ns		(1,2)
t_{30}	LOCK# Valid Time	1.1	4.0	ns		(1,2)
t_{31}	LOCK# Float Time		7.0	ns		(1,2)
t_{32}	M/IO# Valid Time	1.0	4.0	ns		(1,2)
t_{33}	M/IO# Float Time		7.0	ns		(1,2)
t_{34}	PCD Valid Time	1.0	4.0	ns		(1,2)
t_{35}	PCD Float Time		7.0	ns		(1,2)
t_{36}	PCHK# Valid Time	1.0	4.5	ns		(1,2)
t_{37}	PWT Valid Time	1.0	4.0	ns		(1,2)
t_{38}	PWT Float Time		7.0	ns		(1,2)
t_{39}	SCYC Valid Time	1.0	4.0	ns		(1,2)
t_{40}	SCYC Float Time		7.0	ns		(1,2)
t_{41}	SMIACT# Valid Time	1.0	4.0	ns		(1,2)
t_{42}	W/R# Valid Time	1.0	4.0	ns		(1,2)
t_{43}	W/R# Float Time		7.0	ns		(1,2)

Notes:

1. *C_L = 0 pF*
2. *All outputs are glitch free signals, guaranteed to rise and fall monotonically when driven into capacitive loads. Most system loads must be treated as transmission lines. Depending on the length of the transmission line, loading and impedance mismatches, the signal may not rise or fall monotonically at a given point along the transmission line.*

Table 5-7. Input Setup and Hold Timings for 95-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{44}	A[31:5] Setup Time	3.0		ns		
t_{45}	A[31:5] Hold Time	1.0		ns		
t_{46}	A20M# Setup Time	3.0		ns		(1)
t_{47}	A20M# Hold Time	1.0		ns		(1)
t_{48}	AHOLD Setup Time	3.5		ns		
t_{49}	AHOLD Hold Time	1.0		ns		
t_{50}	AP Setup Time	1.7		ns		
t_{51}	AP Hold Time	1.0		ns		
t_{52}	BOFF# Setup Time	3.5		ns		
t_{53}	BOFF# Hold Time	1.0		ns		
t_{54}	BRDY# Setup Time	3.0		ns		
t_{55}	BRDY# Hold Time	1.0		ns		

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{56}	BRDYC# Setup Time	3.0		ns		
t_{57}	BRDYC# Hold Time	1.0		ns		
t_{58}	D[63:0] Read Data Setup Time	1.7		ns		
t_{59}	D[63:0] Read Data Hold Time	1.5		ns		
t_{60}	DP[7:0] Read Data Setup Time	1.7		ns		
t_{61}	DP[7:0] Read Data Hold Time	1.5		ns		
t_{62}	EADS# Setup Time	3.0		ns		
t_{63}	EADS# Hold Time	1.0		ns		
t_{64}	EWBE# Setup Time	1.7		ns		
t_{65}	EWBE# Hold Time	1.0		ns		
t_{66}	FLUSH# Setup Time	1.7		ns		(2)
t_{67}	FLUSH# Hold Time	1.0		ns		(2)
t_{68}	HOLD Setup Time	1.7		ns		
t_{69}	HOLD Hold Time	1.5		ns		
t_{70}	IGNNE# Setup Time	1.7		ns		
t_{71}	IGNNE# Hold Time	1.0		ns		
t_{72}	INIT Setup Time	1.7		ns		
t_{73}	INIT Hold Time	1.0		ns		
t_{74}	INTR Setup Time	1.7		ns		
t_{75}	INTR Hold Time	1.0		ns		
t_{76}	INV Setup Time	1.7		ns		
t_{77}	INV Hold Time	1.0		ns		
t_{78}	KEN# Setup Time	3.0		ns		
t_{79}	KEN# Hold Time	1.0		ns		
t_{80}	NA# Setup Time	1.7		ns		
t_{81}	NA# Hold Time	1.0		ns		
t_{82}	NMI Setup Time	1.7		ns		
t_{83}	NMI Hold Time	1.0		ns		
t_{84}	SMI Setup Time	1.7		ns		
t_{85}	SMI Hold Time	1.0		ns		
t_{86}	STPCLK# Setup Time	1.7		ns		
t_{87}	STPCLK# Hold Time	1.0		ns		
t_{88}	WB/WT# Setup Time	1.7		ns		
t_{89}	WB/WT# Hold Time	1.0		ns		

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 5-8. RESET and Configuration Signals for 95-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{90}	RESET Setup Time	1.7		ns		
t_{91}	RESET Hold Time	1.0		ns		Power Up
t_{92}	RESET Pulse Width, VCC and CLK Stable	15		CLKs		
t_{93}	RESET Active After VCC and CLK Stable	1.0		ms		
t_{94}	BF0, BF1, BF2 Setup Time	1.0		ms		(3)
t_{95}	BF0, BF1, BF2 Hold Time	2		CLKs		(1)
t_{96}	BRDYC# Hold Time	1.0		ns		(4)
t_{97}	BRDYC# Setup Time	2		CLKs		(2)
t_{98}	BRDYC# Hold Time	2		CLKs		(2)
t_{99}	FLUSH# Setup Time	1.7		ns		(1)
t_{100}	FLUSH# Hold Time	1.0		ms		(1)
t_{101}	FLUSH# Setup Time	2		CLKs		(2)
t_{102}	FLUSH# Hold Time	2		CLKs		(2)

Notes:

1. *To be sampled on a specific clock edge, setup and hold times must be met relative to the clock edge on which the RESET signal is first sampled negated.*
2. *To be sampled asynchronously, signals must be stable two cycles before and remain so until two cycles after the deassertion of RESET.*
3. *The BF[2:0] pins must remain stable for at least 1 ms before the negation of RESET.*
4. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*

5.3 AC TIMING TABLES FOR 83-MHZ BUS

Table 5-9. Clock Switching Characteristics for 83-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f	CLK Frequency	41 2/3	83 1/3	MHz		
t_1	CLK Period	12	24	ns		
t_2	CLK High Time	3.0		ns		2V
t_3	CLK Low Time	3.0		ns		0.8V
t_4	CLK Fall Time	0.15	1.5	ns		2V-0.8V
t_5	CLK Rise Time	0.15	1.5	ns		2V-0.8V
	CLK Period Stability		±250	ps		

Table 5-10. Output Delay Timings for 83-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_6	A[31:3] Valid Delay	1.1	4.0	ns		(1,2)
t_7	A[31:3] Float Delay		7.0	ns		(1,2)
t_8	ADS# Valid Delay	1.0	4.0	ns		(1,2)
t_9	ADS# Float Delay		7.0	ns		(1,2)
t_{10}	ADSC# Valid Delay	1.0	4.0	ns		(1,2)
t_{11}	ADSC# Float Delay		7.0	ns		(1,2)
t_{12}	AP Valid Delay	1.0	5.5	ns		(1,2)
t_{13}	AP Float Delay		7.0	ns		(1,2)
t_{14}	APCHK# Valid Delay	1.0	4.5	ns		(1,2)
t_{15}	BE#[7:0] Valid Delay	1.0	4.0	ns		(1,2)
t_{16}	BE#[7:0] Float Delay		7.0	ns		(1,2)
t_{17}	BREQ Valid Delay		4.0	ns		(1,2)
t_{18}	CACHE# Valid Delay	1.0	4.0	ns		(1,2)
t_{18}	CACHE# Float Delay		7.0	ns		(1,2)
t_{20}	D/C# Valid Delay	1.0	4.0	ns		(1,2)
t_{21}	D/C# Float Delay		7.0	ns		(1,2)
t_{22}	D[63:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{23}	D[63:0] Valid Delay		7.0	ns		(1,2)
t_{24}	DP[7:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{25}	DP[7:0] Float Delay		7.0	ns		(1,2)
t_{26}	FERR# Valid Delay	1.0	4.5	ns		(1,2)
t_{27}	HIT# Valid Time	1.0	4.0	ns		(1,2)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{28}	HITM# Valid Time	1.1	4.0	ns		(1,2)
t_{29}	HLDA Valid Time	1.0	4.0	ns		(1,2)
t_{30}	LOCK# Valid Time	1.1	4.0	ns		(1,2)
t_{31}	LOCK# Float Time		7.0	ns		(1,2)
t_{32}	M/IO# Valid Time	1.0	4.0	ns		(1,2)
t_{33}	M/IO# Float Time		7.0	ns		(1,2)
t_{34}	PCD Valid Time	1.0	4.0	ns		(1,2)
t_{35}	PCD Float Time		7.0	ns		(1,2)
t_{36}	PCHK# Valid Time	1.0	4.5	ns		(1,2)
t_{37}	PWT Valid Time	1.0	4.0	ns		(1,2)
t_{38}	PWT Float Time		7.0	ns		(1,2)
t_{39}	SCYC Valid Time	1.0	4.0	ns		(1,2)
t_{40}	SCYC Float Time		7.0	ns		(1,2)
t_{41}	SMIACT# Valid Time	1.0	4.0	ns		(1,2)
t_{42}	W/R# Valid Time	1.0	4.0	ns		(1,2)
t_{43}	W/R# Float Time		7.0	ns		(1,2)

Notes:

3. C_L = 0 pF

4. All outputs are glitch free signals, guaranteed to rise and fall monotonically when driven into capacitive loads. Most system loads must be treated as transmission lines. Depending on the length of the transmission line, loading and impedance mismatches, the signal may not rise or fall monotonically at a given point along the transmission line.

Table 5-11. Input Setup and Hold Timings for 83-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{44}	A[31:5] Setup Time	3.0		ns		
t_{45}	A[31:5] Hold Time	1.0		ns		
t_{46}	A20M# Setup Time	3.0		ns		(1)
t_{47}	A20M# Hold Time	1.0		ns		(1)
t_{48}	AHOLD Setup Time	3.5		ns		
t_{49}	AHOLD Hold Time	1.0		ns		
t_{50}	AP Setup Time	1.7		ns		
t_{51}	AP Hold Time	1.0		ns		
t_{52}	BOFF# Setup Time	3.5		ns		
t_{53}	BOFF# Hold Time	1.0		ns		
t_{54}	BRDY# Setup Time	3.0		ns		
t_{55}	BRDY# Hold Time	1.0		ns		

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{56}	BRDYC# Setup Time	3.0		ns		
t_{57}	BRDYC# Hold Time	1.0		ns		
t_{58}	D[63:0] Read Data Setup Time	1.7		ns		
t_{59}	D[63:0] Read Data Hold Time	1.5		ns		
t_{60}	DP[7:0] Read Data Setup Time	1.7		ns		
t_{61}	DP[7:0] Read Data Hold Time	1.5		ns		
t_{62}	EADS# Setup Time	3.0		ns		
t_{63}	EADS# Hold Time	1.0		ns		
t_{64}	EWBE# Setup Time	1.7		ns		
t_{65}	EWBE# Hold Time	1.0		ns		
t_{66}	FLUSH# Setup Time	1.7		ns		(2)
t_{67}	FLUSH# Hold Time	1.0		ns		(2)
t_{68}	HOLD Setup Time	1.7		ns		
t_{69}	HOLD Hold Time	1.5		ns		
t_{70}	IGNNE# Setup Time	1.7		ns		
t_{71}	IGNNE# Hold Time	1.0		ns		
t_{72}	INIT Setup Time	1.7		ns		
t_{73}	INIT Hold Time	1.0		ns		
t_{74}	INTR Setup Time	1.7		ns		
t_{75}	INTR Hold Time	1.0		ns		
t_{76}	INV Setup Time	1.7		ns		
t_{77}	INV Hold Time	1.0		ns		
t_{78}	KEN# Setup Time	3.0		ns		
t_{79}	KEN# Hold Time	1.0		ns		
t_{80}	NA# Setup Time	1.7		ns		
t_{81}	NA# Hold Time	1.0		ns		
t_{82}	NMI Setup Time	1.7		ns		
t_{83}	NMI Hold Time	1.0		ns		
t_{84}	SMI Setup Time	1.7		ns		
t_{85}	SMI Hold Time	1.0		ns		
t_{86}	STPCLK# Setup Time	1.7		ns		
t_{87}	STPCLK# Hold Time	1.0		ns		
t_{88}	WB/WT# Setup Time	1.7		ns		
t_{89}	WB/WT# Hold Time	1.0		ns		

Notes:

3. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*

4. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 5-12. RESET and Configuration Signals for 83-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{90}	RESET Setup Time	1.7		ns		
t_{91}	RESET Hold Time	1.0		ns		Power Up
t_{92}	RESET Pulse Width, VCC and CLK Stable	15		CLKs		
t_{93}	RESET Active After VCC and CLK Stable	1.0		ms		
t_{94}	BF0, BF1, BF2 Setup Time	1.0		ms		(3)
t_{95}	BF0, BF1, BF2 Hold Time	2		CLKs		(1)
t_{96}	BRDYC# Hold Time	1.0		ns		(4)
t_{97}	BRDYC# Setup Time	2		CLKs		(2)
t_{98}	BRDYC# Hold Time	2		CLKs		(2)
t_{99}	FLUSH# Setup Time	1.7		ns		(1)
t_{100}	FLUSH# Hold Time	1.0		ms		(1)
t_{101}	FLUSH# Setup Time	2		CLKs		(2)
t_{102}	FLUSH# Hold Time	2		CLKs		(2)

Notes:

5. *To be sampled on a specific clock edge, setup and hold times must be met relative to the clock edge on which the RESET signal is first sampled negated.*

6. *To be sampled asynchronously, signals must be stable two cycles before and remain so until two cycles after the deassertion of RESET.*

7. *The BF[2:0] pins must remain stable for at least 1 ms before the negation of RESET.*

8. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*

5.4 AC TIMING TABLES FOR 75-MHZ BUS

Table 5-13. Clock Switching Characteristics for 75-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f	CLK Frequency	37 1/2	75	MHz		
t_1	CLK Period	13 1/3	26 2/3	ns		
t_2	CLK High Time	4.0		ns		2V
t_3	CLK Low Time	4.0		ns		0.8V
t_4	CLK Fall Time	0.15	1.5	ns		2V-0.8V
t_5	CLK Rise Time	0.15	1.5	ns		2V-0.8V
	CLK Period Stability		±250	ps		

Table 5-14. Output Delay Timings for 75-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_6	A[31:3] Valid Delay	1.1	4.5	ns		(1,2)
t_7	A[31:3] Float Delay		7.0	ns		(1,2)
t_8	ADS# Valid Delay	1.0	4.5	ns		(1,2)
t_9	ADS# Float Delay		7.0	ns		(1,2)
t_{10}	ADSC# Valid Delay	1.0	4.5	ns		(1,2)
t_{11}	ADSC# Float Delay		7.0	ns		(1,2)
t_{12}	AP Valid Delay	1.0	5.5	ns		(1,2)
t_{13}	AP Float Delay		7.0	ns		(1,2)
t_{14}	APCHK# Valid Delay	1.0	4.5	ns		(1,2)
t_{15}	BE#[7:0] Valid Delay	1.0	4.5	ns		(1,2)
t_{16}	BE#[7:0] Float Delay		7.0	ns		(1,2)
t_{17}	BREQ Valid Delay		4.5	ns		(1,2)
t_{18}	CACHE# Valid Delay	1.0	4.5	ns		(1,2)
t_{18}	CACHE# Float Delay		7.0	ns		(1,2)
t_{20}	D/C# Valid Delay	1.0	4.5	ns		(1,2)
t_{21}	D/C# Float Delay		7.0	ns		(1,2)
t_{22}	D[63:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{23}	D[63:0] Valid Delay		7.0	ns		(1,2)
t_{24}	DP[7:0] Valid Delay	1.3	4.5	ns		(1,2)
t_{25}	DP[7:0] Float Delay		7.0	ns		(1,2)
t_{26}	FERR# Valid Delay	1.0	4.5	ns		(1,2)
t_{27}	HIT# Valid Time	1.0	4.5	ns		(1,2)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{28}	HITM# Valid Time	1.1	4.5	ns		(1,2)
t_{29}	HLDA Valid Time	1.0	4.5	ns		(1,2)
t_{30}	LOCK# Valid Time	1.1	4.5	ns		(1,2)
t_{31}	LOCK# Float Time		7.0	ns		(1,2)
t_{32}	M/IO# Valid Time	1.0	4.5	ns		(1,2)
t_{33}	M/IO# Float Time		7.0	ns		(1,2)
t_{34}	PCD Valid Time	1.0	4.5	ns		(1,2)
t_{35}	PCD Float Time		7.0	ns		(1,2)
t_{36}	PCHK# Valid Time	1.0	4.5	ns		(1,2)
t_{37}	PWT Valid Time	1.0	4.5	ns		(1,2)
t_{38}	PWT Float Time		7.0	ns		(1,2)
t_{39}	SCYC Valid Time	1.0	4.5	ns		(1,2)
t_{40}	SCYC Float Time		7.0	ns		(1,2)
t_{41}	SMIACT# Valid Time	1.0	4.5	ns		(1,2)
t_{42}	W/R# Valid Time	1.0	4.5	ns		(1,2)
t_{43}	W/R# Float Time		7.0	ns		(1,2)

Notes:

1. *C_L = 0 pF*
2. *All outputs are glitch free signals, guaranteed to rise and fall monotonically when driven into capacitive loads. Most system loads must be treated as transmission lines. Depending on the length of the transmission line, loading and impedance mismatches, the signal may not rise or fall monotonically at a given point along the transmission line.*

Table 5-15. Input Setup and Hold Timings for 75-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{44}	A[31:5] Setup Time	3.0		ns		
t_{45}	A[31:5] Hold Time	1.0		ns		
t_{46}	A20M# Setup Time	3.0		ns		(1)
t_{47}	A20M# Hold Time	1.0		ns		(1)
t_{48}	AHOLD Setup Time	3.5		ns		
t_{49}	AHOLD Hold Time	1.0		ns		
t_{50}	AP Setup Time	1.7		ns		
t_{51}	AP Hold Time	1.0		ns		
t_{52}	BOFF# Setup Time	3.5		ns		
t_{53}	BOFF# Hold Time	1.0		ns		
t_{54}	BRDY# Setup Time	3.0		ns		
t_{55}	BRDY# Hold Time	1.0		ns		

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{56}	BRDYC# Setup Time	3.0		ns		
t_{57}	BRDYC# Hold Time	1.0		ns		
t_{58}	D[63:0] Read Data Setup Time	1.7		ns		
t_{59}	D[63:0] Read Data Hold Time	1.5		ns		
t_{60}	DP[7:0] Read Data Setup Time	1.7		ns		
t_{61}	DP[7:0] Read Data Hold Time	1.5		ns		
t_{62}	EADS# Setup Time	3.0		ns		
t_{63}	EADS# Hold Time	1.0		ns		
t_{64}	EWBE# Setup Time	1.7		ns		
t_{65}	EWBE# Hold Time	1.0		ns		
t_{66}	FLUSH# Setup Time	1.7		ns		(2)
t_{67}	FLUSH# Hold Time	1.0		ns		(2)
t_{68}	HOLD Setup Time	1.7		ns		
t_{69}	HOLD Hold Time	1.5		ns		
t_{70}	IGNNE# Setup Time	1.7		ns		
t_{71}	IGNNE# Hold Time	1.0		ns		
t_{72}	INIT Setup Time	1.7		ns		
t_{73}	INIT Hold Time	1.0		ns		
t_{74}	INTR Setup Time	1.7		ns		
t_{75}	INTR Hold Time	1.0		ns		
t_{76}	INV Setup Time	1.7		ns		
t_{77}	INV Hold Time	1.0		ns		
t_{78}	KEN# Setup Time	3.0		ns		
t_{79}	KEN# Hold Time	1.0		ns		
t_{80}	NA# Setup Time	1.7		ns		
t_{81}	NA# Hold Time	1.0		ns		
t_{82}	NMI Setup Time	1.7		ns		
t_{83}	NMI Hold Time	1.0		ns		
t_{84}	SMI Setup Time	1.7		ns		
t_{85}	SMI Hold Time	1.0		ns		
t_{86}	STPCLK# Setup Time	1.7		ns		
t_{87}	STPCLK# Hold Time	1.0		ns		
t_{88}	WB/WT# Setup Time	1.7		ns		
t_{89}	WB/WT# Hold Time	1.0		ns		

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 5-16. RESET and Configuration Signals for 75-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{90}	RESET Setup Time	1.7		ns		
t_{91}	RESET Hold Time	1.0		ns		Power Up
t_{92}	RESET Pulse Width, VCC and CLK Stable	15		CLKs		
t_{93}	RESET Active After VCC and CLK Stable	1.0		ms		
t_{94}	BF0, BF1, BF2 Setup Time	1.0		ms		(3)
t_{95}	BF0, BF1, BF2 Hold Time	2		CLKs		(1)
t_{96}	BRDYC# Hold Time	1.0		ns		(4)
t_{97}	BRDYC# Setup Time	2		CLKs		(2)
t_{98}	BRDYC# Hold Time	2		CLKs		(2)
t_{99}	FLUSH# Setup Time	1.7		ns		(1)
t_{100}	FLUSH# Hold Time	1.0		ms		(1)
t_{101}	FLUSH# Setup Time	2		CLKs		(2)
t_{102}	FLUSH# Hold Time	2		CLKs		(2)

Notes:

1. *To be sampled on a specific clock edge, setup and hold times must be met relative to the clock edge on which the RESET signal is first sampled negated.*
2. *To be sampled asynchronously, signals must be stable two cycles before and remain so until two cycles after the deassertion of RESET.*
3. *The BF[2:0] pins must remain stable for at least 1 ms before the negation of RESET.*
4. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*

5.5 AC TIMING TABLES FOR 66-MHZ BUS

Table 5-17. Clock Switching Characteristics for 66-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f	CLK Frequency	33 1/3	66 2/3	MHz		
t_1	CLK Period	15	30	ns		
t_2	CLK High Time	4.0		ns		2V
t_3	CLK Low Time	4.0		ns		0.8V
t_4	CLK Fall Time	0.15	1.5	ns		2V-0.8V
t_5	CLK Rise Time	0.15	1.5	ns		2V-0.8V
	CLK Period Stability		±250	ps		

Table 5-18. Output Delay Timings for 66-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_6	A[31:3] Valid Delay	1.1	6.3	ns		(1,2)
t_7	A[31:3] Float Delay		10.0	ns		(1,2)
t_8	ADS# Valid Delay	1.0	6.0	ns		(1,2)
t_9	ADS# Float Delay		10.0	ns		(1,2)
t_{10}	ADSC# Valid Delay	1.0	7.0	ns		(1,2)
t_{11}	ADSC# Float Delay		10.0	ns		(1,2)
t_{12}	AP Valid Delay	1.0	8.5	ns		(1,2)
t_{13}	AP Float Delay		10.0	ns		(1,2)
t_{14}	APCHK# Valid Delay	1.0	8.3	ns		(1,2)
t_{15}	BE#[7:0] Valid Delay	1.0	7.0	ns		(1,2)
t_{16}	BE#[7:0] Float Delay		10.0	ns		(1,2)
t_{17}	BREQ Valid Delay		8.0	ns		(1,2)
t_{18}	CACHE# Valid Delay	1.0	7.0	ns		(1,2)
t_{18}	CACHE# Float Delay		10.0	ns		(1,2)
t_{20}	D/C# Valid Delay	1.0	7.0	ns		(1,2)
t_{21}	D/C# Float Delay		10.0	ns		(1,2)
t_{22}	D[63:0] Valid Delay	1.3	7.5	ns		(1,2)
t_{23}	D[63:0] Valid Delay		10.0	ns		(1,2)
t_{24}	DP[7:0] Valid Delay	1.3	7.5	ns		(1,2)
t_{25}	DP[7:0] Float Delay		10.0	ns		(1,2)
t_{26}	FERR# Valid Delay	1.0	8.3	ns		(1,2)
t_{27}	HIT# Valid Time	1.0	6.8	ns		(1,2)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{28}	HITM# Valid Time	1.1	6.0	ns		(1,2)
t_{29}	HLDA Valid Time	1.0	6.8	ns		(1,2)
t_{30}	LOCK# Valid Time	1.0	7.0	ns		(1,2)
t_{31}	LOCK# Float Time		10.0	ns		(1,2)
t_{32}	M/IO# Valid Time	1.0	5.9	ns		(1,2)
t_{33}	M/IO# Float Time		10.0	ns		(1,2)
t_{34}	PCD Valid Time	1.0	7.0	ns		(1,2)
t_{35}	PCD Float Time		10.0	ns		(1,2)
t_{36}	PCHK# Valid Time	1.0	7.0	ns		(1,2)
t_{37}	PWT Valid Time	1.0	7.0	ns		(1,2)
t_{38}	PWT Float Time		10.0	ns		(1,2)
t_{39}	SCYC Valid Time	1.0	7.0	ns		(1,2)
t_{40}	SCYC Float Time		10.0	ns		(1,2)
t_{41}	SMIACT# Valid Time	1.0	7.3	ns		(1,2)
t_{42}	W/R# Valid Time	1.0	7.0	ns		(1,2)
t_{43}	W/R# Float Time		10.0	ns		(1,2)

Notes:

1. *C_L = 0 pF*
2. *All outputs are glitch free signals, guaranteed to rise and fall monotonically when driven into capacitive loads. Most system loads must be treated as transmission lines. Depending on the length of the transmission line, loading and impedance mismatches, the signal may not rise or fall monotonically at a given point along the transmission line.*

Table 5-19. Input Setup and Hold Timings for 66-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{44}	A[31:5] Setup Time	6.0		ns		
t_{45}	A[31:5] Hold Time	1.0		ns		
t_{46}	A20M# Setup Time	5.0		ns		(1)
t_{47}	A20M# Hold Time	1.0		ns		(1)
t_{48}	AHOLD Setup Time	5.5		ns		
t_{49}	AHOLD Hold Time	1.0		ns		
t_{50}	AP Setup Time	5.0		ns		
t_{51}	AP Hold Time	1.0		ns		
t_{52}	BOFF# Setup Time	5.5		ns		
t_{53}	BOFF# Hold Time	1.0		ns		
t_{54}	BRDY# Setup Time	5.0		ns		
t_{55}	BRDY# Hold Time	1.0		ns		

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{56}	BRDYC# Setup Time	5.0		ns		
t_{57}	BRDYC# Hold Time	1.0		ns		
t_{58}	D[63:0] Read Data Setup Time	2.8		ns		
t_{59}	D[63:0] Read Data Hold Time	1.5		ns		
t_{60}	DP[7:0] Read Data Setup Time	2.8		ns		
t_{61}	DP[7:0] Read Data Hold Time	1.5		ns		
t_{62}	EADS# Setup Time	5.0		ns		
t_{63}	EADS# Hold Time	1.0		ns		
t_{64}	EWBE# Setup Time	5.0		ns		
t_{65}	EWBE# Hold Time	1.0		ns		
t_{66}	FLUSH# Setup Time	5.0		ns		(2)
t_{67}	FLUSH# Hold Time	1.0		ns		(2)
t_{68}	HOLD Setup Time	5.0		ns		
t_{69}	HOLD Hold Time	1.5		ns		
t_{70}	IGNNE# Setup Time	5.0		ns		
t_{71}	IGNNE# Hold Time	1.0		ns		
t_{72}	INIT Setup Time	5.0		ns		
t_{73}	INIT Hold Time	1.0		ns		
t_{74}	INTR Setup Time	5.0		ns		
t_{75}	INTR Hold Time	1.0		ns		
t_{76}	INV Setup Time	5.0		ns		
t_{77}	INV Hold Time	1.0		ns		
t_{78}	KEN# Setup Time	5.0		ns		
t_{79}	KEN# Hold Time	1.0		ns		
t_{80}	NA# Setup Time	4.5		ns		
t_{81}	NA# Hold Time	1.0		ns		
t_{82}	NMI Setup Time	5.0		ns		
t_{83}	NMI Hold Time	1.0		ns		
t_{84}	SMI Setup Time	5.0		ns		
t_{85}	SMI Hold Time	1.0		ns		
t_{86}	STPCLK# Setup Time	5.0		ns		
t_{87}	STPCLK# Hold Time	1.0		ns		
t_{88}	WB/WT# Setup Time	4.5		ns		
t_{89}	WB/WT# Hold Time	1.0		ns		

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 5-20. RESET and Configuration Signals for 66-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{90}	RESET Setup Time	5.0		ns		
t_{91}	RESET Hold Time	1.0		ns		Power Up
t_{92}	RESET Pulse Width, VCC and CLK Stable	15		CLKs		
t_{93}	RESET Active After VCC and CLK Stable	1.0		ms		
t_{94}	BF0, BF1, BF2 Setup Time	1.0		ms		(3)
t_{95}	BF0, BF1, BF2 Hold Time	2		CLKs		(1)
t_{96}	BRDYC# Hold Time	1.0		ns		(4)
t_{97}	BRDYC# Setup Time	2		CLKs		(2)
t_{98}	BRDYC# Hold Time	2		CLKs		(2)
t_{99}	FLUSH# Setup Time	5.0		ns		(1)
t_{100}	FLUSH# Hold Time	1.0		ms		(1)
t_{101}	FLUSH# Setup Time	2		CLKs		(2)
t_{102}	FLUSH# Hold Time	2		CLKs		(2)

Notes:

1. *To be sampled on a specific clock edge, setup and hold times must be met relative to the clock edge on which the RESET signal is first sampled negated.*
2. *To be sampled asynchronously, signals must be stable two cycles before and remain so until two cycles after the deassertion of RESET.*
3. *The BF[2:0] pins must remain stable for at least 1 ms before the negation of RESET.*
4. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*

5.6 AC TIMING TABLES FOR 60-MHZ BUS

Table 5-21. Clock Switching Characteristics for 60-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
f	CLK Frequency	30	60	MHz		
t_1	CLK Period	16 2/3	33 1/3	ns		
t_2	CLK High Time	4.0		ns		2V
t_3	CLK Low Time	4.0		ns		0.8V
t_4	CLK Fall Time	0.15	1.5	ns		2V-0.8V
t_5	CLK Rise Time	0.15	1.5	ns		2V-0.8V
	CLK Period Stability		±250	ps		

Table 5-22. Output Delay Timings for 60-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_6	A[31:3] Valid Delay	1.1	6.3	ns		(1,2)
t_7	A[31:3] Float Delay		10.0	ns		(1,2)
t_8	ADS# Valid Delay	1.0	6.0	ns		(1,2)
t_9	ADS# Float Delay		10.0	ns		(1,2)
t_{10}	ADSC# Valid Delay	1.0	7.0	ns		(1,2)
t_{11}	ADSC# Float Delay		10.0	ns		(1,2)
t_{12}	AP Valid Delay	1.0	8.5	ns		(1,2)
t_{13}	AP Float Delay		10.0	ns		(1,2)
t_{14}	APCHK# Valid Delay	1.0	8.3	ns		(1,2)
t_{15}	BE#[7:0] Valid Delay	1.0	7.0	ns		(1,2)
t_{16}	BE#[7:0] Float Delay		10.0	ns		(1,2)
t_{17}	BREQ Valid Delay		8.0	ns		(1,2)
t_{18}	CACHE# Valid Delay	1.0	7.0	ns		(1,2)
t_{18}	CACHE# Float Delay		10.0	ns		(1,2)
t_{20}	D/C# Valid Delay	1.0	7.0	ns		(1,2)
t_{21}	D/C# Float Delay		10.0	ns		(1,2)
t_{22}	D[63:0] Valid Delay	1.3	7.5	ns		(1,2)
t_{23}	D[63:0] Valid Delay		10.0	ns		(1,2)
t_{24}	DP[7:0] Valid Delay	1.3	7.5	ns		(1,2)
t_{25}	DP[7:0] Float Delay		10.0	ns		(1,2)
t_{26}	FERR# Valid Delay	1.0	8.3	ns		(1,2)
t_{27}	HIT# Valid Time	1.0	6.8	ns		(1,2)

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{28}	HITM# Valid Time	1.1	6.0	ns		(1,2)
t_{29}	HLDA Valid Time	1.0	6.8	ns		(1,2)
t_{30}	LOCK# Valid Time	1.0	7.0	ns		(1,2)
t_{31}	LOCK# Float Time		10.0	ns		(1,2)
t_{32}	M/IO# Valid Time	1.0	5.9	ns		(1,2)
t_{33}	M/IO# Float Time		10.0	ns		(1,2)
t_{34}	PCD Valid Time	1.0	7.0	ns		(1,2)
t_{35}	PCD Float Time		10.0	ns		(1,2)
t_{36}	PCHK# Valid Time	1.0	7.0	ns		(1,2)
t_{37}	PWT Valid Time	1.0	7.0	ns		(1,2)
t_{38}	PWT Float Time		10.0	ns		(1,2)
t_{39}	SCYC Valid Time	1.0	7.0	ns		(1,2)
t_{40}	SCYC Float Time		10.0	ns		(1,2)
t_{41}	SMIACT# Valid Time	1.0	7.3	ns		(1,2)
t_{42}	W/R# Valid Time	1.0	7.0	ns		(1,2)
t_{43}	W/R# Float Time		10.0	ns		(1,2)

Notes:

1. *C_L = 0 pF*
2. *All outputs are glitch free signals, guaranteed to rise and fall monotonically when driven into capacitive loads. Most system loads must be treated as transmission lines. Depending on the length of the transmission line, loading and impedance mismatches, the signal may not rise or fall monotonically at a given point along the transmission line.*

Table 5-23. Input Setup and Hold Timings for 60-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{44}	A[31:5] Setup Time	6.0		ns		
t_{45}	A[31:5] Hold Time	1.0		ns		
t_{46}	A20M# Setup Time	5.0		ns		(1)
t_{47}	A20M# Hold Time	1.0		ns		(1)
t_{48}	AHOLD Setup Time	5.5		ns		
t_{49}	AHOLD Hold Time	1.0		ns		
t_{50}	AP Setup Time	5.0		ns		
t_{51}	AP Hold Time	1.0		ns		
t_{52}	BOFF# Setup Time	5.5		ns		
t_{53}	BOFF# Hold Time	1.0		ns		
t_{54}	BRDY# Setup Time	5.0		ns		
t_{55}	BRDY# Hold Time	1.0		ns		

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{56}	BRDYC# Setup Time	5.0		ns		
t_{57}	BRDYC# Hold Time	1.0		ns		
t_{58}	D[63:0] Read Data Setup Time	2.8		ns		
t_{59}	D[63:0] Read Data Hold Time	1.5		ns		
t_{60}	DP[7:0] Read Data Setup Time	2.8		ns		
t_{61}	DP[7:0] Read Data Hold Time	1.5		ns		
t_{62}	EADS# Setup Time	5.0		ns		
t_{63}	EADS# Hold Time	1.0		ns		
t_{64}	EWBE# Setup Time	5.0		ns		
t_{65}	EWBE# Hold Time	1.0		ns		
t_{66}	FLUSH# Setup Time	5.0		ns		(2)
t_{67}	FLUSH# Hold Time	1.0		ns		(2)
t_{68}	HOLD Setup Time	5.0		ns		
t_{69}	HOLD Hold Time	1.5		ns		
t_{70}	IGNNE# Setup Time	5.0		ns		
t_{71}	IGNNE# Hold Time	1.0		ns		
t_{72}	INIT Setup Time	5.0		ns		
t_{73}	INIT Hold Time	1.0		ns		
t_{74}	INTR Setup Time	5.0		ns		
t_{75}	INTR Hold Time	1.0		ns		
t_{76}	INV Setup Time	5.0		ns		
t_{77}	INV Hold Time	1.0		ns		
t_{78}	KEN# Setup Time	5.0		ns		
t_{79}	KEN# Hold Time	1.0		ns		
t_{80}	NA# Setup Time	4.5		ns		
t_{81}	NA# Hold Time	1.0		ns		
t_{82}	NMI Setup Time	5.0		ns		
t_{83}	NMI Hold Time	1.0		ns		
t_{84}	SMI Setup Time	5.0		ns		
t_{85}	SMI Hold Time	1.0		ns		
t_{86}	STPCLK# Setup Time	5.0		ns		
t_{87}	STPCLK# Hold Time	1.0		ns		
t_{88}	WB/WT# Setup Time	4.5		ns		
t_{89}	WB/WT# Hold Time	1.0		ns		

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 5-24. RESET and Configuration Signals for 60-MHz Bus

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
t_{90}	RESET Setup Time	5.0		ns		
t_{91}	RESET Hold Time	1.0		ns		Power Up
t_{92}	RESET Pulse Width, VCC and CLK Stable	15		CLKs		
t_{93}	RESET Active After VCC and CLK Stable	1.0		ms		
t_{94}	BF0, BF1, BF2 Setup Time	1.0		ms		(3)
t_{95}	BF0, BF1, BF2 Hold Time	2		CLKs		(1)
t_{96}	BRDYC# Hold Time	1.0		ns		(4)
t_{97}	BRDYC# Setup Time	2		CLKs		(2)
t_{98}	BRDYC# Hold Time	2		CLKs		(2)
t_{99}	FLUSH# Setup Time	5.0		ns		(1)
t_{100}	FLUSH# Hold Time	1.0		ms		(1)
t_{101}	FLUSH# Setup Time	2		CLKs		(2)
t_{102}	FLUSH# Hold Time	2		CLKs		(2)

Notes:

1. *To be sampled on a specific clock edge, setup and hold times must be met relative to the clock edge on which the RESET signal is first sampled negated.*
2. *To be sampled asynchronously, signals must be stable two cycles before and remain so until two cycles after the deassertion of RESET.*
3. *The BF[2:0] pins must remain stable for at least 1 ms before the negation of RESET.*
4. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*

5.7 DC SPECIFICATIONS

5.7.1 Recommended Operating Conditions

Functional operation of the IDT WinChip 3 processor is guaranteed if the conditions in Table 5-4 are met. Sustained operation outside of the recommended operating conditions may damage the device.

Table 5-25. Recommended Operating Conditions

PARAMETER	*MIN*	*MAX*	*UNITS*	*NOTES*
Operating Case Temperature	0	70	°C	
Mobile V_{CC2} Voltage	2.1	2.3	V	
Desktop V_{CC2} Voltage	2.7	2.9	V	
V_{CC3} Voltage	3.135	3.465	V	
V_{IH3} - High Level Input Voltage	2.0	V_{cc2} + 0.3	V	
V_{IL3} - Low level input voltage	-0.3	0.8	V	
I_{OH} – High level output current		8.0	mA	@ V = $V_{OH(min)}$
I_{OL} – Low level output current		-8.0	mA	@ V = $V_{OL(max)}$

5.7.2 Maximum Ratings

While functional operation is not guaranteed beyond the operating ranges listed in Table 5-4, the device may be subjected to the limits specified in Table 5-5 without causing long-term damage.

These conditions must not be imposed on the device for a sustained period—any such sustained imposition may damage the device. Likewise exposure to conditions in excess of the maximum ratings may damage the device.

Table 5-26. Maximum Ratings

PARAMETER	*MIN*	*MAX*	*UNITS*	*NOTES*
Operating Case Temperature	-65	110	°C	
Storage Temperature	-65	150	°C	
Supply Voltage (V_{CC})	-0.5	4.0	V	
I/O Voltage	-0.5	V_{CC3} + 0.5 or V_{CC3}(max)	V	

5.7.3 DC Characteristics

Table 5-27. DC Characteristics

PARAMETER	*MIN*	*MAX*	*UNITS*	*NOTES*
V_{OH} - High Level Output Voltage	2.4	V_{cc3}	V	@ I_{oh} = 8mA
V_{OL} - Low Level Output Voltage	0	0.4	V	@ I_{ol} = -8mA
I_L - Input Leakage Current		± 15	µA	
I_{LU} - Input Leakage Current for inputs with pull-ups		200	µA	
I_{LD} - Input Leakage Current for inputs with pull-downs		-400	µA	

5.7.4 Power Dissipation

Tables 5-24 and 5-25 give power consumption for the two voltage ranges supported for the WinChip 3.

Table 5-28. Power Consumption (0.25mm)@ 2.8V

PARAMETER	TYPICAL	MAX	UNITS	NOTES
I_{DD} - Normal Mode Operating Current				
WinChip 3-266 (3.5X 66 MHz)	6.3	8.4	Watts	
WinChip 3-300 (2.33X 100 MHz)	6.3	8.4	Watts	
WinChip 3-300 (4X 66 MHz)	7.0	9.3	Watts	
WinChip 3-333 (2.5X 100 MHz)	6.6	8.8	Watts	
WinChip 3-333 (2.66X 100 MHz)	7.0	9.3	Watts	
I_{DD} – StopGrant / AutoHalt Mode Operating Current				No snooping activity
WinChip 3-266 (3.5X 66 MHz)		3.5	Watts	
WinChip 3-300 (2.33X 100 MHz)		3.5	Watts	
WinChip 3-300 (4X 66 MHz)		3.6	Watts	
WinChip 3-333 (2.5X 100 MHz)		3.5	Watts	
WinChip 3-333 (2.66X 100 MHz)		3.6	Watts	
I_{DD} – StopClock Mode Operating Current				
WinChip 3-266 (3.5X 66 MHz)		2.8	Watts	
WinChip 3-300 (2.33X 100 MHz)		2.8	Watts	
WinChip 3-300 (4X 66 MHz)		2.8	Watts	
WinChip 3-333 (2.5X 100 MHz)		2.8	Watts	
WinChip 3-333 (2.66X 100 MHz)		2.8	Watts	

Note:

The above power consumption is preliminary and based on 70°C case and 2.8Volts.

Typical power is derived from standard operating system instruction sequences.

Thermal solutions must be designed using Maximum power conditions.

Table 5-29. Power Consumption (0.25µm) @ 2.2V

PARAMETER	TYPICAL	MAX	UNITS	NOTES
I_{DD} - Normal Mode Operating Power				
WinChip 3-233 (3X 66 MHz)	3.0	4.0	Watts	
WinChip 3-266 (3.5X 66 MHz)	3.4	4.5	Watts	
WinChip 3-300 (2.33X 100 MHz)	3.4	4.5	Watts	
WinChip 3-333 (2.5X 100 MHz)	3.6	4.8	Watts	
I_{DD} - StopGrant / AutoHalt Mode Operating Power				No snooping activity
WinChip 3-233 (3X 66 MHz)		1.3	Watts	
WinChip 3-266 (3.5X 66 MHz)		1.3	Watts	
WinChip 3-300 (2.33X 100 MHz)		1.3	Watts	
WinChip 3-333 (2.5X 100 MHz)		1.3	Watts	
I_{DD} – StopClock Mode Operating Power				
WinChip 3-233 (3X 66 MHz)		0.9	Watts	
WinChip 3-266 (3.5X 66 MHz)		0.9	Watts	
WinChip 3-300 (2.33X 100 MHz)		0.9	Watts	
WinChip 3-333 (2.5X 100 MHz)		0.9	Watts	

Note:

The above power consumption is preliminary and based on 70°C case and 2.2 Volts.

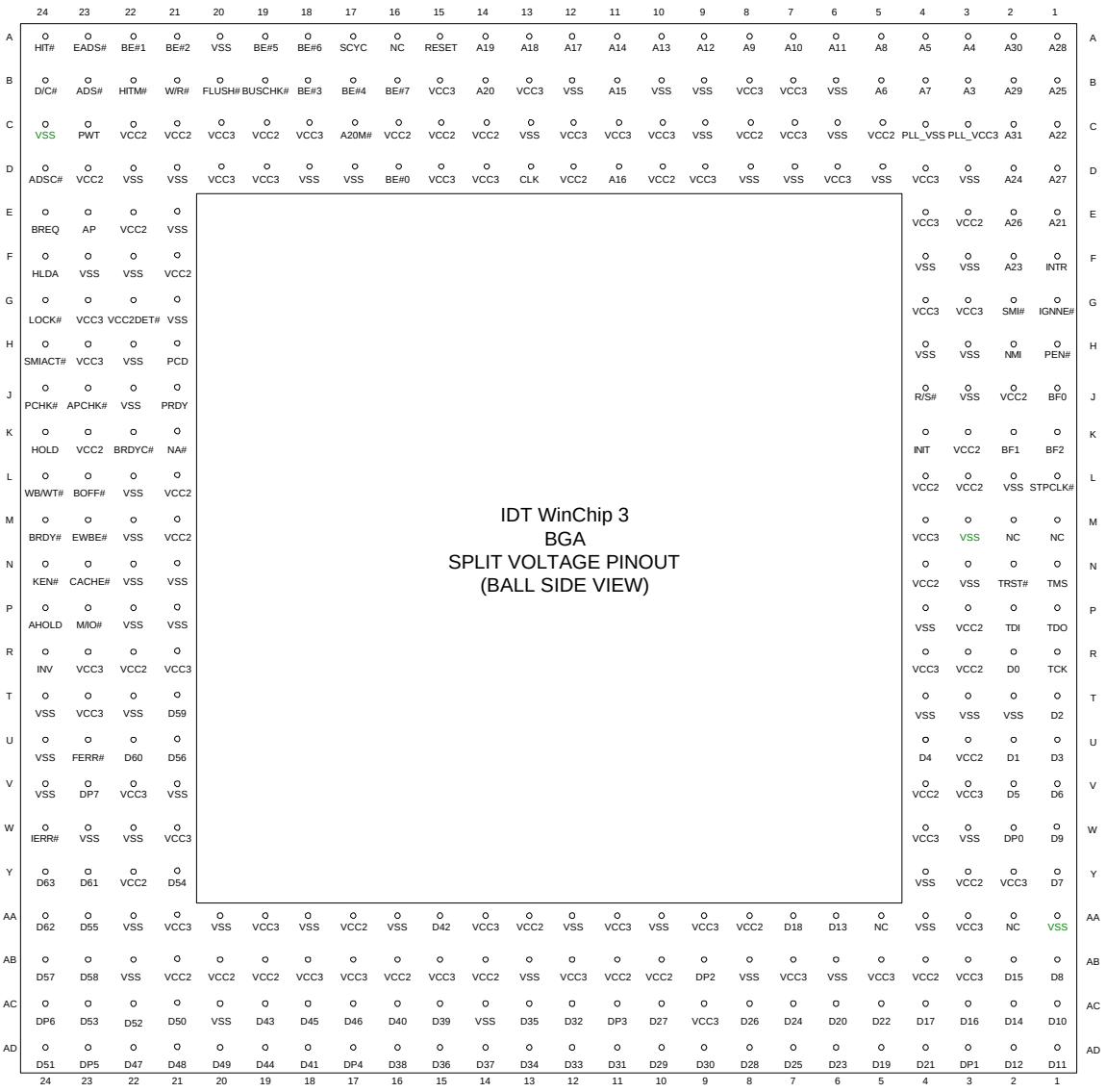
Typical power is derived from standard operating system instruction sequences.

Thermal solutions must be designed using Maximum power conditions.

6 MECHANICAL SPECIFICATIONS

The IDT WinChip 3 processor is available in 2 cost-effective packaging technologies: Ceramic Pin Grid Array (CPGA) and Ball Grid Array (BGA).

6.1 BGA PACKAGE



	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	HIT#	EADS#	BE#1	BE#2	VSS	BE#5	BE#6	SCYC	NC	RESET	A19	A18	A17	A14	A13	A12	A9	A10	A11	A8	A5	A4	A30	A28	A
B	D/C#	ADS#	HITM#	W/R#	FLUSH#	BUSCHK#	BE#3	BE#4	BE#7	VCC3	A20	VCC3	VSS	A15	VSS	VSS	VCC3	VCC3	VSS	A6	A7	A3	A29	A25	B
C	VSS	PWT	VCC2	VCC2	VCC3	VCC2	VCC3	A20M#	VCC2	VCC2	VCC2	VSS	VCC3	VCC3	VCC3	VSS	VCC2	VCC3	VSS	VCC2	PLL_VSS	PLL_VCC3	A31	A22	C
D	ADSC#	VCC2	VSS	VSS	VCC3	VCC3	VSS	VSS	BE#0	VCC3	VCC3	CLK	VCC2	A16	VCC2	VCC3	VSS	VSS	VCC3	VSS	VCC3	VSS	A24	A27	D
E	BREQ	AP	VCC2	VSS																	VCC3	VCC2	A26	A21	E
F	HLDA	VSS	VSS	VCC2																	VSS	VSS	A23	INTR	F
G	LOCK#	VCC3	VCC2DET#	VSS																	VCC3	VCC3	SMI#	IGNNE#	G
H	SMIACT#	VCC3	VSS	PCD																	VSS	VSS	NMI	PEN#	H
J	PCHK#	APCHK#	VSS	PRDY																	R/S#	VSS	VCC2	BF0	J
K	HOLD	VCC2	BRDYC#	NA#																	INIT	VCC2	BF1	BF2	K
L	WB/WT#	BOFF#	VSS	VCC2																	VCC2	VCC2	VSS	STPCLK#	L
M	BRDY#	EWBE#	VSS	VCC2																	VCC3	VSS	NC	NC	M
N	KEN#	CACHE#	VSS	VSS																	VCC2	VSS	TRST#	TMS	N
P	AHOLD	M/IO#	VSS	VSS																	VSS	VCC2	TDI	TDO	P
R	INV	VCC3	VCC2	VCC3																	VCC3	VCC2	D0	TCK	R
T	VSS	VCC3	VSS	D59																	VSS	VSS	VSS	D2	T
U	VSS	FERR#	D60	D56																	D4	VCC2	D1	D3	U
V	VSS	DP7	VCC3	VSS																	VCC2	VCC3	D5	D6	V
W	IERR#	VSS	VSS	VCC3																	VCC3	VSS	DP0	D9	W
Y	D63	D61	VCC2	D54																	VSS	VCC2	VCC3	D7	Y
AA	D62	D55	VSS	VCC3	VSS	VCC3	VSS	VCC2	VSS	D42	VCC3	VCC2	VSS	VCC3	VSS	VCC3	VCC2	D18	D13	NC	VSS	VCC3	NC	VSS	AA
AB	D57	D58	VSS	VCC2	VCC2	VCC2	VCC3	VCC3	VCC2	VCC3	VCC2	VSS	VCC3	VCC2	VCC2	DP2	VSS	VCC3	VSS	VCC3	VCC2	VCC3	D15	D8	AB
AC	DP6	D53	D52	D50	VSS	D43	D45	D46	D40	D39	VSS	D35	D32	DP3	D27	VCC3	D26	D24	D20	D22	D17	D16	D14	D10	AC
AD	D51	DP5	D47	D48	D49	D44	D41	DP4	D38	D36	D37	D34	D33	D31	D29	D30	D28	D25	D23	D19	D21	DP1	D12	D11	AD
	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 6-1. BGA Pin Cross Reference

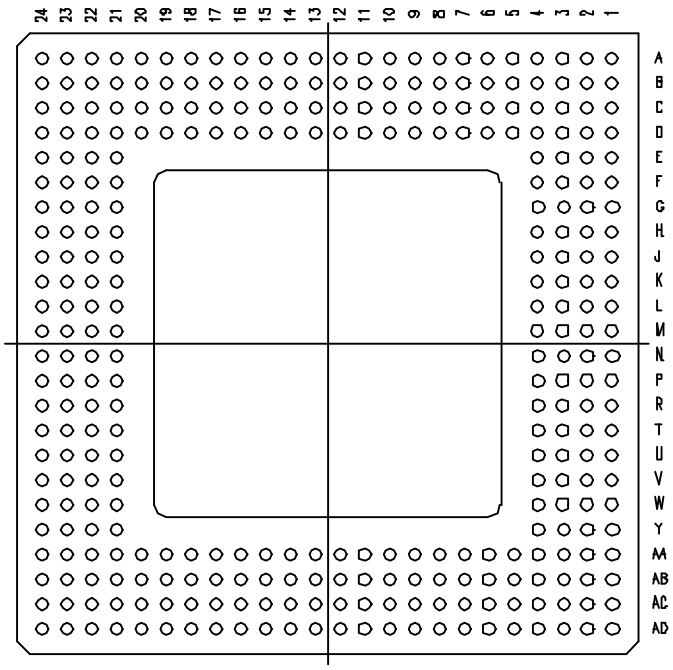
Address		Data		Control		Test		NC	V_{cc3}	V_{cc2}	V_{ss}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.	Pin No.
A3	B-3	D0	R-2	A20M#	C-17	TCK	R-1	M-1	M-4	L-4	C-13
A4	A-3	D1	U-2	ADS#	B-23	TDI	P-2	M-2	R-4	L-3	L-2
A5	A-4	D2	T-1	ADSC#	D-24	TDO	P-1	AA-2	V-3	P-3	M-3
A6	B-5	D3	U-1	AHOLD	P-24	TMS	N-1	A-16	W-4	N-4	N-3
A7	B-4	D4	U-4	AP	E-23	TRST#	N-2	AA-5	B-13	R-3	P-4
A8	A-5	D5	V-2	APCHK#	J-23				C-12	U-3	T-3
A9	A-8	D6	V-1	BE0#	D-16				C-11	V-4	T-2
A10	A-7	D7	Y-1	BE1#	A-22				C-10	D-12	T-4
A11	A-6	D8	AB-1	BE2#	A-21				D-9	D-10	W-3
A12	A-9	D9	W-1	BE3#	B-18				B-8	C-8	B-12
A13	A-10	D10	AC-1	BE4#	B-17				B-7	AB-10	B-10
A14	A-11	D11	AD-1	BE5#	A-19				C-7	AB-11	B-9
A15	B-11	D12	AD-2	BE6#	A-18				AA-21	Y-22	AA-22
A16	D-11	D13	AA-6	BE7#	B-16				W-21	C-5	V-21
A17	A-12	D14	AC-2	BF0	J-1				D-4	E-3	W-22
A18	A-13	D15	AB-2	BF1	K-2				E-4	J-2	C-6
A19	A-14	D16	AC-3	BF2	K-1				G-4	K-3	D-5
A20	B-14	D17	AC-4	BOFF#	L-23				G-3	C-21	D-3
A21	E-1	D18	AA-7	BRDY#	M-24				D-19	C-19	F-4
A22	C-1	D19	AD-5	BRDYC#	K-22				C-20	C-16	F-3
A23	F-2	D20	AC-6	BREQ	E-24				C-18	C-15	H-4
A24	D-2	D21	AD-4	BUSCHK#	B-19				D-15	C-14	H-3
A25	B-1	D22	AC-5	CACHE#	N-23				D-14	AB-14	J-3
A26	E-2	D23	AD-6	CLK	D-13				B-15	AB-16	D-18
A27	D-1	D24	AC-7	D/C#	B-24				D-6	Y-3	D-17
A28	A-1	D25	AD-7	DP0	W-2				AB-18	AB-4	A-20
A29	B-2	D26	AC-8	DP1	AD-3				AC-9	AA-8	C-9
A30	A-2	D27	AC-10	DP2	AB-9				AA-11	K-23	D-8
A31	C-2	D28	AD-8	DP3	AC-11				AB-12	F-21	D-7
		D29	AD-10	DP4	AD-17				AA-14	E-22	B-6
		D30	AD-9	DP5	AD-23				AB-15	D-23	AA-10
		D31	AD-11	DP6	AC-24				Y-2	C-22	AA-12
		D32	AC-12	DP7	V-23				AA-3	R-22	AB-13
		D33	AD-12	EADS#	A-23				AB-3	M-21	AC-14
		D34	AD-13	EWBE#	M-23				AB-5	L-21	AA-16

Address		Data		Control		Test		NC	V_{cc3}	V_{cc2}	V_{ss}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.	Pin No.
		D35	AC-13	FERR#	U-23				AB-7	AA-17	Y-4
		D36	AD-15	FLUSH#	B-20				AA-9	AB-19	AA-1
		D37	AD-14	HIT#	A-24				H-23	AB-20	AA-4
		D38	AD-16	HITM#	B-22				G-23	AB-21	AB-6
		D39	AC-15	HLDA	F-24				D-20	AA-13	AB-8
		D40	AC-16	HOLD	K-24				V-22		J-22
		D41	AD-18	IERR#	W-24				R-21		H-22
		D42	AA-15	IGNNE#	G-1				T-23		G-21
		D43	AC-19	INIT	K-4				R-23		F-23
		D44	AD-19	INTR	F-1				AB-17		F-22
		D45	AC-18	INV	R-24				AA-19		C-24
		D46	AC-17	KEN#	N-24				C-3[1]		E-21
		D47	AD-22	LOCK#	G-24						D-22
		D48	AD-21	M/IO#	P-23						W-23
		D49	AD-20	NA#	K-21						T-22
		D50	AC-21	NMI	H-2						P-21
		D51	AD-24	PCD	H-21						P-22
		D52	AC-22	PCHK#	J-24						V-24
		D53	AC-23	PEN#	H-1						N-21
		D54	Y-21	PRDY	J-21						U-24
		D55	AA-23	PWT	C-23						N-22
		D56	U-21	RESET	A-15						T-24
		D57	AB-24	R/S#	J-4						M-22
		D58	AB-23	SCYC	A-17						L-22
		D59	T-21	SMI#	G-2						AA-18
		D60	U-22	SMIACT#	H-24						AC-20
		D61	Y-23	STPCLK#	L-1						AA-20
		D62	AA-24	W/R#	B-21						AB-22
		D63	Y-24	WB/WT#	L-24						C-4[2]
				VCC2DET#	G-22						D-21

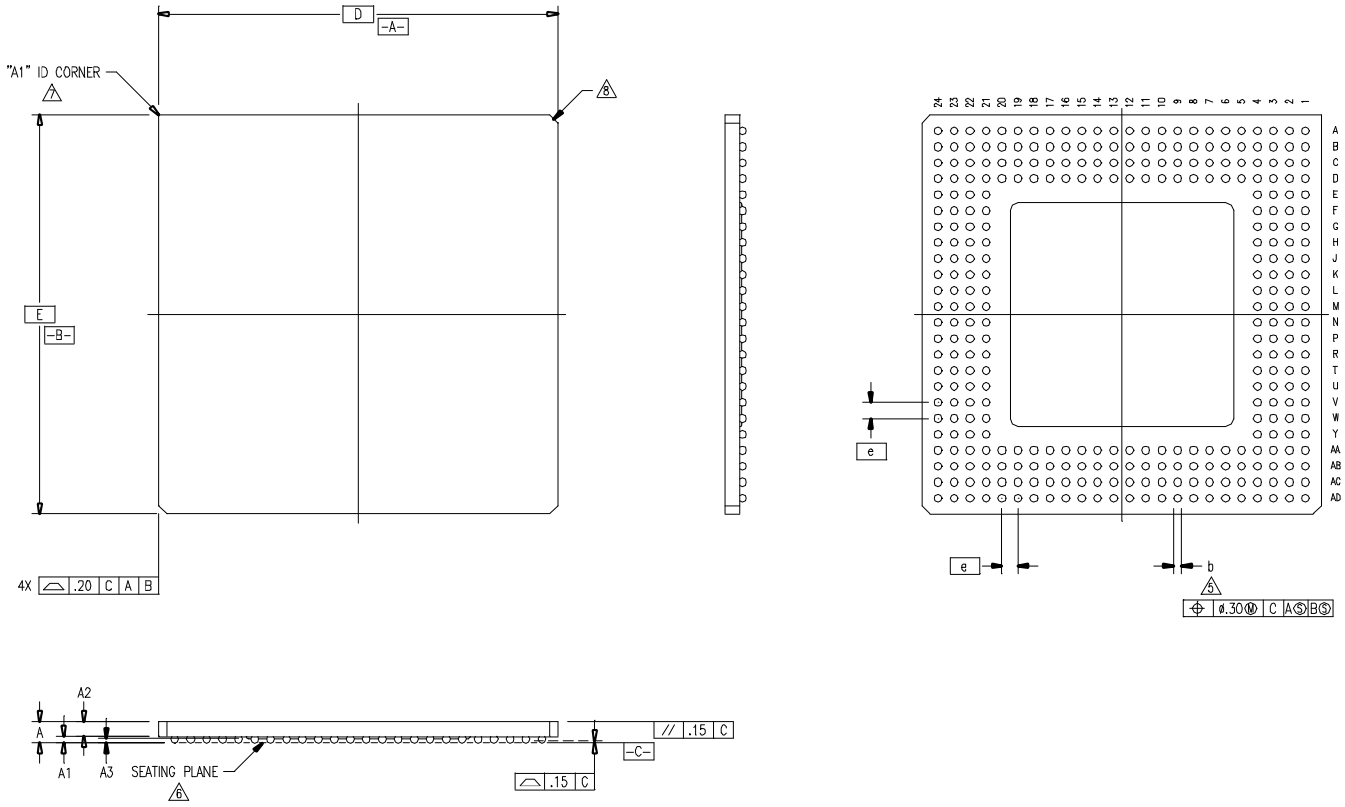
[1] *C-3 in the split-voltage BGA package is the VCC3 supply to the PLL. It should be cleanly and separately routed to the planar's VCC3 plane.*

[2] *C-4 is the VSS supply to the PLL in the BGA package. It should be cleanly and separately routed to the planar's VSS plane.*

Figure 4-4: BGA Dimensions



SYMBOL	JEDEC VARIATION BAL			NOTE
	MIN	NOM	MAX	
A	–	–	1.47	
A1	.30	.40	.50	
A2	.85	.91	.97	
D	25.00 BSC			
E	25.00 BSC			
M	24 (DEPOPULATED)			3
N	320			4
e	1.00 BSC			
b	.50	.60	.70	5
CENTER BALL MATRIX	N/A			


"A1" ID CORNER
D
-A-
E
-B-
4X .20 C A B
e
b
ø.30 M C A S B S
A2
A
A1
A3
SEATING PLANE
.15 C
-C-

6.2 CPGA PACKAGE

The IDT WinChip 3 processor's CPGA package is mechanically compatible with Intel's ceramic and plastic staggered pin grid array (SPGA and PPGA) packages. See Intel's *Pentium Processor Family Developer's Manual*, for comparison.

Figure 6-1. CPGA Pinout (Pinside View)

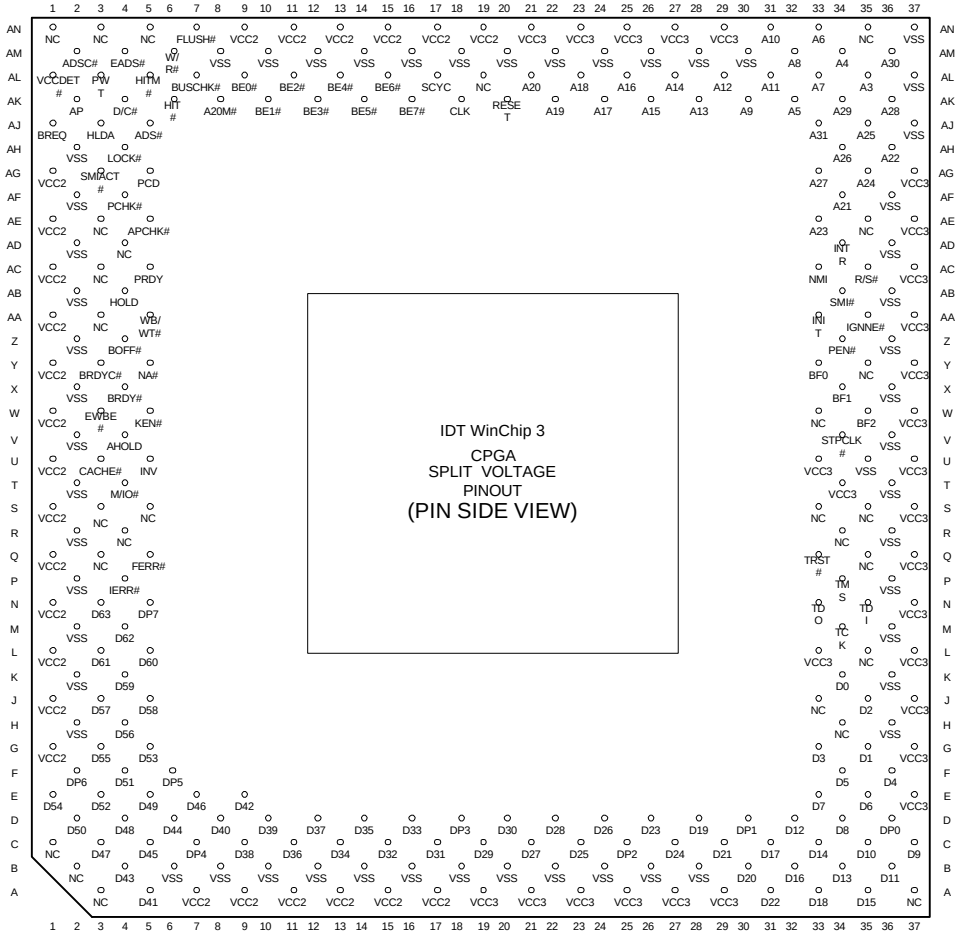


Figure 6-2. CPGA Pinout (Top Side View)

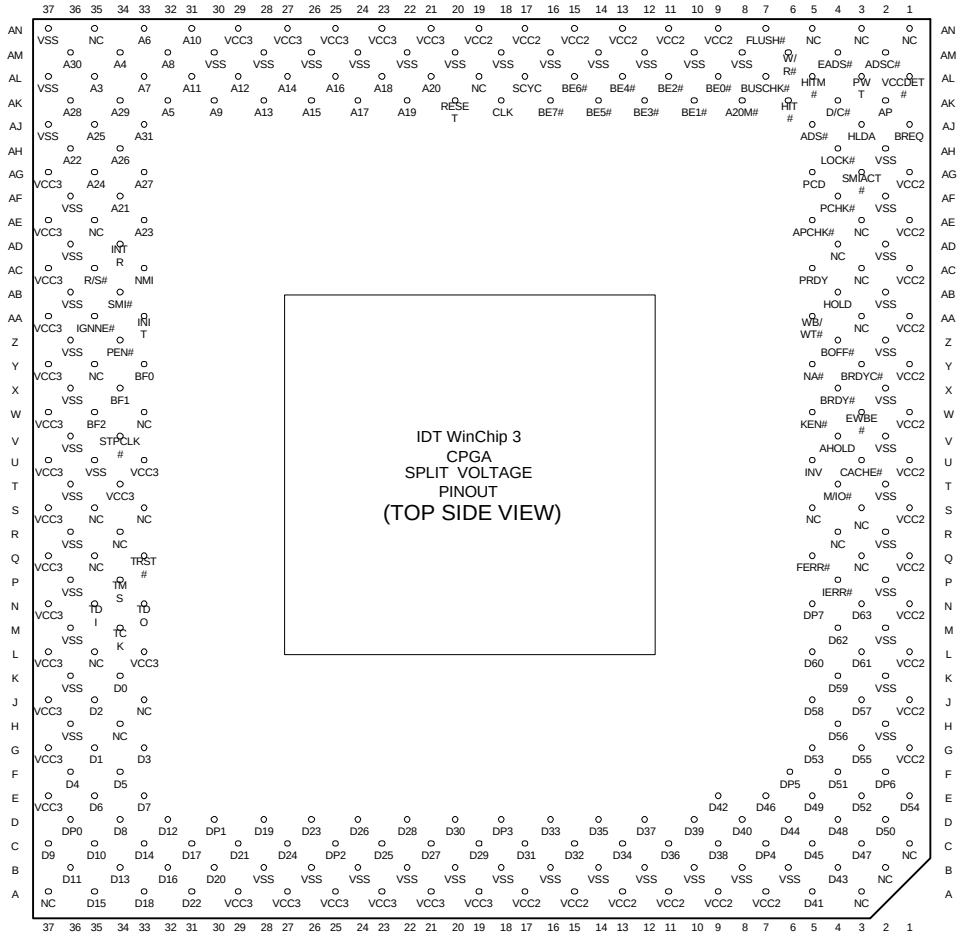


Table 6-2. CPGA Pin Cross Reference

Address		Data		Control		Test		NC	V_{cc2}	V_{cc3}	V_{ss}	Reserved
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.	Pin No.	Pin No.
A3	AL-35	D0	K-34	A20M#	AK-08	TCK	M-34	A-37	A-07	A-19	B-06	Q-03
A4	AM-34	D1	G-35	ADS#	AJ-05	TDI	N-35	R-34	A-09	A-21	B-08	R-04
A5	AK-32	D2	J-35	ADSC#	AM-02	TDO	N-33	S-33	A-11	A-23	B-10	S-03
A6	AN-33	D3	G-33	AHOLD	V-04	TMS	P-34	S-35	A-13	A-25	B-12	S-05
A7	AL-33	D4	F-36	AP	AK-02	TRST#	Q-33	W-33	A-15	A-27	B-14	AA-03
A8	AM-32	D5	F-34	APCHK#	AE-05			AL-19	A-17	A-29	B-16	AC-03
A9	AK-30	D6	E-35	BE0#	AL-09			AN-01	G-01	E-37	B-18	AD-04
A10	AN-31	D7	E-33	BE1#	AK-10			AN-35	J-01	G-37	B-20	AE-03
A11	AL-31	D8	D-34	BE2#	AL-11			A-03	L-01	J-37	B-22	AE-35
A12	AL-29	D9	C-37	BE3#	AK-12			B-02	N-01	L-33	B-24	
A13	AK-28	D10	C-35	BE4#	AL-13			C-01	Q-01	L-37	B-26	
A14	AL-27	D11	B-36	BE5#	AK-14			AN-03	S-01	N-37	B-28	
A15	AK-26	D12	D-32	BE6#	AL-15			AN-05	U-01	Q-37	H-02	
A16	AL-25	D13	B-34	BE7#	AK-16			H-34	W-01	S-37	H-36	
A17	AK-24	D14	C-33	BF0	Y-33			J-33	Y-01	T-34	K-02	
A18	AL-23	D15	A-35	BF1	X-34			L-35	AA-01	U-33	K-36	
A19	AK-22	D16	B-32	BF2	W-35			Q-35	AC-01	U-37	M-02	
A20	AL-21	D17	C-31	BOFF#	Z-04			Y-35	AE-01	W-37	M-36	
A21	AF-34	D18	A-33	BRDY#	X-04				AG-01	Y-37	P-02	
A22	AH-36	D19	D-28	BRDYC#	Y-03				AN-09	AA-37	P-36	
A23	AE-33	D20	B-30	BREQ	AJ-01				AN-11	AC-37	R-02	
A24	AG-35	D21	C-29	BUSCHK#	AL-07				AN-13	AE-37	R-36	
A25	AJ-35	D22	A-31	CACHE#	U-03				AN-15	AG-37	T-02	
A26	AH-34	D23	D-26	CLK	AK-18				AN-17	AN-21	T-36	
A27	AG-33	D24	C-27	D/C#	AK-04				AN-19	AN-23	U-35	
A28	AK-36	D25	C-23	DP0	D-36					AN-25	V-02	
A29	AK-34	D26	D-24	DP1	D-30					AN-27	V-36	
A30	AM-36	D27	C-21	DP2	C-25					AN-29	X-02	
A31	AJ-33	D28	D-22	DP3	D-18						X-36	
		D29	C-19	DP4	C-07						Z-02	
		D30	D-20	DP5	F-06						Z-36	
		D31	C-17	DP6	F-02						AB-02	
		D32	C-15	DP7	N-05						AB-36	
		D33	D-16	EADS#	AM-04						AD-02	
		D34	C-13	EWBE#	W-03						AD-36	
		D35	D-14	FERR#	Q-05						AF-02	
		D36	C-11	FLUSH#	AN-07						AF-36	
		D37	D-12	HIT#	AK-06						AH-02	

Address		**Data**		**Control**		**Test**		**NC**	**V_{cc2}**	**V_{cc3}**	**V_{ss}**	**Reserved**
Pin Name	*Pin No.*	*Pin Name*	*Pin No.*	*Pin Name*	*Pin No.*	*Pin Name*	*Pin No.*	*Pin No.*	*Pin No.*	*Pin No.*	*Pin No.*	*Pin No.*
		D38	C-09	HITM#	AL-05						AJ-37	
		D39	D-10	HLDA	AJ-03						AL-37	
		D40	D-08	HOLD	AB-04						AM-08	
		D41	A-05	IERR#	P-04						AM-10	
		D42	E-09	IGNNE#	AA-35						AM-12	
		D43	B-04	INIT	AA-33						AM-14	
		D44	D-06	INTR	AD-34						AM-16	
		D45	C-05	INV	U-05						AM-18	
		D46	E-07	KEN#	W-05						AM-20	
		D47	C-03	LOCK#	AH-04						AM-22	
		D48	D-04	M/IO#	T-04						AM-24	
		D49	E-05	NA#	Y-05						AM-26	
		D50	D-02	NMI	AC-33						AM-28	
		D51	F-04	PCD	AG-05						AM-30	
		D52	E-03	PCHK#	AF-04						AN-37	
		D53	G-05	PEN#	Z-34							
		D54	E-01	PRDY	AC-05							
		D55	G-03	PWT	AL-03							
		D56	H-04	RESET	AK-20							
		D57	J-03	R/S#	AC-35							
		D58	J-05	SCYC	AL-17							
		D59	K-04	SMI#	AB-34							
		D60	L-05	SMIACT#	AG-03							
		D61	L-03	STPCLK#	V-34							
		D62	M-04	W/R#	AM-06							
		D63	N-03	WB/WT#	AA-05							
				VCC2DET#	AL01							

Table 6-3. CPGA Dimensions

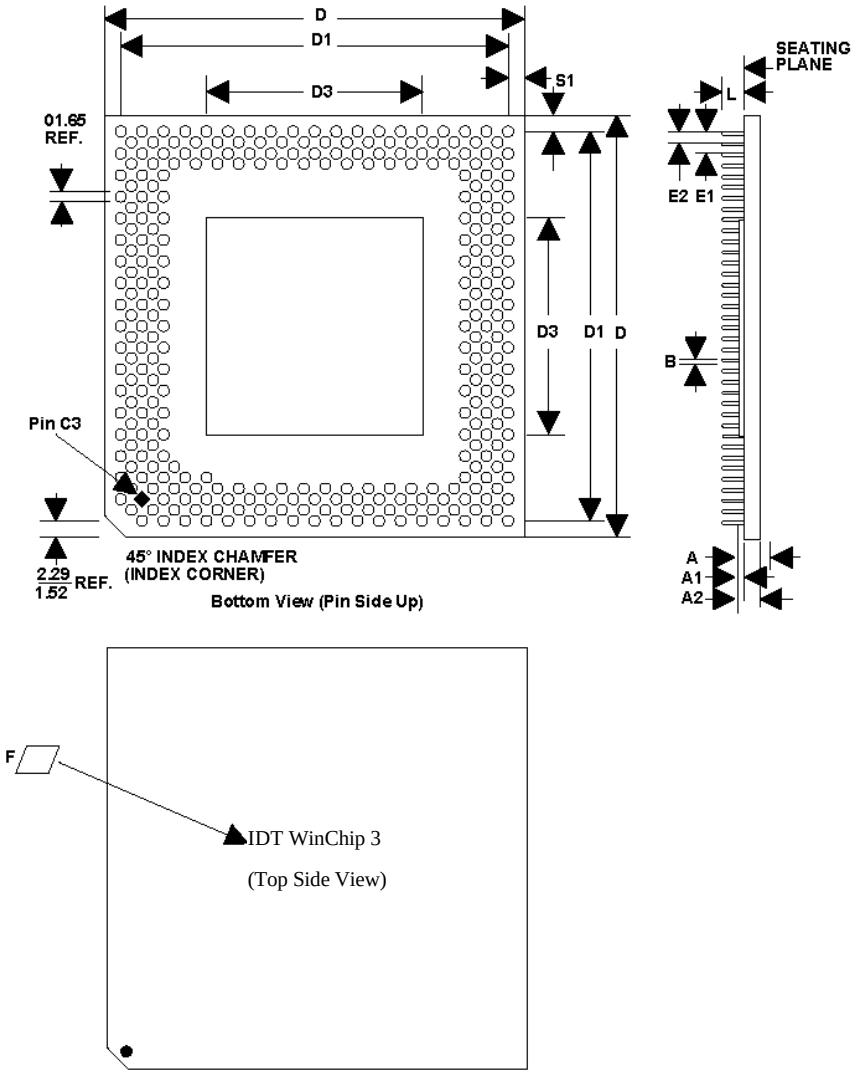


Table 6-4. CPGA Package Dimensions

	MILLIMETERS			*INCHES*		
Symbol	***Min***	***Max***	***Notes***	***Min***	***Max***	***Notes***
A1	0.69	0.84	Lid	0.027	0.033	Lid
A2	3.31	3.81	Lid	0.130	0.150	Lid
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
E1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S1	1.52	2.54		0.060	0.100	

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7 THERMAL SPECIFICATIONS

7.1 INTRODUCTION

The IDT WinChip 3 is specified for operation with device case temperatures in the range of 0°C to 70°C. Operation outside of this range will result in functional failures and potentially damage the device.

Care must be taken to ensure that the case temperature remains within the specified range at all times during operation. An effective heat sink with adequate airflow is therefore a requirement during operation.

7.2 TYPICAL ENVIRONMENTS

Typical thermal solutions involve three components: a heat sink, an interface material between the heat sink and the package, and a source of airflow. The best thermal solutions rely on the use of all three components. To the extent that any of these components are not used, the other components must be improved to compensate for such omission. In particular, the use of interface material such as thermal grease, silicone paste, or graphite paper can make a 40°C difference in the case temperature (see Table 7-4). Likewise, the imposition of airflow is realistically a requirement (see Table 7-1).

7.3 MEASURING T_C

The *Intel Pentium Processor Developer's Manual* describes proper thermal measuring techniques in detail in Chapter 10.

The case temperature (T_C) should be measured by attaching a thermocouple to the center of the IDT WinChip 3 package. The heat produced by the processor is very localized so measuring the case temperature anywhere else will underestimate the case temperature.

The presence of a thermocouple is inherently invasive; effort must be taken to minimize the effect of the measurement. The thermocouple should be attached to the processor through a small hole drilled in the heat sink. Thermal grease should be used to ensure that the thermocouple makes good contact with the package, but the thermocouple should not come in direct contact with the heat sink.

Physical Test Conditions

Case temperature measurements should be made in the worst case operating environments. Ideally, systems should be maximally configured, and tested at the worst-case ambient temperature.

Test Patterns

During normal operation the processor attempts to minimize power consumption. Consequently, normal power consumption is much lower than the maximum power consumption. Thermal testing should be done while running software which causes the processor to operate at its thermal limits. Your IDT sales representative can supply you with an executable program that will maximize power consumption.

7.4 ESTIMATING T_C

The IDT WinChip 3 processor's case temperature can be estimated based on the general characteristics of the thermal environment. This estimate is not intended as a replacement for actual measurement.

Case temperature can be estimated from Tables 7-1 and 7-2 below, where,

$T_A \equiv$ Ambient Temperature

$T_C \equiv$ Case Temperature

$\theta_{CA} \equiv$ case-to-ambient thermal resistance

$\theta_{JA} \equiv$ junction-to-ambient thermal resistance

$\theta_{JC} \equiv$ junction-to-case thermal resistance

$P \equiv$ power consumption (Watts)

and,

$$T_J = T_C + (P * \theta_{JC})$$

$$T_A = T_J - (P * \theta_{JA})$$

$$T_A = T_C - (P * \theta_{CA})$$

$$\theta_{CA} = \theta_{JA} - \theta_{JC}$$

Table 7-1. CPGA qJC and qJA

		qJA (°C/WATT) VS. LAMINAR AIRFLOW (LINEAR FT/MIN)					
Heat Sink in Inches (height)	θ_{JC} (°C/Watt)	0	100	200	400	600	800
0.25	0.8	9.1	8.0	6.6	4.5	3.6	3.0
0.35	0.8	8.8	7.5	6.0	4.0	3.3	2.8
0.45	0.8	8.4	7.0	5.3	3.6	2.9	2.5
0.55	0.8	8.1	6.5	4.7	3.2	2.6	2.3
0.65	0.8	7.7	6.0	4.3	3.0	2.4	2.1
0.80	0.8	7.0	5.3	3.9	3.8	2.2	2.0
1.00	0.8	6.3	4.7	3.6	2.6	2.1	1.8
1.20	0.8	5.9	4.3	3.3	2.4	2.0	1.8
1.40	0.8	5.4	3.9	3.0	2.2	1.9	1.7
No Heat Sink	1.2	14.3	13.0	11.6	8.7	7.3	6.4

Environment: these estimates assume the use of thermal grease between the processor and the heat sink. Heat sinks are 1.95" square.

7.5 RECOMMENDED THERMAL SOLUTIONS

For a complete listing of approved heat sinks and thermal interface materials please view our web site at www.winchip.com.

7.6 CONTACTS

For a complete listing of thermal heat sink contact please view our web site at www.winchip.com.

APPENDIX A. MACHINE SPECIFIC REGISTERS

A.1 GENERAL

Tables A-1 and A-2 summarize the *IDT WinChip 3* processor machine-specific registers (MSRs). Further description of each MSR follows the table. MSRs are read using the RDMSR instruction and written using the WRMSR instruction. Note that there are differences in the specifics of memory range management between the *IDT WinChip 3* and its predecessor, the *IDT WinChip C6*.

There are four basic groups of MSRs (not necessarily with contiguous addresses). Other than as defined below, a reference to an undefined MSR causes a General Protection exception.

1. Those that are very similar in function (but possibly different in some detail) to the Pentium processor MSRs. Generally, the same MSR address is used. These registers can have some utility to low-level programs (like BIOS).

   Note that some of the first sixteen Pentium MSRs (addresses 0 to 15) have no function in the *IDT WinChip 3* processor. These MSRs do not cause a GP when used on the *IDT WinChip 3* processor; instead, reads to these MSRs return zero, and writes are ignored.

2. Memory Configuration Registers which use MSR addresses that are not used on the Pentium processor. These MSRs define memory ranges with associated attributes. These MSRs are similar to the Pentium Pro processor MTRRs and to the Cyrix 6x86MX/MII processor's ARR registers. Note that the memory trait definition for the *IDT WinChip 3* is not compatible with its predecessor, the *IDT WinChip C6*.

3. MSRs used for cache and TLB testing. These use MSR addresses that are not used on the Pentium. These test functions are very low-level and complicated to use. They are not documented in this datasheet but the information will be provided to customers given an appropriate justification.

4. There are some undocumented internal-use MSRs used for low-level hardware testing purposes. Attempts to read or write these undocumented MSRs cause unpredictable and disastrous results; so don't use MSRs that are not documented in this datasheet!

MSRs are not reinitialized by the bus INIT interrupt; the setting of MSRs is preserved across INIT.

Table A-1. Category 1 MSRs (Functionally Similar to Pentium)

MSR	MSR NAME	ECX	EDX	EAX	TYPE	NOTES
no MSR		00h-01h	n/a	n/a	RW	1
TR1	Test Register 1	02h	n/a	Control bits	RW	3
no MSR		03h-0Dh	n/a	n/a	RW	1
TR12	Test Register 12	0Eh	n/a	Control bits	RW	3
no MSR		0Fh	n/a	n/a	RW	1
TSC	Time Stamp Counter	10h	Count[63:32]	Count[31:0]	RW	2
EC_CTRL	Event Counter Control	11h	n/a	Control bits	RW	2
EC0	Event Counter 0	12h	Count[39:32]	Count[31:0]	RW	2
EC1	Event Counter 1	13h	Count[39:32]	Count[31:0]	RW	2
FCR	Feature Control Reg	107h	n/a	FCR value	RW	4
FCR2	Feature Control Reg 2	108h	FCR2_Hi	FCR2 value	RW	5
FCR3	Feature Control Reg 3	109h	FCR3_Hi	FCR3 value	WO	5
FCR4	Feature Control Reg 4	10Ah	n/a	FCR4 value	RO	

Notes

1. Pentium processors have MSRs at these addresses. On the *IDT WinChip 3* processor, reads to these address return zero and writes are ignored.

2. Functionally similar to the same Pentium MSR. However, some minor details are different.

3. A subset of the same Pentium MSR—only those bits meaningful to the *IDT WinChip 3* processor have any effect; the rest read as 0 and are ignored when written.

4. Conceptually similar to the Pentium MSR 0Eh ("TR12") that controls detailed functions like disabling the caches. The *IDT WinChip 3* processor controls are different, thus the FCR is placed at a different address than the Pentium TR12 register.

5. FCR2 and FCR3 provide system software with the ability to specify the Vendor ID string returned by the CPUID instruction.

Table A-2. Category 2 MSRs (Memory Configuration Registers)

MSR	ECX	EDX	EAX	TYPE	NOTES
MCR 0	110h	Base Address [31:12]	Address Mask [31:12] & Ctrl Value [11:0]	WO	
MCR 1	111h	same as above	same as above	WO	
MCR 2	112h	same as above	same as above	WO	
MCR 3	113h	same as above	same as above	WO	
MCR 4	114h	same as above	same as above	WO	
MCR 5	115h	same as above	same as above	WO	
MCR 6	116h	same as above	same as above	WO	
MCR 7	117h	same as above	same as above	WO	
MCR_CTRL	120h	-	control value	WO	

A.2 CATEGORY 1 MSRS

02h: TR1 (Pentium Processor Parity Reversal Register)

31:2	1	0
Reserved (Ignored on write; returns 0 on read)	NS	*Res*
30	1	1

Both the *IDT WinChip 3* processor and the Intel Pentium processor have a MSR 02 bit 1 that performs the same function on an *IDT WinChip 3* processor as on a Pentium processor. Other bits return 0 when read and are ignored when written.

NS: 0 = Assert IERR# and cause Shutdown on internal parity error

1 = Assert IERR# and *do not* cause Shutdown on internal parity error

0Eh: TR12 (Pentium Processor Feature Control)

31:10	9	8:7	6	5:4	3	2:0
Reserved (Ignored on write; returns 0 on read)	ITR	*Res*	AHD	*Res*	CI	*Res*
22	1	2	1	2	1	3

Both the *IDT WinChip 3* processor and Pentium processor have MSR 0E bits 3, 6, and 9 that perform the same functions on an *IDT WinChip 3* processor as on a Pentium processor. Other bits return 0 when read and are ignored when written.

CI: 0 = Ignored.

1 = Same as for the Pentium processor: Cache line fills (to both caches) are suppressed; all cache misses are performed as single transfer cycles. The PCD output pin is not affected. Note that the caches are not flushed.

AHD: 0 = Ignored.

1 = Same as for the Pentium processor: disable AutoHalt Powerdown function

ITR: 0 = Ignored.

1 = Same as for the Pentium processor: enable SMM I/O Restart function

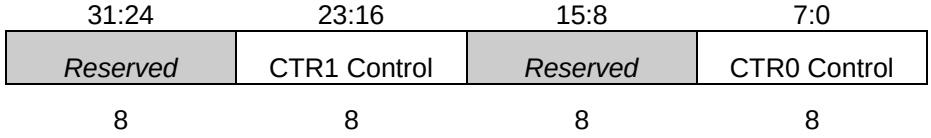
10h: TSC (Time Stamp Counter)

Both the *IDT WinChip 3* processor and the Pentium processor have a 64-bit MSR that materializes the Time Stamp Counter (TSC). Both systems increment the TSC once per processor clock.

On the *IDT WinChip 3* processor, the MSR (and the value returned by the RDTSC instruction) is an alias for the internal event-counter MSRs (CTR0/CTR1). In normal system operation, the TSC register counts internal processor clocks.

However, if the user code changes the item that CTR0 or CTR1 is counting (see the counter MSR descriptions), then the TSC register also changes what it is counting. There is no practical reason why the machine-specific event counting should be changed by software. On a Pentium processor, the TSC is a separate counter from CTR0/CTR1.

11h: CESR (Control & Event Select Register)



Both the *IDT WinChip 3* processor and Pentium have an MSR that contains bits defining the behavior of the two hardware event counters: CTR0 and CTR1.

The CTR0 and CTR1 control fields define which of several possible events can be counted for each counter. Each counter has the same set of possible events.

The events that can be counted, and their identification numbers, are different from the Pentium processor events (which are different from the Pentium Pro processor events). The Pentium processor has only six bits to identify the event counter, but has additional controls (such as event versus clock counting) in bits 9-6 of each control field.

The CESR should be written before the associated CTR0 and CTR1 are written to initialize the counters. The counts are not necessarily perfectly exact; the counters are intended for use over a large number of events and may differ by one or two counts from what might be expected.

Most counter events are internal implementation-dependent debug functions having no meaning to software. The counters that can have end-user utility are:

EVENT	DESCRIPTION
0	Data read
1	Data write
2	Data TLB miss
3	Data read cache miss
4	Data write cache miss
6	Data cache writebacks
8	Data cache snoop hits
9	Push/push pop/pop pairing
11	Misaligned data memory (not I/O)
12	Code read
13	Code TLB miss
14	Instruction fetch cache miss
19	BHT hits
20	BHT candidate
22	Instructions executed
23	Instructions in pipe 2 (V-pipe)
24	Bus utilization
29	I/O read or write cycle
40	Data read or data write
43	MMX instructions U-Pipe (EC0)
43	MMX instructions V-Pipe (EC1)
55	Returns predicted incorrectly (EC0)
55	Returns predicted correctly (EC1)
63	Internal clocks (default event for CTR0)

12h-13h: CTR0 & CTR1 (Event Counters 0 & 1)

Both the *IDT WinChip 3* processor and Pentium processor have two 40-bit hardware event counters (bits 31:8 of EDX are ignored).

107h: FCR (Feature Control Register)

The FCR controls the major optional feature capabilities of the *IDT WinChip 3* processor. It is analogous to the Pentium processor TR12 (actually MSR 0Eh) that controls things like BTB enable, cache enable, and so forth. The Cyrix 6x86MX/MII processor's CCRs (Configuration Control Registers) perform a similar function, as does the AMD-K6 processor's HDCR MSR.

Table A-2 contains the bit values for the FCR. The default settings shown for the FCR bits are not necessarily exact. The actual settings can be changed as part of the manufacturing process and thus a particular *IDT WinChip 3* processor version can have slightly different default settings than shown here. All reserved bit values of the FCR must be preserved by using a read-modify-write sequence to update the FCR.

Table A-3. FCR Bit Assignments

BIT	NAME	DESCRIPTION	DEFAULT
0		Reserved	0
1	ECX8	Enables CPUID reporting CX8	0
2	EIERRINT	Enables INT18 (Machine Check) for internal errors	0
3	DPM	Disable dynamic power management	0
4	DMCE	Disables Machine Check Exception	0
5	DSTPCLK	Disables supporting STPCLK	0
6	ELINEAR	Enables Linear Burst Mode	0
7	DSMC	Disables strict cache coherency (self-modifying-code)	0
8	DTLOCK	Disables locking of updates to accessed or dirty bits in page directory/table entries	1
9	EMMX	Enables MMX-compatible instructions	1
10		Reserved	0
11	DPDC	Disables Page Directory cache	0
12	EBRPRED	Enables Branch Prediction	1
13	DIC	Disables I-Cache.	0
14	DDC	Disables D-Cache.	0
15	DNA	Disables bus pipelining (NA response)	0
16	ERETSTK	Enables CALL-RET Stack operation	1
17		Reserved	0
18		Reserved	1
19	E2MMX	Enables pairing of MMX-compatible instructions	1
20	EAMD3D	Enables AMD-3D compatible instructions	1
21		*Reserved*	1
22:25	SID	Stepping ID	0
26		*Reserved*	0
27		*Reserved*	0
28		*Reserved*	0
29	DCPUID	Disables CPUID instruction	0
30	EMOVTR	Enables move-to-test register instructions	0
31		*Reserved*	0

ECX8: 0 **=** The CPUID instruction does not report the presence of the CMPXCHG8B instruction (CX8 = 0)**.** The instruction actually exists and operates correctly, however.

1 = The CPUID instruction reports that the CMPXCHG8B instruction is supported (CX8 = 1).

EIERRINT: 0 = Normal internal error behavior (IERR# and possible Shutdown**).**

1 = Causes INT18 instead of Shutdown for internal error.

DPM: 0 = Normal dynamic power management behavior.

1 = Disables all dynamic power management.

DMCE: 0 = Machine Check exception enabled.

1 = Disable Machine Check exception; a bus check or internal error condition does not cause an exception.

DSTPCLK: 0 = STPCLK interrupt properly supported.

1 = Ignores SPCLK interrupt.

ELINEAR: 0 = Interleaved burst ordering is enabled.

1 = Linear burst ordering is enabled.

DSMC: 0 **=** Strict cache coherency is enabled to support Pentium processor style self-modifying code.

1 = Disables strict cache coherency. I-cache/D-cache coherent only if branch is taken after store instruction which modifies instructions to be executed subsequently.

DTLOCK: 0 **=** Updates to the accessed and dirty bits in PDE/PTE entries are performed using the locked read-modify-write semantics which flushes the data from the D-Cache (like Pentium processor).

1 = Updates to the accessed and dirty bits in PDE/PTE entries are performed without locking the bus or flushing data from the D-Cache.

EMMX: 0 = Disables MMX-compatible instructions: they decode as invalid instructions.

1 = Enables MMX-compatible instructions.

DPDC: 0 = Enables use of internal Page Directory Cache.

1 = Disables use of internal Page Directory Cache.

EBRPRED: 0 **=** Disables branch prediction function.

1 = Enables branch prediction function.

DIC: 0 = Enables use of I-Cache.

1 = Disables use of I-Cache: cache misses are performed as single transfer bus cycles, PCD is de-asserted. This overrides any setting of CR0.CD and CR0.NW.

DDC: 0 = Enables use of D-Cache.

1 = Disables use of D-Cache: same semantics as for DIC except for D-Cache.

DNA: 0 = Enables bus pipelining operation.

1 = Disables bus pipelining operation: bus signal NA is ignored.

ERETSTK: 0 **=** Disables CALL-RETurn stack function.

1 = Enables CALL-RETurn stack function: RET branch target prediction is performed.

E2MMX: 0 **=** Disables pairing of MMX instructions.

1 = Enables pairing of MMX instructions.

EAMD3D: 0 **=** Disables AMD 3D-compatible instructions.

1 = Enables AMD 3D-compatible instructions.

DCPUID: 0 **=** The CPUID instruction is supported.

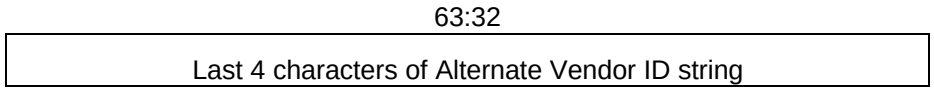
1 = The CPUID instruction is disabled and causes an invalid instruction exception.

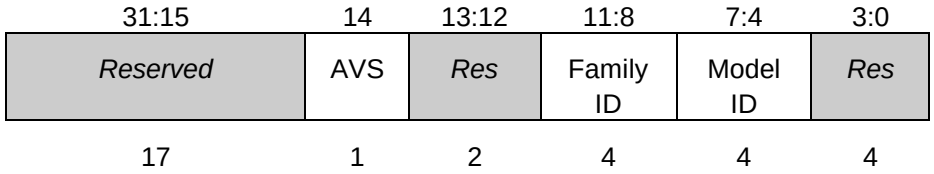
EMOVTR: 0 = The Intel486 move-to/from-test register instructions are not supported and their behavior is the same as on a Pentium processor (invalid instruction exception).

1 = The test register instructions do not cause an invalid instruction exception but rather are treated as NOPs.

108h: FCR2 (Feature Control Register 2)

This MSR contains more feature control bits — many of which are undefined. It is important that all reserved bits are preserved by using a read-modify-write sequence to update the MSR.





AVS: 0 = The CPUID instruction vendor ID is "CentaurHauls"

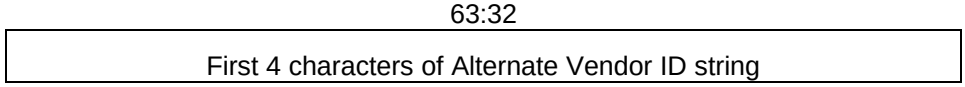
1 = The CPUID instruction returns the alternate Vendor ID. The first 8 characters of the alternate Vendor ID are stored in FCR3 and the last 4 characters in FCR2[63:32]. These 12 characters are undefined after RESET and may be loaded by system software using WRMSR.

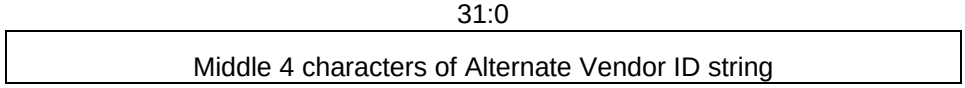
Family ID: This field will be returned as the family ID field by subsequent uses of the CPUID instruction

Model ID: This field will be returned as the model ID field by subsequent uses of the CPUID instruction

109h: FCR3 (Feature Control Register 3)

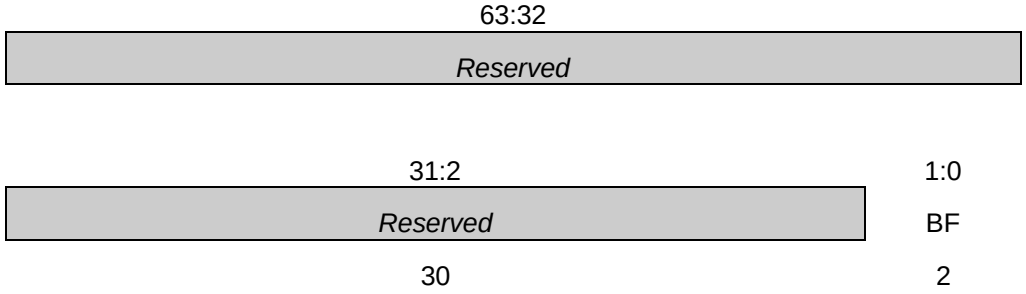
This MSR contains the first 8 characters of the alternate Vendor ID. The alternate Vendor ID is returned by the CPUID instruction when FCR2[AVS] is set to 1. FCR3 is a write-only MSR.





10Ah: FCR4 (Feature Control Register 4)

This MSR is read-only because only status bits are currently defined.



In the WinChip 3, the multiplier information can be read from machine-specific registers (MSR 0x10A and 0x147) as follows:

Ratio	MSR 0x147 [26:23]	MSR 0x10A [1:0]
2.5X	0011b	00b
3.0X	0100b	00b
3.33X	1000b	01b
3.5X	0101b	00b
4.5X	0111b	00b
2.33X	0101b	01b
4.0X	0110b	00b
2.66X	0110b	01b

Ratio = (MSR 0x147 [26:23] + 2) ÷ (MSR 0x10A[1:0] + 2)

A.3 MEMORY CONFIGURATION REGISTERS

General

The *IDT WinChip 3* processor provides extensions over the P55 to define variable size memory ranges with associated special attributes. These Memory Configuration Registers (MCRs) are similar to the MTRRs of the Pentium Pro processor and the Address Region Registers (ARRs) of the Cyrix 6x86MX/MII processor. All of these approaches perform similar functions but differ in specifics. In fact, there are differences in the MCR details between the *IDT WinChip 3* and its predecessor, the *IDT WinChip C6*.

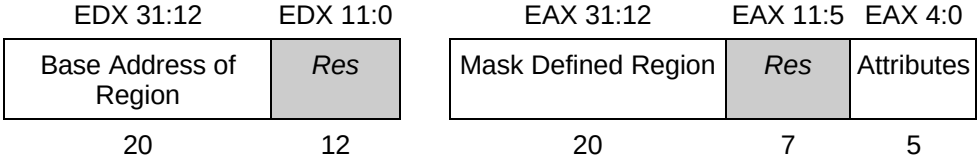
The basic function performed is to define memory regions and special attributes for these regions such as write-combining and weakly-ordered reads. These special attributes are deviations from formal x86 architectural behavior but, in practice, work fine for specific memory regions in a PC. The advantage of these special attributes is improved performance for the affected memory regions.

Memory Configuration Registers

The *IDT WinChip 3* processor has eight MCRs, each appearing as a 64-bit MSR. The default value at reset is zero for all fields. This value causes all memory to have normal x86 attributes of no byte-combining and strongly ordered writes.

Note that the MCRs are *write-only*.

The MCR format is:



Base

This is the starting physical address of the memory region. Each definable memory region starts at a 4-KB page boundary; thus the low order 12 bits of the address are ignored.

Mask

This is a bit mask defining the size of the memory region. A memory region hit exists for a MCR if:

Mask address AND memory address = Base address AND mask address in all bit positions (31:12)

Example 1.

For example, consider the memory range from `0x000A0000` to `0x000BFFFF`. This is most efficiently done by masking off the low order bits that constitute the range.

Viewing the addresses in binary:

```
0x000A0000  = 0000 0000 0000 1010 0000 0000 0000 0000

0x000BFFFF  = 0000 0000 0000 1011 1111 1111 1111 1111
```

Notice that the upper 15 bits are identical, whereas the lower 17 bits define the address within the range. So a single MRD can describe this range as:

```
MCR Base  =  0000 0000 0000 1010 0000 or 0x000A0

MCR Mask  =  1111 1111 1111 1110 0000 or 0xFFFE0
```

Note that the lower twelve bits of the mask and base are ignored in the match calculation.

Example 2.

Consider a more complex scenario where a range from 0x00080000 to 0x00017FFF is required. Shown in binary as:

```
0x00080000  =  0000 0000 0000 1000 0000 0000 0000 0000

0x0017FFFF  =  0000 0000 0001 0111 1111 1111 1111 1111
```

In this case, the upper 11 bits are identical throughout the range. The next two bits vary, but not all combinations are part of the desired range. The range has to be broken down into two ranges that have common base bits where all combinations of the lower order bits are within the original region. This implies:

```
0x00080000  =  0000 0000 0000 1000 0000 0000 0000 0000

0x000FFFFF  =  0000 0000 0000 1111 1111 1111 1111 1111
```

and

```
0x00100000  =  0000 0000 0001 0000 0000 0000 0000 0000

0x0017FFFF  =  0000 0000 0001 0111 1111 1111 1111 1111
```

These map into MCRs:

```
MCR0 Base =  0000 0000 0000 1000 0000 or 0x00080

MCR0 Mask =  1111 1111 1111 1000 0000 or 0xFFF80
```

and

```
MCR1 Base =  0000 0000 0001 0000 0000 or 0x00100

MCR1 Mask =  1111 1111 1111 1000 0000 or 0xFFF80
```

Attributes

There are five bits of attribute control defined for each memory region as described in Table A.6-1. Note that this definition is different from the predecessor *IDT WinChip C6*. In order to avoid unintended programming by system software the *IDT WinChip 3* defines the Trait Mode Control field in MCR_CTRL, which must be set to the appropriate value in order for the MCRs to be enabled.

Table A-4

BIT	DESCRIPTION	DEFAULT	NOTES
0	Write Combining: 0: no effect 1: Writes may be combined with previous writes to the same DWORD before executing on the bus	0	
1	Non-Cacheable: 0: no effect 1: Accesses within this range will not disrupt the cache. This is useful for describing a video buffer. It is a hint to the processor that the memory controller will consider this non-cacheable (KEN# not asserted) and therefore the processor can potentially avoid a castout of a modified line.	0	
2	Reserved.	0	
3	Weak Write Ordering (WWO): 0: no effect 1: writes to this region may be reordered with respect to each other, but this may cause issues with DMA-ing devices	0	
4	Weak Read Ordering (WRO): 0: no effect 1: reads which require access to the bus may be reordered in front of writes which are also destined to the bus	0	

MCR Control Register

The MCR_CTRL MSR controls various pervasive behaviors of write-combining and write-ordering. The write combining definitions for string and non-stack and non-string are defined in the following table.

Table A-5

BIT	DESCRIPTION	DEFAULT	NOTES
1:0	Write combining definition for non-stack & non-string. 00: Forward Combining 01: Forward and Overlapped Combining 10: Forward and Reverse Combining 11: Forward, Reverse, and Overlapped Combining	00	Read-Write
3:2	Write combining definition for string. 00: Forward Combining 01: Forward and Overlapped Combining 10: Forward and Reverse Combining 11: Forward, Reverse, and Overlapped Combining	00	Read-Write
4	Weak Write-Ordering Enable	0	Read-Write
5	Reserved	0	
8:6	Trait Mode Control, must match MCR_CTRL[19:17] in order to enable	000	Read-

BIT	DESCRIPTION	DEFAULT	NOTES
	Memory Configuration Registers: 001: Enables IDT WinChip 3 MCRs other: Disables MCRs Before programming the MCRs system software should identify the processor version to ensure that the MCRs are programmed appropriately. MCR_CTRL[19:17] contains a unique value that identifies the version of the MCR traits supported by the processor. System software should copy MCR_CTRL[19:17] to MCR_CTRL[8:6] if, and only if, it recognizes the version.		Write
9	MCR 0 in use 0: MCR0[4:0] attributes is all zero 1: MCR0[4:0] attributes is non-zero	0	Read-Only (RO)
10	MCR 1 in use (see MCR 0)	0	RO
11	MCR 2 in use (see MCR 0)	0	RO
12	MCR 3 in use (see MCR 0)	0	RO
13	MCR 4 in use (see MCR 0)	0	RO
14	MCR 5 in use (see MCR 0)	0	RO
15	MCR 6 in use (see MCR 0)	0	RO
16	MCR 7 in use (see MCR 0)	0	RO
19:17	Trait Mode Key, must write this value to MCR_CTRL[8:6] in order to enable Memory Configuration Registers. System software should copy MCR_CTRL[19:17] to MCR_CTRL[8:6] if, and only if, it recognizes the version.	001	Read-Only
24:20	Reserved	11111	Read-Write

Write-Combining

The *IDT WinChip 3* processor's write-combining feature allows multiple writes to be combined into a single bus write. This is permissible if the writes are destined to the same 8-byte memory address.

Write-combining can greatly reduce the memory bandwidth requirements of writes that miss the cache. However, if the associated writes are destined to memory mapped I/O locations, problems can arise.

For example, if an ISA bus 8-bit device is controlled with a data register at address 0 and a control register at address 1, and the control register must be written before the data can be written, it is possible for the order of writes to be changed if write-combining is inappropriately configured.

If, for example, the device writes to address 1 and then to address 0 and the two are combined, a 16-bit word will go to the ISA bus where it will be split for the 8-bit device into two writes. Unfortunately, most ISA bridges split 16-bit operands into two transfers with the low byte first. Consequently, the order of the two writes is reversed.

To eliminate this problem, the *IDT WinChip 3* processor is very configurable. Aside from disabling byte-combining, it is also possible to limit the type of instructions that are allowed to combine. Further, it is possible to prevent the processor from combining in reverse address order. Lastly, it is possible to prevent the processor from combine-matching (overlapping) byte addresses.

In practice it is reasonable for system BIOS to enable write-combining of all types for all of system memory.

Non-Cacheable

The IDT WinChip 3 processor improves over the IDT WinChip C6 processor with the addition of the Non-Cacheable memory trait. This trait is used by the processor to indicate that the current physical address will not end up in the processor's L1 cache. This information prevents the processor from allocating space for the access. This prevents unnecessary invalidation of the L1.

The NC trait should only be set for regions of memory that will never be treated as cacheable.

Weak Write-Ordering

The Pentium processor ensures that writes occur in the same order as they occur in the code execution. This is termed strong write-ordering. This restriction can be a performance impact in that it blocks processor execution when a store hits an E or M line in the cache if another store is waiting to be retired on the bus.

Normally systems do not require strong write-ordering unless they have bus-mastering I/O devices that use memory mapped I/O for control purposes. (Most DMA devices are slaves, and do not use memory-mapped I/O. The floppy controller, for example, is a DMA device, but does not use memory-mapped I/O.)

However, since there are devices that could not perform correctly with weak write ordering, this function should only be used in systems where the type of peripherals are tightly controlled and known to not require strongly ordered writes. Weak write ordering should never be turned on by a generic BIOS, for example.

Weak Read-Ordering

The Pentium processor also ensures that reads and writes occur in the same order on the bus as they do in the executed code. This prevents the processor from initiating a bus read before preceding writes have completed on the bus. This causes unnecessary delay in processor execution.

Normally it is possible to re-order reads in front of writes, provided the associated addresses do not overlap, and the addresses are not destined for devices which uses memory-mapped I/O.

The IDT WinChip 3 supports this behavior (under the moniker "weak read-ordering") in its MRDs. It is recommended that the BIOS enable weak read-ordering for normal system memory.

Combining Ranges

It is possible to describe fairly complex ranges with a few descriptors. Generally, this does not involve overlapping MCRs. However, overlapping ranges are permitted and their behavior is useful in some cases.

The behavior of an access to a given memory location is defined by the logical OR of the attribute bits of the MCRs it matches. So, if a memory location does not match any MCRs, its aggregate attribute is 0. If, on the other hand, it matches two MCRs, one with an attribute of 0x10 and the other with an attribute of 0x01, the aggregate attribute is 0x11. This enables weak read ordering on all accesses and allows write-combining as defined by the MCR_CTRL[3:0].

APPENDIX B. COMPATIBILITY

B.1 INTRODUCTION

In general, the *IDT WinChip 3* processor is exactly compatible with both the bus and software-visible architecture of the Intel Pentium processor.

An *IDT WinChip 3* processor can plug into existing Intel Pentium-based PC system boards and operate without requiring change to the system hardware. Also, an *IDT WinChip 3* processor can run all existing industry-standard PC object-code operating systems and application programs.

However, all processors developed for use in PCs ("x86" processors) have some minor incompatibilities in low-level implementation-dependent functions. For example, it is possible to write esoteric software for the Intel 486 processor (cache tests, for example) that produces different results when run on the supposedly compatible Intel Pentium processor.

Similarly, there are low-level incompatibilities between the Intel Pentium and the Intel Pentium Pro processors. Similarly, there are low-level incompatibilities among all x86 "clone" processors such as the AMD-K6 and the Cyrix 6x86MX/MII processors. The *IDT WinChip 3* processor has similar low-level differences with the various Intel and x86 clone processors.

Fortunately, these technical incompatibilities among x86 implementations are in areas that have no meaningful use to most programs, and that are well-understood by software developers (and are thus avoided). Therefore, in practice, these types of differences pose no real barriers to program compatibility across various implementations.

This appendix summarizes areas where the *IDT WinChip 3* processor differs in behavior from the Intel Pentium processor. These differences are generally "don't cares"; that is, they are transparent to system hardware and programs.

A separate *IDT WinChip 3 Errata* document describes the IDT WinChip 3 processor *errata*: differences between the actual IDT WinChip 3 processor behavior and the expected results.

B.2 BUS COMPATIBILITY

Bus Cycle Activity

When compared cycle by cycle, the *IDT WinChip 3* and Intel Pentium processors do not have exactly the same bus cycles. This is anticipated, unavoidable, and desirable (the *IDT WinChip 3* processor provides increased bus performance). This difference results from the *IDT WinChip 3* processor's different internal architecture and larger cache. This is not an issue because the Intel Pentium processor itself varies at different frequencies and all other competitive processors also have differing bus cycle activity.

Bus Alignment

Although the Intel Pentium processor has a 64-bit bus, it splits loads and stores that cross 32-bit boundaries. The *IDT WinChip 3* processor splits memory loads and stores at 64-bit boundaries. However, I/O reads and writes are split on 32-bit boundaries.

Like the Pentium processor, when split cycles are required, the *IDT WinChip 3* processor performs the higher address' access first, then performs the lower address' access.

The *IDT WinChip 3*'s bus alignment is not anticipated to be a compatibility issue. The Cyrix 6x86 and AMD-K5 processors also split memory loads and stores at 64-bit boundaries. (Also, the Cyrix 6x86 performs the low addressed access first except for 32-bit misaligned I/Os in which case the higher access is performed first.)

Snoop Responsibility Pickup

The Pentium processor assumes responsibility for incoming cache lines at the point where it determines the cacheability of the line. The cacheability is determined at the first assertion of NA# or BRDY# for the cycle. Subsequent to cacheability determination, the processor will respond to snoops for that line even though it is not completely read into the processor.

The *IDT WinChip 3* processor generally mimics this behavior. However, if a bus cycle is pipe lined over a previous cycle and gets a BOFF# assertion before its cacheability for the second line has been determined, the *IDT WinChip 3* processor assumes responsibility for subsequent snoops to *both* lines when cacheability is determined for the *first* retried line.

Descriptor Updates

The exact size of the locked bus transactions used to update the accessed bit in non-accessed descriptors is slightly different between the Pentium processor and the *IDT WinChip 3* processor.

TLB Retries

Intel processors are not consistent about how and when they take page protection exceptions. The Pentium Pro's operation is architecturally cleaner than the Pentium's operation, so the *IDT WinChip 3* mimics the Pentium Pro's behavior. If a memory address hits either of the TLBs and the associated TLB entry would indicate that a protection page fault should be taken, the page tables are retried to ensure that the TLB entry is up to date. Only if the retried TLB entry still indicates that a page protection exception should occur does the exception actually take place.

Table Walk D and A Bit Updates

The *IDT WinChip 3* processor does not snoop its instruction cache during table walks. Consequently, if the access (A) or dirty (D) bit need to be updated, and the table or directory entry is in the L1 instruction cache, the L1 instruction cache does not reflect the updated value.

While it is possible to create code that detects this inconsistency, it is highly unlikely that any application or operating system relies on the update.

SCYC

The SCYC signal is loosely defined on the Intel Pentium processor. On the *IDT WinChip 3* processor, SCYC is asserted only during external locked read-modify-write cycles that are unaligned.

STPCLK# in Auto Halt State

If the processor sees an assertion on STPCLK# while resting in the Auto Halt Power Down State, it awakens briefly, and goes into the Stop Grant State. This differs from the Intel Pentium processor, which ignores STPCLK# in Auto Halt. The AMD-K6 x86 processor behaves the same as the *IDT WinChip 3* processor.

B.3 INTEGER INSTRUCTION COMPATIBILITY

CPUID Vendor ID String

The vendor identification string returned by the CPUID instruction is different, of course, among the various Pentium-compatible processor manufacturers. A very few programs (games) are dependent upon the "GenuineIntel" string returned by the Intel processors and thus will not perform correctly with the default "CentaurHauls" string returned by the *IDT WinChip 3* processor.

The *IDT WinChip 3* processor has a feature that allows the user to define the vendor ID string returned by the CPUID instruction. This allows programs that are dependent on specific vendor ID strings to be run. This feature is described in Appendix A.

CPUID Feature Flags

As defined in Chapter 3, the feature definition flags returned by the CPUID instruction differs among various Pentium-compatible processors.

Machine-Specific Registers

As defined in Appendix A, the machines-specific registers (MSRs) of an *IDT WinChip 3* processor are just that: machine-specific. That is, there are differences between the *IDT WinChip 3* processor MSRs and the Pentium processor's MSRs (and all other x86 processors).

Undefined EFLAGS Settings

The Intel Pentium documentation defines the setting of the EFLAGS bits for several instructions as "undefined". In some cases the setting of undefined flags is consistent among Pentium-compatible processors and some programs depend upon these settings. In these cases, the *IDT WinChip 3* processor sets the flags the same as does the Pentium processor.

In some cases where the various Pentium-compatible processors differ on these undefined flag settings, the *IDT WinChip 3* processor settings differ from the Pentium processor settings.

CMPXCHG8B

The CMPXCHG8B instruction is supported by the *IDT WinChip 3* processor. However, it is not reported as being supported in the CPUID instruction. This was required to maintain compatibility with some Windows NT versions.

B.4 FLOATING-POINT COMPATIBILITY

Transcendental Accuracy

The results of the transcendental instructions (FSIN, etc.) are slightly different among the various x86 processors—including between the Intel486 processor and the Pentium processor. The *IDT WinChip 3* processor typically gets results within one-half ULP (units in the lower position) average and within one ULP worst-case of the correct mathematical result within the reduced argument range.

Undefined Condition Bits

The Intel Pentium documentation defines the setting of the FPU Status Word condition bits for several instructions as "undefined". In some cases the setting of undefined flags is consistent among Pentium-compatible processors and some programs depend upon these settings. In these cases, the *IDT WinChip 3* processor sets the flags the same as does the Pentium processor.

In some cases where the various Pentium-compatible processors differ on these undefined flag settings, the *IDT WinChip 3* processor settings differ from the Pentium processor settings.