

CGS74B305

Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation & Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

Functional Description

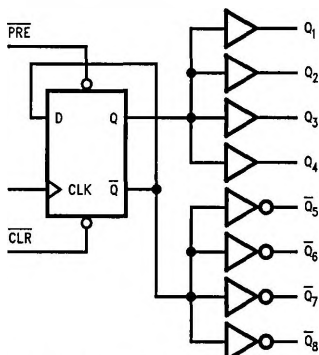
The CGS74B305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. PRE and CLR inputs are provided to set Q and Q outputs high or low independent of CLK pin.

Features

- Clock Generation & Support (CGS) devices ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST™ LSI process
- 750 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Logic Diagram



Circuit description of the '305

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Pin Description

Pin Names	Description
CLK	Clock Input
O ₁ –O ₈	Outputs
PRE	Preset
CLR	Clear

Truth Table

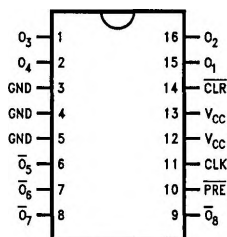
CGS74B305

Inputs			Outputs	
CLR	PRE	CLK	O ₁ -O ₄	O ₅ -O ₈
L	H	X	L	H
H	L	X	H	L
L	L	X	L*	L*
H	H	↑	\bar{Q}_0	Q ₀
H	H	L	Q ₀	\bar{Q}_0

*This state will not persist when CLR/PRE returns to high.

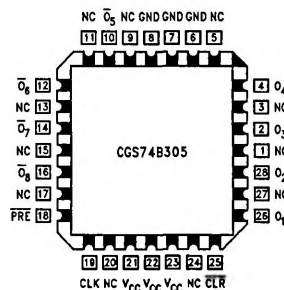
Connection Diagrams

**Pin Assignment
for DIP and SOIC
'305**



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Pin Assignment 28-Pin PCC



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})				7.0V
Input Voltage (V _I)				7.0V
Operating Free	74B303			0°C to +70°C
Air Temperature	64B303			−40°C to +85°C
Storage Temperature Range				−65°C to +150°C
Typical θ _{JA}				303/304/305
Airflow (LFM)	0	225	500	°C/W
Plastic (N) Package	95	70	60	°C/W
Jedec SOIC (M) Package	118	96	86	°C/W
PCC (V) Package	69	53	45	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
High Level Input Voltage (V_{IH})	2V
Low Level Input Voltage (V_{IL})	0.8V
High Level Output Current (I_{OH})	-24 mA
Low Level Output Current (I_{OL})	-48 mA
Free Air Operating Temperature (T_A)	0°C to 70°C

NOTE: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics CGS74/64B303/304/305

Over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}	High Level Output Voltage	$I_{OH} = -2\text{ mA}$, $V_{CC} = 4.5V$	$V_{CC} - 2$			V
		$I_{OH} = 24\text{ mA}$, $V_{CC} = 4.5V$	2.0			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = 48\text{ mA}$		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$		-0.1	-0.50	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$	-50		-150	mA
I_{CC}	Supply Current 303	$V_{CC} = 5.5V$	Outputs High	27	60	mA
			Outputs Low	45	60	mA
I_{CC}	Supply Current 304	$V_{CC} = 5.5V$	Outputs High	20	30	mA
			Outputs Low	42	55	mA
I_{CC}	Supply Current 305	$V_{CC} = 5.5V$	Outputs High	35	45	mA
			Outputs Low	42	55	mA
C_{IN}	Input Capacitance	$V_{CC} = 5V$		5		pF

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$

Symbol	Parameter	CGS74B305			CGS64B305			Units
		V _{CC} = 4.5V to 5.5V T _A = 0°C to 70°C C _L = 0 pF–50 pF R _L = 500Ω			V _{CC} = 4.5V to 5.5V T _A = –40°C to +85°C C _L = 0 pF–50 pF R _L = 500Ω			
		Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Maximum Input Frequency	130			120			MHz
t _{PLH} , t _{PHL}	Propagation Delay CK(n) to O _n	4		8.5	4		8.5	ns
t _{PLH} , t _{PHL}	Propagation Delay PRE/CLR	4 4		10.5 10.5	4 4		11 11	ns
t _{SU}	Set Up Time before CLK	5			5			ns
t _W	CLK HI CLK LO CLR/PRE	4 4 4			4 4 4			ns

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$

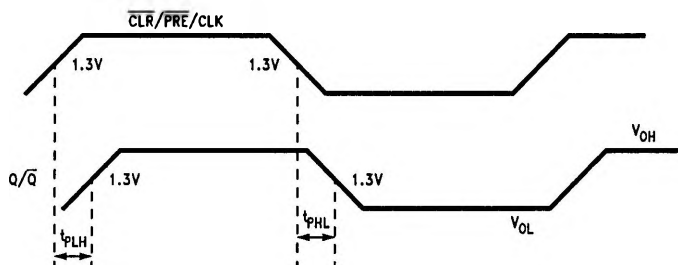
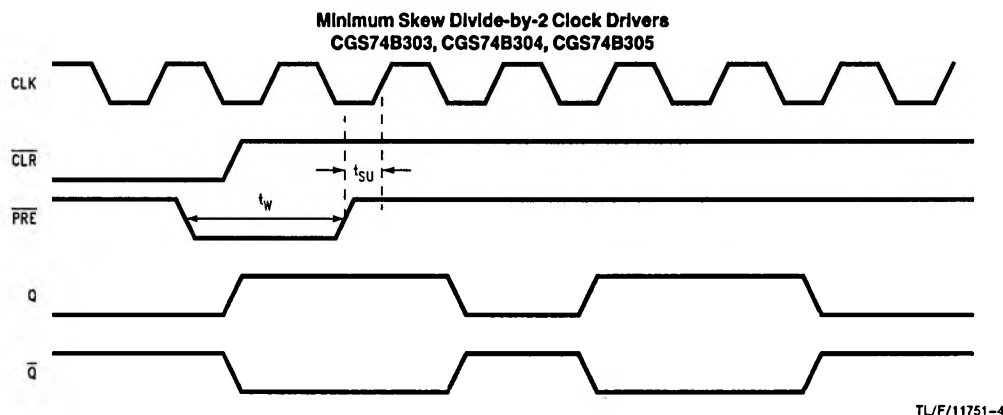
Symbol	Parameter	V _{CC} [*] (V)	CGS74B305			CGS64B305			Units
			T _A = 0°C to 70°C C _L = 0 pF–50 pF R _L = 500Ω			T _A = −40°C to +85°C C _L = 0 pF–50 pF R _L = 500Ω			
			Min	Typ	Max	Min	Typ	Max	
t _{OSHL Q}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.4	0.75		0.4	0.75	ns
t _{OSLH Q}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.4	0.75		0.4	0.75	ns
t _{OSHL Q̄}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.4	0.75		0.4	0.75	ns
t _{OSLH Q̄}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.4	0.75		0.4	0.75	ns
t _{OSLH/HL Q, Q̄}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.9	1.45		0.9	1.45	ns
t _{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	PDIP	5.0		1.45			1.45	ns
		SOIC	5.0		1.45			1.45	
		PCC	5.0		1.35			1.35	
t _{rise} , t _{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads	5.0		1.1 0.9	2.0 2.0		1.1 0.9	2.0 2.0	ns

*Voltage Range 5.0 is 5.0V $\pm 0.5V$.

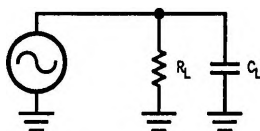
Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the outputs. V_{CC} bypass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

Timing Diagrams



Test Circuit



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R_L is 600 Ω
 C_L is 50 pF for all prop delays and skew measurements.
 C_L is 30 pF for t_{rise} and t_{fall} measurements.

Notes:

- Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.
- All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.
- Load capacitance includes the test jig.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
<p>t_{OSHL}, t_{OSLH}</p> <p>Common Edge Skew:</p> <p>Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = t_{PHL_{max}} - t_{PHL_{min}}$</p> <p>Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = t_{PLH_{max}} - t_{PLH_{min}}$</p> <p>Propagation delays are measured across the outputs of any given device.</p>	<p>FIGURE A</p>	<ul style="list-style-type: none"> • t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/clock operations.
<p>t_{PS}</p> <p>Pin Skew or Transition Skew:</p> <p>$t_{PS} = t_{PHL_i} - t_{PLH_i}$</p> <p>Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. t_{PS} is the maximum difference for outputs $i = 1$ to 8 within a device package.</p>	<p>FIGURE B</p>	<ul style="list-style-type: none"> • t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).