CLC103

CLC103 Fast Setting, High Current Wideband

Literature Number: SNOS841

National Semiconductor

Comlinear CLC103
Fast Settling, High Current Wideband Op Amp

General Description

The CLC103 is a high-power, wideband op amp designed for the most demanding high-speed applications. The wide bandwidth, fast settling, linear phase, and very low harmonic distortion provide the designer with the signal fidelity needed in applications such as driving flash A to Ds. **The 80MHz full-power bandwidth and 200mA output current of the CLC103 eliminate the need for power buffers in most applications;** the CLC103 is an excellent choice for driving large high-speed signals into coaxial lines.

In the design of the CLC103 special care was taken in order to guarantee that the output settle quickly to within 0.4% of the final value for use with ultra fast flash A to D converters. This is one of the most demanding of all op amp requirements since settling time is affected by the op amp's bandwidth, passband gain flatness, and harmonic distortion. This high degree of performance ensures excellent performance in many other demanding applications as well.

The dynamic performance of the CLC103 is based on Comlinear's proprietary op amp topology. This new design provides performance far beyond that available from conventional op amp designs; unlike conventional op amps where optimum gain-bandwidth product occurs at a high gain, minimum settling time at a gain of −1, and maximum slew rate at a gain of +1, the Comlinear design provides consistent, predictable performance across its entire gain range. For example, the table below shows how **the −3dB bandwidth remains nearly constant over a wide range of gains.** And since the amplifier is inherently stable, no external compensation is required. The result is shorter design time and the ability to accommodate design changes (in gain, for example) without loss of performance or redesign of compensation circuits.

The CLC103 is constructed using thin film resistor/bipolar transistor technology, and is available in two versions:

CLC103AI	-25°C to +85°C	24-pin ceramic DIP
CLC103AM	-55°C to +125°C	24-pin ceramic DIP, MIL-STD-883, Level B

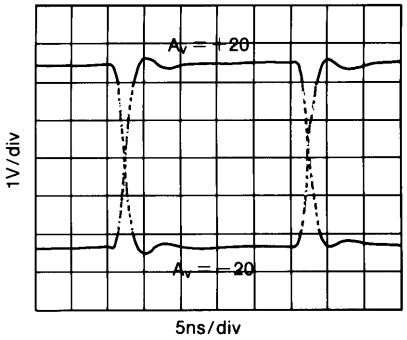
Features

- 80MHz full-power bandwidth ($20V_{pp}$, 100Ω)
- 200mA output current
- 0.4% settling in 10ns
- 600V/µs slew rate
- 4ns rise and fall times (20V)

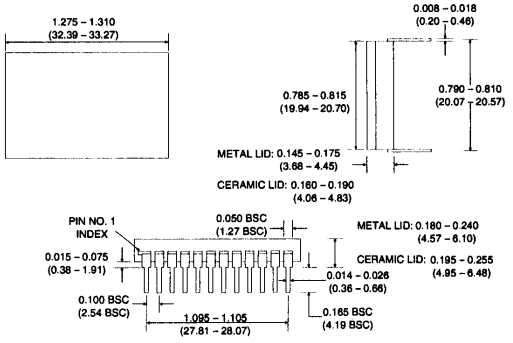
Applications

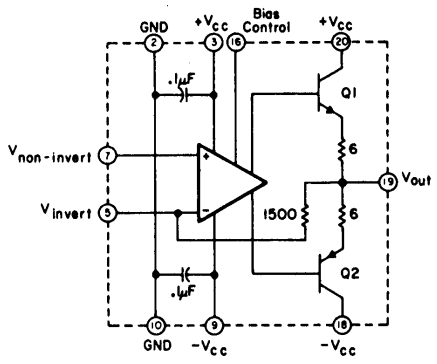
- Coaxial line driving
- DAC current to voltage amplifier
- Flash A to D
- Baseband and video communications
- Radar and IF processors

Small Signal Pulse Response



Package Dimensions





CLC103 Equivalent Circuit Diagram
(all undesignated pins are internally unconnected)

Typical Performance

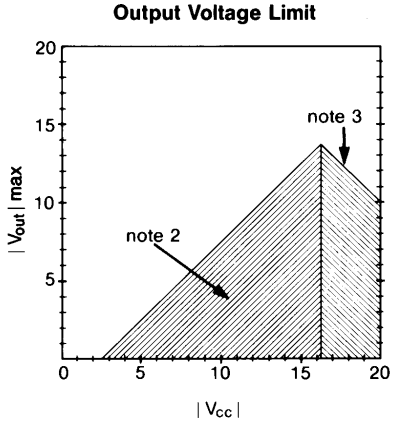
parameter	gain setting +4	+20	+40	−4	−20	−40	units
−3dB bandwidth	230	150	130	155	145	125	MHz
rise time (20V)	4	4	4	4	4	4	ns
slew rate	6	6	6	6	6	6	V/ns
settling time (0.4%)	10	10	12	10	10	12	ns

CLC103 Electrical Characteristics (A_V = +20, V_{CC} = ±15V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature [1]	CLC103AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature [1]	CLC103AI	+25°C	−25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
* −3dB bandwidth	V_{out} <4V_{pp}	150	>125	>135	>120	MHz	SSBW
gain flatness	V_{out} <4V_{pp}						
* peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.3	dB	GFPL
* peaking	>50MHz	0.2	<1.5	<0.6	<0.6	dB	GFPH
* rolloff	at 100MHz	—	<0.4	<0.6	<0.8	dB	GFR
group delay	to 75MHz	3.0	—	—	—	ns	GD
linear phase deviation	to 75MHz	1	<3	<2	<4	°	LPD
reverse isolation – non-inverting	to 150MHz	55	>45	>45	>45	dB	RINI
TIME DOMAIN RESPONSE							
rise and fall time	5V step	2.3	<2.8	<2.6	<2.9	ns	TRS
	20V step	4	<5	<5	<5	ns	TRL
settling time to 0.4%	10V step	10	<25	<20	<25	ns	TSP
overshoot	5V step	5	<15	<10	<10	%	OS
slew rate (overdriven input)		6	>5	>5	>5	V/ns	SR
overload recovery							
<50ns pulse, 200% overdrive		30	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
* 2nd harmonic distortion	2V_{pp}, 20MHz	−48	<−40	<−40	<−40	dBc	HD2
* 3rd harmonic distortion	2V_{pp}, 20MHz	−48	<−40	<−40	<−40	dBc	HD3
equivalent input noise							
noise floor	>100kHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	1kHz to 100MHz	28	<56	<56	<56	μV	INV
noise floor	>5MHz	−158	<−152	<−152	<−152	dBm(1Hz)	SNF
integrated noise	5MHz to 100MHz	28	<56	<56	<56	μV	INV
STATIC, DC PERFORMANCE							
* input offset voltage		10	<30	<25	<30	mV	VIO
average temperature coefficient		35	<120	<120	<120	μV/°C	DVIO
* input bias current	non-inverting	10	<40	<30	<40	μA	IBN
average temperature coefficient		20	<125	<125	<125	nA/°C	DIBN
* input bias current	inverting	20	<110	<60	<110	μA	IBI
average temperature coefficient		250	<500	<500	<500	nA/°C	DIBI
* power supply rejection ratio		54	>45	>45	>45	dB	PSRR
common mode rejection ratio		38	>30	>30	>30	dB	CMRR
* supply current	no load	30	<36	<34	<36	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	250	>100	>100	>100	kΩ	RIN
	capacitance	2.4	<3	<3	<3	pF	CIN
output impedance	at DC	—	<0.1	<0.1	<0.1	Ω	RO
	at 100MHz	2, 45	—	—	—	Ω, nH	ZO
output voltage range	no load	—	>±11	>±11	>±11	V	VO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings



supply voltage (V_{CC})	±20V
output current	±200mA
thermal resistance (θ_{ca})	see thermal model
junction temperature	+175°C
operating temperature	AI: −25°C to +85°C
	AM: −55°C to +125°C
storage temperature	−65°C to +150°C
lead temperature (soldering 10s)	+300°C

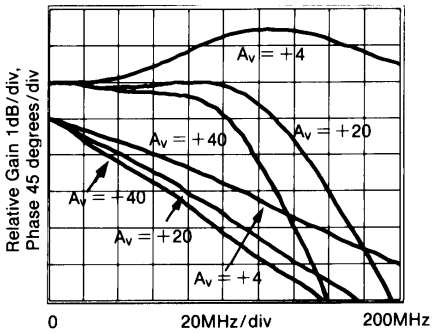
***note 1:** Parameters preceded by an * are the final electrical test parameters and are 100% tested. AM units are tested at – 55˚C, +25˚C, and +125˚C. AI units are tested only at +25˚C although their performance is guaranteed at – 25˚C and +85˚C as indicated above.

note 2: This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%, maximum input voltage may be as large as twice the maximum. V_{cm} should never exceed ±5V. (V_{cm} is the voltage at the non-inverting input, pin 7.)

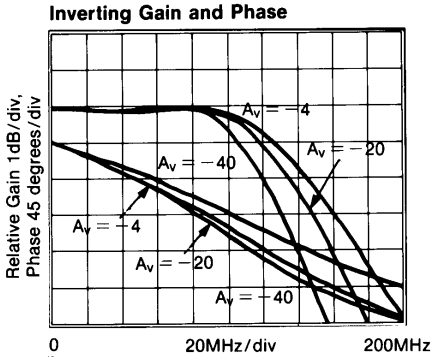
note 3: This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V_{CC} is ±15V.

CLC103 Typical Performance Characteristics (A_V = +20, V_{CC} = ±15V, R_L = 100Ω; unless specified)

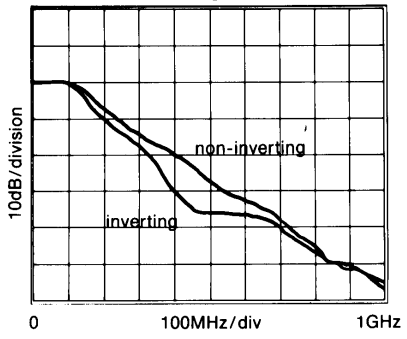
Non-Inverting Gain and Phase



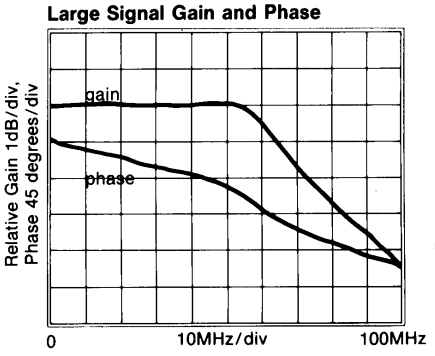
Inverting Gain and Phase



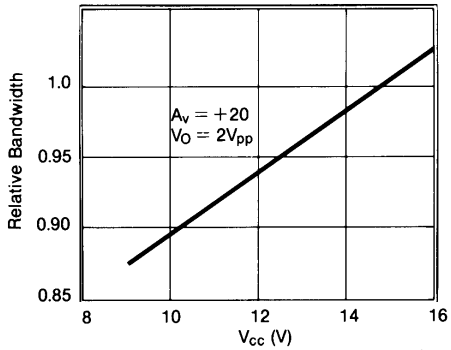
Broadband Inverting and Non-Inverting Gain



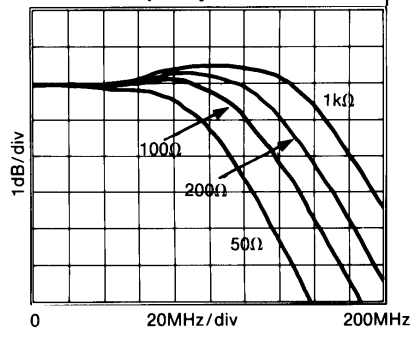
Large Signal Gain and Phase



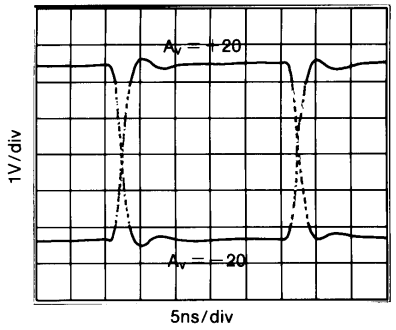
Relative Bandwidth vs. V_{cc}



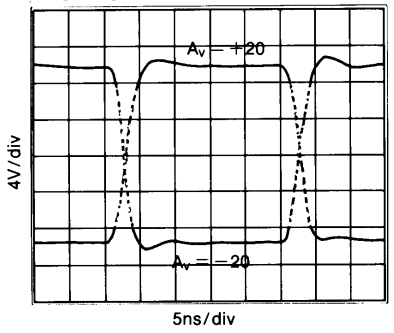
Gain vs. Frequency for Various Loads



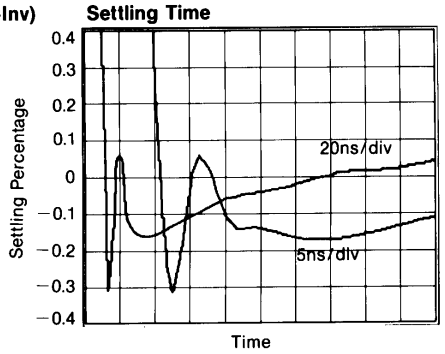
Small Signal Pulse Response (Inv, Non-Inv)



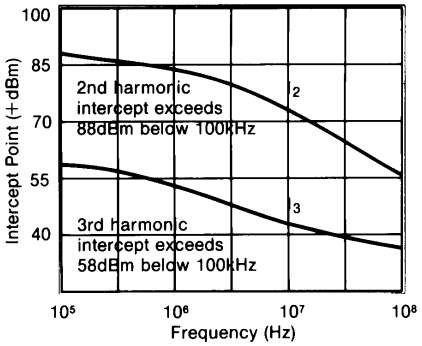
Large Signal Pulse Response (Inv, Non-Inv)



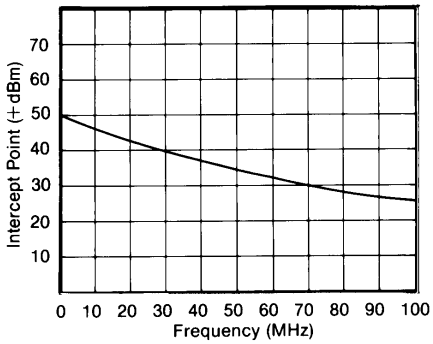
Settling Time



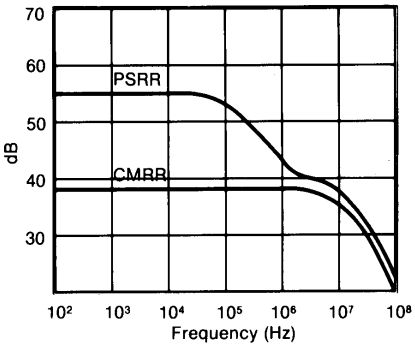
2nd and 3rd Harmonic Distortion Intercept



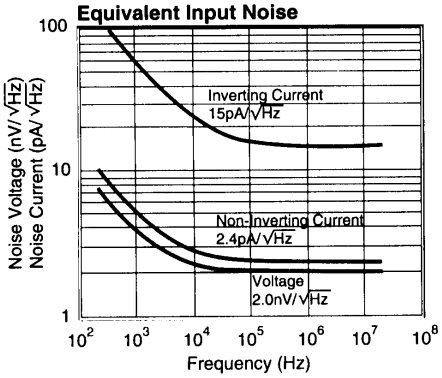
2-Tone 3rd Order Intermod. Intercept

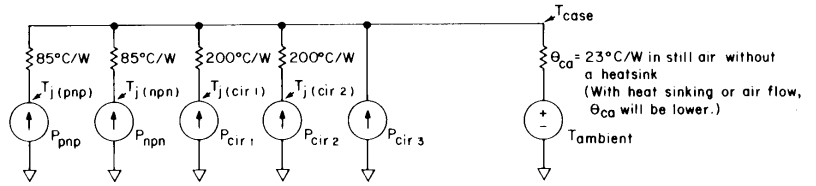


CMRR and PSRR



Equivalent Input Noise





P_{cir1} = 10mA [(+V_{cc})−V_{out}]
P_{cir2} = 10mA [V_{out} −(−V_{cc})]
P_{cir3} = I_C [(+V_{cc}) −(−V_{cc})] where I_C = 10mA at ±15V
P_{XXX} = I_{col} [(±V_{cc})−V_{out} −I_{col} (R_{col} +6)] where I_{col} = V_{out}/R_{load} or 9mA, whichever is greater. (Include R_f in R_{load}.)

(For positive V_{out} and V_{cc}, P_{XXX} is the power in the npn device. For negative V_{out} and V_{cc}, this power is in the pnp device.)
R_{col} is an external resistor (22 ohms recommended) between the xxx collector and ±V_{cc}.
$T_{j\,(pnp)}$ = (P_{pnp}) 85°C/W + (P_{total}) θ_{ca} + $T_{ambient}$, similar for $T_{j\,(npn)}$.
$T_{j\,(cir1)}$ = (P_{cir1}) 200°C/W + (P_{total}) θ_{ca} + $T_{ambient}$, similar for $T_{j\,(cir2)}$.

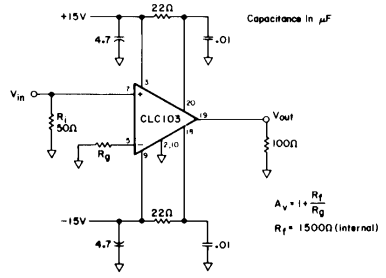


Figure 1: recommended non-inverting gain circuit

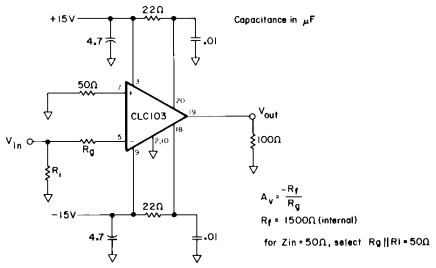


Figure 2: recommended inverting gain circuit

Test fixture layout artwork is available upon request.

CLC103 Operation

The CLC103 is based on Comlinear's proprietary op amp topology, a unique design which uses current feedback instead of the usual voltage feedback. This design provides dynamic performance far beyond that previously available, yet it is used basically the same as the familiar voltage-feedback op amp (see the gain equations above). A complete discussion of current feedback is given in application note AN300-1.

Layout Considerations

To obtain optimum performance from any circuit operating at high frequencies, good PC layout is essential. Fortunately, the stable, well-behaved response of the CLC103 makes operation at high frequencies less sensitive to layout than is the case with other wideband op amps, even though the CLC103 has a much wider bandwidth.

In general, a good layout is one which minimizes the unwanted coupling of a signal between nodes in a circuit. A continuous ground plane from the signal input to output on the circuit side of the board is helpful. Traces should be kept short to minimize inductance. If long traces are needed, use microstrip transmission lines which are terminated in their characteristic impedance. At some high-impedance nodes, or in sensitive areas such as near pin 5 of the CLC103, stray capacitance should be kept small by keeping nodes small and removing ground plane directly around the node.

The $\pm V_{cc}$ connections to the CLC103 are internally bypassed to ground with 0.1μF capacitors to provide good high-frequency decoupling. It is recommended that 1μF or larger tantalum capacitors be provided for low-frequency decoupling. The 0.01μF capacitors shown at pins 18 and 20 in figures 1 and 2 should be kept within 0.1" of those pins. A wide strip of ground plane should be provided for a signal return path between the load-resistor ground and these capacitors.

Since the layout of the PC board forms such an important part of the circuit, much time can be saved if prototype amplifier boards are tested early in the design stage. Encased/connectorized amplifiers are available from Comlinear.

Settling Time, Offset, and Drift

After an output transition has occurred, the output settles very rapidly to the final value and no change occurs for several microseconds. Thereafter, thermal gradients inside the CLC103 will cause the output to begin to drift. When this cannot be tolerated, or when the initial offset voltage and drift is unacceptable, the use of a composite amplifier is advised.

A composite amplifier can also be referred to as a feed-forward amplifier. Most feed-forward techniques such as those used in the vast majority of wideband op amps, involve the use of a wideband AC-coupled channel in parallel with a low-bandwidth, high-gain DC-coupled amplifier. For the composite amplifier suggested for use with the CLC103, the CLC103 replaces the wideband AC-coupled amplifier and a low-cost monolithic op amp is used to supply high open-loop gain at low frequencies. Since the CLC103 is strictly DC coupled throughout, crossover distortion of less than 0.01dB and 1° results.

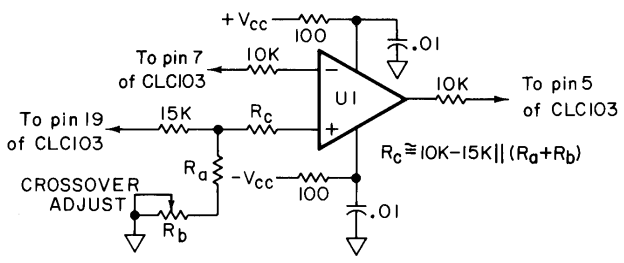


Figure 3: non-inverting gain composite amp to be used with figure 1 circuit

For composite operation in the non-inverting mode, the circuit in figure 1 should be modified by the addition of the circuit shown in figure 3. For inverting operation, modify the circuit in figure 2 by the addition of the circuit in figure 4. Keep all resistors which connect to the CLC103 within 0.2" of the CLC103 pins. The other side of these resistors should likewise be as close to U1 as possible. For good overall results, U1 should be similar to the LF356; this gives 5μV/°C input offset drift and the crossover frequency occurs at about 2MHz. Since U1 has a feedback network composed of $R_a + R_b$ and a 15kΩ resistor, which is in parallel with R_g and the internal 1.5kΩ feedback resistor of the CLC103, R_b must be adjusted to match the feedback ratios of the two networks. This is done by driving the composite amplifier with a 70kHz square wave large enough to produce a transition from +5V to −5V at the CLC103 output and adjusting R_b until the output of U1 is at a minimum. R_a should be about $9.5R_g$ for best results; thus, R_b should be adjusted around the value of $0.5R_g$.

Bias Control

In normal operation, the bias control pin (pin 16) is left unconnected. However, if control over the bias of the amplifier is desired, the bias control pin may be driven with a TTL signal; a TTL high level will turn the amplifier off.

Distortion and Noise

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the CLC103. First, convert the output voltage V_O to $V_{rms} = (V_{pp}/2\sqrt{2})$ and then to $P = (10\log_{10}(20V_{rms}^2))$ to get the output power in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below the level of P, as will the two-tone third order intermodulation products. These approximations are useful for P<−1dB compression levels.

Approximate noise figure can be determined for the CLC103 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s\Delta f}\right]$$

where v_n is the rms noise voltage and i_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise, so Δf should equal one (1) and v_n and i_n should be read directly off the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Application Notes and Assistance

Application notes that address topics such as data conversion, fiber optics, and general high-frequency circuit design are available from Comlinear or your Comlinear sales engineer.

Comlinear maintains a staff of highly-qualified applications engineers to provide technical and design assistance.

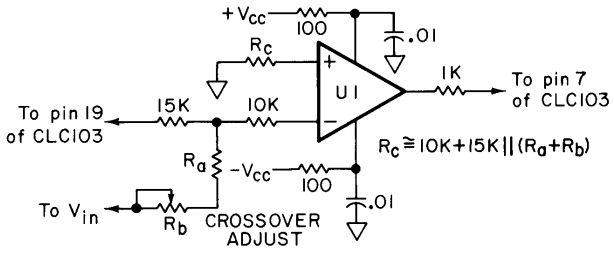


Figure 4: inverting gain composite amplifier to be used with figure 2 circuit

This page intentionally left blank.

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265