CLC502

CLC502 Clamping, Low Gain Op Amp with Fast 14-bit Settling

Literature Number: SNOS859B

National Semiconductor

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CLC502
Clamping, Low Gain Op Amp with Fast 14-bit Settling

General Description

The CLC502 is an operational amplifier designed for low gain applications requiring output voltage clamping. This feature allows the designer to set maximum positive and negative output voltage levels for the amplifier – thus allowing the CLC502 to protect downstream circuitry, such as delicate converter systems from destructive transients or signals which would otherwise cause saturation. The overload recovery time of only 8ns permits systems to resume operation quickly after overdrive.

High accuracy systems will also benefit from the CLC502's fast, accurate settling. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC502 is ideal as the input amplifier in high accuracy (12 bits and above) A/D systems. Unlike most other high speed op amps, the CLC502 is free of settling tails. And, as the settling plots show, settling to 0.01% accuracy is an even faster 18ns typical.

The CLC502 is also useful in other applications which require low gain amplification (± 1 to ±8) and the clamping or overload recovery features. For example, even low resolution imaging circuits, which often have to cope with overloading signal levels, can benefit from clamping and overload recovery.

The CLC502 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-91743

*Space level versions also available.

*For more information, visit http://www.national.com/mil

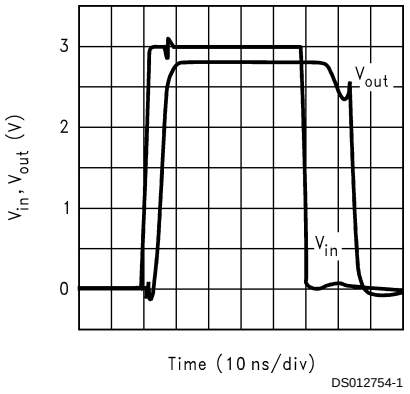
Features

- Output clamping with fast recovery
- 0.0025% settling in 25ns (32ns max)
- Low power, 170mW
- Low distortion. −50dBc at 20MHz

Applications

- Output clamping applications
- High accuracy A/D systems (12-14 bits)
- High accuracy D/A converters
- Pulse amplitude modulation systems

Clamped Pulse Response (8x Overdrive)



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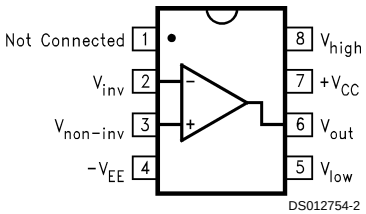
Connection Diagram



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Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin Plastic DIP	−40˚C to +85˚C	CLC502AJP	CLC502AJP	N08E
8-pin Plastic SOIC	−40˚C to +85˚C	CLC502AJE	CLC502AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage	$\pm V_{CC}$
Junction Temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD (Human Body Model)	1000V

Operating Ratings

Thermal Resistance

Package	θ_{JC}	θ_{JA}
MDIP	65˚C/W	120˚C/W
SOIC	60˚C/W	140˚C/W

Electrical Characteristics

(A_V = +2, V_{CC} = ±5V, R_L =100Ω, R_f = 250Ω, V_H = +3V, V_L = −3V)

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Ambient Temperature		CLC502AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Performance							
SSBW	-3dB Bandwidth	V_{OUT} <0.5V_{PP}	150	>100	>110	>100	MHz
LSBW		V_{OUT}<5V_{PP}	65	>40	>40	>40	MHz
	Gain Flatness	V_{OUT}< 0.5V_{PP}					
GFPL	Peaking	DC to 25MHz	0	<0.4	<0.3	<0.4	dB
GFPH	Peaking	>25MHz	0	<0.7	<0.5	<0.7	dB
GFR	Rolloff (Note 5)	DC to 50MHz	0.5	<1.0	<1.0	<1.0	dB
LPD	Linear Phase Deviation	DC to 50MHz	0.4	<1.2	<1.0	<1.2	deg
Time Domain Performance							
TRS	Rise and Fall Time	0.5V Step	2.7	<3.5	<3.2	<3.5	ns
TRL		5V Step	5.0	<8	<8	<8	ns
TS14	Settling Time to ± 0.0025%	2V Step	25	<32	<32	<32	ns
TSP	± 0.01%	2V Step	18	<25	<25	<25	ns
TSS	± 0.1%	2V Step	10	<15	<15	<15	ns
OS	Overshoot	0.5V Step	0	<10	<10	<10	%
SR	Slew Rate		800	>500	>500	>500	V/µs
Distortion And Noise Performance							
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz	−50	<−38	<−43	<−43	dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz	−60	<−53	<−53	<−53	dBc
	Equivalent Input Noise						
SNF	Noise Floor	>1MHz	−157	<−155	<−155	<−155	dBm (1Hz)
INV	Integrated Noise	1MHz to 150MHz	40	<49	<49	<49	µV
DG	Differential Gain (Note 4)		0.01	–	–	–	%
DP	Differential Phase (Note 4)		0.05	–	–	–	deg
Clamp performance							
OVC	Overshoot in Clamp	2x Overdrive	5	–	<10	–	%
TSO	Overload Recovery from Clamp	2x Overdrive	8	<15	<15	<15	ns
VOC	Clamp Accuracy(Note 3)	2x Overdrive	±0.2	<±0.3	<±0.3	<±0.3	V
ICL	Input Bias Current on V_H, or V_L		20	<75	<35	<35	µA
CBW	−3dB Bandwidth	V_L or V_H = 2V_{PP}	50	–	–	–	MHz
CMC	Clamp Voltage Range	V_H or V_L		<±3.0	<±3.3	<±3.3	V
Static, DC Performance							
VIO	Input Offset Voltage (Note 3)		0.5	<2.6	<1.6	<2.8	mV

Electrical Characteristics (Continued)

(A_V = +2, V_{CC} = ±5V, R_L =100Ω, R_f = 250Ω, V_H = +3V, V_L = −3V)

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Static, DC Performance							
DVIO	Average Temperature Coefficient		3	<12	–	<12	µV/°C
IBN	Input Bias Current (Note 3)	Non-Inverting	10	<45	<25	<35	µA
DIBN	Average Temperature Coefficient		100	<250	–	<100	nA/°C
IBI	Input Bias current (Note 3)	Inverting	10	<50	<30	<40	µA
DIBI	Average Temperature Coefficient		100	<250	–	<100	nA/°C
PSRR	Power Supply Rejection Ratio		68	>55	>60	>60	dB
CMRR	Common Mode Rejection Ratio		65	>55	>60	>60	dB
ICC	Supply Current (Note 3)	No Load	17	<23	<23	<23	mA
Miscellaneous Performance							
RIN	Non-Inverting Input	Resistance	150	>50	>85	>85	kΩ
CIN		Capacitance	35	<5.5	<5.5	<5.5	pF
RO	Output Impedance	at DC	0.1	<0.2	<0.2	<0.2	Ω
CMIR	Common Mode Input Range		3.0	>2.0	>2.5	>2.5	V
VO	Output Voltage Range	No Load	±3.5V	>±3.0	>±3.2	>±3.2	V
IO	Output Current		±55	>±25	>±45	>±45	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

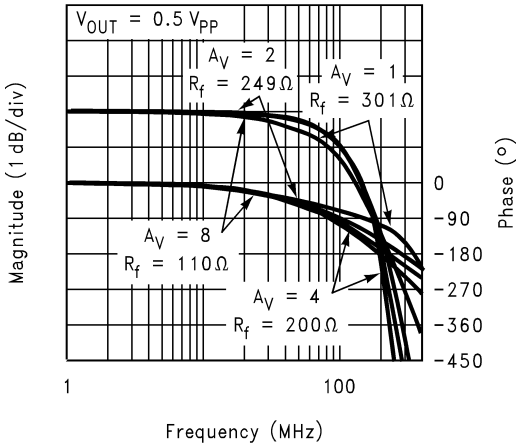
Note 3: AJ-level: spec. is 100% tested at +25°C.

Note 4: Differential gain and phase measure at A_v = +2V, R = 250Ω

Note 5: R_L = 150Ω, $1V_{PP}$ equivalent video signal, 0-100 IRE, 40 IRE_{PP} 0 IRE = 0 volts, at 75Ω load and 3.58 MHz

Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω, V_H = +3V, V_L = −3V)

Non-Inverting Frequency Response



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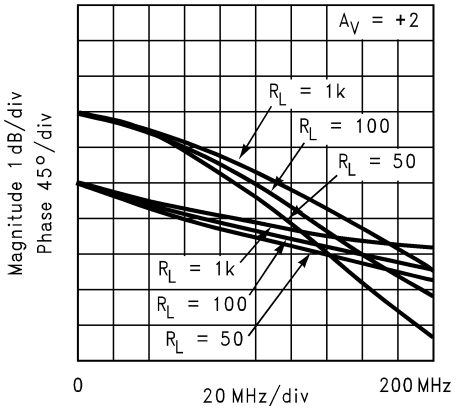
Inverting Frequency Response



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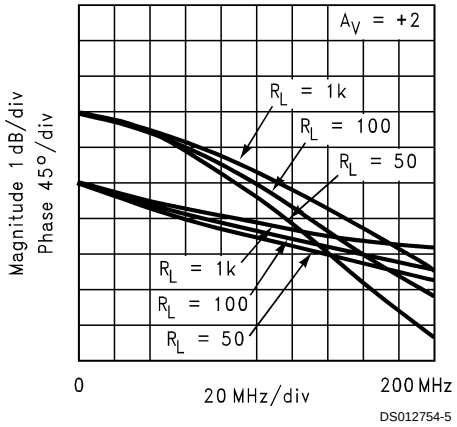
Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω, V_H = +3V, V_L = −3V)) (Continued)

Frequency Response for Various R_Ls



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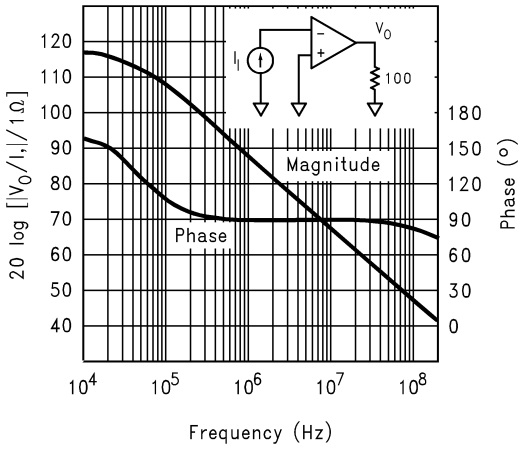
Open-Loop Transimpedance Gain, Z(s)



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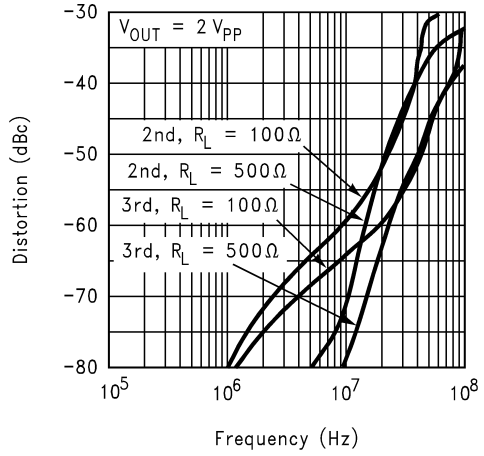
2nd and 3rd Harmonic Distortion



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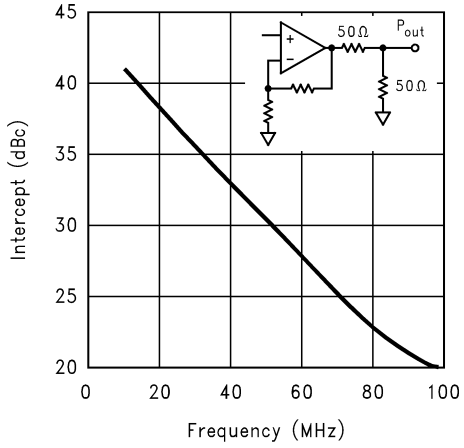
2-Tone, 3rd Order Intermodulation Intercept



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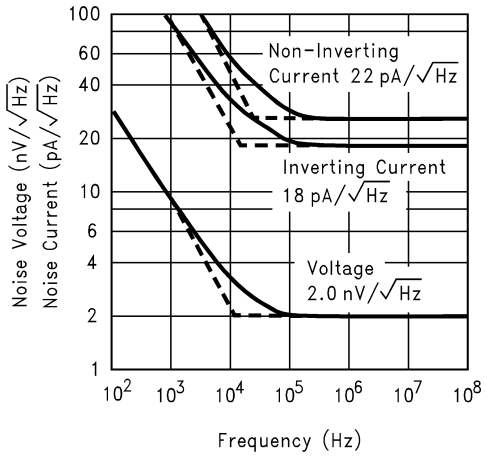
Equivalent Input Noise



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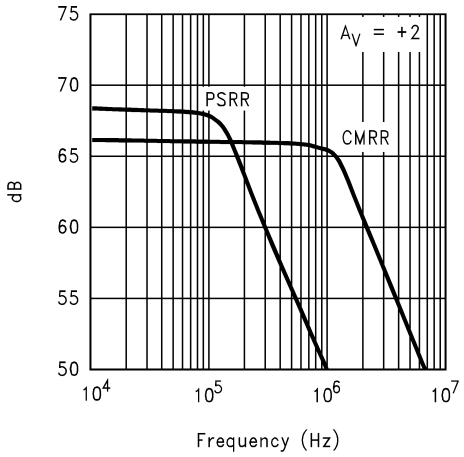
CMRR and PSRR



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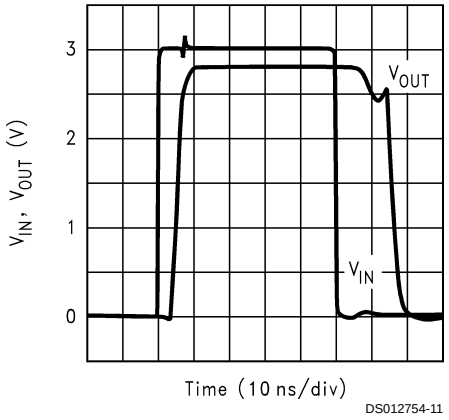
Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω, V_H = +3V, V_L = −3V)) (Continued)

Clamped Pulse Response (8x Overdrive)



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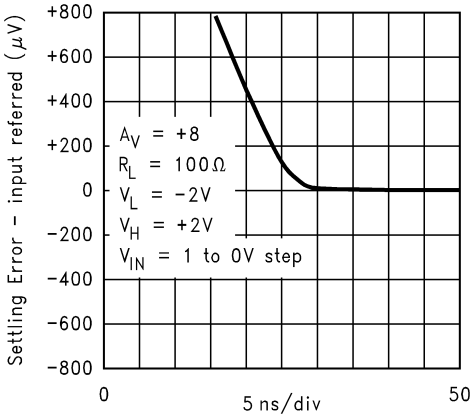
Settling, Clamped (4x overdrive)



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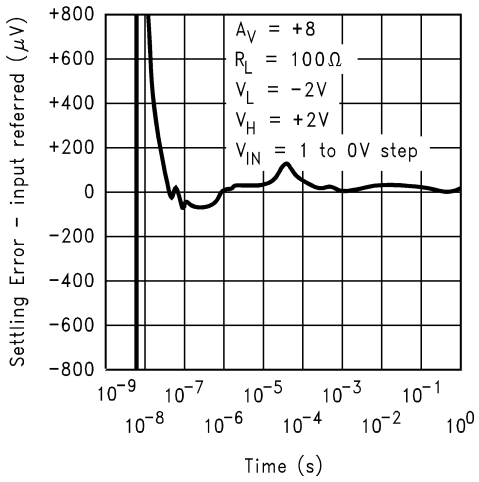
Long-Term Settling, Clamped (4x overdrive)



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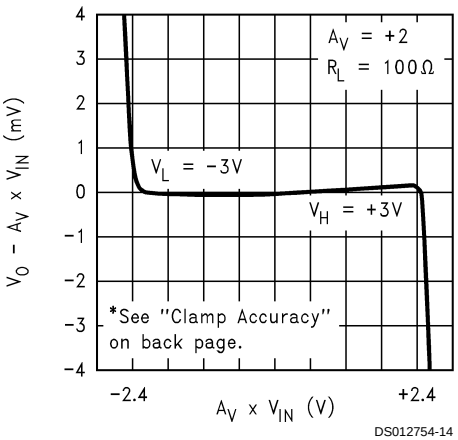
Nonlinearity Near Clamp Voltage



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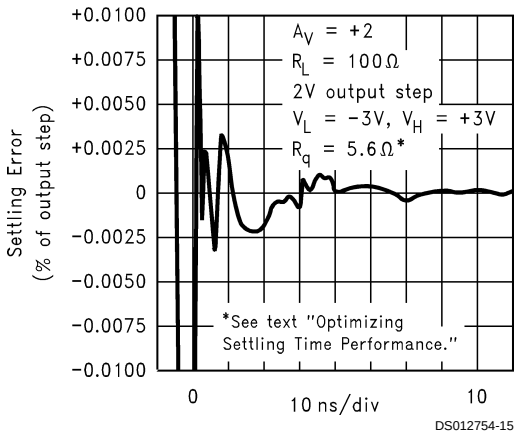
Settling, Umclamped



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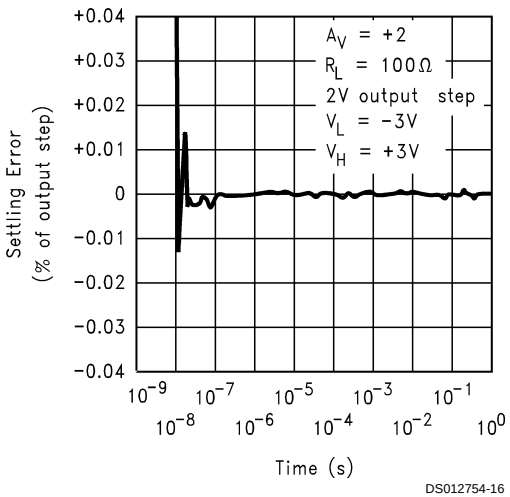
Long-Term Settling, Unclamped



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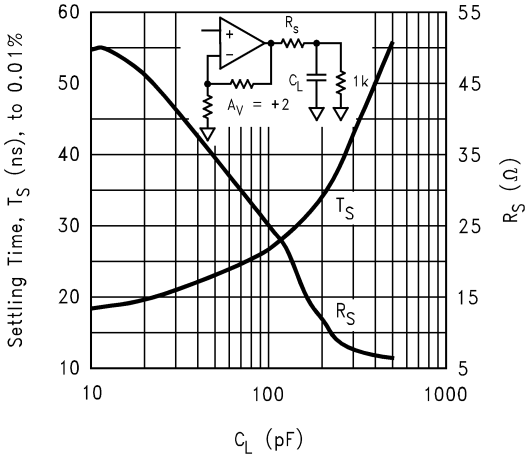
Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 250Ω, V_H = +3V, V_L = −3V)) (Continued)

Settling Time vs. Capacitive Load



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Application Division

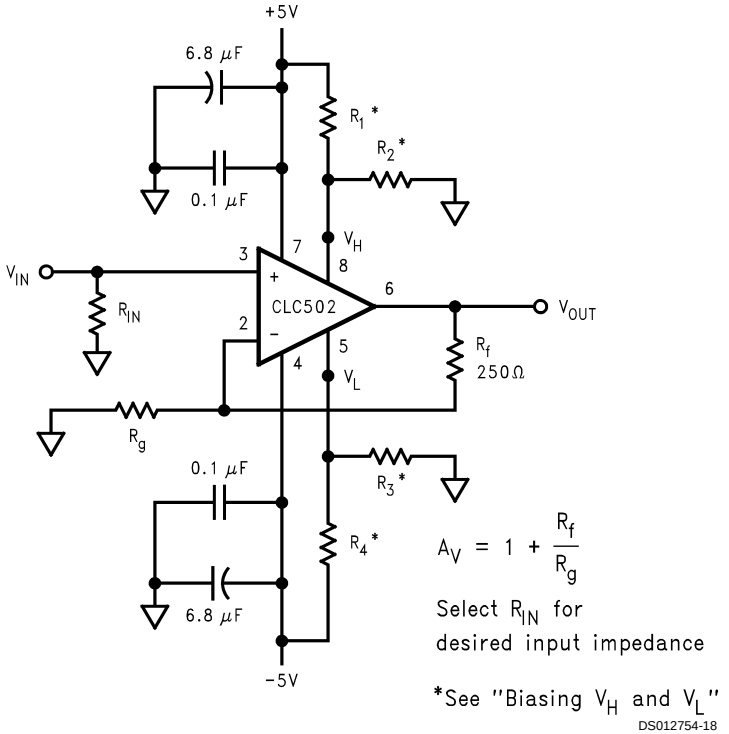

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FIGURE 1. Recommended Non-Inverting Gain Circuit

Application Division (Continued)

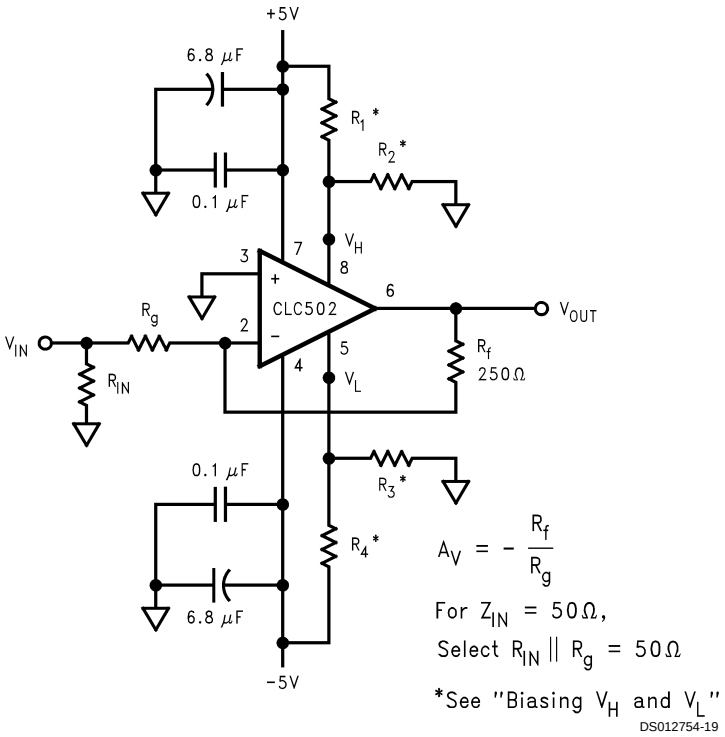


FIGURE 2. Recommended Inverting Gain Circuit

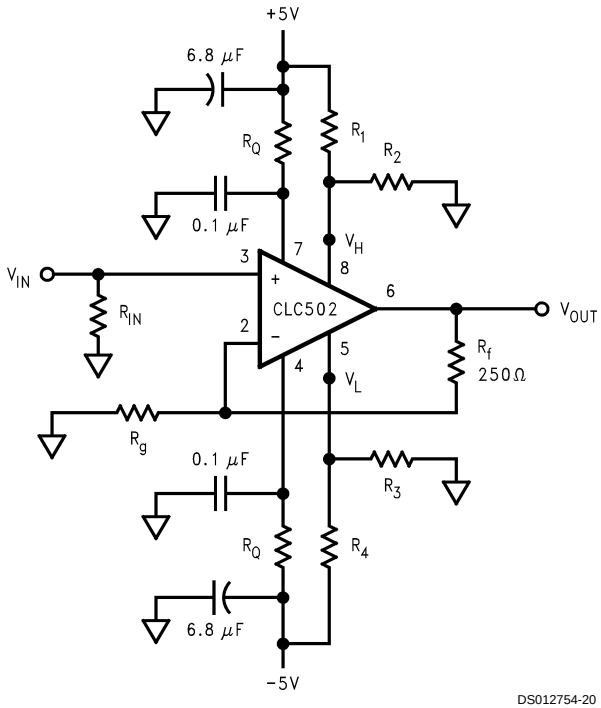


FIGURE 3. Location of Damping Resistors (R_Q)

Application Division (Continued)

Clamp Operation

The maximum positive or negative excursion of the output voltage is determined by voltages applied to the clamping pins, V_H and V_L. V_H determines the positive clamping level; V_L determines the negative level. For example, if V_H is set at +2V and V_L is set at −0.5V the output voltage is restricted within this −0.5V to +2V range. When the output voltage tries to exceed this level, the amplifier goes into "clamp mode" and the output voltage limits at the clamp voltage.

Clamp Accuracy and Amplifier Linearity

Ideally, the clamped output voltage and the clamp voltage should be identical. In practice, however, there are two sources of clamp inaccuracy: the inherent clamp accuracy (which is shown in the specification page) and resistor divider action of open-loop output resistance of 10Ω and the load resistor. Or, in equation form,

$$V_{OUT,\ clamp} = (V_{H\ or\ L} \pm 300\,mV)\frac{R_L}{R_L + 10\Omega.} \quad (1)$$

When settling the clamp voltages, the designer should also recognize that within about 200mV of the clamp voltages, amplifier linearity begins to deteriorate. (See plot on previous page.)

Biasing V_H and V_L

Each of the clamping pins is buffered internally so simple resistive voltage divider circuits work well in providing the clamp voltages. V_L and V_H can be set by choosing the divider resistors using:

$$V_H = (5V)\left(\frac{R_2}{R_1 + R_2}\right) \quad V_L = (-5V)\left(\frac{R_3}{R_3 + R_4}\right) \quad (2)$$

As a general guideline, let $R_1 + R_2 \cong R_3 + R_4 \cong 5k\Omega$.

V_H should be biased more positively than V_L. V_H may be biased below 0V; however, with this biasing, the output voltage will actually clamp at 0V unless a simple pull down circuit is added to the op amp output (when clamped against V_H, the output cannot sink current). An analogous situation and design solution exists for V_L when it is biased above 0V, but in this case, a pull up circuit is used to source current when the amplifier is clamped against V_L.

The clamp voltage range rating is that for normal operation. Problems in over driven linearity may occur if the clamps are set outside this range so this is not suggested under any conditions. If the clamping capability is not required, the CLC402 (low gain op amp with fast 14-bit settling) may be a more appropriate part.

The clamps, which have a bandwidth of about 50MHz, may be driven by high frequency signal source. This allows the clamping level to be modulated, which is useful in many applications such as pulse amplitude modulation. The source resistance of the signal source should be less than 500Ω to ensure stability.

Clamp-Mode Dynamics

As can be seen in the clamped pulse response plot, clamping is virtually instantaneous. Note, however, that there can be a small amount of overshoot, as indicated on the specification page. The output voltage stays at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. When the input voltage decreases, it will eventually reach a point where it is no longer trying to drive the output voltage above the clamp voltage. When this occurs, there is typically a 5-10ns "overload recovery from clamp," which is the time it takes for the op amp to resume linear operation. The normal op amp parameters, such as the rise time, apply when the op amp is in linear operation.

Optimizing Settling Time Performance

To obtain the best possible settling time performance for the CLC502, some additional design criteria must be considered, particularly when driving loads of less than 500Ω. When driving a 100Ω load, a step of a few volts on the output will create a large step of current in the power supplies. In some cases, this step will cause a small ringing on the power supply due to the bypass capacitor (.1µF) oscillating with the inductance in the power supply trace. The critical trace is the power supply trace between the two capacitors (a trace inductance of 20nH will be enough to degrade settling time performance). The frequency of the ring can be determined by

$$f = \frac{1}{2\pi\sqrt{C^* L_{Trace}}} \quad (3)$$

and any reduction in this frequency will improve performance due to better power supply rejection at lower frequencies . To obtain the best performance, small resistor, R_Q, may be added in the trace to dampen the circuit (See *Figure 3*). An R_Q of 5-10Ω will result in excellent settling performance and will have only minor impact on other performance characteristics. No provision for R_Q has been made on the evaluation board available from National as part #730013. It can, however, be easily added by cutting a trace and adding a 5- 10Ω resistor, as shown in *Figure 3*, for both supplies.

DC Accuracy and Notes

Since the two inputs for the CLC502 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. The two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting source resistance ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determine similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin source resistance.

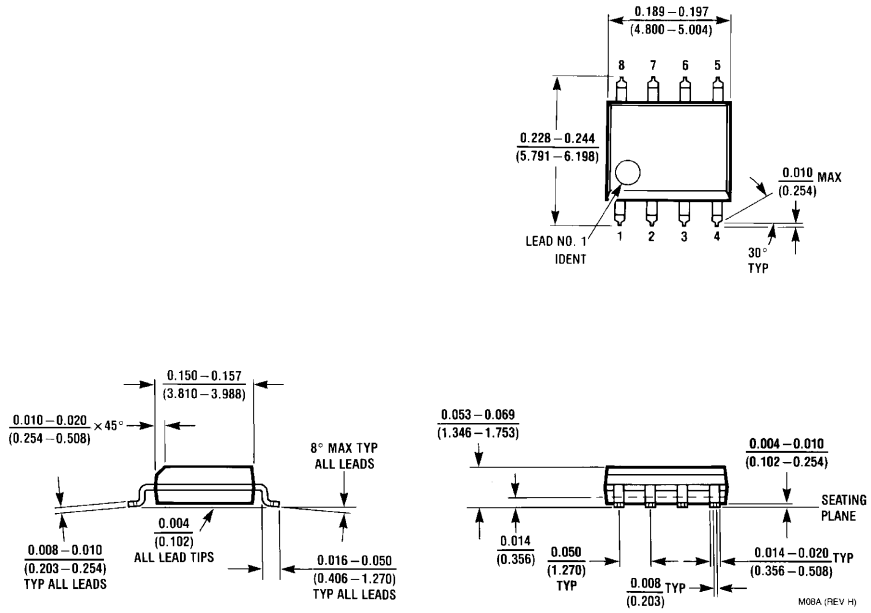
$$\text{Output Offset } V_o = \pm \text{ IBN x } R_s\ (1 + R_f/R_g) \pm \text{VIO } (1 + R_f/R_g) \pm \text{ IBI x } R_f$$

Printed Circuit Layout

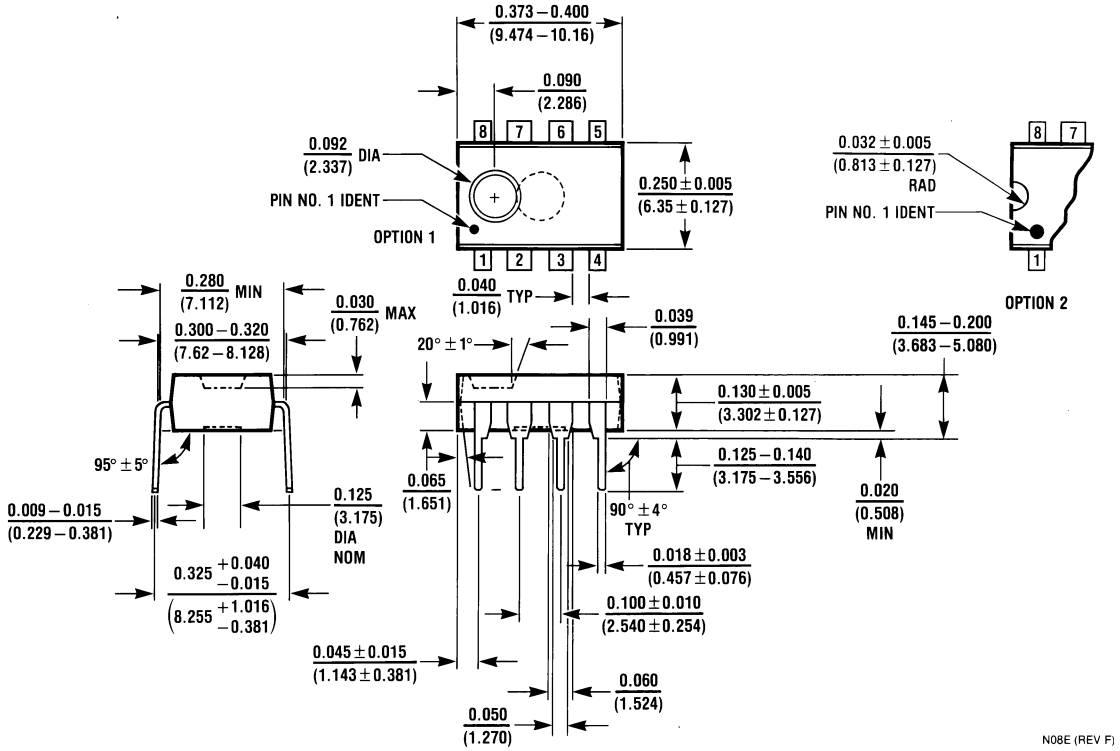
As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

The device is also very sensitive to parasitic capacitance on the output pin. The plots include a suggested series R_S to de-couple this effect. Evaluation boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC502 are available.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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