August 2001

National Semiconductor

CLC5903
Dual Digital Tuner / AGC

General Overview

The CLC5903 Dual Digital Tuner / AGC IC is a two channel digital downconverter (DDC) with integrated automatic gain control (AGC). The CLC5903 is a key component in the Enhanced Diversity Receiver Chipset (EDRCS) which includes one CLC5903 Dual Digital Tuner / AGC, two CLC5957 12-bit analog-to-digital converters (ADCs), and two CLC5526 digitally controlled variable gain amplifiers (DVGAs). This system allows direct IF sampling of signals up to 300MHz for enhanced receiver performance and reduced system costs.

The CLC5903 is an enhanced replacement for the CLC5902 in the Diversity Receiver Chipset (DRCS). The main improvements relative to the CLC5902 are a 50% increase in maximum sample rate from 52MHz to 78MHz, a 62% reduction in power consumption from 760mW to 290mW, and the added flexibility to independently program filter coefficients in the two channels. A block diagram for a DRCS-based narrowband communications system is shown in Figure 1.

The CLC5903 offers high dynamic range digital tuning and filtering based on hard-wired digital signal processing (DSP) technology. Each channel has independent tuning, phase offset, filter coefficients, and gain settings. Channel filtering is performed by a series of three filters. The first is a 4-stage Cascaded Integrator Comb (CIC) filter with a programmable decimation ratio from 8 to 2048. Next there are two symmetric FIR filters, a 21-tap and a 63-tap, both with independent programmable coefficients. The first FIR filter decimates the data by 2, the second FIR decimates by either 2 or 4. Channel filter bandwidth at 52MSPS ranges from ±650kHz down to ±1.3kHz. At 78MSPS, the maximum bandwidth increases to ±975kHz.

The CLC5903's AGC controller monitors the ADC output and controls the ADC input signal level by adjusting the DVGA setting. AGC threshold, deadband+hysteresis, and the loop time constant are user defined. Total dynamic range of greater than 120dB full-scale signal to noise in a 200kHz bandwidth can be achieved with the Diversity Receiver Chipset.

Features

- 78MSPS Operation
- Low Power, 145mW/channel, 52 MHz, Dec=192
- Two Independent Channels with 14-bit inputs
- Serial Daisy-chain Mode for quad receivers
- Greater than 100 dB image rejection
- Greater than 100 dB spurious free dynamic range
- 0.02 Hz tuning resolution
- User Programmable AGC with enhanced Power Detector
- Channel Filters include a Fourth Order CIC followed by 21-tap and 63-tap Symmetric FIRs
- FIR filters process 21-bit Data with 16-bit Programmable Coefficients
- Two independent FIR coefficient memories which can be routed to either or both channels.
- Flexible output formats include 12-bit Floating Point or 8, 16, 24, and 32 bit Fixed Point
- Serial and Parallel output ports
- JTAG Boundary Scan
- 8-bit Microprocessor Interface
- 128 pin PQFP
- 100% Software compatible with the CLC5902
- Pin compatible with the CLC5902 except for V_{DD} voltage

Applications

- Cellular Basestations
- Satellite Receivers
- Wireless Local Loop Receivers
- Digital Communications

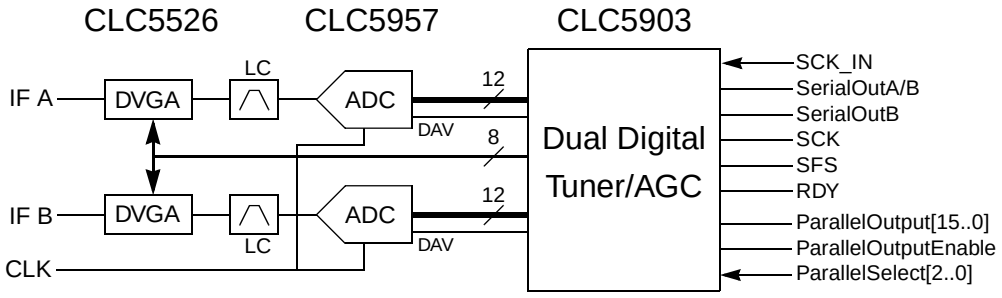


Figure 1. Diversity Receiver Chipset Block Diagram

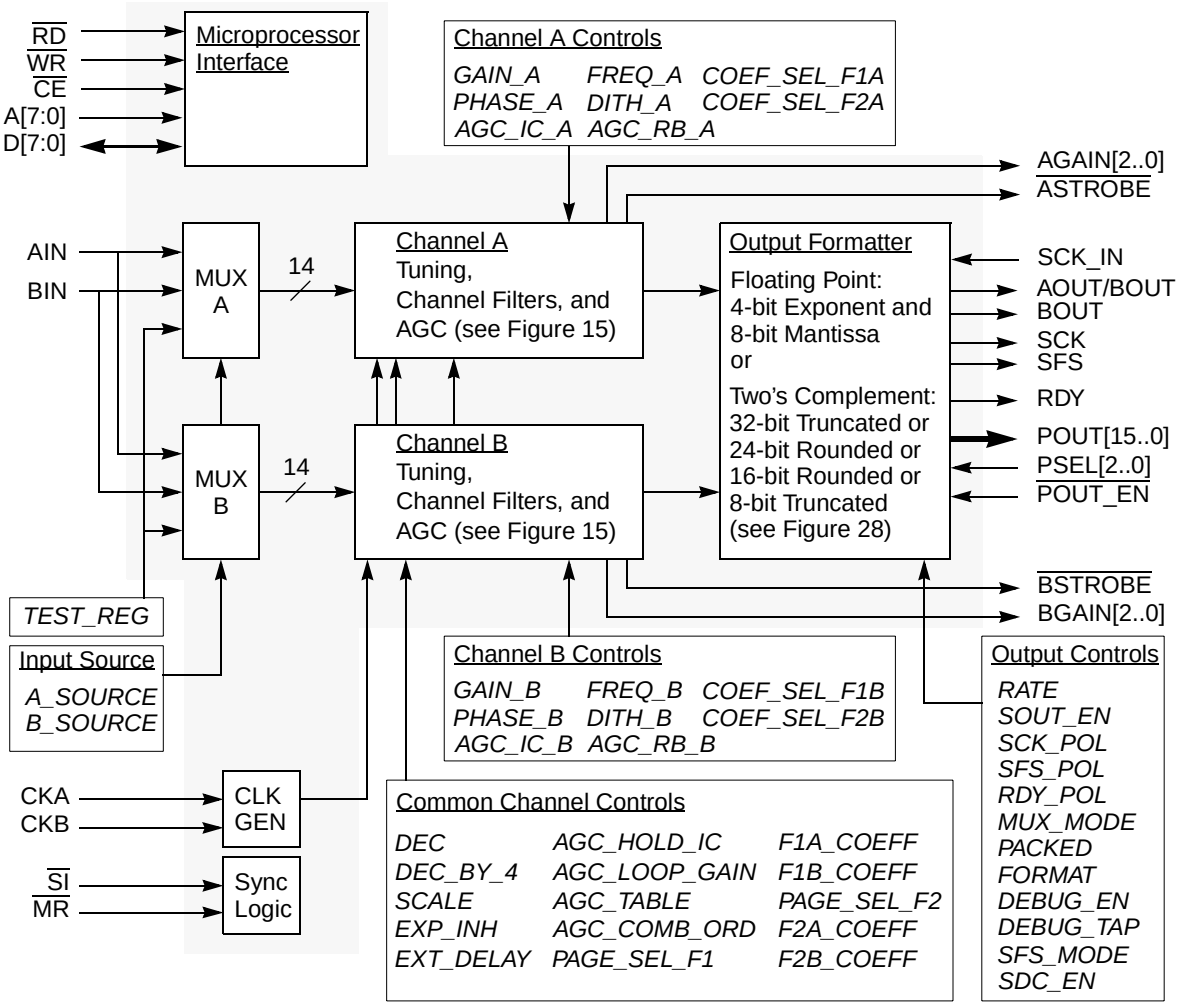


Figure 2. CLC5903 Dual Digital Tuner / AGC Block Diagram with Control Register Associations

Functional Description

The CLC5903 block diagram is shown in Figure 2. The CLC5903 contains two identical digital down-conversion (DDC) circuits. Each DDC accepts an independently clocked 14-bit sample at up to 78MSPS, down converts from a selected carrier frequency to baseband, decimates the signal rate by a programmable factor ranging from 32 to 16384, provides channel filtering, and outputs quadrature symbols.

A crossbar switch enables either of the two inputs or a test register to be routed to either DDC channel. Flexible channel filtering is provided by the two programmable decimating FIR filters. The final filter outputs can be converted to a 12-bit floating point format or standard two's complement format. The output data is available at both serial and parallel ports.

The CLC5903 maintains over 100 dB of spurious free dynamic range and over 100 dB of out-of-band rejection. This allows considerable latitude in channel filter partitioning between the analog and digital domains.

The frequencies, phase offsets, and phase dither of the two sine/cosine numerically controlled oscillators (NCOs) can be independently specified. Two sets of coefficient memories and a crossbar switch allow shared or independent filter coefficients and bandwidth for each channel. Both channels share the same decimation ratio and input/output formats.

Each channel has its own AGC circuit for use with narrowband radio channels where most of the channel filtering precedes the ADC. The AGC closes the loop around the CLC5526 DVGA, compressing the dynamic range of the signal into the ADC. AGC gain compensation in the CLC5903 removes the DVGA gain steps at the output. The time alignment of this gain compensation circuit can be adjusted to support ADCs with different latencies. The AGC can be configured to operate continuously or set to a fixed gain step. The two AGC circuits operate independently but share the same programmed parameters and control signals.

The chip receives configuration and control information over a microprocessor-compatible bus consisting of an 8-bit data I/O port, an 8-bit address port, a chip enable strobe, a read strobe, and a write strobe. The chip's control registers (8 bits each) are memory mapped into the 8-bit address space of the control port. Page select bits allow access to the overlaid A and B set of FIR coefficients.

JTAG boundary scan and on-chip diagnostic circuits are provided to simplify system debug and test.

The CLC5903 supports 3.3V I/O even though the core logic voltage is 1.8V. The CLC5903 outputs swing to the 3.3V rail so they can be directly connected to 5V TTL inputs if desired.

Absolute Maximum Ratings

Positive IO Supply Voltage (V_{DDIO})	-0.3V to 4.2V
Positive CoreSupply Voltage (V_{DD})	-0.3V to 2.4V
Voltage on Any Input or Output Pin	-0.3V to V_{DDIO}+0.5V
Input Current at Any Pin	±25mA
Package Input Current	±50mA
Package Dissipation at T_A=25°C	1W
ESD Susceptibility Human Body Model Machine Model	 2000V 200V
Soldering Temperature, Infrared, 10 seconds	300°C
Storage Temperature	-65°C to 150°C

NOTE: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Operating Ratings

Positive IO Supply Voltage (V_{DDIO})	3.3V ±10%
Positive Core Supply Voltage (V_{DD})	1.8V ±10%
Operating Temperature Range	-40°C to +85°C

Package Thermal Resistance

Package	θja	θjc
128 pin PQFP	39°C/W	20°C/W

Reliability Information

Transistor Count	1.4 million

Ordering Information

Order Code	Temperature Range	Description
CLC5903VLA	-40°C to +85°C	128-pin PQFP (industrial temperature range)

CLC5903 Electrical Characteristics (Note 1)

DC Characteristics

(F_S=78MHz, CIC Decimation=48, F2 Decimation=2; unless specified)

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Voltage input low	-0.5		0.7	V
V_{IH}	Voltage input high	2.3		V_{DDIO}+0.5	V
I_{OZ}	Input current			20	uA
V_{OL}	Voltage output low (I_{OL} = 4mA/16mA, see Note 2)			0.4	V
V_{OH}	Voltage output high (I_{OH} = -4mA/-16mA, see Note 2)	2.4			V
C_{IN}	Input capacitance			5.0	pF

AC Characteristics

(F_S=78MHz, CIC Decimation=48, F2 Decimation=2; unless specified)

Symbol	Parameter (C_L=50pF)	Min	Typ	Max	Units
F_{CK}	Clock (**CKA**|**B**) Frequency (Figure 6)			78	MHz
SFDR	Spurious Free Dynamic Range		-100		dBFS
SNR	Signal to Noise Ratio		-127		dBFS
	Tuning Resolution		0.02		Hz
	Phase Resolution		0.005		°
t_{MRA}	$\overline{\textbf{MR}}$ Active Time (Figure 4)	4			**CK** periods
t_{MRIC}	$\overline{\textbf{MR}}$ Inactive to first Control Port Access (Figure 4)	10			**CK** periods
t_{MRSU}	$\overline{\textbf{MR}}$ Setup Time to **CKA**|**B** (Figure 4)	6			ns
t_{MRH}	$\overline{\textbf{MR}}$ Hold Time to **CKA**|**B** (Figure 4)	2			ns

AC Characteristics (Continued)

(F_S=78MHz, CIC Decimation=48, F2 Decimation=2; unless specified)

Symbol	Parameter (C_L=50pF)	Min	Typ	Max	Units
t_{SISU}	**$\overline{SI}$** Setup Time to **CKA**|**B** (Figure 5)	6			ns
t_{SIH}	**$\overline{SI}$** Hold Time from **CKA**|**B** (Figure 5)	2			ns
t_{SIW}	**$\overline{SI}$** Pulse Width (Figure 5)	4			**CK** periods
t_{CKDC}	**CKA**|**B** duty cycle (Figure 6)	40		60	%
t_{RF}	**CKA**|**B** rise and fall times (V_{IL} to V_{IH}) (Figure 6)			2	ns
t_{SU}	Input setup before **CKA**|**B** goes high (**A**|**BIN**) (Figure 6)	3			ns
t_{HD}	Input hold time after **CKA**|**B** goes high (**A**|**BIN**) (Figure 6)	1			ns
t_{CKL}	Minimum time low for **CK** = **CKA** | **CKB** (Figure 7)	3.1			ns
t_{STIW}	**$\overline{A}$**|**$\overline{BSTROBE}$** Inactive Pulse Width (Figure 8)		2		**CK** period
t_{GSTB}	**A**|**BGAIN** setup before **$\overline{A}$**|**$\overline{BSTROBE}$** (Figure 8)	6			ns
t_{SFSV}	**SCK** to **SFS** Valid (Note 3) (Figure 9)	-1		5	ns
t_{OV}	**SCK** to **A**|**BOUT** Valid (Note 4) (Figure 9)	-1		5	ns
t_{RDYW}	**RDY** Pulse Width (Figure 9)		2		**CK** periods
t_{RDYV}	**SCK** to **RDY** valid (Figure 9)	-1		5	ns
t_{OENV}	**POUT_EN** Active to **POUT[15..0]** Valid (Figure 10)			12	ns
t_{OENT}	**POUT_EN** Inactive to **POUT[15..0]** Tri-State (Figure 10)			10	ns
t_{SELV}	**PSEL[2..0]** to **POUT[15..0]** Valid (Figure 11)			13	ns
t_{POV}	**RDY** to **POUT[15..0]** New Value Valid (Note 5) (Figure 12)			7	ns
t_{JPCO}	Propagation Delay **TCK** to **TDO** (Figure 13)			25	ns
t_{JSCO}	Propagation Delay **TCK** to Data Out (Figure 13)			35	ns
t_{JPDZ}	Disable Time **TCK** to **TDO** (Figure 13)			25	ns
t_{JSDZ}	Disable Time **TCK** to Data Out (Figure 13)			35	ns
t_{JPEN}	Enable Time **TCK** to **TDO** (Figure 13)	0		25	ns
t_{JSEN}	Enable Time **TCK** to Data Out (Figure 13)	0		35	ns
t_{JSSU}	Setup Time Data to **TCK** (Figure 13)	10			ns
t_{JPSU}	Setup Time **TDI**, **TMS** to **TCK** (Figure 13)	10			ns
t_{JSH}	Hold Time Data to **TCK** (Figure 13)	45			ns
t_{JPH}	Hold Time **TCK** to **TDI**, **TMS** (Figure 13)	45			ns
t_{JCH}	**TCK** Pulse Width High (Figure 13)	50			ns
t_{JCL}	**TCK** Pulse Width Low (Figure 13)	40			ns
$JTAG_{FMAX}$	**TCK** Maximum Frequency (Figure 13)			10	MHz
t_{CSU}	Control Setup before the controlling signal goes low (Figure 14)	5			ns
t_{CHD}	Control hold after the controlling signal goes high (Figure 14)	5			ns
t_{CSPW}	Controlling strobe pulse width (Write) (Figure 14)	30			ns
t_{CDLY}	Control output delay controlling signal low to **D** (Read) (Figure 14)			30	ns

AC Characteristics (Continued)

(F_S=78MHz, CIC Decimation=48, F2 Decimation=2; unless specified)

Symbol	Parameter (C_L=50pF)	Min	Typ	Max	Units
t_{CZ}	Control tri-state delay after controlling signal high (Figure 14)			20	ns
I_{DD}	Dynamic Supply Current (F_{CK} =78MHz, N=48, SCK=39MHz)		120	200	mA
I_{DDIO}	Dynamic Supply Current (F_{CK} =78MHz, N=48, SCK=39MHz)		65	100	mA

Note 1: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 2: All output pins provide 16mA output drive except TDO (pin 116) which provides 4mA output drive.

Note 3: t_{SFSV} refers to the rising edge of **SCK** when SCK_POL=0 and the falling edge when SCK_POL=1.

Note 4: t_{OV} refers to the rising edge of **SCK** when SCK_POL=0 and the falling edge when SCK_POL=1.

Note 5: t_{RDYV} refers to the rising edge of **RDY** when RDY_POL=0 and the falling edge when RDY_POL=1.

CLC5903VLA Pinout

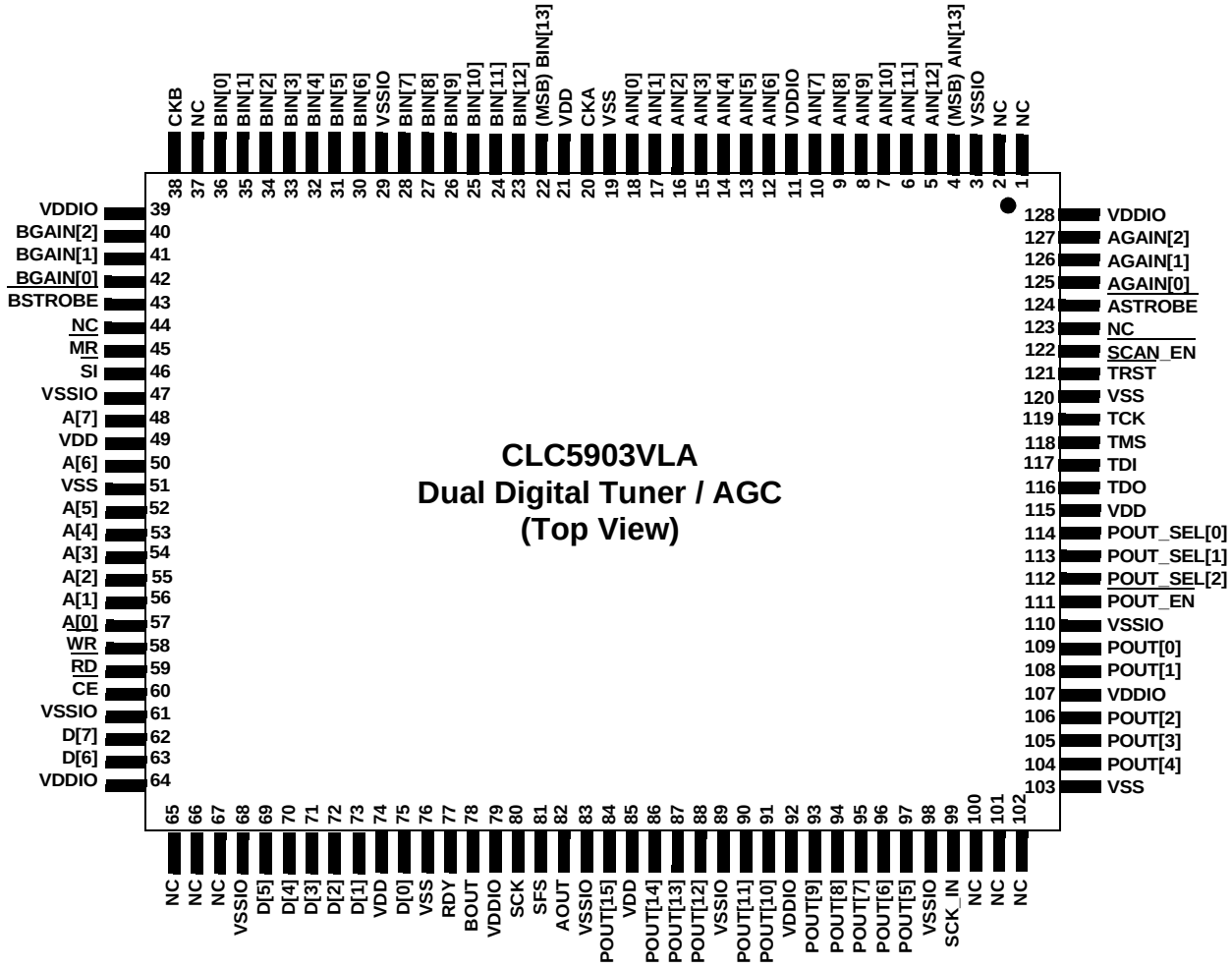


Figure 3. CLC5903VLA PQFP Pinout

Pin Descriptions

Signal	Pin	Description
$\overline{MR}$	45	MASTER RESET, *Active low* Resets all registers within the chip. **$\overline{ASTROBE}$** and **$\overline{BSTROBE}$** are asserted during **$\overline{MR}$**.
AIN[13:0], BIN[13:0]	4:10,12:18 22:28,30:36	INPUT DATA, *Active high* 2's complement input data. **AIN[13]** and **BIN[13]** are the MSBs. The data is clocked into the chip on the rising edge of the corresponding clock (**CKA**, **CKB**). The CLC595X connects directly to these input pins with no additional logic. Tie unused input bits low.
AOUT BOUT	82 78	SERIAL OUTPUT DATA, *Active high* The 2's complement serial output data is transmitted on these pins, MSB first. The output bits change on the rising edge of **SCK** (falling edge if SCK_POL=1) and should be captured on the falling edge of **SCK** (rising if SCK_POL=1). These pins are tri-stated at power up and are enabled by the SOUT_EN control register bit. See Figure 9 and Figure 29 timing diagrams. In Debug Mode **AOUT**=**DEBUG[1]**, **BOUT**=**DEBUG[0]**.
AGAIN[2:0], BGAIN[2:0]	125:127 40:42	OUTPUT DATA TO DVGA, *Active high* 3 bit bus that sets the gain of the DVGA determined by the AGC circuit.
$\overline{ASTROBE}$, $\overline{BSTROBE}$	124 43	DVGA STROBE, Active low Strobes the data into the DVGA. See Figure 8 and Figure 34 timing diagrams.
SCK	80	SERIAL DATA CLOCK, *Active high or low* The serial data is clocked out of the chip by this clock. The active edge of the clock is user programmable. This pin is tri-stated at power up and is enabled by the SOUT_EN control register bit. See Figure 9 and Figure 29 timing diagrams. In Debug Mode outputs an appropriate clock for the debug data. If RATE=0 the input **CK** duty cycle will be reflected to **SCK**.
SCK_IN	99	SERIAL DATA CLOCK INPUT, *Active high or low* Data bits from a serial daisy-chain slave are clocked into a serial daisy-chain master on the falling edge of **SCK_IN** (rising if SCK_POL=1 on the slave). Tie low if not used.
SFS	81	SERIAL FRAME STROBE, *Active high or low* The serial word strobe. This strobe delineates the words within the serial output streams. This strobe is a pulse at the beginning of each serial word (PACKED=0) or each serial word I/Q pair (PACKED=1). The polarity of this signal is user programmable. This pin is tri-stated at power up and is enabled by the SOUT_EN control register bit. See Figure 9 and Figure 29 timing diagrams. In Debug Mode **SFS**=**DEBUG[2]**.
POUT[15:0]	84,86:88,90,91, 93:97,104:106, 108,109	PARALLEL OUTPUT DATA, *Active high* The output data is transmitted on these pins in parallel format. The **POUT_SEL[2..0]** pins select one of eight 16-bit output words. The **POUT_EN** pin enables these outputs. **POUT[15]** is the MSB. In Debug Mode **POUT[15..0]**=**DEBUG[19..4]**.
POUT_SEL[2:0]	112:114	PARALLEL OUTPUT DATA SELECT, *Active high* The 16-bit output word is selected with these 3 pins according to Table 2. Not used in Debug Mode. For a serial daisy-chain master, **POUT_SEL[2:0]** become inputs from the slave: **POUT_SEL[2]**=**SFS**$_{SLAVE}$, **POUT_SEL[1]**=**BOUT**$_{SLAVE}$, and **POUT_SEL[0]**=**AOUT**$_{SLAVE}$. Tie low if not used.
$\overline{POUT\_EN}$	111	PARALLEL OUTPUT ENABLE. *Active low* This pin enables the chip to output the selected output word on the **POUT[15:0]** pins. Not used in Debug Mode. Tie high if not used.
RDY	77	READY FLAG, *Active high or low* The chip asserts this signal to identify the beginning of an output sample period (OSP). The polarity of this signal is user programmable. This signal is typically used as an interrupt to a DSP chip, but can also be used as a start pulse to dedicated circuitry. This pin is active regardless of the state of SOUT_EN. In Debug Mode **RDY**=**DEBUG[3]**.
CKA, CKB	20, 38	INPUT CLOCK. *Active high* The clock inputs to the chip. The corresponding **AIN** and **BIN** signals are clocked into the chip on the rising edge of this signal. **CKA** and **CKB** are OR'd together on chip to create the **CK** signal. **$\overline{SI}$** is clocked into the chip on the rising edge of **CK**. Tie low if not used.
$\overline{SI}$	46	SYNC IN. *Active low* The sync input to the chip. The decimation counters, dither, and NCO phase can be synchronized by **SI**. This sync is clocked into the chip on the rising edge of **CK** (**CK** = **CKA** + **CKB**). Tie this pin high if external sync is not required. All sample data is flushed by **$\overline{SI}$**. To properly initialize the DVGA **$\overline{ASTROBE}$** and **$\overline{BSTROBE}$** are asserted during **$\overline{SI}$**.

Pin Descriptions (Continued)

Signal	Pin	Description
D[7:0]	62,63,69:73,75	DATA BUS. *Active high* This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive output data on these pins when **$\overline{\text{CE}}$** is low, **$\overline{\text{RD}}$** is low, and **$\overline{\text{WR}}$** is high.
A[7:0]	48,50,52:57	ADDRESS BUS. *Active high* These pins are used to address the control registers within the chip. Each of the control registers within the chip are assigned a unique address in a flat address space. A control register can be written to or read from by setting **A[7:0]** to the register's address.
$\overline{\text{RD}}$	59	READ ENABLE. *Active low* This pin enables the chip to output the contents of the selected register on the **D[7:0]** pins when **$\overline{\text{CE}}$** is also low.
$\overline{\text{WR}}$	58	WRITE ENABLE. *Active low* This pin enables the chip to write the value on the **D[7:0]** pins into the selected register when **$\overline{\text{CE}}$** is also low. This pin can also function as **RD/$\overline{\text{WR}}$** if **RD** is held low.
$\overline{\text{CE}}$	60	CHIP ENABLE. *Active low* This control strobe enables the read or write operation. The contents of the register selected by **A[7:0]** will be output on **D[7:0]** when **$\overline{\text{RD}}$** is low and **$\overline{\text{CE}}$** is low. If **$\overline{\text{WR}}$** is low and **$\overline{\text{CE}}$** is low, then the selected register will be loaded with the contents of **D[7:0]**.
TDO	116	TEST DATA OUT. *Active high*
TDI	117	TEST DATA IN. *Active high with pull-up*
TMS	118	TEST MODE SELECT. *Active high with pull-up*
TCK	119	TEST CLOCK. *Active high*. Tie low if JTAG is not used.
$\overline{\text{TRST}}$	121	TEST RESET. *Active low with pull-up* Asynchronous reset for TAP controller. Tie low or to **$\overline{\text{MR}}$** if JTAG is not used.
$\overline{\text{SCAN\_EN}}$	122	SCAN ENABLE. *Active low with pull-up* Enables access to internal scan registers. Tie high. Used for manufacturing test only!
VSS	19,51,76, 103,120	Core Ground. Quantity 5.
VDD	21,49,74, 85,115	Core Power, 1.8V. Quantity 5.
VSSIO	3,29,47,61,68, 83,89,98,110	I/O Ground. Quantity 9.
VDDIO	11,39,64,79, 92,107,128	I/O Power, 3.3V. Quantity 7.

Timing Diagrams

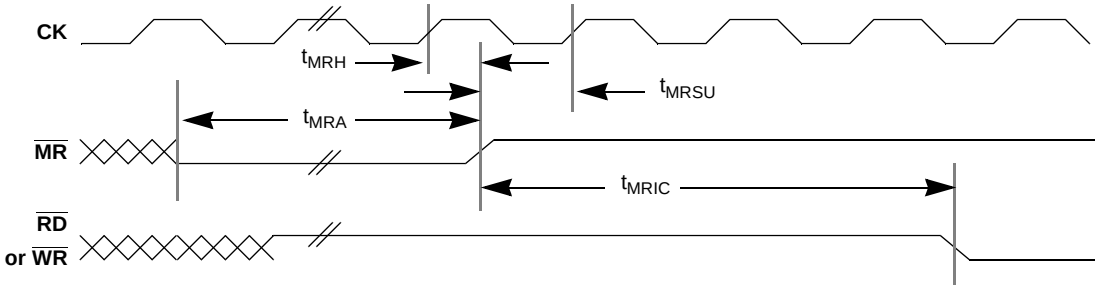


Figure 4. CLC5903 Master Reset Timing

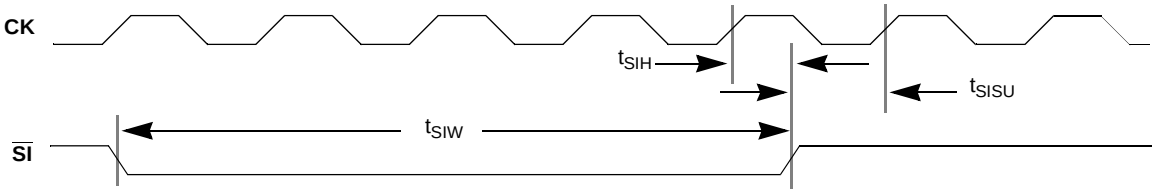
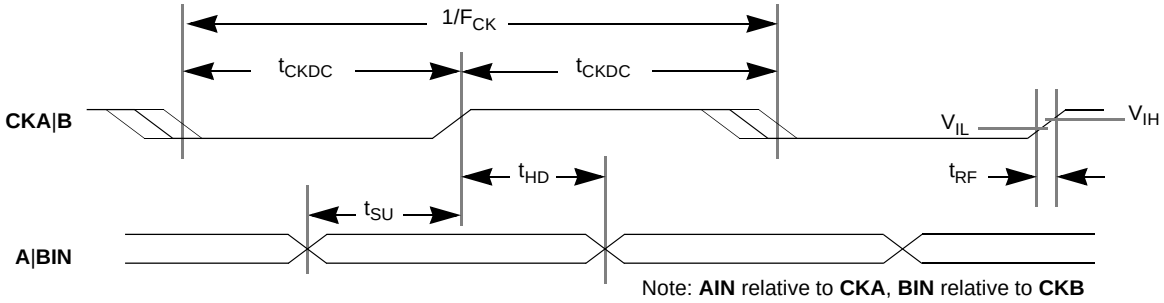
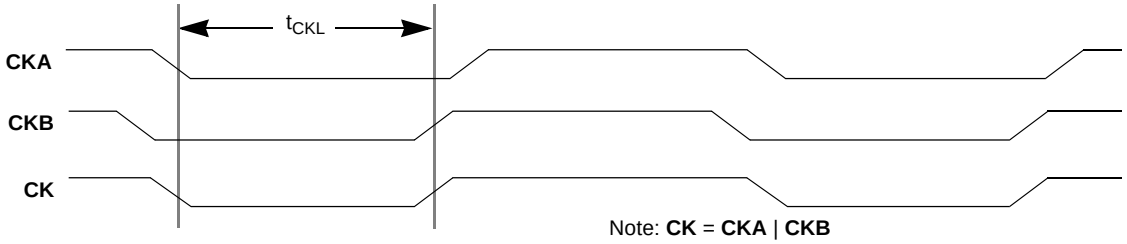


Figure 5. CLC5903 Synchronization Input ($\overline{SI}$) Timing



Note: **AIN** relative to **CKA**, **BIN** relative to **CKB**

Figure 6. CLC5903 ADC Input and Clock Timing



Note: **CK** = **CKA** | **CKB**

Figure 7. CLC5903 CKA vs. CKB Timing

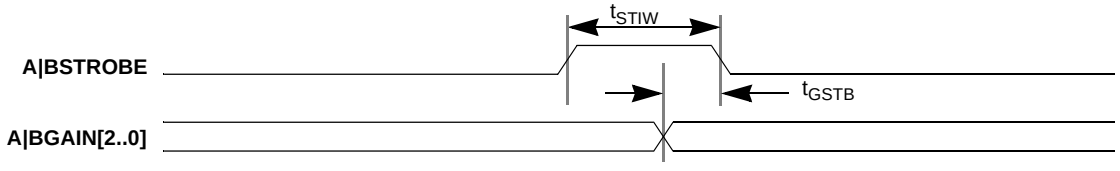


Figure 8. CLC5903 DVGA Interface Timing

Timing Diagrams (Continued)

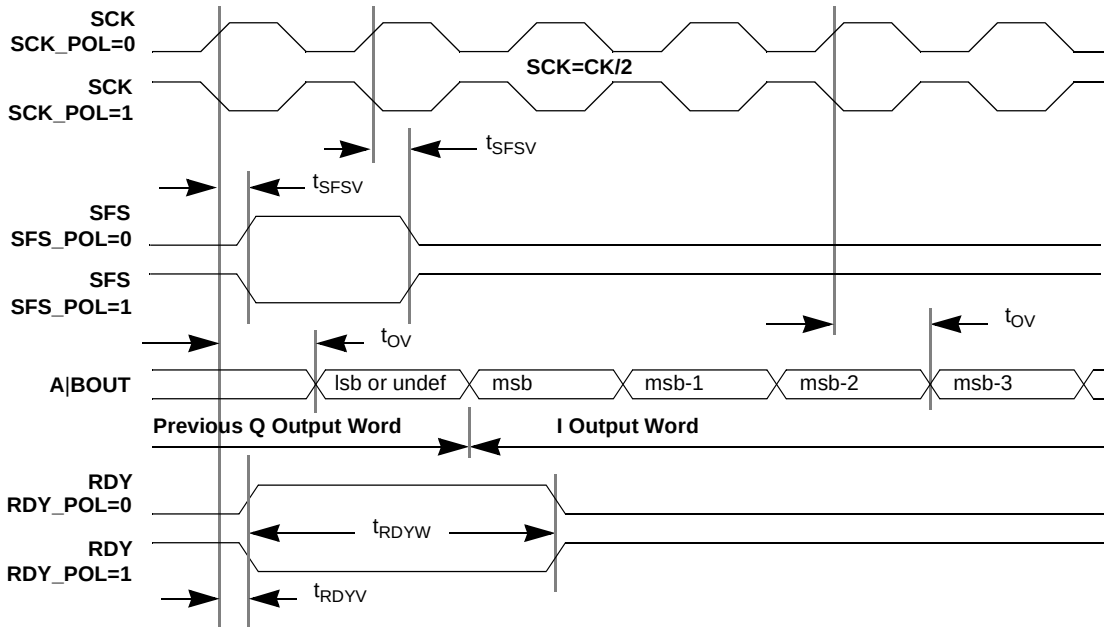


Figure 9. CLC5903 Serial Port Timing

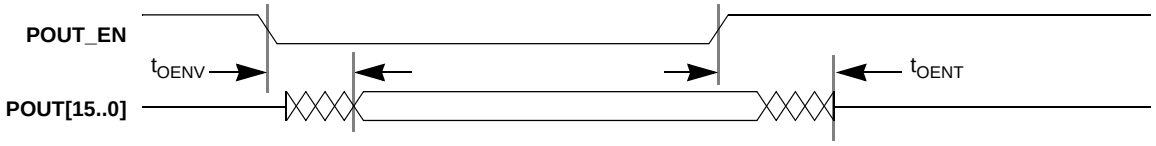


Figure 10. CLC5903 Parallel Output Enable Timing

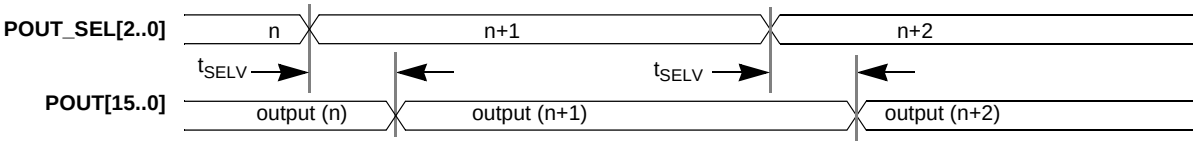


Figure 11. CLC5903 Parallel Output Select Timing

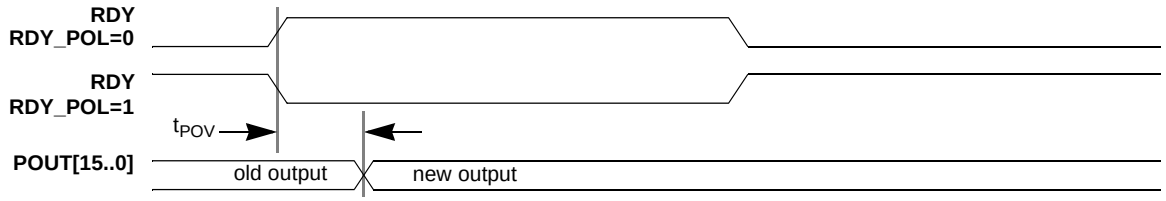


Figure 12. CLC5903 Parallel Output Data Ready Timing

Timing Diagrams (Continued)

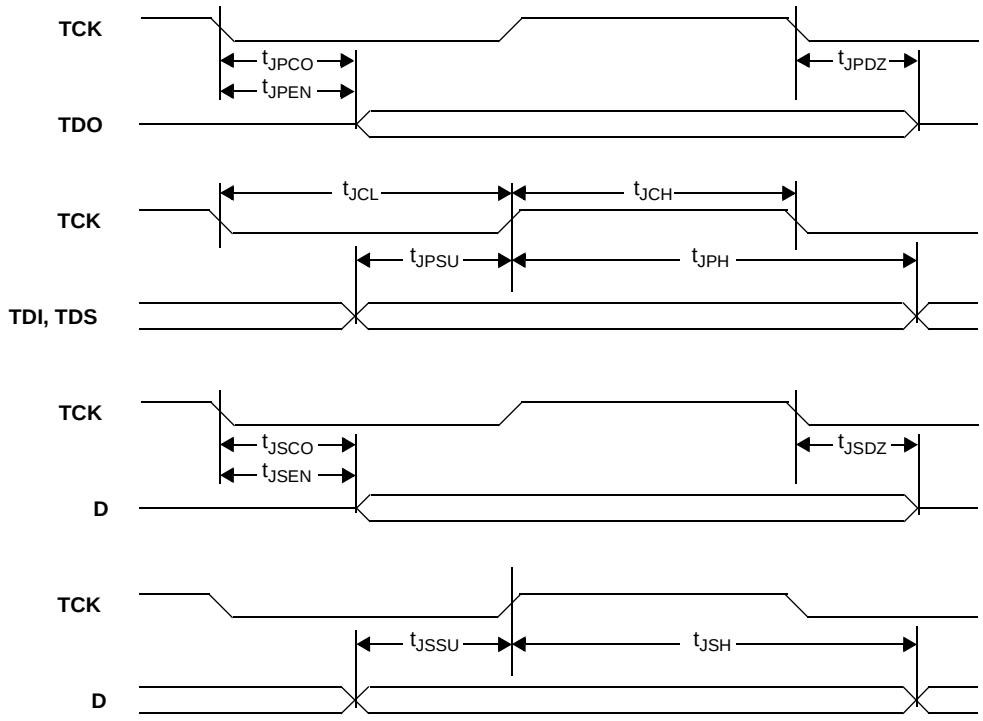


Figure 13. CLC5903 JTAG Port Timing

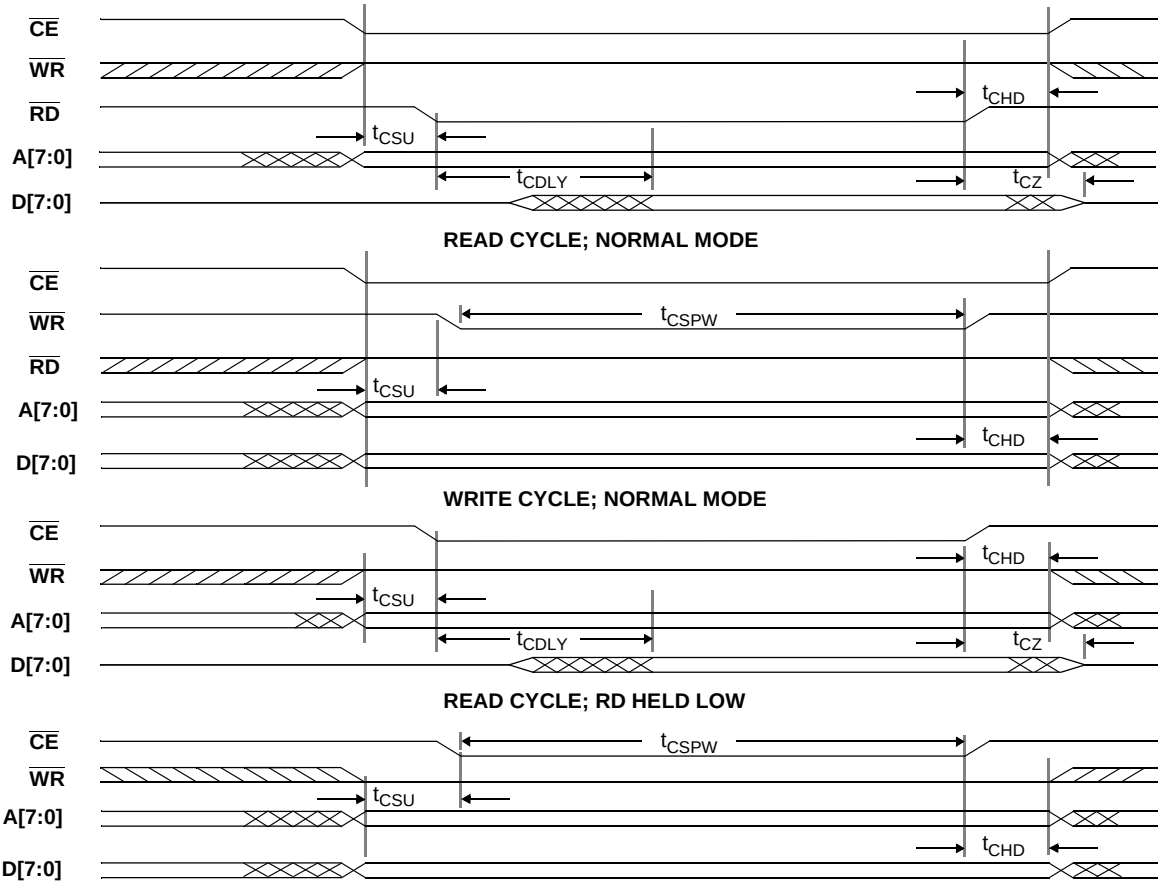


Figure 14. CLC5903 Control I/O Timing

Detailed Description

Control Interface

The CLC5903 is configured by writing control information into 148 control registers within the chip. The contents of these control registers and how to use them are described under *Control Register Addresses and Defaults* on page 20. The registers are written to or read from using the **D[7:0]**, **A[7:0]**, **$\overline{CE}$**, **$\overline{RD}$** and **$\overline{WR}$** pins (see Table for pin descriptions). This interface is designed to allow the CLC5903 to appear to an external processor as a memory mapped peripheral. See Figure 14 for details.

The control interface is asynchronous with respect to the system clock, **CK** (**CK** = **CKA** + **CKB**). This allows the registers to be written or read at any time. In some cases this might cause an invalid operation since the interface is not internally synchronized. In order to assure correct operation, **$\overline{SI}$** must be asserted after the control registers are written.

The **D[7:0]**, **A[7:0]**, **$\overline{WR}$**, **$\overline{RD}$** and **$\overline{CE}$** pins should not be driven above the positive supply voltage.

Master Reset

A master reset pin, **$\overline{MR}$**, is provided to initialize the CLC5903 to a known condition and should be strobed after power up. This signal will clear all sample data and all user programmed data (filter coefficients and AGC settings). All outputs will be disabled (tri-stated). **$\overline{ASTROBE}$** and **$\overline{BSTROBE}$** will be asserted to initialize the DVGA values. *Control Register Addresses and Defaults* on page 20 describes the control register default values.

Synchronizing Multiple CLC5903 Chips

A system containing two or more CLC5903 chips will need to be synchronized if coherent operation is desired. To synchronize multiple CLC5903 chips, connect all of the sync input pins together so they can be driven by a common sync strobe. Synchronization occurs on the rising edge of **CKA|B** when **$\overline{SI}$** goes back high. When **$\overline{SI}$** is asserted all sample data will be flushed immediately, the numerically controlled oscillator (NCO) phase offset will be initialized, the NCO dither generators will be reset, and the CIC decimation ratio will be initialized. Only the configuration data loaded into the microprocessor interface remains unaffected.

$\overline{SI}$ may be held low as long as desired after a minimum of 4 **CK** periods.

Input Source

The input crossbar switch allows either **AIN**, **BIN**, or a test register to be routed to the channel A or channel B AGC/DDC. The AGC outputs, **AGAIN** and **BGAIN**, are not switched. If **AIN** and **BIN** are exchanged the AGC loop will be open and the AGCs will not function properly. **AIN** and **BIN** should meet the timing requirements shown in Figure 6.

Selecting the test register as the input source allows the AGC or DDC operation to be verified with a known input. See the test and diagnostics section for further discussion.

Down Converters

A detailed block diagram of each DDC channel is shown in Figure 15. Each down converter uses a complex NCO and mixer to quadrature downconvert a signal to baseband. The "FLOAT TO FIXED CONVERTER" treats the 15-bit mixer output as a mantissa and the AGC output, **EXP**, as a 3-bit exponent. It performs a bit shift on the data based on the value of **EXP**. This bit shifting is used to expand the compressed dynamic range resulting from the DVGA operation. The DVGA gain is adjusted in 6dB steps which are equivalent to each digital bit shift.

Digitally compensating for the DVGA gain steps in the CLC5903 causes the DDC output to be linear with respect to the DVGA input. The AGC operation will be completely transparent at the CLC5903 output.

The exponent (**EXP**) can be forced to its maximum value by setting the EXP_INH bit. If $x_{in}(n)$ is the DDC input, the signal after the "FLOAT TO FIXED CONVERTER" is

$$x_3(n) = x_{in}(n) \bullet \cos(\omega n) \bullet 2^{EXP} \qquad (1)$$

for the I component. Changing the 'cos' to 'sin' in this equation will provide the Q component.

The "FLOAT TO FIXED CONVERTER" circuit expands the dynamic range compression performed by the DVGA. Signals from this point onward extend across the full dynamic range of the signals applied to the DVGA input. This allows the AGC to operate continuously through a burst without producing artifacts in the signal due to the settling response of the decimation filters after a 6dB DVGA gain adjustment. For example, if the DVGA input signal were to increase causing the ADC output level to cross the AGC threshold level, the gain of the DVGA would change by -6dB. The 6dB step is allowed to propagate through the ADC and mixers and is compensated out just before the filtering. The accuracy of

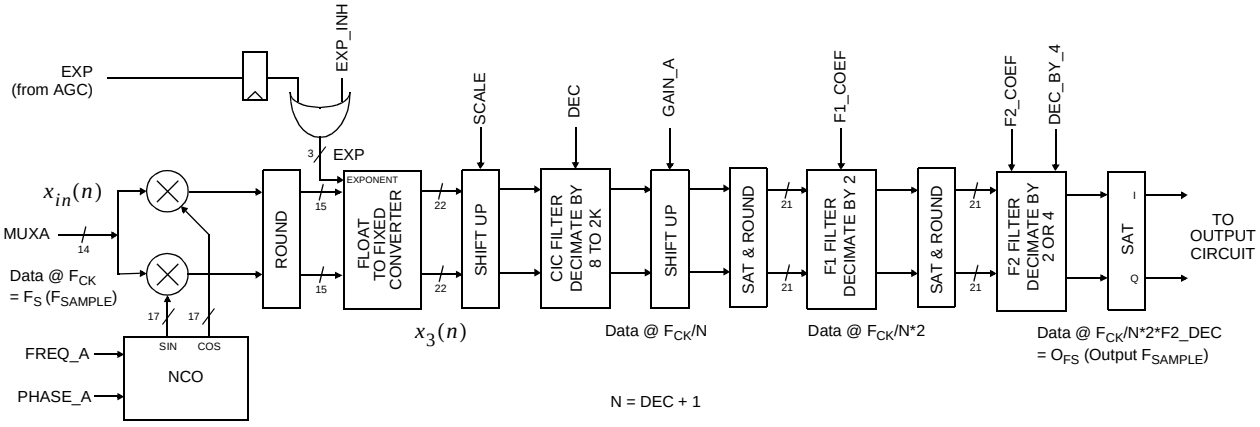


Figure 15. CLC5903 Down Converter, Channel A (Channel B is identical)

Detailed Description (Continued)

the compensation is dependent on timing and the accuracy of the DVGA gain step. The CLC5903 allows the timing of the gain compensation to be adjusted in the EXT_DELAY register. This operating mode requires 21 bits (14-bit ADC output + 7-bit shift) to represent the full linear dynamic range of the signal. The output word must be set to either 24-bit or 32-bit to take advantage of the entire dynamic range available. The CLC5903 can also be configured to output a floating point format with up to 138dB of numerical resolution using only 12 output bits.

The “SHIFT UP” circuit will be discussed in the Four Stage CIC filter section on page 13.

A 4-stage cascaded-integrator-comb (CIC) filter and a two-stage decimate by 4 or 8 finite impulse response (FIR) filter are used to lowpass filter and isolate the desired signal. The CIC filter reduces the sample rate by a programmable factor ranging from 8 to 2048 (decimation ratio). The CIC outputs are followed by a gain stage and then followed by a two-stage decimate by 4 or 8 filter. The gain circuit allows the user to boost the gain of weak signals by up to 42 dB in 6 dB steps. It also rounds the signal to 21 bits and saturates at plus or minus full scale.

The first stage of the two stage filter is a 21-tap, symmetric decimate by 2 FIR filter (F1) with programmable 16 bit tap weights. The coefficients of the first 11 taps are downloaded to the chip as 16 bit words. Since the filter is a symmetric configuration only the first 11 coefficients must be loaded. The F1 section on page 14 provides a generic set of coefficients that compensate for the rolloff of the CIC filter and provide a passband flat to 0.01dB with 70 dB of out of band rejection. A second coefficient set is provided that has a narrower output passband and greater out-of-band rejection. The second set of coefficients is ideal for systems such as GSM where far-image rejection is more important than adjacent channel rejection.

The second stage is a 63 tap decimate by 2 or 4 programmable FIR filter (F2) also with 16 bit tap weights. Filter coefficients for a flat response from $-0.4F_S$ to $+0.4F_S$ of the output sample rate with 80dB of out of band rejection are provided in the F2 section. A second set of F2 coefficients is also provided to enhance performance for GSM systems. The user can also design and download their own final filter to customize the channel’s spectral response. Typical uses of programmable filter F2 include matched (root-raised cosine) filtering, or filtering to generate oversampled outputs with greater out of band rejection. The 63 tap symmetrical filter is downloaded into the chip as 32 words, 16 bits each. Saturation to plus or minus full scale is performed at the output of F1 and F2 to clip the signal rather than allow it to roll over.

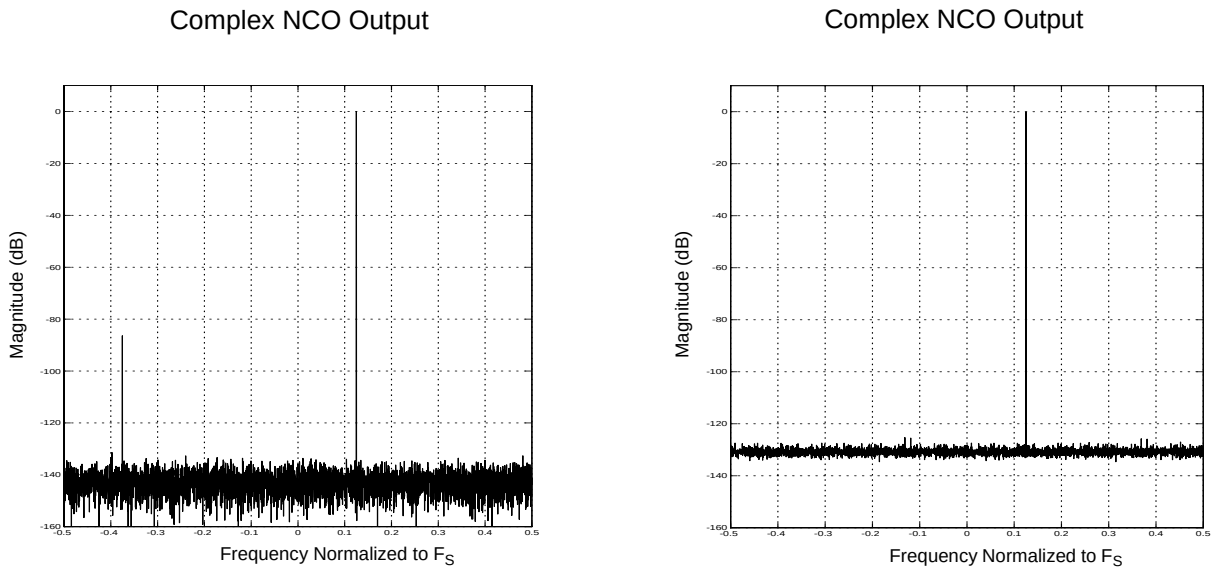
The CLC5903 provides two sets of coefficient memory for both F1 and F2. These coefficient memories can be independently routed to channel A, channel B, or both channel A and B with a crossbar switch. The coefficients can be switched on the fly but some time will be required before valid output data is available.

The Numerically Controlled Oscillator

The tuning frequency of each down converter is specified as a 32 bit word (.02Hz resolution at **CK**=52MHz) and the phase offset is specified as a 16 bit word (.005°). These two parameters are applied to the Numerically Controlled Oscillator (NCO) circuit to generate sine and cosine signals used by the digital mixer. The NCOs can be synchronized with NCOs on other chips via the sync pin $\overline{\textbf{SI}}$. This allows multiple down converter outputs to be coherently combined, each with a unique phase and amplitude.

The tuning frequency is set by loading the FREQ register according to the formula $FREQ = 2^{32}F/F_{CK}$, where F is the desired tuning frequency and F_{CK} is the chip’s clock rate. FREQ is a 2’s complement word. The range for F is from $-F_{CK}/2$ to $+F_{CK}(1-2^{-31})/2$.

In some cases the sampling process causes the order of the I and Q components to be reversed. Should this occur simply invert the polarity of the tuning frequency F.



(a) Before Phase Dithering (b) After Phase Dithering

Figure 16. Example of NCO spurs due to phase truncation

Detailed Description (Continued)

The 2's complement format represents full-scale negative as 10000000 and full-scale positive as 01111111 for an 8-bit example.

The 16 bit phase offset is set by loading the PHASE register according to the formula PHASE = $2^{16}P/2\pi$, where P is the desired phase in radians ranging between 0 and 2π. PHASE is an unsigned 16-bit number. P ranges from 0 to $2\pi(1-2^{-16})$.

Phase dithering can be enabled to reduce the spurious signals created by the NCO due to phase truncation. This truncation is unavoidable since the frequency resolution is much finer than the phase resolution. With dither enabled, spurs due to phase truncation are below -100 dBc for all frequencies and phase offsets. Each NCO has its own dither source and the initial state of one is maximally offset with respect to the other so that they are effectively uncorrelated. The phase dither sources are on by default. They are independently controlled by the DITH_A and DITH_B bits. The amplitude resolution of the ROM creates a worst-case spur amplitude of -101dBc rendering amplitude dither unnecessary.

The spectrum plots in Figure 16 show the effectiveness of phase dither in reducing NCO spurs due to phase truncation for a worst-case example (just below $F_S/8$). With dither off, the spur is at -86.4dBFS. With dither on, the spur is below -125dBFS, disappearing into the noise floor. This spur is spread into the noise floor which results in an SNR of -83.6dBFS. The channel filter's processing gain will further improve the SNR.

Figure 17 shows the spur levels as the tuning frequency is scanned over a narrow portion of the frequency range. The spurs are again a result of phase quantization but their locations move about as the frequency scan progresses. As before, the peak spur level drops when dithering is enabled. When dither is enabled and the fundamental frequency is exactly at $F_S/8$, the worst-case spur due to amplitude quantization can be observed at -101dBc in Figure 18.

Four Stage CIC Filter

The mixer outputs are decimated by a factor of N in a four stage CIC filter. N is programmable to any integer between 8 and 2048. Decimation is programmed in the DEC register where DEC = N - 1. The programmable decimation allows the chip's usable output bandwidth to range from about 2.6kHz to 1.3MHz when the input data rate (which is equal to the chip's clock rate, F_{CK}) is 52 MHz. For the maximum sample rate of 78MHz, the CLC5903's output bandwidth will range from about 4.76kHz to 1.95MHz. A block diagram of the CIC filter is shown in Figure 19.

The CIC filter is primarily used to decimate the high-rate incoming data while providing a rough lowpass characteristic. The lowpass filter will have a sin(x)/x response (similar to the AGC's CIC shown in Figure 35 on page 23) where the first null is at F_S/N.

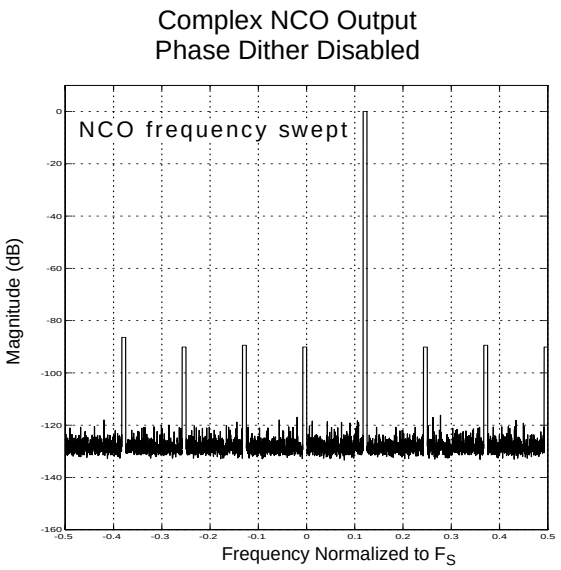


Figure 17. NCO Spurs due to Phase Quantization

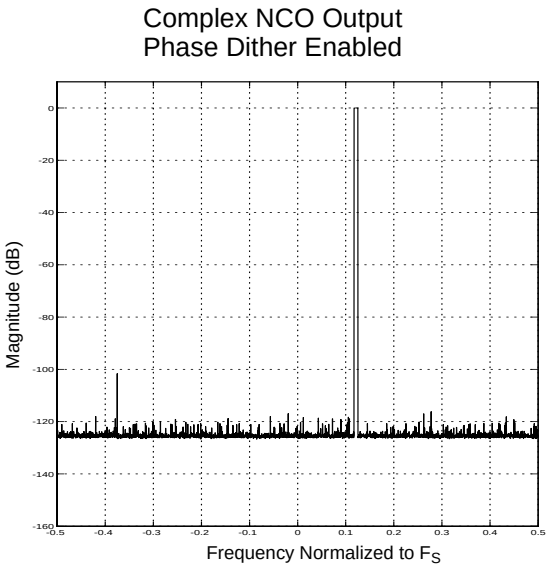


Figure 18. Worst Case Amplitude Spur, NCO at $F_S/8$

The CIC filter has a gain equal to N^4 (filter decimation^4) which must be compensated for in the "SHIFT UP" circuit shown in Figure 19 as well as Figure 15. This circuit has a gain equal to $2^{(SCALE-44)}$, where SCALE ranges from 0 to 40. This circuit divides the input signal by 2^{44} providing maxi-

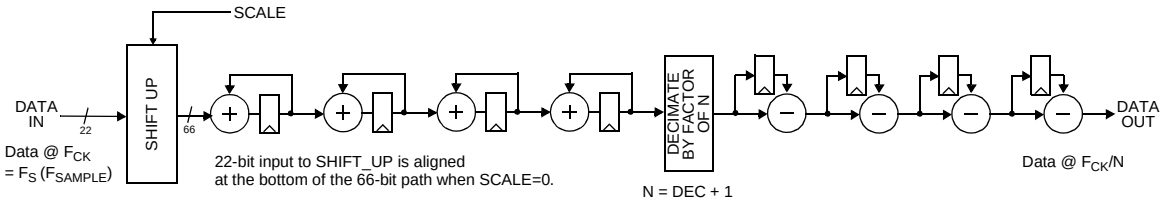


Figure 19. Four-stage decimate by N CIC filter

Detailed Description (Continued)

mum headroom through the CIC filter. For optimal noise performance the SCALE value is set to increase this level until the CIC filter is just below the point of distortion. A value is normally calculated and loaded for SCALE such that $GAIN_{SHIFTUP} \cdot GAIN_{CIC} \leq 1$. The actual gain of the CIC filter will only be unity for power-of-two decimation values. In other cases the gain will be somewhat less than unity.

Channel Gain

The gain of each channel can be boosted up to 42 dB by shifting the output of the CIC filter up by 0 to 7 bits prior to rounding it to 21 bits. For channel A, the gain of this stage is: $GAIN = 2^{GAIN\_A}$, where GAIN_A ranges from 0 to 7. Overflow due to the GAIN circuit is saturated (clipped) at plus or minus full scale. Each channel can be given its own GAIN setting.

First Programmable FIR Filter (F1)

The CIC/GAIN outputs are followed by two stages of filtering. The first stage is a 21 tap decimate-by-2 symmetric FIR filter with programmable coefficients. Typically, this filter compensates for a slight droop induced by the CIC filter while removing undesired alias images above Nyquist. In addition, it often provides stopband assistance to F2 when deep stop bands are required. The filter coefficients are 16-bit 2's complement numbers. Unity gain will be achieved through the filter if the sum of the 21 coefficients is equal to 2^{16}. If the sum is not 2^{16}, then F1 will introduce a gain equal to (sum of coefficients)/2^{16}. The 21 coefficients are identified as coefficients $h_1(n),\ n = 0, \ldots, 20$ where $h_1(10)$ is the center tap. The coefficients are symmetric, so only the first 11 are loaded into the chip.

Two example sets of coefficients are provided here. The first set of coefficients, referred to as the standard set (STD), compensates for the droop of the CIC filter providing a passband which is flat (0.01 dB ripple) over 95% of the final output bandwidth with 70dB of out-of-band rejection (see Figure 20). The filter has a gain of 0.999 and is symmetric with the following 11 unique taps (1|21, 2|20, ..., 10|12, 11):

29, -85, -308, -56, 1068, 1405, -2056, -6009,
1303, 21121, 32703

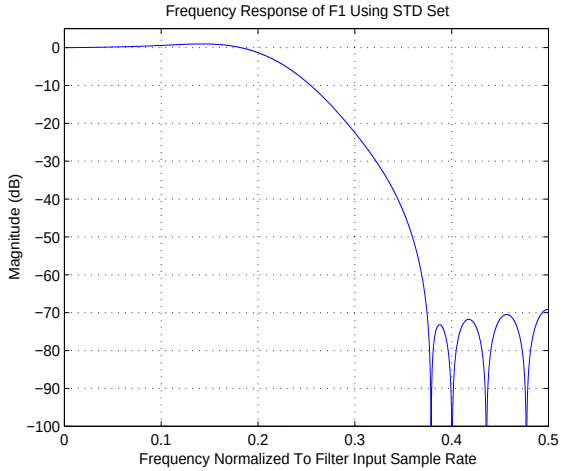


Figure 20. F1 STD frequency response

The second set of coefficients (GSM set) are intended for applications that need deeper stop bands or need oversampled outputs. These requirements are common in cellular systems where out of band rejection requirements can exceed 100dB (see Figure 21). They are useful for wideband radio architectures where the channelization is done after the ADC. These filter coefficients introduce a gain of 0.984 and are:

-49, -340, -1008, -1617, -1269, 425, 3027, 6030,
9115, 11620, 12606

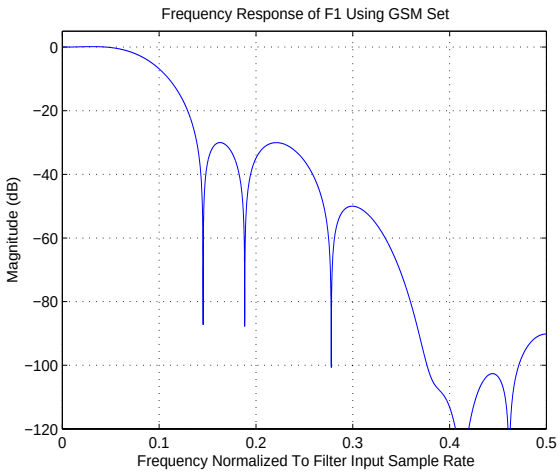


Figure 21. F1 GSM frequency response

Second Programmable FIR Filter (F2)

The second stage decimate by two or four filter also uses externally downloaded filter coefficients. F2 determines the final channel filter response. The filter coefficients are 16-bit 2's complement numbers. Unity gain will be achieved through the filter if the sum of the 63 coefficients is equal to 2^{16}. If the sum is not 2^{16}, then the F2 will introduce a gain equal to (sum of coefficients)/2^{16}.

The 63 coefficients are identified as $h_2(n),\ n = 0,\ldots,62$ where $h_2(31)$ is the center tap. The coefficients are symmetric, so only the first 32 are loaded into the chip.

An example filter (STD F2 coefficients, see Figure 22) with 80dB out-of-band rejection, gain of 1.00, and 0.03 dB peak to peak passband ripple is created by this set of 32 unique coefficients:

-14, -20, 19, 73, 43, -70, -82, 84, 171, -49, -269,
-34, 374, 192, -449,

-430, 460,751, -357, -1144, 81, 1581, 443, -2026,
-1337, 2437, 2886,

-2770, -6127, 2987, 20544, 29647

A second set of F2 coefficients (GSM set, see Figure 23) suitable for meeting the stringent wideband GSM requirements with a gain of 0.999 are:

-536, -986, 42, 962, 869, 225, 141, 93, -280,
-708, -774, -579, -384,

-79, 536, 1056, 1152, 1067, 789, 32, -935, -1668,
-2104, -2137, -1444,

71, 2130, 4450, 6884, 9053, 10413, 10832

The filter coefficients of both filters can be used to tailor the spectral response to the user's needs. For example, the first can be loaded with the standard set to provide a flat

Detailed Description (Continued)

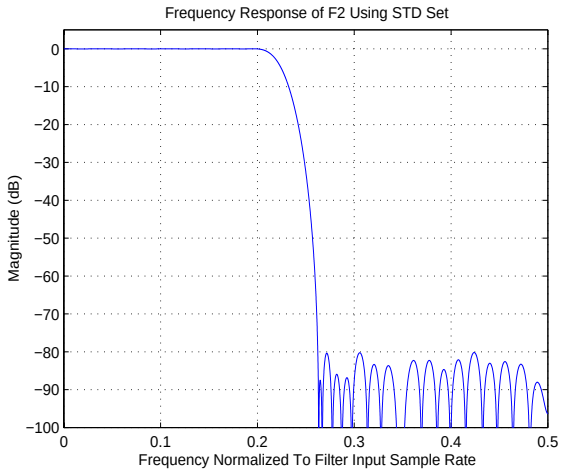


Figure 22. F2 STD frequency response

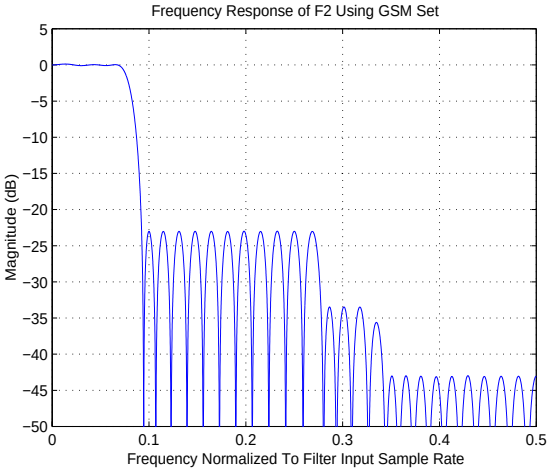


Figure 23. F2 GSM frequency response

response through to the second filter. The latter can then be programmed as a Nyquist (typically a root-raised-cosine) filter for matched filtering of digital data.

The complete channel filter response for standard coefficients is shown in Figure 24. Passband flatness is shown in Figure 25. The complete filter response for GSM coefficients is shown in Figure 26. GSM Passband flatness is shown in Figure 27.

The mask shown in Figure 26 is derived from the ETSI GSM 5.05 specifications for a normal Basestation Transceiver (BTS). For interferers, 9dB was added to the carrier to interference (C/I) ratios. For blockers, 9dB was added to the difference between the blocker level and 3dB above the reference sensitivity level.

Channel Bandwidth vs. Sample Rate

When the CLC5903 is used for GSM systems, a bandwidth of about 200kHz is desired. With a sample rate of 52MHz, the total decimation of 192 provides the desired 270.833kHz output sample rate. This output sample rate in combination with the FIR filter coefficients create the desired channel bandwidth. If the sample rate is increased to 65MHz, the decimation must also be increased to 65MHz/270.833kHz or 240. This new decimation rate will maintain the same output

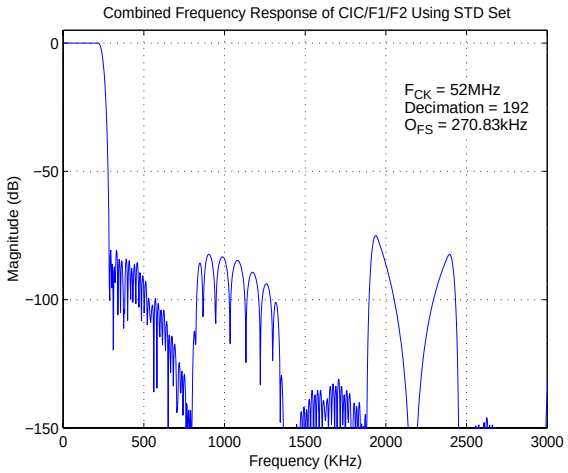


Figure 24. CIC, F1, & F2 STD frequency response

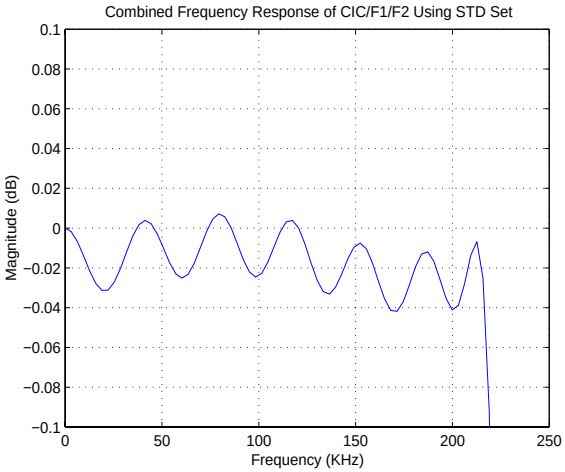


Figure 25. CIC, F1, & F2 STD Passband Flatness

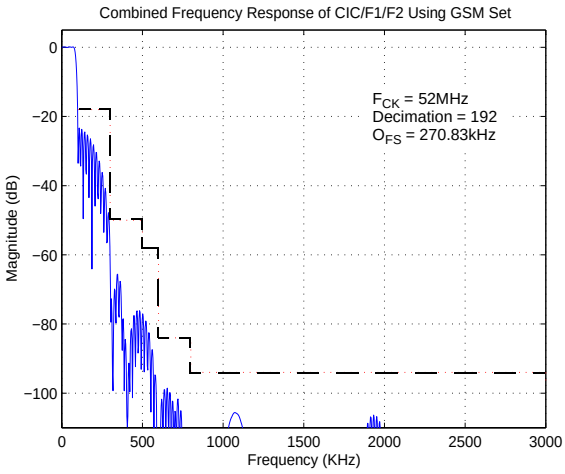


Figure 26. CIC, F1, & F2 GSM frequency response

bandwidth. At 78MHz, the decimation must increase again to 78MHz/270.833kHz or 288. The output bandwidth may only be changed in relation to the output sample rate by creating a new set of FIR filter coefficients. As the filter bandwidth

Detailed Description (Continued)

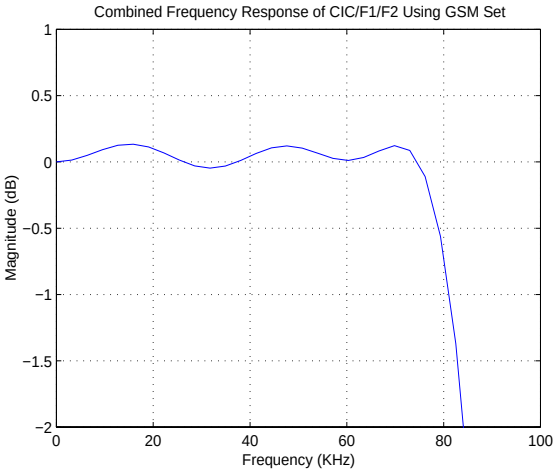


Figure 27. CIC, F1, & F2 GSM Passband Flatness

decreases relative to the output sample rate, the CIC droop compensation performed by F1 may no longer be required.

Overall Channel Gain

The overall gain of the chip is a function of the amount of decimation (N), the settings of the "SHIFT UP" circuit (SCALE), the GAIN setting, the sum of the F1 coefficients, and the sum of the F2 coefficients. The overall gain is shown below in Equation 2.

$$G_{DDC} = \frac{1}{2}(DEC+1)^4 \cdot 2^{[SCALE-44-AGAIN\cdot(1-EXP\_INH)]} \cdot 2^{GAIN} \cdot G_{F1} \cdot G_{F2} \quad (2)$$

Where:

$$G_{F1} = \frac{\sum_{i=1}^{21} h_1(i)}{2^{16}} \quad (3)$$

and:

$$G_{F2} = \frac{\sum_{i=1}^{63} h_2(i)}{2^{16}} \quad (4)$$

It is assumed that the DDC output words are treated as fractional 2's complement words. The numerators of G_{F1} and G_{F2} equal the sums of the impulse response coefficients of F1 and F2, respectively. For the STD and GSM sets, G_{F1} and G_{F2} are nearly equal to unity. Observe that the $AGAIN$ term in (2) is cancelled by the DVGA operation so that the entire gain of the DRCS is independent of the DVGA setting when EXP_INH=0. The $\frac{1}{2}$ appearing in (2) is the result of the 6dB conversion loss in the mixer. For full-scale square wave inputs the $\frac{1}{2}$ should be set to 1 to prevent signal distortion.

Data Latency and Group Delay

The CLC5903 latency calculation assumes that the FIR filter latency will be equal to the time required for data to propagate through one half of the taps. The CIC filter provides 4N equivalent taps where N is the CIC decimation ratio. F1 and F2 provide 21 and 63 taps respectively. When these filters are reflected back to the input rate, the effective taps are increased by decimation. This results in a total of 298N taps when the F2 decimation is 2 and 550N taps when the F2 decimation is 4.

The latency is then 149N CK periods when the F2 decimation is 2 and 275N CK periods when the F2 decimation is 4.

The CLC5903 filters are linear phase filters so the group delay remains constant.

Output Modes

After processing by the DDC, the data is then formatted for output.

All output data is two's complement. The serial outputs power up in a tri-state condition and must be enabled when the chip is configured. Parallel outputs are enabled by the $\overline{\text{POUT\_EN}}$ pin.

Output formats include truncation to 8 or 32 bits, rounding to 16 or 24 bits, and a 12-bit floating point format (4-bit exponent, 8-bit mantissa, 138dB numeric range). This function is performed in the OUTPUT CIRCUIT shown in Figure 28.

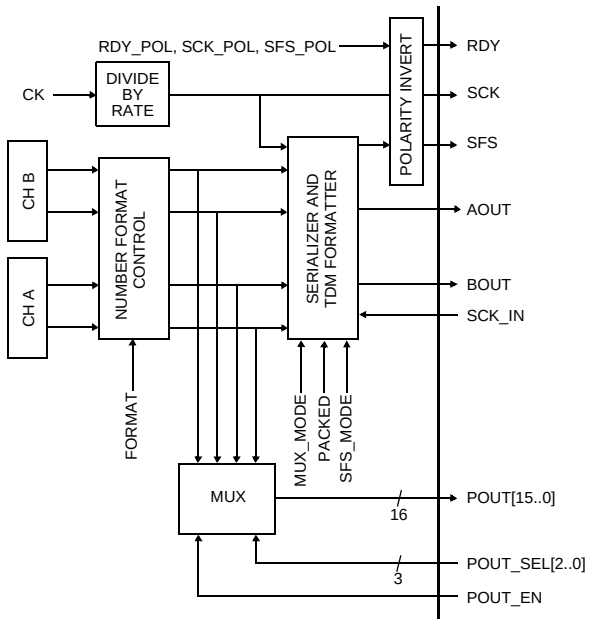
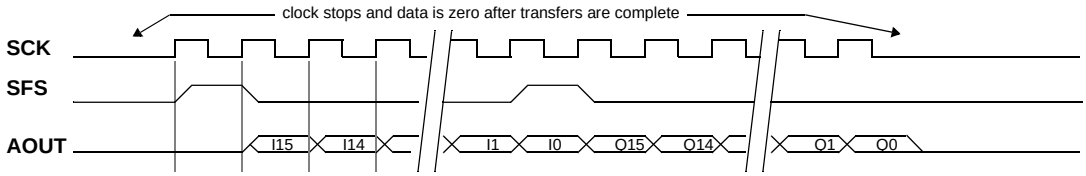


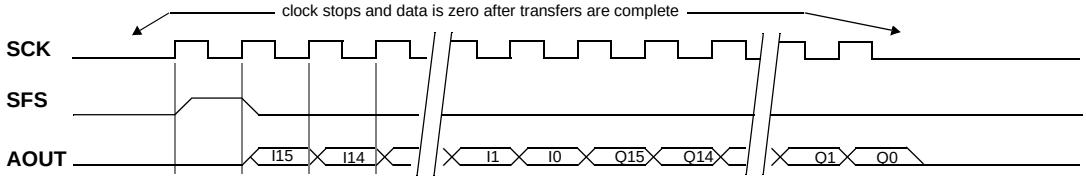
Figure 28. CLC5903 output circuit

The channel outputs are accessible through serial output pins and a 16-bit parallel output port. The **RDY** pin is provided to notify the user that a new output sample period (OSP) has begun. OSP refers to the interval between output samples at the decimated output rate. For example, if the input rate (and clock rate) is 52 MHz and the overall decimation factor is 192 (N=48, F2 decimation=2) the OSP will be 3.69 microseconds which corresponds to an output sample

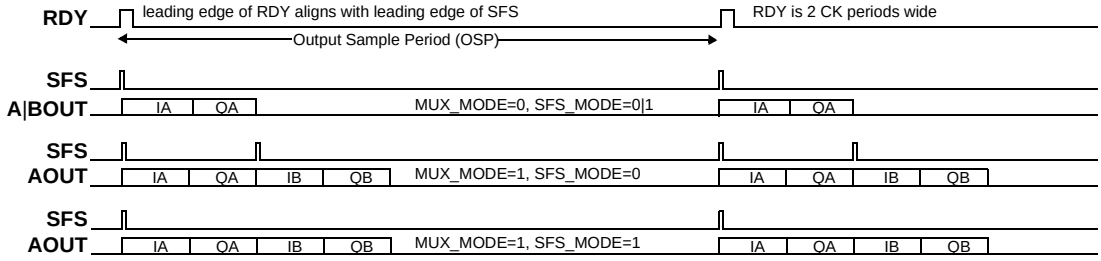
Output Modes (Continued)



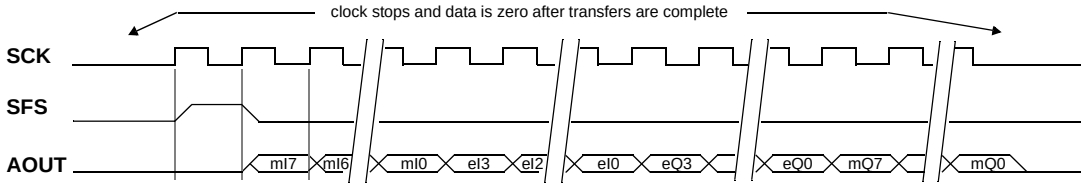
(a) UNPACKED MODE, FRAME SYNC AT THE START OF EACH WORD



(b) PACKED MODE, ONE FRAME SYNC AT THE START OF EACH DOUBLE-WORD TRANSFER



(c) ONE OR TWO CHANNEL MUX AND SFS MODES (PACKED MODE IS ON)



(d) FLOATING POINT FORMAT

Figure 29. Serial output formats. Refer to Figure 9 for detailed timing information

rate of 270.833kHz. An OSP starts when a sample is ready and stops when the next one is ready.

Serial Outputs

The CLC5903 provides a serial clock (**SCK**), a frame strobe (**SFS**) and two data lines (**AOUT** and **BOUT**) to output serial data. The MUX_MODE control register specifies whether the two channel outputs are transmitted on two separate serial pins, or multiplexed onto one pin in a time division multiplexed (TDM) format. Separate output pins are not provided for the I and Q halves of complex data. The I and Q outputs are always multiplexed onto the same serial pin. The I-component is output first, followed by the Q-component. By setting the PACKED mode bit to '1' a complex pair may be treated as a single double-wide word. The **RDY** signal is used to identify the first word of a complex pair of the TDM formatted output when the SFS_MODE bit is set to '0'. Setting SFS_MODE to '1' causes the CLC5903 to output a single **SFS** pulse for each output period. This **SFS** pulse will be coincident with **RDY** and only a single **SCK** period wide. The TDM modes are summarized in Table 1.

SFS_MODE	MUX_MODE	SERIAL OUTPUTS	
		AOUT	BOUT
0	0	OUT_A	OUT_B
	1	OUT_A, OUT_B	LOW
1	0	OUT_A	OUT_B
	1	OUT_A, OUT_B	LOW

Table 1. TDM Modes

The serial outputs use the format shown in Figure 29. Figure 29(a) shows the standard output mode (the PACKED mode bit is low). The chip clocks the frame and data out of the chip on the rising edge of **SCK** (or falling edge if the SCK_POL bit in the input control register is set high). Data should be captured on the falling edge of **SCK** (rising if SCK_POL=1). The

Output Modes (Continued)

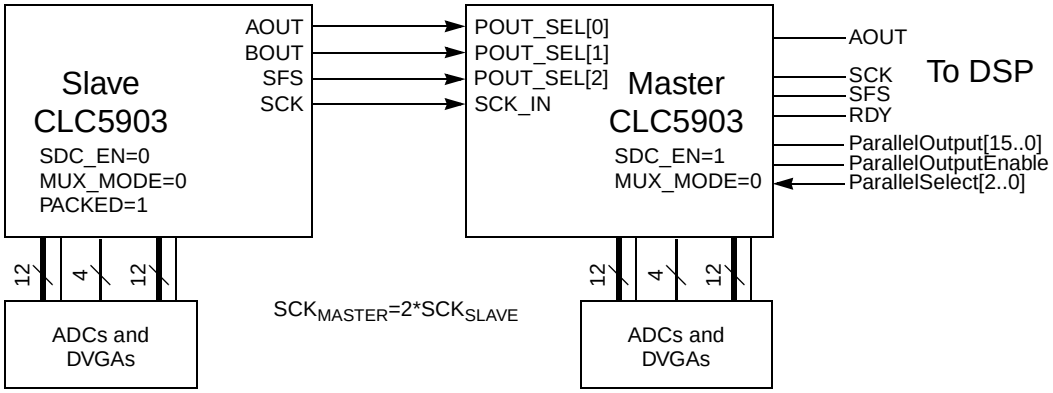


Figure 30. Serial Daisy-Chain Mode

chip sends the I data first by setting **SFS** high (or low if SFS_POL in the input control register is set high) for one clock cycle, and then transmitting the data, MSB first, on as many **SCK** cycles as are necessary. Without a pause, the Q data is transferred next as shown in Figure 29(a). If the PACKED control bit is high, then the I and Q components are sent as a double length word with only one **SFS** strobe as shown in Figure 29(b). If both channels are multiplexed out the same serial pin, then the subsequent I/Q channel words will be transmitted immediately following the first I/Q pair as shown in Figure 29(c). Figure 29(c) also shows how SFS_MODE=1 allows the **SFS** signal to be used to identify the I and Q channels in the TDM serial transmission. The serial output rate is programmed by the RATE register to **CK** divided by 1, 2, 4, 8, 16, or 32. The serial interface will not work properly if the programmed rate of **SCK** is insufficient to clock out all the bits in one OSP.

Serial Port Daisy-Chain Mode

Two CLC5903s can be connected in series so that a single DSP serial port can receive four DDC output channels. This mode is enabled by setting the SDC_EN bit to '1' on the serial daisy-chan (SDC) master. The SDC master is the CLC5903 which is connected to the DSP while the SDC slave's serial output drives the master. The SDC master's RATE register must be set so that its **SCK** rate is twice that of the SDC slave, the SDC master must have MUX_MODE=1, the SDC slave must have MUX_MODE=0 and PACKED=1, and both chips must come out of a $\overline{\textbf{MR}}$ or $\overline{\textbf{SI}}$ event within four **CK** periods of each other. In this configuration, the master's serial output data is shifted out to the DSP then the slave's serial data is shifted out. All the serial output data will be muxed onto the master's **AOUT** pin as shown in Figure 30.

Serial Port Output Number Formats

Several numeric formats are selectable using the FORMAT control register. The I/Q samples can be rounded to 16 or 24 bits, or truncated to 8 bits. The packed mode works as described above for these fixed point formats. A floating point format with 138dB of dynamic range in 12 bits is also provided. The mantissa (m) is 8 bits and the exponent (e) is 4 bits. The MSB of each segment is transmitted first. When this mode is selected, the I/Q samples are packed regardless of the state of MUX_MODE, and the data is sent as mI/eI/eQ/mQ which allows the two exponents to form an 8-bit word. This is shown in Figure 29(d). For all formats, once the defined length of the word is complete, **SCK** stops toggling.

Parallel Outputs

Output data from the channels can also be taken from a 16-bit parallel port. A 3-bit word applied to the **POUT_SEL[2:0]** pins determines which 16-bit segment is multiplexed to the parallel port. Table 2 defines this mapping. To allow for bussing of multiple chips, the parallel port is tri-stated unless $\overline{\textbf{POUT\_EN}}$ is low. The **RDY** signal indicates the start of an OSP and that new data is ready at the parallel output. The user has one OSP to cycle through whichever registers are needed. The RATE register must be set so that each OSP is at least 5 SCK periods.

Parallel Port Output Numeric Formats

The I/Q samples can be rounded to 16 or 24 bits or the full 32 bit word can be read. By setting the word size to 32 bits it is possible to read out the top 16 bits and only observe the top 8 bits if desired. Additionally, the output samples can be formatted as floating point numbers with an 8-bit mantissa and a 4 bit exponent. For the fixed-point formats, the valid bits are justified into the MSBs of the registers of Table 2 and

POUT_SEL	Normal Register Contents	Floating Point Register Contents
0	IA upper 16 bits	0000/eIA/mIA
1	IA lower 16 bits	0x0000
2	QA upper 16 bits	0000/eQA/mQA
3	QA lower 16 bits	0x0000
4	IB upper 16 bits	0000/eIB/mIB
5	IB lower 16 bits	0x0000
6	QB upper 16 bits	0000/eQB/mQB
7	QB lower 16 bits	0x0000

Table 2. Register Selection for Parallel Output

all other bits are set to zero. For the floating point format, the valid bits are placed in the upper 16 bits of the appropriate channel register using the format 0000/eI/mI for the I samples.

AGC

The CLC5903 AGC processor monitors the output level of the ADC and servos it to the desired setpoint. The ADC input is controlled by the DVGA to maintain the proper setpoint

AGC (Continued)

level. DVGA operation results in a compression of the signal through the ADC. The DVGA signal compression is reversed in the CLC5903 to provide > 120dB of linear dynamic range. This is illustrated in Figure 31.

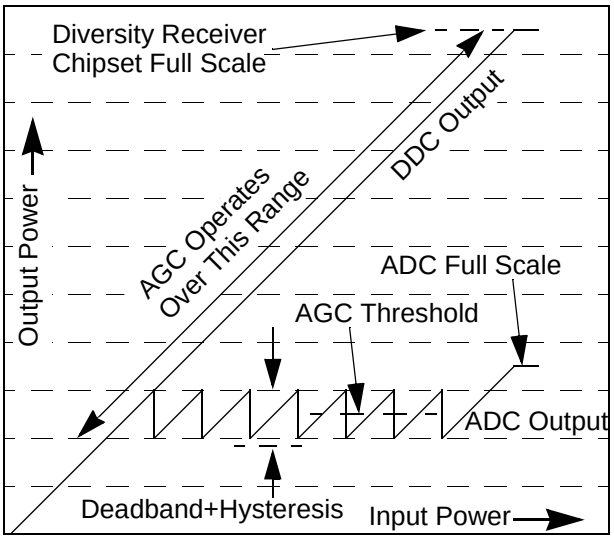


Figure 31. Output Gain Scaling vs. Input Signal

In order to use the AGC, the DRCS Control Panel software may be used to calculate the programmable parameters. To generate these parameters, only the desired setpoint, deadband+hysteresis, and loop time constant need to be supplied. All subsequent calculations are performed by the software. Complete details of the AGC operation are provided in an appendix but are not required reading.

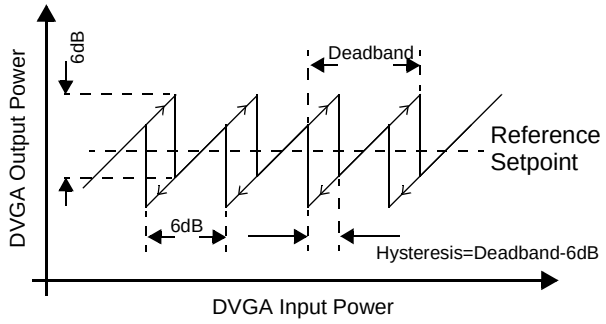


Figure 32. AGC Setup.

AGC setpoint and deadband+hysteresis are illustrated in Figure 32. The loop time constant is a measure of how fast the loop will track a changing signal. Values down to approximately 1.0 microsecond will be stable with the second order LC noise filter. Since the DVGA operates with 6dB steps the deadband should always be greater than 6dB to prevent oscillation. An increased deadband value will reduce the amount of AGC operation. A decreased deadband value will increase the amount of AGC operation but will hold the ADC output closer to the setpoint. The threshold should be set so that transients do not cause sustained overrange at the ADC inputs. The threshold setting can also be used to set the ADC input near its optimal performance level.

The AGC will free run when AGC_HOLD_IC is set to '0'. It may be set to a fixed gain by setting AGC_HOLD_IC to '1' after programming the desired gain in the AGC_IC_A and AGC_IC_B registers. Allowing the AGC to free run should be appropriate for most applications.

Programming the AGC_COMB_ORD register allows the AGC power detector bandwidth to be reduced if desired. This will tend to improve the power detector's ability to reject the signal carrier frequency and reduce overall AGC activity. Figure 35 on page 23 shows the power detector response.

Power Management

The CLC5903 can be placed in a low power (static) state by stopping the input clock. To prevent this from placing the CLC5903 into unexpected states, the **$\overline{\text{SI}}$** pin of the CLC5903 should be asserted prior to disabling the input clock and held asserted until the input clock has returned to a stable condition.

Test and Diagnostics

The CLC5903 supports IEEE 1149.1 compliant JTAG Boundary Scan for the I/O's. The following pins are used:

$\overline{\text{TRST}}$	(test reset)
TMS	(test mode select)
TDI	(test data in)
TDO	(test data out)
TCK	(test clock)

The following JTAG instructions are supported:

Instruction	Description
BYPASS	Connects TDI directly to TDO
EXTEST	Drives the 'extest' TAP controller output
IDCODE	Connects the 32-bit ID register to TDO
SAMPLE/PRELOAD	Drives the 'samp_load' TAP controller output
HIGHZ	Tri-states the outputs

The JTAG Boundary Scan can be used to verify printed circuit board continuity at the system level.

The user is able to program a value into TEST_REG and substitute this for the normal channel inputs from the **AIN/BIN** pins by selecting it with the crossbar. With the NCO frequency set to zero this allows the DDCs and the output interface of the chip to be verified. Also, the AGC loop can be opened by setting AGC_HOLD_IC high and setting the gain of the DVGA by programming the appropriate value into the AGC_IC_A/B register.

Real-time access to the following signals is provided by configuring the control interface debug register:

- NCO sine and cosine outputs
- data after round following mixers
- data before F1 and F2
- data after the CIC filter within the AGC

The access points are multiplexed to a 20-bit parallel output port which is created from signal pins **POUT[15:0]**, **AOUT**, **BOUT**, **SFS**, and **RDY** according to the table below:

Normal Mode Pin	Debug Mode Pin
POUT[15:0]	DEBUG[19..4]
RDY	DEBUG[3]
SFS	DEBUG[2]
AOUT	DEBUG[1]
BOUT	DEBUG[0]

Test and Diagnostics (Continued)

SCK will be set to the proper strobe rate for each debug tap point. **POUT_EN** and **PSEL[2..0]** have no effect in Debug Mode. The outputs are turned on when the Debug Mode bit is set. Normal serial outputs are also disabled.

Control Registers

The chip is configured and controlled through the use of 8-bit control registers. These registers are accessed for reading or writing using the control bus pins ($\overline{CE}$, $\overline{RD}$, $\overline{WR}$, A[7:0], and D[7:0]) described in the Control Interface section.

The two sets of FIR coefficients are overlaid at the same memory address. Use the PAGE_SEL registers to access the second set of coefficients.

The register names and descriptions are listed below under *Control Register Addresses and Defaults* on page 20. A quick reference table is provided in the *Condensed CLC5903 Address Map* on page 22.

Control Register Addresses and Defaults

Register Name	Width	Type	Default[a]	Addr	Bit	Description
DEC	11b	R/W	7	0(LSBs) 1(MSBs)	7:0 2:0	CIC decimation control. N=DEC+1. Valid range is from 7 to 2047. Format is an unsigned integer. This affects both channels.
DEC_BY_4	1b	R/W	0	1	4	Controls the decimation factor in F2. 0=Decimate by 2. 1=Decimate by 4. This affects both channels.
SCALE	6b	R/W	0	2	5:0	CIC SCALE parameter. Format is an unsigned integer representing the number of left bit shifts to perform on the data prior to the CIC filter. Valid range is from 0 to 40. This affects both channels.
GAIN_A	3b	R/W	0	3	2:0	Value of left bit shift prior to F1 for channel A.
GAIN_B	3b	R/W	0	4	2:0	Value of left bit shift prior to F1 for channel B.
RATE	1B	R/W	1	5	7:0	Determines rate of serial output clock. The output rate is FCK/(RATE+1). Unsigned integer values of 0, 1, 3, 7, 15, and 31 are allowed.
SOUT_EN	1b	R/W	0	6	0	Enables the serial output pins **AOUT**, **BOUT**, **SCK**, and **SFS**. 0=Tristate. 1=Enabled.
SCK_POL	1b	R/W	0	6	1	Determines polarity of the **SCK** output. 0=**AOUT**, **BOUT**, and **SFS** change on the rising edge of SCK (capture on falling edge). 1=They change on the falling edge of SCK.
SFS_POL	1b	R/W	0	6	2	Determines polarity of the **SFS** output. 0=Active High. 1=Active Low.
RDY_POL	1b	R/W	0	6	3	Determines polarity of the **RDY** output. 0=Active High. 1=Active Low.
MUX_MODE	1b	R/W	0	6	4	Determines the mode of the serial outputs. 0=Each channel is output on its respective pin, 1=Both channels are multiplexed and output on **AOUT**. See also Table 1.
PACKED	1b	R/W	0	6	5	Controls when **SFS** goes active. 0=**SFS** pulses prior to the start of the I and the Q words. 1=**SFS** pulses only once prior to the start of each I/Q sample pair (i.e. the pair is treated as a double-sized word) The I word precedes the Q word. See Figure 29.
FORMAT	2b	R/W	0	6	7:6	Determines output number format. 0=Truncate serial output to 8 bits. Parallel output is truncated to 32 bits. 1=Round both serial and parallel to 16 bits. All other bits are set to 0. 2=Round both serial and parallel to 24 bits. All other bits are set to 0. 3=Output floating point. 8-bit mantissa, 4-bit exponent. All other bits are set to 0.
FREQ_A	4B	R/W	0	7-10	7:0	Frequency word for channel A. Format is a 32-bit, 2's complement number spread across 4 registers. The LSBs are in the lower registers. The NCO frequency F is F/F_{CK}=FREQ_A/2^{32}.
PHASE_A	2B	R/W	0	11-12	7:0	Phase word for channel A. Format is a 16-bit, unsigned magnitude number spread across 2 registers. The LSBs are in the lower registers. The NCO phase PHI is PHI=2*pi*PHASE_A/2^16.
FREQ_B	4B	R/W	0	13-16	7:0	Frequency word for channel B. Format is a 32-bit, 2's complement number spread across 4 registers. The LSBs are in the lower registers. The NCO frequency F is F/F_{CK}=FREQ_B/2^{32}.
PHASE_B	2B	R/W	0	17-18	7:0	Phase word for channel B. Format is a 16-bit, unsigned magnitude number spread across 2 registers. The LSBs are in the lower registers. The NCO phase PHI is PHI=2*pi*PHASE_B/2^16.
A_SOURCE	2	R/W	0	19	1:0	0=Select **AIN** as channel input source. 1=Select **BIN.** 2=3=Select TEST_REG as channel input source.
B_SOURCE	2	R/W	1	19	3:2	0=Select **AIN** as channel input source. 1=Select **BIN.** 2=3=Select TEST_REG as channel input source.
EXP_INH	1b	R/W	0	20	0	0=Allow exponent to pass into FLOAT TO FIXED converter. 1=Force exponent in DDC channel to a 7 (maximum digital gain). This affects both channels.
Reserved	1b	R/W	1	20	1	AGC_FORCE on the CLC5902. Do not use.
Reserved	1b	R/W	0	20	2	AGC_RESET_EN on the CLC5902. Do not use.
AGC_HOLD_IC	1b	R/W	0	20	3	0=Normal closed-loop operation. 1=Hold integrator at initial condition. This affects both channels.
AGC_LOOP_GAIN	2b	R/W	0	20	4:5:	Bit shift value for AGC loop. Valid range is from 0 to 3. This affects both channels.
Reserved	2B	R/W	0	21-22	7:0	AGC_COUNT on the CLC5902. Do not use.

Control Register Addresses and Defaults (Continued)

Register Name	Width	Type	Default[a]	Addr	Bit	Description
AGC_IC_A	1B	R/W	0	23	7:0	AGC fixed gain for channel A. Format is an 8-bit, unsigned magnitude number. The channel A DVGA gain will be set to the inverted three MSBs.
AGC_IC_B	1B	R/W	0	24	7:0	AGC fixed gain for channel B. Format is an 8-bit, unsigned magnitude number. The channel B DVGA gain will be set to the inverted three MSBs.
AGC_RB_A	1B	R	0	25	7:0	AGC integrator readback value for channel A. Format is an 8-bit, unsigned magnitude number. The user can read the magnitude MSBs of the channel A integrator from this register.
AGC_RB_B	1B	R	0	26	7:0	AGC integrator readback value for channel B. Format is an 8-bit, unsigned magnitude number. The user can read the magnitude MSBs of the channel B integrator from this register.
TEST_REG	14b	R/W	0	27(LSBs) 28(MSBs)	7:0 5:0	Test input source. Instead of processing values from the **A**|**BIN** pins, the value from this location is used instead. Format is 14-bit 2s complement number spread across 2 registers.
Reserved	1B	-	-	29	7:0	For future use.
Reserved	1B	-	-	30	7:0	For future use.
DEBUG_EN	1b	R/W	0	31	0	0=Normal. 1=Enables access to the internal probe points.
DEBUG_TAP	5b	R/W	0	31	5:1	Selects internal node tap for debug. 0 selects F1 output for BI, 20 bits 1 selects F1 output for BQ, 20 bits 2 selects F1 output for AQ, 20 bits 3 selects F1 output for AI, 20 bits 4 selects F1 input for BI, 20 bits 5 selects F1 input for BQ, 20 bits 6 selects F1 input for AI, 20 bits 7 selects F1 input for AQ, 20 bits 8 selects NCO A, cosine output. 17 bits, 3 LSBs are 0. 9 selects NCO A, sine output, 17 bits, 3 LSBs are 0. 10 selects NCO B, cosine output, 17 bits, 3 LSBs are 0. 11 selects NCO B, sine output, 17 bits, 3 LSBs are 0. 12 selects NCO AI, rounded output, 15 bits, 5 LSBs are 0. 13 selects NCO AQ, rounded output, 15 bits, 5 LSBs are 0. 14 selects NCO BI, rounded output, 15 bits, 5 LSBs are 0. 15 selects NCO BQ, rounded output, 15 bits, 5 LSBs are 0. 16-31 selects AGC CIC filter output. 9 MSBs from ch A, next 9 bits from ch B, 2 LSBs are 0.
DITH_A	1b	R/W	1	31	6	0=Disable NCO dither source for channel A. 1=Enable.
DITH_B	1b	R/W	1	31	7	0=Disable NCO dither source for channel B. 1=Enable.
AGC_TABLE	32B	R/W	0	128-159	7:0	RAM space that defines key AGC loop parameters. Format is 32 separate 8-bit, 2's complement numbers. This is common to both channels.
F1_COEFF	22B	R/W	0	160-181	7:0	Coefficients for F1. Format is 11 separate 16-bit, 2's complement numbers, each one spread across 2 registers. The LSBs are in the lower registers. For example, coefficient h0[7:0] is in address 160, h0[15:8] is in address 161, h1[7:0] is in address 162, h1[15:8] is in address 163. PAGE_SEL_F1=1 maps these addresses to coefficient memory B.
F2_COEFF	64B	R/W	0	182-245	7:0	Coefficients for F2. Format is 32 separate 16-bit, 2's complement numbers, each one spread across 2 registers. The LSBs are in the lower registers. For example, coefficient h0[7:0] is in address 182, h0[15:8] is in address 183, h1[7:0] is in address 184, h1[15:8] is in address 185. PAGE_SEL_F2=1 maps these addresses to coefficient memory B.
COEF_SEL_F1A	1b	R/W	0	246	0	Channel A F1 coefficient select register. 0=memory A, 1=memory B.
COEF_SEL_F1B	1b	R/W	0	246	1	Channel B F1 coefficient select register. 0=memory A, 1=memory B.
PAGE_SEL_F1	1b	R/W	0	246	2	F1 coefficient page select register. 0=memory A, 1=memory B.
COEF_SEL_F2A	1b	R/W	0	247	0	Channel A F2 coefficient select register. 0=memory A, 1=memory B.
COEF_SEL_F2B	1b	R/W	0	247	1	Channel B F2 coefficient select register. 0=memory A, 1=memory B.
PAGE_SEL_F2	1b	R/W	0	247	2	F2 coefficient page select register. 0=memory A, 1=memory B.
SFS_MODE	1b	R/W	0	248	0	0=**SFS** asserted at the start of each output word when PACKED=1 or each I/Q pair when PACKED=0, 1=**SFS** asserted at the start of each output sample period.
SDC_EN	1b	R/W	0	248	1	0=normal serial mode, 1=serial daisy-chain master mode.
AGC_COMB_ORD	2b	R/W	0	249	1:0	Enable reduced bandwidth AGC power detector. 0=2nd-order decimate-by-eight CIC, 1=1-tap comb added to CIC, 2=4-tap comb added to CIC.
EXT_DELAY	5b	R/W	0	249	6:2	Number of **CK** period delays in excess of 4 needed to align the DVGA gain step with the digital gain compensation step. Use the default of zero for the CLC5957 ADC.

a. These are the default values set by a master reset (**$\overline{\text{MR}}$**). Sync in (**$\overline{\text{SI}}$**) will not affect any of these values.

Condensed CLC5903 Address Map

Register Name	Addr	Addr Hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEC	0	0x00	Dec7	Dec6	Dec5	Dec4	Dec3	Dec2	Dec1	Dec0
DEC_BY_4	1	0x01				DecBy4		Dec10	Dec9	Dec8
SCALE	2	0x02			Sc5	Sc4	Sc3	Sc2	Sc1	Sc0
GAIN_A	3	0x03						GA2	GA1	GA0
GAIN_B	4	0x04						GB2	GB1	GB0
RATE	5	0x05	Rate7	Rate6	Rate5	Rate4	Rate3	Rate2	Rate1	Rate0
SERIAL_CTRL	6	0x06	FMT1	FMT0	Packed	MuxMode	RDY_POL	SFS_POL	SCK_POL	SOUT_EN
FREQ_A	7	0x07	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
	8	0x08	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
	9	0x09	FA23	FA22	FA21	FA20	FA19	FA18	FA17	FA16
	10	0x0A	FA31	FA30	FA29	FA28	FA27	FA26	FA25	FA24
PHASE_A	11	0x0B	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
	12	0x0C	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
FREQ_B	13	0x0D	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
	14	0x0E	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
	15	0x0F	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
	16	0x10	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
PHASE_B	17	0x11	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
	18	0x12	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8
SOURCE	19	0x13					BS1	BS0	AS1	AS0
AGC_CTRL	20	0x14			AgcLG1	AgcLG0	AgcHldIC	Reserved	Reserved	ExpInh
AGC_COUNT	21	0x15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	22	0x16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
AGC_IC_A	23	0x17	AgcIcA7	AgcIcA6	AgcIcA5	AgcIcA4	AgcIcA3	AgcIcA2	AgcIcA1	AgcIcA0
AGC_IC_B	24	0x18	AgcIcB7	AgcIcB6	AgcIcB5	AgcIcB4	AgcIcB3	AgcIcB2	AgcIcB1	AgcIcB0
AGC_RB_A	25	0x19	AgcRbA7	AgcRbA6	AgcRbA5	AgcRbA4	AgcRbA3	AgcRbA2	AgcRbA1	AgcRbA0
AGC_RB_A	26	0x1A	AgcRbB7	AgcRbB6	AgcRbB5	AgcRbB4	AgcRbB3	AgcRbB2	AgcRbB1	AgcRbB0
TEST_REG	27	0x1B	Test7	Test6	Test5	Test4	Test3	Test2	Test1	Test0
	28	0x1C			Test13	Test12	Test11	Test10	Test9	Test8
DEBUG	31	0x1F	DITH_B	DITH_A	TapSel4	TapSel3	TapSel2	TapSel1	TapSel0	DebugEnable
AGC_TABLE	128	0x80		The AGC Table loads from the low address to the high address in this order:						
	159	0x9F		"1st location, 2nd location…"						
F1_COEFF	160	0xA0								
	181	0xB5		The FIR Coefficients load from the low address to the high address in this order:						
F2_COEFF	182	0xB6		"1st location low byte, 1st location high byte, 2nd location…"						
	245	0xF5		The Page Select bits determine which set of coefficient memory is written.						
F1_CTRL	246	0xF6						PgSelF1	CfSelF1B	CfSelF1A
F2_CTRL	247	0xF7						PgSelF2	CfSelF2B	CfSelF2A
SERIAL_CTRL2	248	0xF8							SdcEn	SfsMode
AGC_CTRL2	249	0xF9		ExtDelay4	ExtDelay3	ExtDelay2	ExtDelay1	ExtDelay0	CombOrd1	CombOrd0

AGC Theory of Operation

A block diagram of the AGC is shown in Figure 33. The DVGA interface comprises four pins for each of the channels. The first three pins of this interface are a 3-bit binary word that controls the DVGA gain in 6dB steps (**AGAIN**). The final pin is **ASTROBE** which allows the **AGAIN** bits to be latched into the DVGA's register. A key feature of the **ASTROBE,** illustrated Figure 34, is that it toggles only if the data on **AGAIN** has changed from the previous cycle. Not shown is that **ASTROBE** and **BSTROBE** are independent. For example, **ASTROBE** only toggles when **AGAIN** has changed. **BSTROBE** will not toggle because **AGAIN** has changed. This is done to minimize unnecessary digital noise on the sensitive analog path through the DVGA. **ASTROBE** and **BSTROBE** are asserted during **MR** and **SI** to properly initialize the DVGAs.

The absolute value circuit and the 2-stage, decimate-by-8 CIC filter comprise the power detection part of the AGC. The power detector bandwidth is set by the CIC filter to $F_{CK}/8$. The absolute value circuit doubles the effective input frequency. This has the effect of reducing the power detector bandwidth from $F_{CK}/8$ to $F_{CK}/16$.

For a full-scale sinusoidal input, the absolute value circuit output is a dc value of $511 \cdot (2/\pi)$. Because the absolute value circuit also generates undesired even harmonic terms, the CIC filter (response shown in Figure 35), is required to, remove these harmonics. The first response null occurs at $F_{CK}/8$, where F_{CK} is the clock frequency, and the response magnitude is at least 25dB below the dc value from $F_{CK}/10$ to $9F_{CK}/10$. Because the 2^{nd} harmonic from the absolute value circuit is about 10dB below the dc this means that the ripple in the detected level is about 0.7dB or less for input frequencies between $F_{CK}/20$ to $19F_{CK}/20$. Setting the AGC_COMB_ORD register to either 1 or 2 will narrow the power detector's bandwidth as shown in Figure 35.

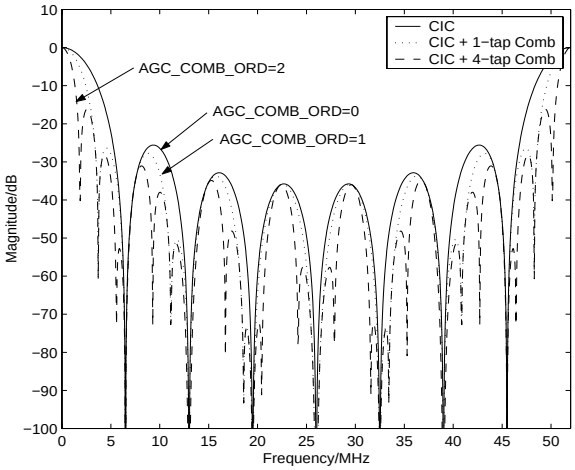


Figure 35. Power detector filter response, 52MHz

The "FIXED TO FLOAT CONVERTER" takes the fixed point 9-bit output from the CIC filter and converts it to a "floating point" number. This conversion is done so that the 32 values in the RAM can be uniformly assigned (dB scale) to detected power levels (54 dB range). This provides a resolution of 1.7dB between detected power levels. The truth table for this converter is given in Table 3. The upper three bits of the output represent the exponent (e) and the lower 2 are the mantissa (m). The exponent is determined by the position of the leading '1' out of the CIC filter. An output of '001XX' corresponds to a leading '1' in bit 2 (LSB is bit 0). The exponent

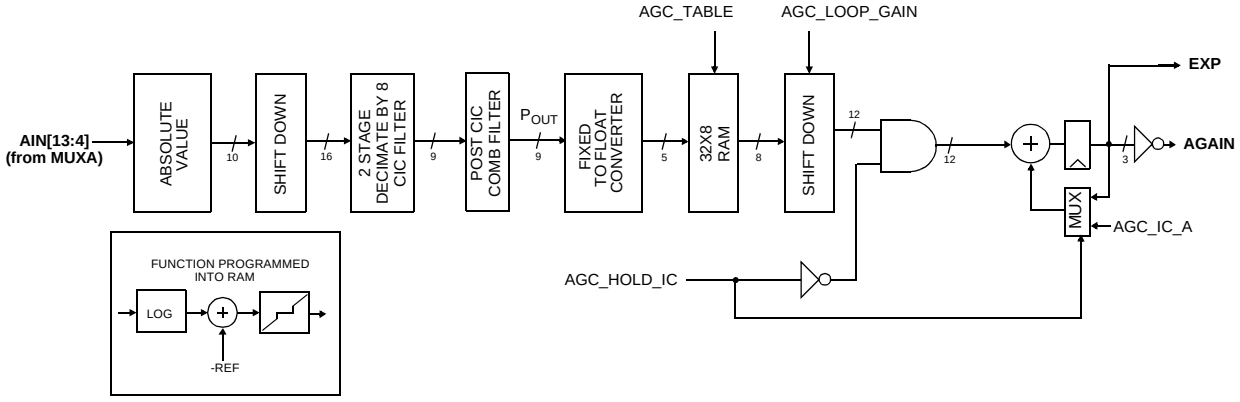


Figure 33. CLC5903 AGC circuit, Channel A

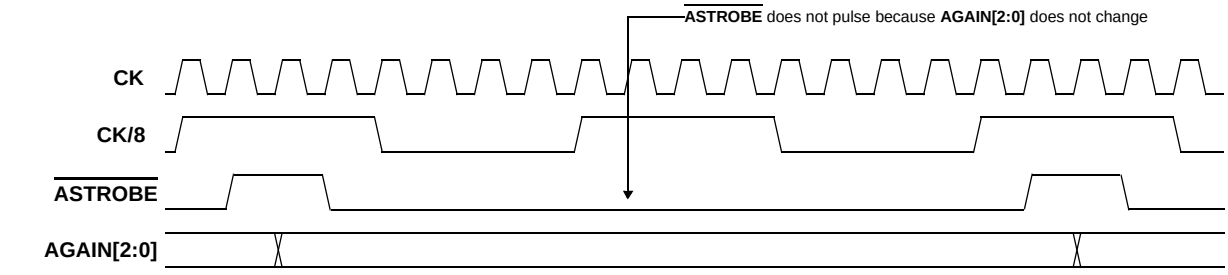


Figure 34. Timing diagram for AGC/DVGA interface, Channel A. Refer to Figure 8 for detailed timing information.

AGC Theory of Operation (Continued)

increases by one each time the leading '1' advances in bit position. The mantissa bits are the two bits that follow the leading '1'. If we define E as the decimal value of the exponent bits and M as the decimal value of the mantissa bits, the output of the CIC filter, P_{OUT}, corresponding to a given "FIXED TO FLOAT CONVERTER" output is,

$$P_{OUT} = [4 \cdot min(E, 1) + M] \cdot 2^{(max(E,1)-1)}, E \geq 1. \quad (5)$$

The max() and min() operators account for row 1 of Table 3 which is a special case because M=P_{OUT}. Equation 5 associates each address of the RAM with a CIC filter output.

INPUT	OUTPUT (eeemm)
0-3	000XX
4-7	001XX
8-15	010XX
16-31	011XX
32-63	100XX
64-127	101XX
128-255	110XX
256-511	111XX

Table 3. Fixed to Float Converter Truth Table

As shown in Figure 33, the 32X8 RAM look-up table implements the functions of log converter, reference subtraction, error amplifier, and deadband. The user must build each of these functions by constructing a set of 8-bit, 2's complement numbers to be loaded into the RAM. Each of these functions and how to construct them are discussed in the following paragraphs.

A log conversion is done in order to keep the loop gain independent of operating point. To see why this is beneficial, the control gain of the DVGA computed without log conversion is,

$$K'_{DVGA} = \frac{\partial}{\partial G}(v_i \cdot 2^{(G-G_o)}), = -v_i \cdot \ln(2) \cdot 2^{(G-G_o)}, \quad (6)$$

where G is the decimal equivalent of GAIN and G_0 accounts for the DVGA gain in excess of unity. This equation assumes that the DVGA gain control polarity is positive as is the case for the CLC5526. The gain around the entire loop must be negative. Observe in Equation 6 that the control gain is dependent on operating point G. If we instead compute the control gain with log conversion,

$$K_{DVGA} = \frac{\partial}{\partial G}[20 \cdot \log(v_i \cdot 2^{(G-G_o)})], = -6.02, \quad (7)$$

which is no longer operating-point dependent. The log function is constructed by computing the CIC filter output associated with each address (Equation 5) and converting these to dB. Full scale (dc signal) is $20\log(511) = 54dB$.

The reference subtraction is constructed by subtracting the desired loop servo point (in dB) from the table values computed in the previous paragraph. For example, if it is desired that the DVGA servo the ADC input level (sinusoidal signal) to -6dBFS, the number to subtract from the data is

$$20\log\left(\frac{511}{2} \cdot \frac{2}{\pi}\right) = 44dB. \quad (8)$$

The table data will then cross through zero at the address corresponding to this reference level. A deadband wider than 6dB should then be constructed symmetrically about this point. This prevents the loop from hunting due to the 6dB gain steps of the DVGA. Any deadband in excess of 6dB appears as hysteresis in the servo point of the loop as illustrated in Figure 32. The deadband is constructed by loading zeros into those addresses on either side of the one which corresponds to the reference level.

The last function of the RAM table is that of error amplification. All the operations preceding this one gave a table slope $S_{RAM} = 1$. This must now be adjusted in order to control the time constant of the loop given by,

$$\tau = \frac{8}{F_{CK}}\left(\frac{1}{G_L} + \frac{1}{2}\right). \quad (9)$$

The term G_L in this equation is the loop gain,

$$G_L = -6.02 \cdot S_{RAM} \cdot 2^{(AGC\_LOOP\_GAIN - 8)}. \quad (10)$$

The design equations are obtained by solving Equation 9 for G_L and Equation 10 for S_{RAM}. AGC_LOOP_GAIN is a control register value that determines the number of bits to shift the output of the RAM down by. This allows some of the loop gain to be moved out of the RAM so that the full output range of the table is utilized but not exceeded. The valid range for AGC_LOOP_GAIN is from 0 to 3 which corresponds to a 1 to 4 bit shift left.

An example set of numbers to implement a loop having a reference of 6dB below full scale, a deadband of 8dB, and a loop gain of 0.108 is:

-102 -102 -88 -80 -75 -70 -66
-63 -61 -56 -53 -50
-47 -42 -39 -36 -33 -29 -25
-22 -19 -15 -11 0
0 0 0 0 0 13 17 20

These values are shown plotted in Figure 36 with respect to the table addresses in (a), and the CIC filter output P_{OUT} in (b). For a 52MHz clock rate and AGC_LOOP_GAIN=2, these values result in a loop time constant of $1.5\mu s$.

The error signal from the loop gain "SHIFT DOWN" circuit is gated into the loop integrator. The gate is controlled by a timing and control circuit discussed in the next paragraph. A MUX within the integrator feedback allows the integrator to be initialized to the value loaded into AGC_IC_A (channel B can be set independently). The conditions under which it is initialized are configured in the registers associated with the timing and control circuit. The top eight bits of the integrator output can also be read back over the microprocessor interface from the AGC_RB_A (or AGC_RB_B) register. The top 3 bits below the sign become **AGAIN** and are output along with $\overline{\textbf{ASTROBE}}$ signal on the DVGA interface pins. The valid range of **AGAIN** is from 0 to 7 which corresponds to a valid range of 0 to 2^{10}-1 for the 11-bit, 2's complement integrator output from which **AGAIN** is derived. This is illustrated in Figure 37. The integrator saturates at these limits to prevent overshoots as the integrator attempts to enter the valid

AGC Theory of Operation (Continued)

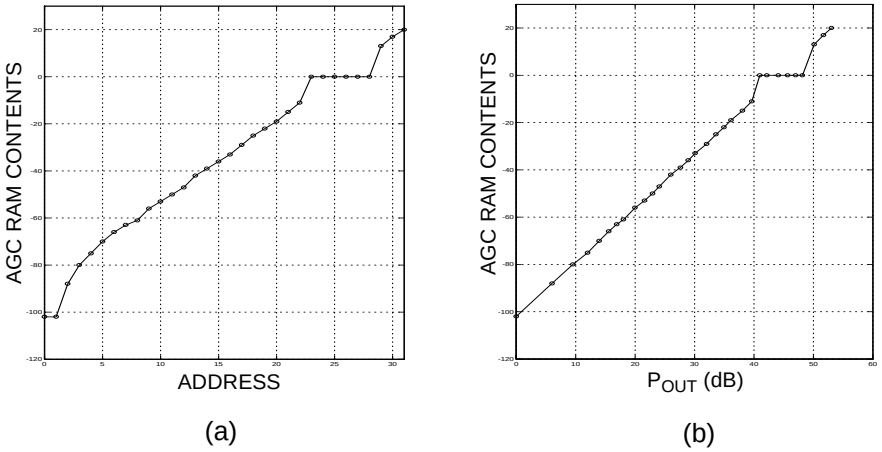


Figure 36. Example of programmed RAM contents

AGAIN[a]	EXP[b]	Input[c]	21	20	19	18	17	16	15	14	...	8	7	6	5	4	3	2	1	0
000 = -12dB	111 = +0dB	-12dB	14	13	12	11	10	9	8	7	...	1	0	L	L	L	L	L	L	L
001 = -6dB	110 = -6dB	-12dB	14	14	13	12	11	10	9	8	...	2	1	0	L	L	L	L	L	L
010 = +0dB	101 = -12dB	-12dB	14	14	14	13	12	11	10	9	...	3	2	1	0	L	L	L	L	L
011 = +6dB	100 = -18dB	-12dB	14	14	14	14	13	12	11	10	...	4	3	2	1	0	L	L	L	L
100 = +12dB	011 = -24dB	-12dB	14	14	14	14	14	13	12	11	...	5	4	3	2	1	0	L	L	L
101 = +18dB	010 = -30dB	-12dB	14	14	14	14	14	14	13	12	...	6	5	4	3	2	1	0	L	L
110 = +24dB	001 = -36dB	-12dB	14	14	14	14	14	14	14	13	...	7	6	5	4	3	2	1	0	L
111 = +30dB	000 = -42dB	-12dB	14	14	14	14	14	14	14	14	...	8	7	6	5	4	3	2	1	0

Table 4. 15-bit Mixer Output Alignment into the 22-bit SHIFT-UP Based On EXP.[d]

a. AGAIN sets the DVGA or analog gain value.
b. EXP sets the "FIXED TO FLOAT CONVERTER" or digital gain value.
c. 22-bit input to SHIFT-UP block in Figure 15 horizontally, linearized SHIFT-UP value vertically.
d. The numbers in the center of the table represent the mixer output bits. 'L' represents a logic low.

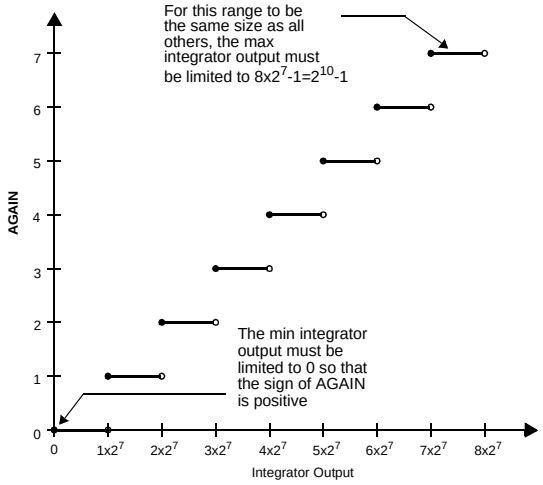


Figure 37. AGC integrator output limits

range. The **AGAIN** value is inverted (**EXP**) and used to adjust the gain of the incoming signal to provide a linear output dynamic range. The relationship between the DVGA analog gain (**AGAIN**) and the "FIXED TO FLOAT CONVERTER" digital gain (**EXP**) is shown in Table 4. The DVGA's compression of the incoming signal in the analog domain vs. the subsequent expansion in the digital domain is shown in Figure 31.

The AGC may be forced to free run by setting AGC_HOLD_IC low. Writing an initial condition to AGC_IC_A|B and then setting AGC_HOLD_IC high will force the AGC to a fixed gain. The three MSBs of the value written to AGC_IC_A|B are inverted and output to drive the DVGA.

Allowing the AGC to free run should be appropriate for most applications. If the INH_EXP bit is not set, the DVGA gain word (**EXP**) is routed to the "FLOAT TO FIXED CONVERTER" in the DDCs prior to the programmable decimation filter. The **EXP** signals are delayed to account for the propagation delay of the DVGA interface and the CLC5957 ADC.

Evaluation Hardware

Evaluation boards are available to facilitate designs based on the CLC5903:

CLC-EDRCS-PCASM

The Enhanced Diversity Receiver Chipset evaluation board providing a complete narrowband receiver from IF to digital symbols.

CLC-CAPT-PCASM

A simple method for capturing output data from CLC ADCs and the CLC5903.

SOFTWARE

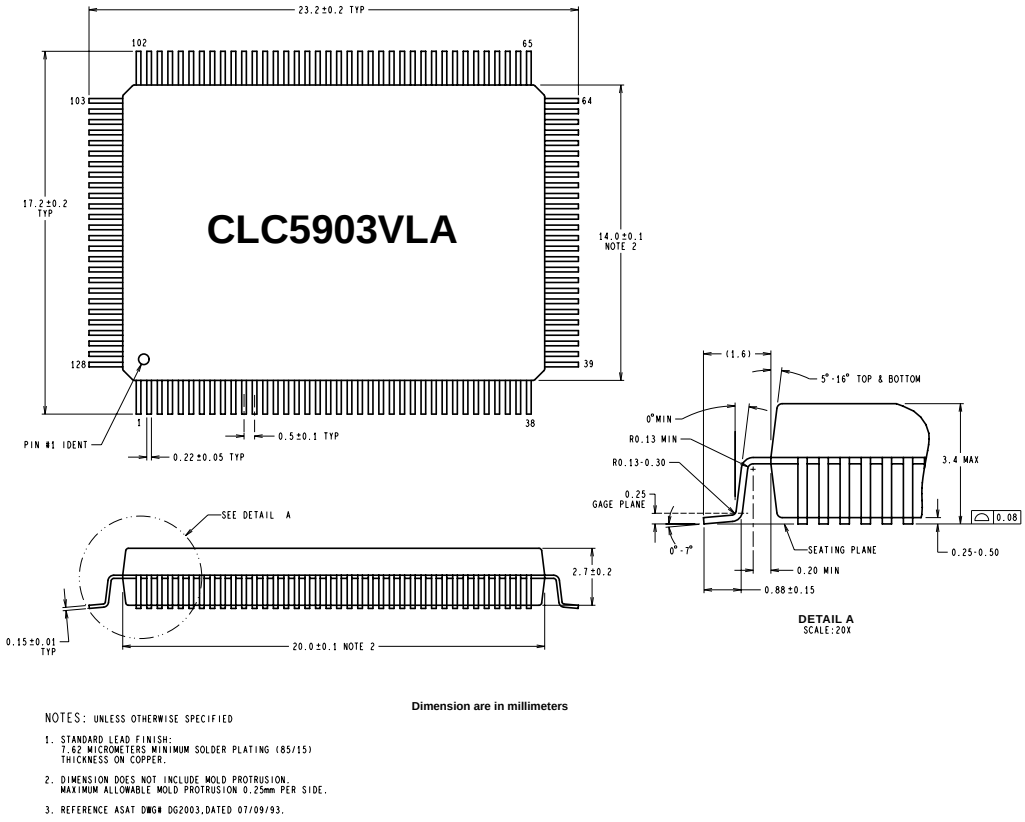
Control panel software for the CLC5903 supports complete device configuration on both evaluation boards.

Capture software manages the capture of data and its storage in a file on a PC.

Matlab script files support data analysis: FFT, DNL, and INL plotting.

This software and additional application information is available on the CLC Evaluation Kit CDROM.

Physical Dimensions inches (millimeters) unless otherwise noted



Dimension are in millimeters

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)
   THICKNESS ON COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
   MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
3. REFERENCE ASAT DWG# DG2003,DATED 07/09/93.

Figure 38. CLC5903VLA PQFP Package Dimensions

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