CubicMOS

16 bit Stereo Audio DAC

CM6312

General Description

The CM6312 is a 16 bit voltage output Digital to Analog Converter, with excellent Power Supply Rejection Ratio (PSRR). And utilizing in CMOS technology features an extremely low power dissipation. With wide range of operation voltage from 2.7V to 7V, it is suitable for battery-powered application.

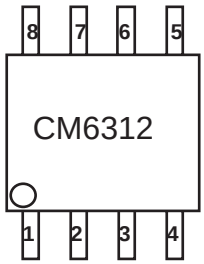
Feature

- ♦ Excellent Power Supply Rejection Ratio (PSRR)
- ♦ Voltage output
- ♦ Low power consumption (3mA)
- ♦ Wide operating voltage range 2.7V to 7V
- ♦ Wide dynamic range (16 bit resolution)
- ♦ Low Total Harmonic Distortion
- ♦ No zero crossing distortion
- ♦ Fast setting time permits 2*, 4*, 8* oversampling(serial input) or double speed operation at 4* oversampling
- ♦ Compatiable with most of the Japanese input formats : time multiplexed, two's complement, TTL
- ♦Space saving package(SOP8)

Applications

- ♦ Motherboard
- ♦ PDA
- ♦ VCD Player, CD-ROM
- ♦ MP-3 Player

Pin Assignmant



Pin No.	CM6311A
1	BCK
2	WS
3	DATA
4	GND
5	V_{DD}
6	V_{OL}
7	V_{REF}
8	V_{OR}

Pin Description

Pin No.	Symbol	Description
1	BCK	Bit clock input
2	WS	Word select input
3	DATA	Data input
4	GND	Groung
5	V_{DD}	Positive supply voltage
6	V_{OL}	Left channel output
7	V_{REF}	Voltage Reference Source
8	V_{OR}	Right channel output

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive supply voltage	-0.3	9.0	V
T_{stg}	Storage temperature range	-65	150	°C
F_{BCK}	Master Clock Frequency		25	MHz
T_A	Operating temperature range	-25	85	°C

Electronical Characteristics

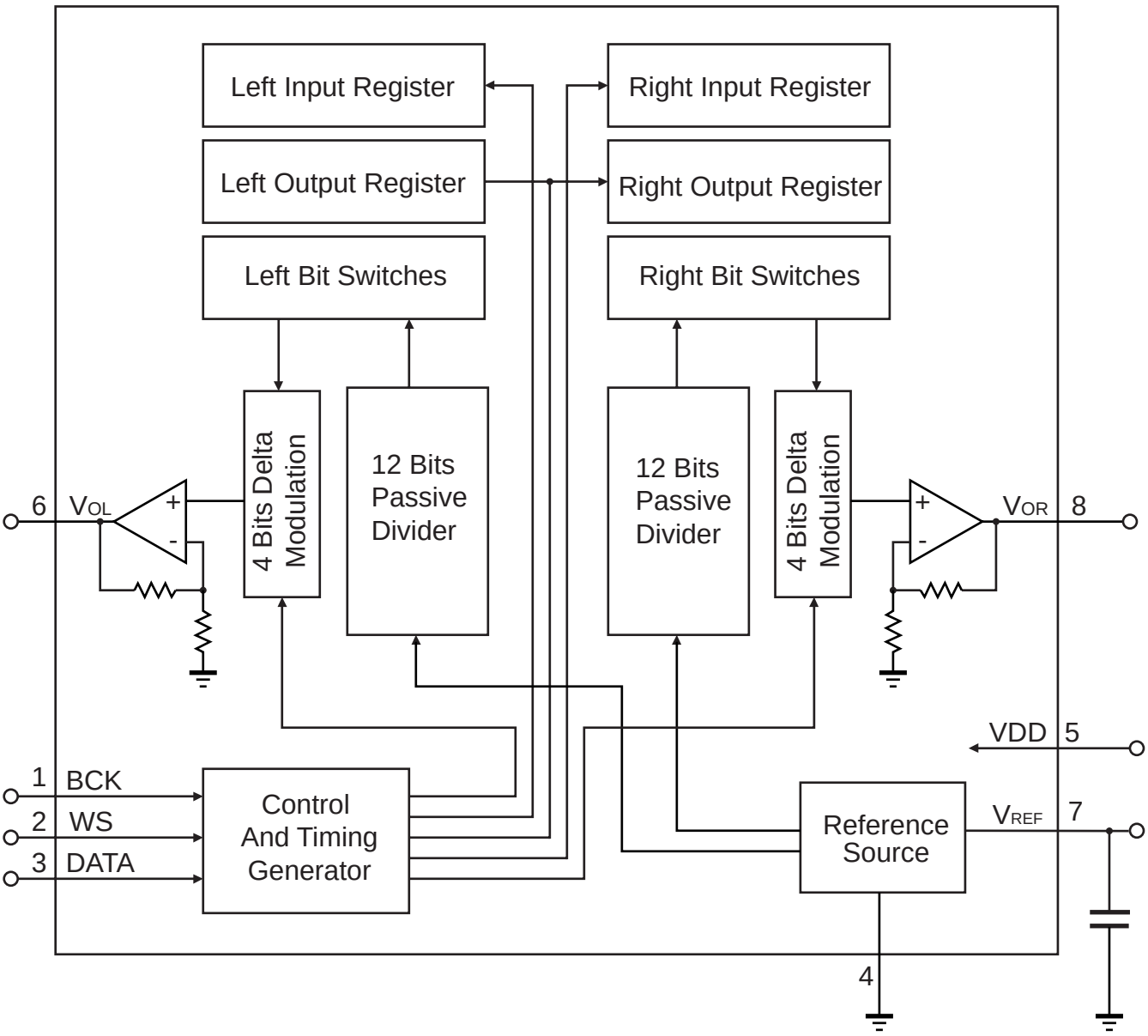
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{DD}	Positive supply voltage		2.7	3.3	7.0	V
I_{DD}	Operating current			3.0	5.0	mA
Digitall inputs (WS, BCK, DATA)						
[I_{IL}]	Input leakage current LOW	0V<=Vin<=VDD			1.0	uA
[I_{IH}]	Input leakage current HIGH	0V<=Vin<=VDD			1.0	uA
F_{BCK}	Input clock frequency		DC		25	MHz
BR	Bit rate data input		DC		25	Mbits/s
F_{WS}	Word select input frequency		DC		1562	kHz

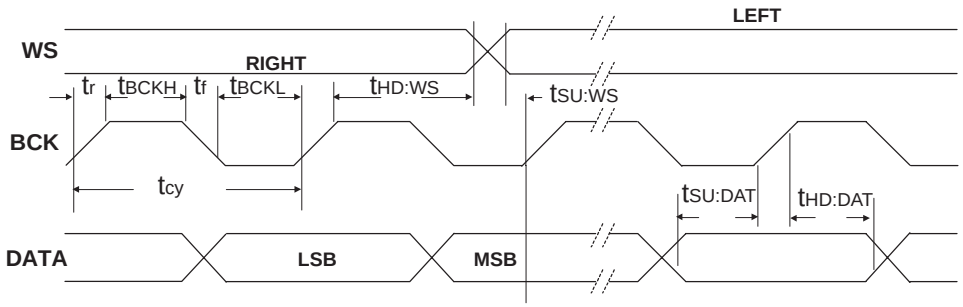
Electronical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing						
tr	Rise time				10	ns
tf	Fall time				10	ns
tcy	Bit clock cycle time		40			ns
t_{BCKH}	Bit clock high time		10			ns
t_{BCKL}	Bit clock low time		10			ns
$t_{SU:DAT}$	Data set up time		10			ns
$t_{HD:DAT}$	Data hold time to bit clock		0			ns
$t_{HD:WS}$	Word select hold time		0			ns
$t_{HD:WS}$	Word select set up time		10			ns
Analog outputs (V_{OL}, V_{OR})						
Res	Resolution				16	bits
V_{FS}	Full scale output voltage	VDD>=2.7V	1.4	1.75	2.1	V
TC_{FS}	Full scale temperature coefficient			0	200	ppm/°C
V_{OS}	Offset voltage		0.15	0.25	0.35	V
(THD+N)/S	Total harmonic distortion plus noise	at 0 dB, note 1		-68	-63	dB
				0.04	0.07	%
		at -60 dB, note 1		-30	-24	dB
				3	6	%
t_{CS}	Voltage setting time to ±1LSB			0.1	0.2	uS
α_{CS}	Channel separation		87	90		dB
[δI_O]	Unbalance between outputs	Note 1		0.1	0.2	dB
[td]	Time delay between output			0	0.1	uS
S/N	Signal to noise ratio	A-weighted at code 0000H	90	92		dB

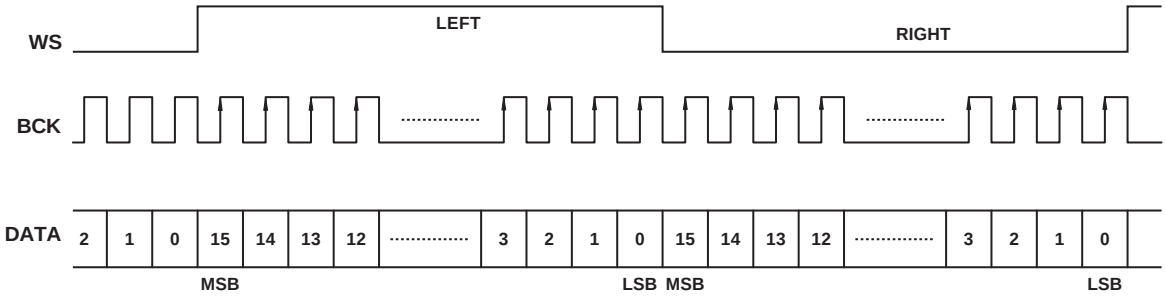
Note 1: Measured with 1kHz sinewave generated at sampling rate of 192 kHz

Block Diagram





Timing and input signals

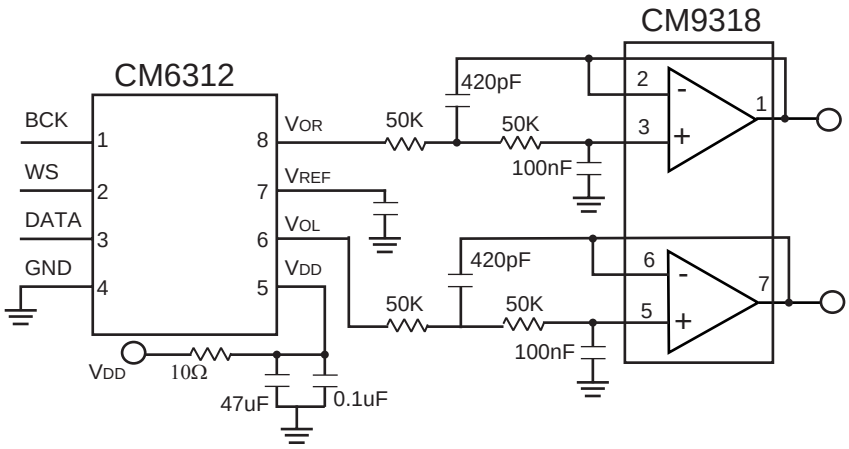


Format of input signals

Application Information

Basic application example

Enclosed circuit show the typical example of a CD application with CM6312, it features typical decoupling components and a third order a nalog post-filter stage providing a line output.



PCB Layout Considerations

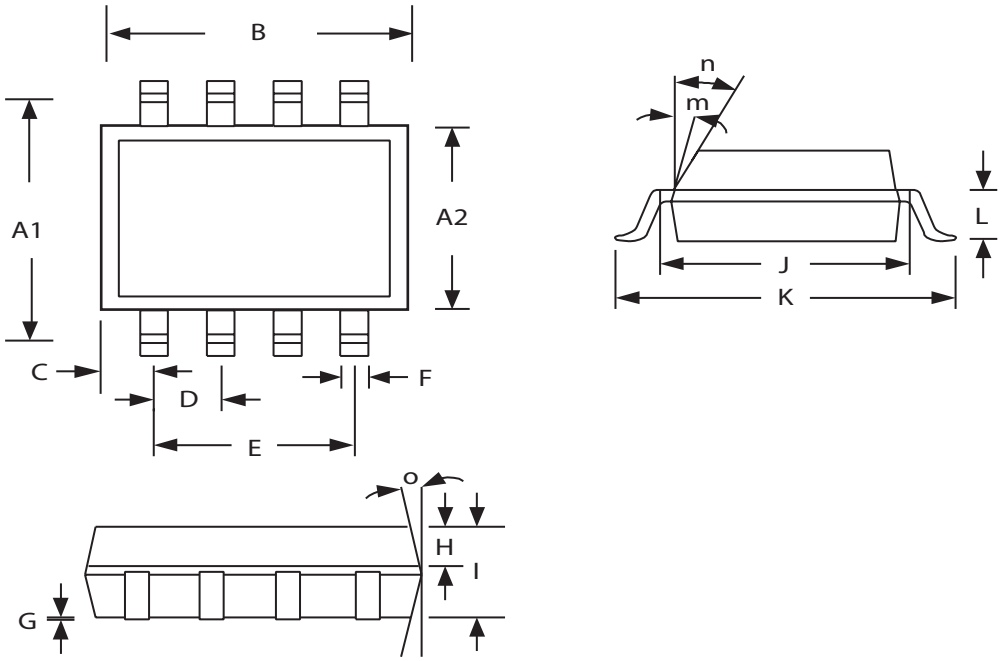
Supply :Care should be taken to supply the CM6312 with a clean, noiseless VDD, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RF filteredsupply.

Grouding : Preferably a ground plane should be used, in order to have a low impedance return available at any point in the lay out. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents.

Topology : The capacitor decoupling high frequency supply interference from VDD to ground should be place as close as physically possible to the IC body, ensuring a low inductance path to ground. The digital input conductors may be shielded by ground leads running analog side. The placement of a passive ground plane underside the entire IC surface gives free additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

Package Dimension

SOP8



DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A1	4.80	5.00	0.190	0.200
A2	3.80	4.00	0.149	0.157
B	4.80	5.00	0.189	0.196
C	0.558		0.022	
D	1.2BSC		0.050BSC	
E	3.810		0.150	
F	0.33	0.51	0.013	0.069
G	0.152	0.202	0.006	0.008
H	0.406		0.016	
I	1.35	1.75	0.053	0.069
J	4.496	4.623	0.177	0.182
K	5.994	6.197	0.236	0.244
L	0.939		0.037	
m	7 °		7 °	
n	45 °		45 °	
o	8 °		8 °	