National Semiconductor

PRELIMINARY

COP414L/COP314L Single-Chip N-Channel Microcontrollers

General Description

The COP414L Single-Chip N-Channel Microcontrollers are members of the COPS™ family, fabricated using N-channel, silicon gate MOS technology. This Controller Oriented Processor is a complete microcomputer containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP414L is an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

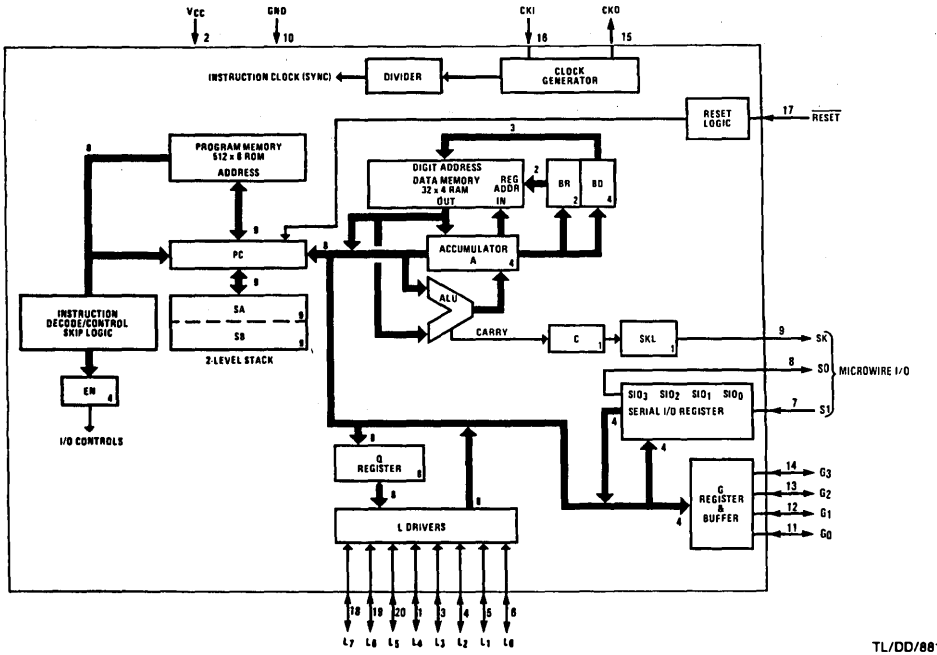
The COP314L is an exact functional equivalent but extended temperature version of COP414L.

The COP414L can be emulated by the COP404C. The COP401L should be used for exact emulation.

Features

- Late waferfab programming of ROM and I/O for fast delivery of units
- Low cost
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 15 I/O lines
- Two-level subroutine stack
- 16 μs instruction time
- Single supply operation (4.5V–6.3V)
- Low current drain (6 mA max)
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device
  — COP314L (−40°C to +85°C)
- Wider supply range (4.5V–9.5V) optionally available

Block Diagram



TL/DD/8814–1

FIGURE 1. COP414L

COP414L

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	
COP414L	0.65W at 25°C
	0.3W at 70°C
Total Source Current	120 mA
Total Sink Current	100 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Standard Operating Voltage (V_{CC})	(Note 1)	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		6	mA
Input Voltage Levels				
CKI Input Levels				
Ceramic Resonator Input (÷8)				
Logic High (V_{IH})	V_{CC} = Max	3.0		V
Logic High (V_{IH})	V_{CC} = 5V ±5%	2.0		
Logic Low (V_{IL})		−0.3	0.4	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		−0.3	0.6	V
$\overline{\text{RESET}}$ Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.6	V
SO Input Level (Test Mode)	(Note 2)	2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	With TTL Trip Level Options	2.0		V
Logic Low	Selected, V_{CC} = 5V ±5%	−0.3	0.8	V
Logic High	With High Trip Level Options	3.6		V
Logic Low	Selected	−0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage		−1	+1	μA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ±10%			
Logic High (V_{OH})	I_{OH} = −25 μA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36 mA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 1		V
Logic Low	I_{OL} = +10 μA		0.2	V

Note 1: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 2: SO output "0" level must be less than 0.8V for normal operation.

COP414L

DC Electrical Characteristics $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Current Levels				
Output Sink Current				
SO and SK Ouputs (I_{OL})	$V_{CC} = 9.5V, V_{OL} = 0.4V$	1.8		mA
	$V_{CC} = 6.3V, V_{OL} = 0.4V$	1.2		mA
	$V_{CC} = 4.5V, V_{OL} = 0.4V$	0.9		mA
L_0–L_7 Outputs, G_0–G_3 and	$V_{CC} = 9.5V, V_{OL} = 0.4V$	0.4		mA
LSTTL D_0–D_3 Outputs (I_{OL})	$V_{CC} = 6.3V, V_{OL} = 0.4V$	0.4		mA
	$V_{CC} = 4.5V, V_{OL} = 0.4V$	0.4		mA
CKI (Single-pin RC Oscillator)	$V_{CC} = 4.5, V_{IH} = 3.5V$	2		mA
CKO	$V_{CC} = 4.5, V_{OL} = 0.4V$	0.2		mA
Output Source Current				
Standard Configuration,	$V_{CC} = 9.5V, V_{OH} = 2.0V$	−140	−800	μA
All Outputs (I_{OH})	$V_{CC} = 6.3V, V_{OH} = 2.0V$	−75	−480	μA
	$V_{CC} = 4.5V, V_{OH} = 2.0V$	−30	−250	μA
Push-Pull Configuration	$V_{CC} = 9.5V, V_{OH} = 4.75V$	−1.4		mA
SO and SK Outputs (I_{OH})	$V_{CC} = 6.3V, V_{OH} = 2.4V$	−1.4		mA
	$V_{CC} = 4.5V, V_{OH} = 1.0V$	−1.2		mA
Input Load Source Current	$V_{CC} = 5.0V, V_{IL} = 0V$	−10	−140	μA
Open Drain Output Leakage		−2.5	+2.5	μA
Total Sink Current Allowed				
All Outputs Combined			100	mA
D Port			100	mA
L_7–L_4, G Port			4	mA
L_3–L_0			4	mA
Any Other Pin			2.0	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7–L_4			60	mA
L_3–L_0			60	mA
Each L Pin			25	mA
Any Other Pin			1.5	mA

COP314L

Absolute Maximum Ratings

Voltage at Any Pin Relative to GND	−0.5V to +10V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation COP314L	0.65W at 25°C 0.20W at 85°C
Total Source Current	120 mA
Total Sink Current	100 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

COP314L: $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Standard Operating Voltage (V_{CC})	(Note 1)	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		8	mA
Input Voltage Levels				
Ceramic Resonator Input (÷8)				
Crystal Input				
Logic High (V_{IH})	V_{CC} = Max	3.0		
Logic High (V_{IH})	V_{CC} = 5V ±5%	2.2		V
Logic Low (V_{IL})		−0.3	0.3	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		−0.3	0.4	V
$\overline{\text{RESET}}$ Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.4	V
SO Input Level (Test Mode)	(Note 2)	2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	With TTL Trip Level Options	2.2		V
Logic Low	Selected, V_{CC} = 5V ±5%	−0.3	0.6	V
Logic High	With High Trip Level Options	3.6		V
Logic Low	Selected	−0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage		−2	+2	μA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ±10%			
Logic High (V_{OH})	I_{OH} = −20 μA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36 mA		0.4	V
CMOS Operation				
Logic High	I_{OH} = −10 μA	V_{CC} − 1		V
Logic Low	I_{OL} = +10 μA		0.2	V

Note 1: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 2: SO output "0" level must be less than 0.6V for normal operation.

COP314L

DC Electrical Characteristics (Continued)

COP314L: $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 7.5V$ unless otherwise noted

Parameter	Conditions	Min	Max	Units
Output Current Levels				
Output Sink Current				
SO and SK Outputs(I_{OL})	$V_{CC} = 7.5V, V_{OL} = 0.4V$	1.4		mA
	$V_{CC} = 5.5V, V_{OL} = 0.4V$	1.0		mA
	$V_{CC} = 4.5V, V_{OL} = 0.4V$	0.8		mA
L_0–L_7 Outputs, G_0–G_3 and	$V_{CC} = 7.5V, V_{OL} = 0.4V$	0.4		mA
LSTTL, D_0–D_3 Outputs (I_{OL})	$V_{CC} = 5.5V, V_{OL} = 0.4V$	0.4		mA
	$V_{CC} = 4.5V, V_{OL} = 0.4V$	0.4		mA
CKI (Single-pin RC Oscillator)	$V_{CC} = 4.5V, V_{IH} = 3.5V$	1.5		mA
CKO	$V_{CC} = 4.5V, V_{OL} = 0.4V$	0.2		mA
Output Source Current				
Standard Configuration,	$V_{CC} = 7.5V, V_{OH} = 2.0V$	−100	−900	μA
All Outputs (I_{OH})	$V_{CC} = 5.5V, V_{OH} = 2.0V$	−55	−600	μA
	$V_{CC} = 4.5V, V_{OH} = 2.0V$	−28	−350	μA
Push-Pull Configuration	$V_{CC} = 7.5V, V_{OH} = 3.75V$	−0.85		mA
SO and SK Outputs (I_{OH})	$V_{CC} = 5.5V, V_{OH} = 2.0V$	−1.1		mA
	$V_{CC} = 4.5V, V_{OH} = 1.0V$	−1.2		mA
Input Load Source Current	$V_{CC} = 5.0V, V_{IL} = 0V$	−10	−200	μA
Open Drain Output Leakage		−5	+5	μA
Total Sink Current Allowed				
All Outputs Combined			100	mA
D Port			100	mA
L_7–L_4, G Port			4	mA
L_3–L_0			4	mA
Any Other Pins			1.5	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7–L_4			60	mA
L_3–L_0			60	mA
Each L Pin			25	mA
Any Other Pins			1.5	mA

AC Electrical Characteristics

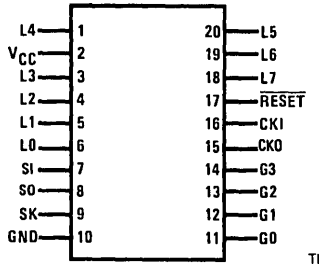
COP414L: 0°C ≤ T_A ≤ 70°C, 4.5V ≤ V_{CC} ≤ 9.5V unless otherwise noted
COP314L: −40°C ≤ T_A ≤ +85°C, 4.5V ≤ V_{CC} ≤ 7.5V unless otherwise noted
COP214L: −40°C ≤ T_A ≤ +110°C, 4.5V ≤ V_{CC} ≤ 7.5V unless otherwise noted

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time — t_C		16	40	μs
CKI				
Input Frequency — f_I	÷8 Mode	0.2	0.5	MHz
	÷4 Mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 0.5 MHz		500	ns
Fall Time			200	ns
CKI Using RC (÷4)	R = 56 kΩ ±5% C = 100 pF ±10%			
Instruction Cycle Time (Note 1)		16	28	μs
CKO as SYNC Input				
t_{SYNC}		400		ns
Inputs				
G_3–G_0, L_7–L_0				
t_{SETUP}		8.0		μs
t_{HOLD}		1.3		μs
SI				
t_{SETUP}		2.0		μs
t_{HOLD}		1.0		μs
Output Propagation Delay	Test Condition: C_L = 50 pF, R_L = 20 kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{pd1}, t_{pd0}			4.0	μs
All Other Outputs				
t_{pd1}, t_{pd0}			5.6	μs

Note 1: Variation due to the device included.

Connection Diagram

Dual-In-Line Package



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Top View

FIGURE 2

Order Number COP214L-XXX/D, COP314L-XXX/D or COP414L-XXX/D
See NS Hermetic Package D20A

Order Number COP214L-XXX/N, COP314L-XXX/N or COP414L-XXX/N
See NS Molded Package N20A

Order Number COP214L-XXX/WM, COP314L-XXX/WM or COP414L-XXX/WM
See NS Surface Mount Package M20B

Pin Descriptions

Pin	Description	Pin	Description
L_7–L_0	8 bidirectional I/O ports with TRI-STATE	CKI	System oscillator input
G_3–G_0	4 bidirectional I/O ports	CKO	System oscillator output
SI	Serial input (or counter input)	$\overline{RESET}$	System reset input
SO	Serial output (or general purpose output)	V_{CC}	Power supply
SK	Logic-controlled clock (or general purpose output)	GND	Ground

Timing Diagrams

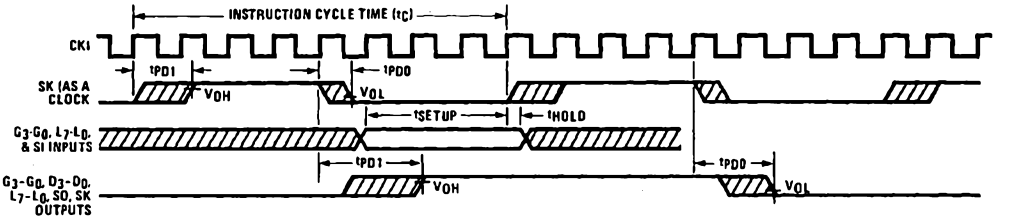

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FIGURE 3. Input/Output Timing Diagrams (Ceramic Resonator Divide-by-8 Mode)

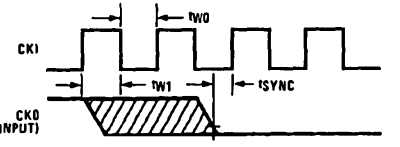

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FIGURE 3a. Synchronization Timing

Functional Description

A block diagram of the COP414L is given in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2V). When a bit is reset, it is a logic "0" (less than 0.8V).

All functional references to the COP414L also apply to the COP314L, and COP214L.

PROGRAM MEMORY

Program Memory consists of a 512-byte ROM. As can be seen by an examination of the COP414L instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 8 pages of 64 words each.

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by the 9-bit subroutine save registers, SA and SB, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

DATA MEMORY

Data memory consists of a 128-bit RAM, organized as 4 data registers of 8 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 3 bits of the 4-bit Bd select 1 of 8 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3,15 instruction.

The most significant bit of Bd is not used to select a RAM digit. Hence each physical digit of RAM may be selected by two different values of Bd as shown in *Figure 4* below. The skip condition for XIS and XDS instructions will be true if Bd changes between 0 and 15, but NOT between 7 and 8 (see Table III).

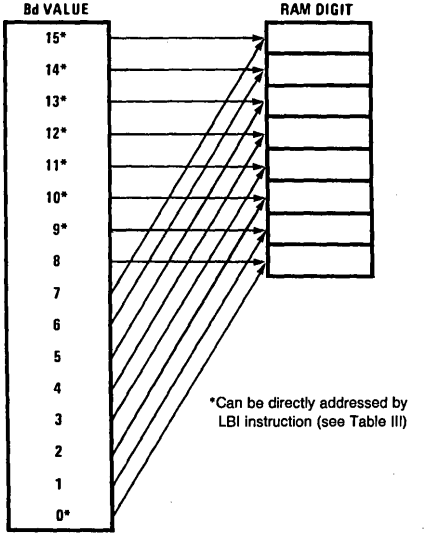

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FIGURE 4. RAM Digit Address to Physical RAM Digit Mapping

Functional Description (Continued)

INTERNAL LOGIC

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions of the COP414L, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

The G register contents are outputs to 4 general-purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M.

The SIO register functions as a 4-bit serial-in serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

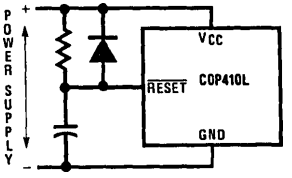
The XAS instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL in the shift register mode, SK outputs SKL ANDed with internal instruction cycle clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3–EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occuring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.
2. EN_1 is not used. It has no effect on COP414L operation.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. EN_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". Table I provides a summary of the modes associated with EN_3 and EN_0.

INITIALIZATION

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 μs. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the $\overline{RESET}$ pin as shown below *(Figure 5)*. The $\overline{RESET}$ pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the $\overline{RESET}$ input, provided it stays low for at least three instruction cycle times.



RC ≥ 5 × Power Supply Rise Time TL/DD/8814-6

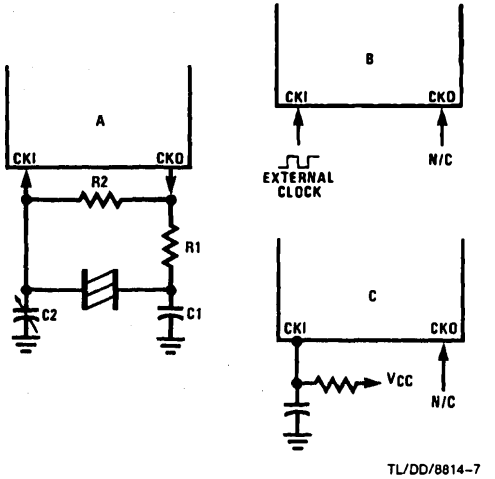
FIGURE 5. Power-Up Clear Circuit

TABLE I. Enable Register Modes—Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

Functional Description (Continued)

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.



TL/DD/8814-7

Ceramic Resonator Oscillator

Resonator Value	Components Values			
	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)
455 kHz	4.7k	1M	220	220

RC Controlled Oscillator

R (kΩ)	C (pF)	Instruction Cycle Time In μs
51	100	19 ±15%
82	56	19 ±13%

Note: 200 kΩ ≥ R ≥ 25 kΩ. 360 pF ≥ C ≥ 50 pF. Does not include tolerances.

FIGURE 6. COP414L Oscillator

OSCILLATOR

There are four basic clock oscillator configurations available as shown by *Figure 6*.

a. Resonator Controlled Oscillator. CKI and CKO are connected to an external ceramic resonator. The instruction cycle frequency equals the resonator frequency divided by 8.

b. External Oscillator. CKI is an external clock input signal. The external frequency is divided by 4 to give the instruction frequency time. CKO is no connection.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is no connection.

CKO PIN OPTIONS

In a resonator controlled oscillator system, CKO is used as an output to the resonator network. CKO is no connection for External or RC controlled oscillator.

I/O OPTIONS

COP414L inputs and outputs have the following optional configurations, illustrated in *Figure 7*:

a. Standard—an enhancement-mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK and all D and G outputs.

b. Open-Drain—an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK and all D and G outputs.

c. Push-Pull—an enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L—same as **a.**, but may be disabled. Available on L outputs only.

e. Open Drain L—same as **b.**, but may be disabled. Available on L outputs only.

f. An on-chip depletion load device to V_{CC}.

g. A Hi-Z input which must be driven to a "1" or "0" by external components.

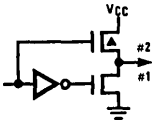
The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1–6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 8* for each of these devices to allow the designer to effectively use these I/O configurations in designing a COP414L system.

The SO, SK outputs can be configured as shown in **a.**, **b.**, or **c.** The G outputs can be configured as shown in **a.** or **b.** Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as in **d.**, or **e.**

An important point to remember if using configuration **d.** with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current. (See *Figure 8*, device 2.) However, when the L port is used as input, the disabled depletion device CANNOT be relied on to source sufficient current to pull an input to a logic "1".

Functional Description (Continued)

a. Standard Output



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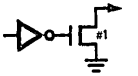
b. Open-Drain Output



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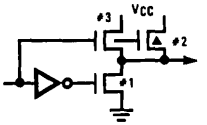
c. Push-Pull Output



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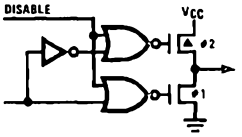
d. Standard L Output



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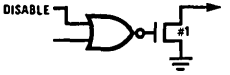
e. Open-Drain L Output



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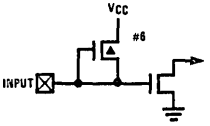
f. Input with Load



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g. Hi-Z Input

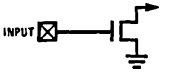

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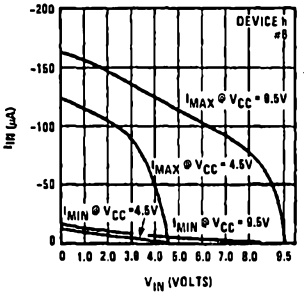
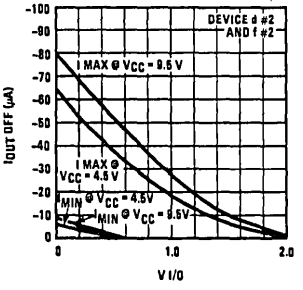
FIGURE 7. Input and Output Configurations

Typical Performance Curves

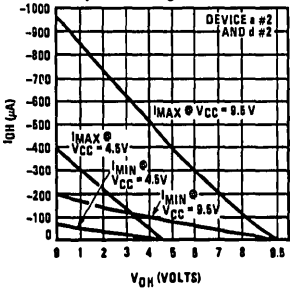
Input Current $\overline{\text{RESET}}$, SI



Input Current for L0 through L7 when Output Programmed Off by Software



Source Current for Standard Output Configuration



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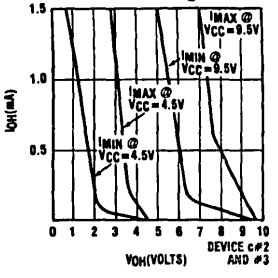
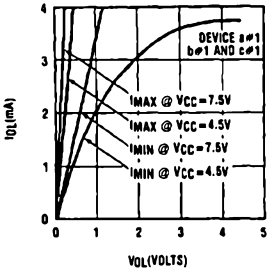
Source Current for SO and SK in Push-Pull Configuration



Output Sink Current For SO and SK



Output Sink Current for L0–L7, and Standard Drive Option for G0–G3

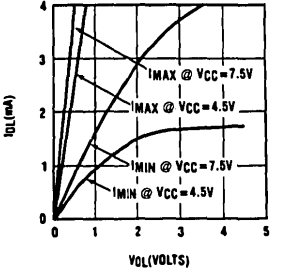


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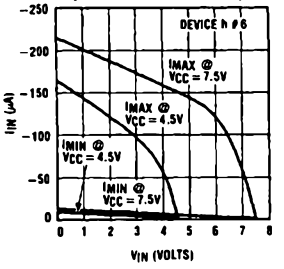
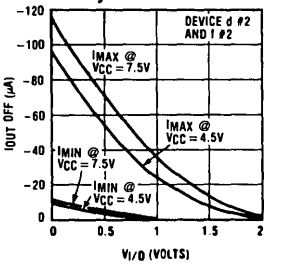
FIGURE 8a. COP414 I/O DC Current Characteristics

Typical Performance Curves (Continued)

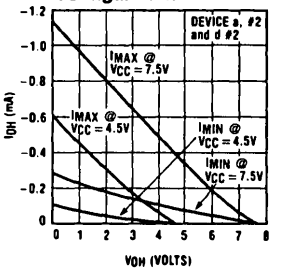
Input Current RESET, SI



Input Current for L0–L7 when Output Programmed Off by Software



Source Current for Standard Output Configuration



Source Current for SO and SK in Push-Pull Configuration

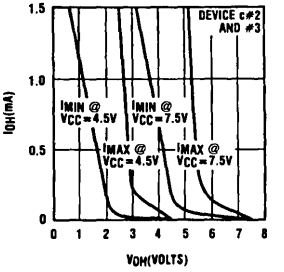


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FIGURE 8b. COP314L Input/Output Characteristics

COP414L Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table III provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP414L instruction set.

TABLE II. COP414L Instruction Set Table Symbols

Symbol	Definition
INTERNAL ARCHITECTURE SYMBOLS	
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 bits of B (register address)
Bd	Lower 4 bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to latch data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM Memory pointed to by B Register
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to latch data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-Controlled Clock Output

Symbol	Definition
INSTRUCTION OPERAND SYMBOLS	
d	4-bit Operand Field, 0–15 binary (RAM Digit Select)
r	2-bit Operand Field, 0–3 binary (RAM Register Select)
a	9-bit Operand Field, 0–511 binary (ROM Address)
y	4-bit Operand Field, 0–15 binary (Immediate Data)
RAM(s)	Contents of RAM location addressed by s
ROM(t)	Contents of ROM location addressed by t
OPERATIONAL SYMBOLS	
+	Plus
−	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of values

TABLE III. COP414L Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	|0011|0000|	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	|0011|0001|	A + RAM(B) → A	None	Add RAM to A
AISC	y	5–	|0101| y |	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CLRA		00	|0000|0000|	0 → A	None	Clear A
COMP		40	|0100|0000|	$\overline{A}$ → A	None	One's complement of A to A
NOP		44	|0100|0100|	None	None	No Operation
RC		32	|0011|0010|	"0" → C	None	Reset C
SC		22	|0010|0010|	"1" → C	None	Set C
XOR		02	|0000|0010|	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

COP414L Instruction Set (Continued)

TABLE III. COP414L Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER OF CONTROL INSTRUCTIONS						
JID		FF	1111 1111	ROM (PC_8,A,M) $PC_{7:0}$	None	Jump Indirect (Note 2)
JMP	a	6– – –	0110 000 a_8 $a_{7:0}$	a → PC	None	Jump
JP	a	– –	1 $a_{6:0}$ (pages 2, 3 only) or 11 $a_{5:0}$ (all other pages)	a → $PC_{6:0}$ a → $PC_{5:0}$	None	Jump within Page (Note 3)
JSRP	a	– –	10 $a_{5:0}$	PC + 1 → SA → SB 010 → $PC_{8:6}$ a → $PC_{5:0}$	None	Jump to Subroutine Page (Note 4)
JSR	a	6– – –	0110 100 a_8 $a_{7:0}$	PC + 1 → SA → SB a → PC	None	Jump to Subroutine
RET		48	0100 1000	SB → SA → PC	None	Return from Subroutine
RETSK		49	0100 1001	SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
MEMORY REFERENCE INSTRUCTIONS						
CAMQ		33 3C	0011 0011 0011 1100	A → $Q_{7:4}$ RAM(B) → $Q_{3:0}$	None	Copy A, RAM to Q
LD	r	–5	00 r 0101	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LQID		BF	1011 1111	ROM(PC_8, A, M) → Q SA → SB	None	Load Q Indirect (Note 2)
RMB	0 1 2 3	4C 45 42 43	0100 1100 0100 0101 0100 0010 0100 0011	0 → $RAM(B)_0$ 0 → $RAM(B)_1$ 0 → $RAM(B)_2$ 0 → $RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100 1101 0100 0111 0100 0110 0100 1011	1 → $RAM(B)_0$ 1 → $RAM(B)_1$ 1 → $RAM(B)_2$ 1 → $RAM(B)_3$	None	Set RAM Bit
STII	y	7–	0111 y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate and Increment Bd
X	r	–6	00 r 0110	RAM(B) ⟷ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3, 15	23 BF	0010 0011 1011 1111	RAM(3,15) ⟷ A	None	Exchange A with RAM (3,15)
XDS	r	–7	00 r 0111	RAM(B) ⟷ A Bd – 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	–4	00 r 0100	RAM(B) ⟷ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd Exclusive-OR Br with r

COP414L Instruction Set (Continued)

TABLE III. COP414L Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 | 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 | 1110	Bd → A	None	Copy Bd to A
LBI	r,d	– –	00 | r | (d – 1) (d = 0,9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 5)
LEI	y	33 6–	0011 | 0011 0010 | y	y → EN	None	Load EN Immediate (Note 6)
TEST INSTRUCTIONS						
SKC		20	0010 | 0000		C = "1"	Skip if C is True
SKE		21	0010 | 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 | 0011 0010 | 0001		$G_{3:0}$ = 0	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 | 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 | 0001	2nd byte	G_0 = 0	
	1	11	0001 | 0001		G_1 = 0	
	2	03	0000 | 0011		G_2 = 0	
	3	13	0001 | 0011		G_3 = 0	
SKMBZ	0	01	0000 | 0001		$RAM(B)_0$ = 0	Skip if RAM Bit is Zero
	1	11	0001 | 0001		$RAM(B)_1$ = 0	
	2	03	0000 | 0011		$RAM(B)_2$ = 0	
	3	13	0001 | 0011		$RAM(B)_3$ = 0	
INPUT/OUTPUT INSTRUCTIONS						
ING		33 2A	0011 | 0011 0010 | 1010	G → A	None	Input G Ports to A
INL		33 2E	0011 | 0011 0010 | 1110	$L_{7:4}$ → RAM(B) $L_{3:0}$ → A	None	Input L Ports to RAM, A
OBD		33 3E	0011 | 0011 0011 | 1110	Bd → D	None	Output Bd to D Outputs
OMG		33 3A	0011 | 0011 0011 | 1010	RAM(B) → G	None	Output RAM to G Ports
XAS		4F	0100 | 1111	A ⟷ SIO, C → SKL	None	Exchange A with SIO (Note 2)

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: For additional information on the operation of the XAS, JID, and LQID instructions, see below.

Note 3: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 4: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 5: The machine code for the lower 4 bits of the LBI instruction equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111_2).

Note 6: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Option List

The COP414L mask-programmable options are assigned numbers which correspond with the COP414L pins.

The following is a list of COP414L options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1: L_4 Driver
- = 0: Standard output
- = 1: Open-drain output

Option 2: V_{CC} Pin
- = 0: Standard V_{CC}
- = 1: Optional higher voltage V_{CC}

Option 3: L_3 Driver
same as Option 1

Option 4: L_2 Driver
same as Option 1

Option 5: L_1 Driver
same as Option 1

Option 6: L_6 Driver
same as Option 1

Option 7: SI Input
- = 0: load device to V_{CC}
- = 1: Hi-Z Output

Option 8: SO Driver
- = 0: Standard output
- = 1: Open-drain output
- = 2: Push-pull output

Option 9: SK Driver
same as Option 8

Option 10:
- = 0: Ground Pin—no options available

Option 11: G_0 I/O Port
- = 0: Standard output
- = 1: Open-drain output

Option 12: G_1 I/O Port
same as Option 11

Option 13: G_2 I/O Port
same as Option 11

Option 14: G_3 I/O Port
same as Option 11

Option 15: CKO Output
- = 0: Clock output to ceramic resonator/crystal
- = 1: No connection

Option 16: CKI Input
- = 0: Ocillator input divided by 8 (500 kHz max)
- = 1: Single pin RC controlled oscillator divided by 4
- = 2: External Schmitt trigger level clock divided by 4

Option 17: $\overline{\text{RESET}}$ Input
- = 0: Load device to V_{CC}
- = 1: Hi-Z Input

Option 18: L_7 Driver
same as Option 1

Option 19: L_6 Driver
same as Option 1

Option 20: L_6 Driver
same as Option 1

Option 21: L Input Levels
- = 0: Standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: Higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 22: G Input Levels
same as Option 21

Option 23: SI Input Levels
same as Option 21

TEST MODE (NON-STANDARD OPERATION)

The SO output has been configured to provide for standard test procedures for the custom-programmed COP414L. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing tests only.

COP414L Option List

Please fill out the Option List and send it with the EPROM.

Option Data

OPTION 1 VALUE = _____ IS: L_4 DRIVER
OPTION 2 VALUE = _____ IS: V_{CC} PIN
OPTION 3 VALUE = _____ IS: L_3 DRIVER
OPTION 4 VALUE = _____ IS: L_2 DRIVER
OPTION 5 VALUE = _____ IS: L_1 DRIVER
OPTION 6 VALUE = _____ IS: L_6 DRIVER
OPTION 7 VALUE = _____ IS: SI INPUT
OPTION 8 VALUE = _____ IS: SO DRIVER
OPTION 9 VALUE = _____ IS: SK DRIVER
OPTION 10 VALUE = 0 IS: GROUND PIN
OPTION 11 VALUE = _____ IS: G_0 I/O PORT
OPTION 12 VALUE = _____ IS: G_1 I/O PORT
OPTION 13 VALUE = _____ IS: G_2 I/O PORT
OPTION 14 VALUE = _____ IS: G_3 I/O PORT
OPTION 15 VALUE = _____ IS: CKO OUTPUT
OPTION 16 VALUE = _____ IS: CKI INPUT
OPTION 17 VALUE = _____ IS: RESET INPUT
OPTION 18 VALUE = _____ IS: L_7 DRIVER
OPTION 19 VALUE = _____ IS: L_6 DRIVER
OPTION 20 VALUE = _____ IS: L_6 DRIVER
OPTION 21 VALUE = _____ IS: L INPUT LEVELS
OPTION 22 VALUE = _____ IS: G INPUT LEVELS
OPTION 23 VALUE = _____ IS: SI INPUT LEVELS