



## COP440/COP441/COP442 and COP340/COP341/COP342 Single-Chip N-Channel Microcontrollers

### General Description

The COP440, COP441, COP442, COP340, COP341, and COP342 Single-Chip N-Channel Microcontrollers are members of the COPSTM microcontrollers family, fabricated using N-channel, silicon gate MOS technology. These are complete microcontrollers with all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, various output configuration options, and an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and data manipulation. The COP440 is a 40-pin chip and the COP441 is a 28-pin version of the same circuit (12 I/O lines removed). The COP442 is a 24-pin version (4 more input lines removed). The COP340, COP341, COP342 are functional equivalents of the above devices respectively, but operate with an extended temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ). Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller oriented processor at a low end-product cost.

### Features

- Enhanced, more powerful instruction set
- $2\text{k} \times 8$  ROM,  $160 \times 4$  RAM
- 35 I/O lines (COP440)
- Zero-crossing detect circuitry with hysteresis
- True multi-vectored interrupt from 4 selectable sources (plus restart)
- Four-level subroutine stack (in RAM)
- $4\ \mu\text{s}$  cycle time
- Single supply operation (4.5V–6.3V)
- Programmable time-base counter
- Internal binary counter/register with MICROWIRE™ compatible serial I/O
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- LED drive capability
- MICROBUST™ compatible
- Software/hardware compatible with other members of the COP400 family
- Extended temperature range devices COP340, COP341, COP342 ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Compatible dual CPU device available (COP2440 series)

### Block Diagram

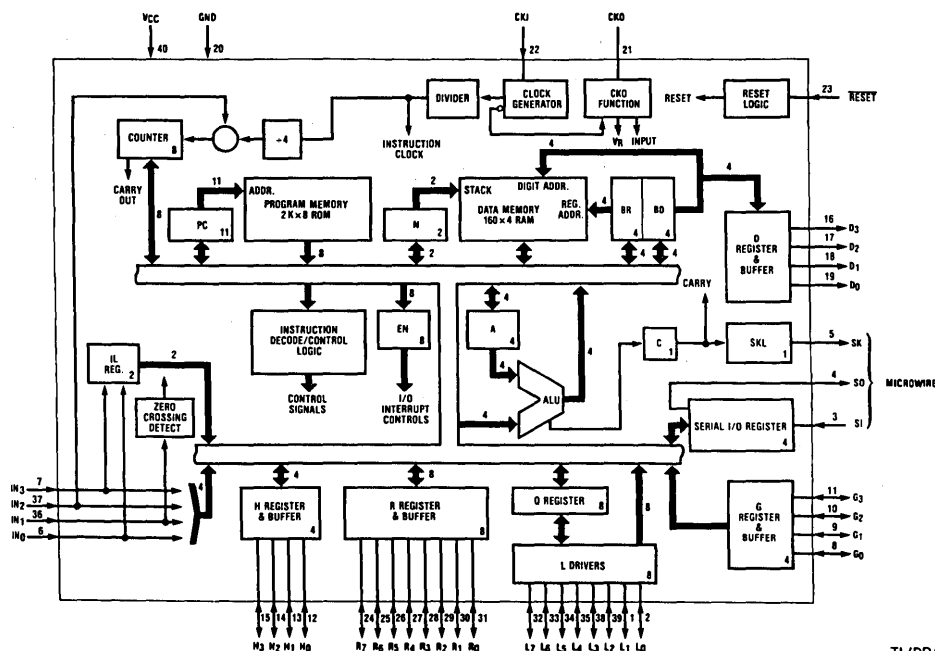


FIGURE 1

TL/DD/6926-1

**COP440/COP441/COP442****Absolute Maximum Ratings**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Zero-Crossing Detect Pin Relative to GND	−1.2V to +15V
Voltage at Any Other Pin Relative to GND	−0.5V to +7V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C

Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.75W at 25°C 0.4W at 70°C
Total Source Current	150 mA
Total Sink Current	75 mA

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

**DC Electrical Characteristics** 0°C ≤ T<sub>A</sub> ≤ +70°C, 4.5V ≤ V<sub>CC</sub> ≤ 6.3V unless otherwise noted

Parameter	Conditions	Min	Max	Units
Operating Voltage (V <sub>CC</sub> )	(Note 3)	4.5	6.3	V
Power Supply Ripple	(Peak to Peak)		0.4	V
Operating Supply Current	(All Inputs and Outputs Open) T <sub>A</sub> = 0°C T <sub>A</sub> = 25°C T <sub>A</sub> = 70°C		44 35 27	mA mA mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷ 16, ÷ 8)				
Logic High (V <sub>IH</sub> )	V <sub>CC</sub> = Max	3.0		V
Logic High (V <sub>IH</sub> )	V <sub>CC</sub> = 5V ± 5%	2.0		V
Logic Low (V <sub>IL</sub> )		−0.3	0.4	V
Schmitt Trigger Input (÷ 4)				
Logic High (V <sub>IH</sub> )		0.7 V <sub>CC</sub>		V
Logic Low (V <sub>IL</sub> )		−0.3	0.6	V
RESET Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V <sub>CC</sub>		V
Logic Low		−0.3	0.6	V
Zero-Crossing Detect Input				
Trip Point	See Figure 7	−0.15	0.15	V
Logic High (V <sub>IH</sub> ) Limit			12	V
Logic Low (V <sub>IL</sub> ) Limit		−0.8		V
SO Input Level (Test Mode)	(Note 5)	2.0	2.5	V
All Other Inputs				
Logic High	V <sub>CC</sub> = Max	3.0		V
Logic High	V <sub>CC</sub> = 5V ± 5%	2.0		V
Logic Low		−0.3	0.8	V
Input Levels High Trip Option				
Logic High		3.6		V
Logic Low		−0.3	1.2	V
Input Capacitance			7.0	pF
Hi-Z Input Leakage		−1.0	+1.0	μA

Note 1: Duty Cycle = t<sub>WI</sub>/(t<sub>WI</sub> + t<sub>WO</sub>).

Note 2: See Figure for additional I/O Characteristics.

Note 3: V<sub>CC</sub> voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 4: Exercise great care not to exceed maximum device power dissipation limits when direct-driving LEDs (or sourcing similar loads) at high temperature.

Note 5: SO output "0" level must be less than 0.8V for normal operation.

**COP440/COP441/COP442****DC Electrical Characteristics**  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$  unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Voltage Levels				
Standard Output				
TTL Operation				
Logic High ( $V_{OH}$ )	$I_{OH} = -100\text{ }\mu\text{A}$	2.4		V
Logic Low ( $V_{OL}$ )	$I_{OL} = 1.6\text{ mA}$		0.4	V
CMOS Operation (Note 1)				
Logic High ( $V_{OH}$ )	$I_{OH} = -10\text{ }\mu\text{A}$	$V_{CC} - 0.4$		V
Logic Low ( $V_{OL}$ )	$I_{OL} = 10\text{ }\mu\text{A}$		0.2	V
Output Current Levels				
Standard Output Source Current	$V_{CC} = 4.5\text{V}$ , $V_{OH} = 2.4\text{V}$	-100	-650	$\mu\text{A}$
LED Direct Drive Output	$V_{CC} = 6\text{V}$ , $V_{OH} = 2\text{V}$			
Logic High ( $I_{OH}$ )		-2.5	-17	mA
TRI-STATE Output Leakage Current		-2.5	+2.5	$\mu\text{A}$
CKO Output				
Oscillator Output Option				
Logic High	$V_{OH} = 2\text{V}$	-0.2		mA
Logic Low	$V_{OL} = 0.4\text{V}$	0.4		mA
$V_R$ RAM Power Supply Option				
Supply Current	$V_R = 3.3\text{V}$		3.0	mA
CKI Sink Current (RC Option)	$V_{IH} = 3.5\text{V}$ , $V_{CC} = 4.5\text{V}$	2.0		mA
Input Current Levels				
Zero-Crossing Detect Input				
Resistance	$V_{IH} = 1.0\text{V}$	0.9	4.6	$\text{k}\Omega$
Input Load Source Current	$V_{IH} = 2.0\text{V}$ , $V_{CC} = 4.5\text{V}$	14	230	$\mu\text{A}$
Total Sink Current Allowed				
All I/O Combined			75	mA
Each L, R Port			20	mA
Each D, G, H Port			10	mA
SO, SK			2.5	mA
Total Source Current Allowed				
All I/O Combined			150	mA
L Port			120	mA
$L_7-L_4$			70	mA
$L_3-L_0$			70	mA
Each L Pin			23	mA
All Other Output Pins			1.6	mA

Note 1: TRI-STATE and LED configurations are excluded.

**COP340/COP341/COP342****Absolute Maximum Ratings**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Zero-Crossing Detect Pin Relative to GND	−1.2V to +15V
Voltage at Any Other Pin Relative to GND	−0.5V to +7V
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C

Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.75W at 25°C 0.25W at 85°C
Total Source Current	150 mA
Total Sink Current	75 mA

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

**DC Electrical Characteristics** −40°C ≤ T<sub>A</sub> ≤ +85°C, 4.5V ≤ V<sub>CC</sub> ≤ 5.5V unless otherwise noted

Parameter	Conditions	Min	Max	Units
Operating Voltage (V <sub>CC</sub> )	(Note 3)	4.5	5.5	V
Power Supply Ripple	(Peak to Peak)		0.4	V
Operating Supply Current	(All Inputs and Outputs Open) T <sub>A</sub> = −40°C T <sub>A</sub> = 25°C T <sub>A</sub> = 85°C		54 35 25	mA mA mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input (÷ 16, ÷ 8)	V <sub>CC</sub> = Max	3.0		V
Logic High (V <sub>IH</sub> )		2.2		V
Logic Low (V <sub>IL</sub> )		−0.3	0.3	V
Schmitt Trigger Input (÷ 4)				
Logic High (V <sub>IH</sub> )		0.7 V <sub>CC</sub>		V
Logic Low (V <sub>IL</sub> )		−0.3	0.4	V
RESET Input Levels	(Schmitt Trigger Input)			
Logic High		0.7 V <sub>CC</sub>		V
Logic Low		−0.3	0.4	V
Zero-Crossing Detect Input	See Figure 7			
Trip Point		−0.15	0.15	V
Logic High (V <sub>IH</sub> ) Limit			12	V
Logic Low (V <sub>IL</sub> ) Limit		−0.8		V
SO Input Level (Test Mode)	(Note 5)	2.2	2.4	V
All Other Inputs	V <sub>CC</sub> = Max	3.0		V
Logic High		2.2		V
Logic Low		−0.3	0.6	V
Input Levels High Trip Option				
Logic High		3.6		V
Logic Low		−0.3	1.2	V
Input Capacitance			7.0	pF
Hi-Z Input Leakage		−2.0	+2.0	μA

Note 1: Duty Cycle = t<sub>WI</sub>/(t<sub>WI</sub> + t<sub>WO</sub>).

Note 2: See Figure for additional I/O Characteristics.

Note 3: V<sub>CC</sub> voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 4: Exercise great care not to exceed maximum device power dissipation limits when direct-driving LEDs (or sourcing similar loads) at high temperature.

Note 5: SO output "0" level must be less than 0.6V for normal operation.

**COP340/COP341/COP342****DC Electrical Characteristics**-40°C ≤ T<sub>A</sub> ≤ +85°C, 4.5V ≤ V<sub>CC</sub> ≤ 5.5V unless otherwise noted (Continued)

Parameter	Conditions	Min	Max	Units
Output Voltage Levels				
Standard Output				
TTL Operation				
Logic High (V <sub>OH</sub> )	I <sub>OH</sub> = -100 μA	2.4		V
Logic Low (V <sub>OL</sub> )	I <sub>OL</sub> = 1.6 mA		0.4	V
CMOS Operation (Note 1)				
Logic High (V <sub>OH</sub> )	I <sub>OH</sub> = -10 μA	V <sub>CC</sub> - 0.5		V
Logic Low (V <sub>OL</sub> )	I <sub>OL</sub> = 10 μA		0.2	V
Output Current Levels				
Standard Output Source Current	V <sub>CC</sub> = 4.5V, V <sub>OH</sub> = 2.4V	-100	-800	μA
LED Direct Drive Output	V <sub>CC</sub> = 5V (Note 4)			
Logic High (I <sub>OH</sub> )	V <sub>OH</sub> = 2V	-1.5	-15	mA
TRI-STATE Output Leakage Current		-5.0	+5.0	μA
CKO Output				
Oscillator Output Option				
Logic High	V <sub>OH</sub> = 2V	-0.2		mA
Logic Low	V <sub>OL</sub> = 0.4V	0.4		mA
V <sub>R</sub> RAM Power Supply Option				
Supply Current	V <sub>R</sub> = 3.3V		4.0	mA
CKI Sink Current (RC Option)	V <sub>CC</sub> = 4.5V, V <sub>IH</sub> = 3.5V	2.0		mA
Input Current Levels				
Zero-Crossing Detect Input				
Resistance	V <sub>IH</sub> = 1.0V	0.9	4.6	kΩ
Input Load Source Current	V <sub>IH</sub> = 2.0V, V <sub>CC</sub> = 4.5V	14	280	μA
Total Sink Current Allowed				
All I/O Combined			75	mA
Each L, R Port			20	mA
Each D, G, H Port			10	mA
SO, SK			2.5	mA
Total Source Current Allowed				
All I/O Combined			150	mA
L Port			120	mA
L <sub>7</sub> -L <sub>4</sub>			70	mA
L <sub>3</sub> -L <sub>0</sub>			70	mA
Each L Pin			23	mA
All Other Output Pins			1.6	mA

**Note 1:** TRI-STATE and LED configurations are excluded.

## AC Electrical Characteristics

COP440/COP441/COP442:  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$  unless otherwise noted

COP340/COP341/COP342:  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$  unless otherwise noted

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time- $t_E$	$\div 16$ Mode	4.0	10	$\mu\text{s}$
CKI Frequency	$\div 8$ Mode	1.6	4.0	MHz
	$\div 4$ Mode	0.8	2.0	MHz
Duty Cycle (Note 1)	$f_I = 4$ MHz	0.4	1.0	MHz
Rise Time	$f_I = 4$ MHz External Clock	30	60	%
Fall Time	$f_I = 4$ MHz External Clock		60	ns
CKI Using RC (Figure 9c)	$\div 4$ Mode		40	ns
Frequency	$R = 15\text{ k}\Omega \pm 5\%$ , $C = 100\text{ pF} \pm 10\%$	0.5	1.0	MHz
Instruction Execution Time- $t_E$ (Note 1)		4.0	8.0	$\mu\text{s}$
<b>INPUTS: (Figure 4)</b>				
SI				
$t_{\text{SETUP}}$		0.3		$\mu\text{s}$
$t_{\text{HOLD}}$		300		ns
All Other Inputs				
$t_{\text{SETUP}}$		1.7		$\mu\text{s}$
$t_{\text{HOLD}}$		300		ns
<b>OUTPUT PROPAGATION DELAY</b>				
CKO	Test Condition: $C_L = 50\text{ pF}$ , $V_{\text{OUT}} = 1.5\text{V}$			
$t_{\text{pd1}}$ , $t_{\text{pd0}}$	Crystal Input		0.17	$\mu\text{s}$
$t_{\text{pd1}}$ , $t_{\text{pd0}}$	Schmitt Trigger Input		0.3	$\mu\text{s}$
SO, SK				
$t_{\text{pd1}}$ , $t_{\text{pd0}}$	$R_L = 2.4\text{ k}\Omega$		1.0	$\mu\text{s}$
All Other Outputs	$R_L = 5.0\text{ k}\Omega$		1.4	$\mu\text{s}$
<b>MICROBUS TIMING</b>				
Read Operation (Figure 2a)	$C_L = 100\text{ pF}$ , $V_{CC} = 5\text{V} \pm 5\%$ TRI-STATE Outputs			
Chip Select Stable Before $\overline{\text{RD}}$ - $t_{\text{CSR}}$		65		ns
Chip Select Hold Time for $\overline{\text{RD}}$ - $t_{\text{RCS}}$		20		ns
$\overline{\text{RD}}$ Pulse Width- $t_{\text{RR}}$		400		ns
Data Delay from $\overline{\text{RD}}$ - $t_{\text{RD}}$			375	ns
$\overline{\text{RD}}$ to Data Floating- $t_{\text{DF}}$			250	ns
Write Operation (Figure 2b)				
Chip Select Stable Before $\overline{\text{WR}}$ - $t_{\text{CSW}}$		65		ns
Chip Select Hold Time for $\overline{\text{WR}}$ - $t_{\text{WCS}}$		20		ns
$\overline{\text{WR}}$ Pulse Width- $t_{\text{WW}}$		400		ns
Data Set-Up Time for $\overline{\text{WR}}$ - $t_{\text{DW}}$		320		ns
Data Hold Time for $\overline{\text{WR}}$ - $t_{\text{WD}}$		100		ns
INTR Transition Time from $\overline{\text{WR}}$ - $t_{\text{WI}}$			700	ns

Note 1: Variation due to the device included.

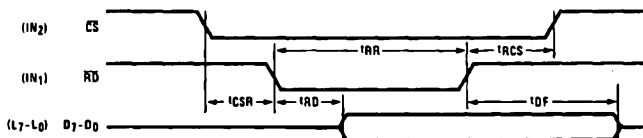


FIGURE 2a. MICROBUS Read Operation Timing

TL/DD/6926-2

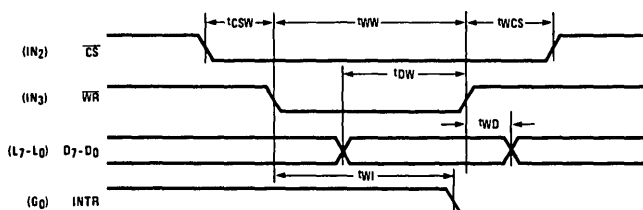
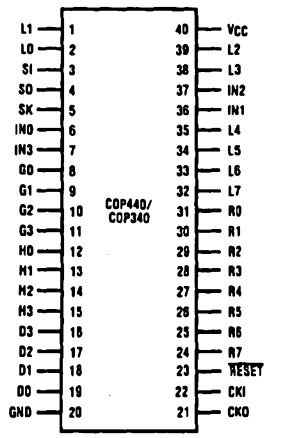


FIGURE 2b. MICROBUS Write Operation Timing

TL/DD/6926-3

## Connection Diagrams

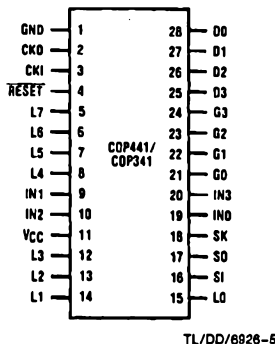
### Dual-In-Line Package



### Top View

Order Number COP440-XXX/D or  
COP340-XXX/D  
See NS Hermetic Package Number  
D40C  
Order Number COP440-XXX/N or  
COP340-XXX/N  
See NS Molded Package Number  
N40A

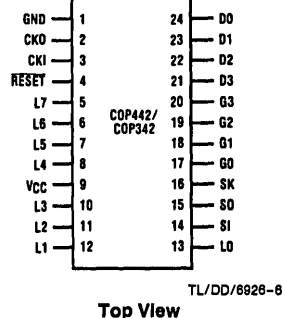
### Dual-In-Line Package



### Top View

Order Number COP441-XXX/D or  
COP341-XXX/D  
See NS Hermetic Package Number  
D28C  
Order Number COP441-XXX/N or  
COP341-XXX/N  
See NS Molded Package Number  
N28B

### Dual-In-Line Package



### Top View

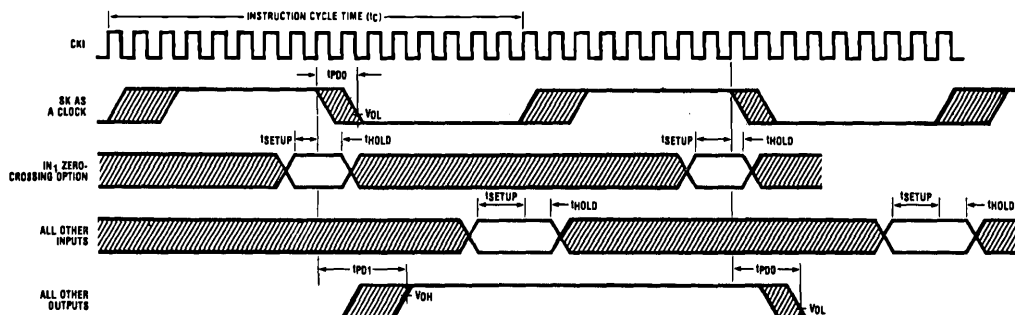
Order Number COP442-XXX/D or  
COP342-XXX/D  
See NS Hermetic Package Number  
D24C  
Order Number COP442-XXX/N or  
COP342-XXX/N  
See NS Molded Package Number  
N24A

## FIGURE 3

## Pin Descriptions

Pin	Description	Pin	Description
L7-L0	8-bit Bidirectional I/O Port with TRI-STATE	CKI	System Oscillator Input
G3-G0	4-bit Bidirectional I/O Port	CKO	System Oscillator Output (or General Purpose Input or RAM Power Supply)
D3-D0	4-bit General Purpose Output Port	RESET	System Reset Input
IN3-IN0	4-bit General Purpose Input Port (Not Available on COP442/COP342)	VCC	Power Supply
S1	Serial Input	GND	Ground
S0	Serial Output (or General Purpose Output)	H3-H0	4-bit Bidirectional I/O Port (COP440/COP340 Only)
SK	Logic-Controlled Clock (or General Purpose Output)	R7-R0	8-Bit Bidirectional I/O Port with TRI-STATE (COP440/COP340 Only)

## Timing Diagram



## FIGURE 4. Input/Output Timing Diagrams (Divide by 16 Mode)

TL/DD/6926-7

## Functional Description

The block diagram of the COP440 is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2.0V). When a bit is reset, it is a logic "0" (less than 0.8V).

### PROGRAM MEMORY

Program Memory consists of a 2,048 byte ROM. As can be seen by an examination of the COP440 instruction set, these words may be program instructions, constants, or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID, LQID, and LID instructions, ROM must often be thought of as being organized into 32 pages of 64 words each.

ROM addressing is accomplished by an 11-bit PC register. Its binary value selects one of the 2,048 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

### DATA MEMORY

Data memory consists of a 640-bit RAM, organized as 10 data registers of 16 4-bit digits. RAM addressing is implemented by an 8-bit B register whose upper 4 bits (Br) select 1 of 10 (0–9) data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into, or from, or exchanged with the A register (accumulator), it may also be loaded into or from the Q latches, L port, R port, EN register, and T counter (internal time base counter). RAM may also be loaded from 4 bits of a ROM word. RAM addressing may also be performed directly to the lower 8 registers by the LDD and XAD instructions based upon the 7-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs. RAM register 8 (Br = 8) also serves as a subroutine stack. Note that it is possible, but not recommended, to alter the contents of the stack by normal data memory access commands.

### INTERNAL LOGIC

The 4-bit A register (accumulator) is the source and destination register for most I/O arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, N register, to load and input 4 bits of the 8-bit Q latch, EN register, or T counter, to input 4 bits of a ROM word, L or R I/O port data, to input 4-bit G, H, or IN ports, and to perform data exchanges with the SIO register. The accumulator is cleared upon reset.

A 4-bit adder performs the arithmetic and logic functions of the COP440, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below).

The 8-bit T counter is a binary up counter which can be loaded to and from M and A. The input to this counter is software selectable from two sources: the first coming from a divide-by-four prescaler (from instruction cycle frequency) thus providing a 10-bit time base counter; the second coming from IN<sub>2</sub> input, changing the T counter into an 8-bit external event counter (see EN register below). In this mode, a low-going pulse ("1" to "0") of at least 2 instruction cycles wide will increment the counter. When the counter overflows, an overflow flag will be set (see SKT instruction below) and an interrupt signal will be sent to processor X. The T counter is cleared on reset.

Four general-purpose inputs, IN<sub>3</sub>–IN<sub>0</sub>, are provided; IN<sub>1</sub>, IN<sub>2</sub> and IN<sub>3</sub> may be selected, by a mask-programmable option, as Read Strobe, Chip Select, and Write Strobe inputs, respectively, for use in MICROBUS applications; IN<sub>1</sub>, by another mask-programmable option, can be selected as a true zero-crossing detector with the output triggering an interrupt or being interrogated by an instruction. These two mask-programmable options are mutually exclusive.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd. The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port. G<sub>0</sub> may be mask-programmed as an output for MICROBUS applications.

The H register contents are outputs to a 4-bit general-purpose bidirectional I/O port.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control. With the MICROBUS option selected, Q can also be loaded with the 8-bit contents of the L I/O ports upon the occurrence of a write strobe from the host CPU. Note that unlike most other COPS controllers, Q is cleared on reset.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. As explained above, the MICROBUS option allows L I/O port data to be latched into the Q register. The L I/O port can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa–Sg and decimal point segments of the display.

The R register, when enabled, outputs to an 8-bit general-purpose, bidirectional, I/O port.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register; see EN register description, below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream.

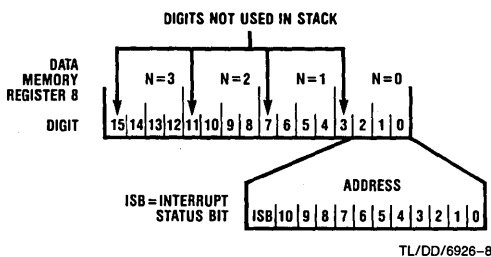
The XAS instruction copies the C flag into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the instruction cycle clock.

The 2-bit N register is a stack pointer to the data memory register 8 where the subroutine return address is located. It points to the next location where the address may be stored



### Functional Description (Continued)

and increments by 1 after each push of the stack, and decrements by 1 before each pop. The N register can be accessed by exchanging its value with A and is cleared on reset. The stack is 4 addresses deep, 12 bits wide, and does not check for overflow or empty conditions. The RAM digit locations where the addresses are stored are shown in *Figure 5*. The LSBs of the addresses are at digits 0, 4, 8, and 12. The MSBs of digits 2, 6, 10, and 14 contain an interrupt status bit (see Interrupt description, below). The four unused digits (3, 7, 11, and 15) can be used as general data storage. When a subroutine call or interrupt occurs, an 11-bit return address and an interrupt status bit are stored in the stack. The N register is then incremented. When a RET or RETSK instruction is executed, the N register is decremented and then the return address is fetched and loaded into the program counter. The address and interrupt status bits remain in the stack, but will be overwritten when the next subroutine call or interrupt occurs.



### FIGURE 5. Subroutine Return Address Stack Organization

The EN register is an internal 8-bit register loaded under program control by the LEI instruction (lower 4 bits) or by the CAME instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register.

0. The least significant bit of the enable register,  $EN_0$ , selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With  $EN_0$  set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of  $EN_3$ . With  $EN_0$  reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK output becomes a logic-controlled clock.

1. With  $EN_1$  set, interrupt is enabled with  $EN_4$  and  $EN_5$  selecting the interrupt source. Immediately following an interrupt,  $EN_1$  is reset to disable further interrupts.
2. With  $EN_2$  set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting  $EN_2$  disables the L drivers, placing the L I/O port in a high-impedance input state. A special feature of the COP440 and COP441 is that the MICROBUS option will change the function of this bit to disable any writing into  $G_0$  when  $EN_2$  is set.
3.  $EN_3$ , in conjunction with  $EN_0$ , affects the SO output. With  $EN_0$  set (binary counter option selected) SO will output the value loaded into  $EN_3$ . With  $EN_0$  reset (serial shift register option selected), setting  $EN_3$  enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting  $EN_3$  with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to "0". Table I below provides a summary of the modes associated with  $EN_3$  and  $EN_0$ .
4.  $EN_5$  and  $EN_4$  select the source of the interrupt signal.
5. The possible sources are as follows:

EN <sub>5</sub>	EN <sub>4</sub>	Interrupt Source
0	0	IN <sub>1</sub> (low-going pulse)
0	1	CKO input (if mask-programmed as an input)
1	0	Zero-crossing (or IN <sub>1</sub> level transition)
1	1	T counter overflows

**EN<sub>4</sub> determines the interrupt routine location.**

6. With EN<sub>6</sub> set, the internal 8-bit T counter will use IN<sub>2</sub> as its input. With EN<sub>6</sub> reset, the input to the T counter is the output of a divide by four prescaler (from instruction cycle frequency), thus providing a 10-bit time-base counter.
7. With EN<sub>7</sub> set, the R outputs are enabled; if EN<sub>7</sub> = 0, the R outputs are disabled.

## INTERRUPT

The following features are associated with the interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC + 1) together with an interrupt status bit, onto the program counter stack residing in data memory. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN<sub>1</sub> is reset. If EN<sub>4</sub> is reset, the next program address is hex 100; if EN<sub>4</sub> is set, the next program address is hex 300; thus providing a different interrupt location for different interrupt sources.

**TABLE I. Enable Register Modes — Bits EN<sub>3</sub> and EN<sub>0</sub>**

EN <sub>3</sub>	EN <sub>0</sub>	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = Clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = Clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

## Functional Description (Continued)

b. An interrupt will be acknowledged only after the following conditions are met:

1.  $EN_1$  has been set.
2. For an external interrupt input, the signal pulse must be at least two instruction cycles wide.
3. A currently executing instruction has been completed.
4. All successive transfer of control instructions and successive LBI's have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).

c. The instruction at hex address 0FF must be a NOP.

d. A CAME or LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

e. If the interrupt signal source is being changed, the interrupt must be disabled prior to, or at, the same time with the change to avoid false interrupts. An interrupt may be enabled only if the interrupt source is not changing. A sample code for changing the interrupt source and enabling the interrupt is as follows:

```
CAME      ; disable interrupt & alter interrupt source
SMB 1     ; set interrupt enable bit
CAME      ; enable interrupt
```

f. An interrupt status bit is stored together with the return address in the stack. The status bit is set if an interrupt occurs at a point in the program where the next instruction is to be skipped; upon returning from the interrupt routine, this set status bit will cause the next instruction to be skipped. Subroutine and interrupt nesting inside interrupt routines are allowed. Note that this differs from the COP420/420C/420L/444L series.

### MICROBUS INTERFACE

(not available in COP442, COP342)

The COP440 series has an option which allows them to be used as peripheral microprocessor devices, inputting and outputting data from and to a host microprocessor ( $\mu P$ ).  $IN_1$ ,  $IN_2$  and  $IN_3$  general purpose inputs become MICROBUS-compatible read-strobe, chip-select, and write-strobe lines, respectively.  $IN_1$  becomes  $\overline{RD}$ —a logic "0" on this input

will cause Q latch data to be enabled to the L ports for input to the  $\mu P$ .  $IN_2$  becomes  $\overline{CS}$ —a logic "0" on this line selects the COPS processor as the  $\mu P$  peripheral device by enabling the operation of the  $\overline{RD}$  and  $\overline{WR}$  lines and allows for the selection of one of several peripheral components.  $IN_3$  becomes  $\overline{WR}$ —a logic "0" on this line will write bus data from the L ports to the Q latches for input to the COPS processor.  $G_0$  becomes  $INTR$ , a "ready" output, reset by a write pulse from the  $\mu P$  on the  $\overline{WR}$  line, providing the "handshaking" capability necessary for asynchronous data transfer between the host CPU and the COPS processor.  $G_0$  output can be separated from other G outputs by the  $EN_2$  bit (see EN description above).

This option has been designed for compatibility with National's MICROBUS—a standard interconnect system for 8-bit parallel data transfer between MOS/LSI CPUs and interfacing devices. (See MICROBUS National Publication.) The functional and timing relationships between the COPS processor signal lines affected by this option are as specified for the MICROBUS interface, and are given in the AC electrical characteristics and shown in the timing diagrams (Figure 2). Connection of the COP440 to the MICROBUS is shown in Figure 6.

Note: TRI-STATE outputs must be used on L port.

### ZERO-CROSSING DETECTION

(not available on the COP442, COP342)

The following features are associated with the  $IN_1$  pin:  $ININ$  and  $INIL$  instructions input the state of  $IN_1$  to  $A_1$ ;  $IN_1$  interrupt generates an interrupt pulse when a low-going transition ("1" to "0") occurs on  $IN_1$ ; zero-crossing interrupt generates an interrupt pulse when an  $IN_1$  transition occurs (both "1" to "0" and "0" to "1").

If the zero-crossing detector is mask-programmed in (see Figure 7a), the  $INIL$  instruction and zero-crossing interrupt will input the state of  $IN_1$  through the true zero-crossing detector ("1" if input > 0V, "0" if input < 0V). The  $ININ$  instruction and  $IN_1$  interrupt will then have unique logic HIGH and LOW levels depending on the  $IN$  port input level chosen. If normal (TTL) level is chosen, logic HIGH level is 3.0V (3.3V for COP340/341) and logic LOW level is 0.8V

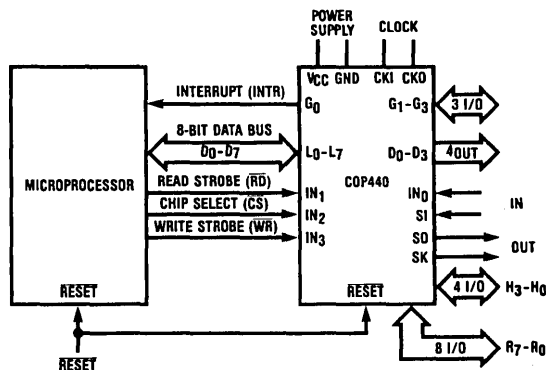


FIGURE 6. MICROBUS Option Interconnect

TL/DD/6926-9



## Functional Description (Continued)

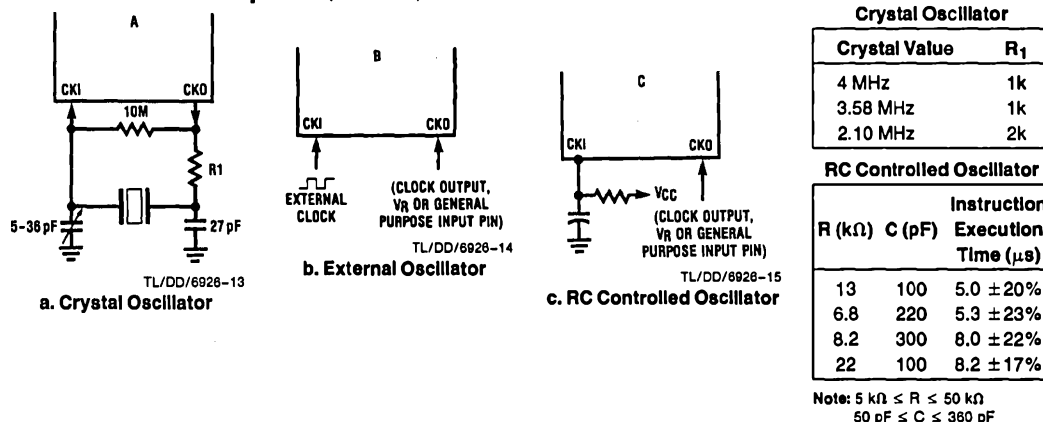


FIGURE 9. COP440/441/442 Oscillators

its connection to a standby/backup power supply to maintain the data integrity of RAM registers 0-3 with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either of the two latter options is appropriate in applications where the system configuration does not require use of the CKO pin for timing functions.

**RAM KEEP-ALIVE OPTION**

Selecting CKO as the RAM power supply ( $V_R$ ) allows the user to shut off the chip power supply ( $V_{CC}$ ) and maintain data in the lower 4 registers of the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. **RESET** must go low before  $V_{CC}$  goes below spec during power-off;  $V_{CC}$  must be within spec before **RESET** goes high on power-up.
2. When  $V_{CC}$  is on,  $V_R$  must be within the operating voltage range of the chip, and within 1V of  $V_{CC}$ .
3.  $V_R$  must be ≥ 3.3V with  $V_{CC}$  off.

**I/O OPTIONS**

COP440 inputs have the following optional configurations, illustrated in Figure 10.

- a. An on-chip depletion load device to  $V_{CC}$ .
- b. A Hi-Z input which must be driven to a "1" or "0" by external components.
- c. A resistive load to GND for the zero-crossing input option (IN<sub>1</sub> only).

COP440 outputs have the following optional configurations:

- d. **Standard**—an enhancement mode device to ground in conjunction with a depletion-mode device to  $V_{CC}$ , compatible with TTL and CMOS input requirements. Available on SO, SK, D, G, and H outputs.
- e. **Open-Drain**—an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, D, G, L, H, and R outputs.
- f. **Push-Pull**—an enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to  $V_{CC}$ . This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

g. **Standard L,R**—same as d., but may be disabled. Available on L and R outputs only (disabled on reset).

h. **LED Direct Drive**—an enhancement-mode device to ground and  $V_{CC}$  together with a depletion device to  $V_{CC}$  meeting the typical current sourcing requirements of the segments of an LED display. The sourcing devices are clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the output in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

Note 1: When the driver is disabled, the depletion device may cause the output to settle down to an intermediate level between  $V_{CC}$  and GND. This voltage cannot be relied upon as a "1" level when reading the L inputs. The external signal must drive it to a "1" level.

Note 2: Much power is dissipated by this driver in driving an LED. Care must be taken to limit the power dissipation of the chip to within the absolute maximum ratings specified.

i. **TRI-STATE Push-Pull**—an enhancement-mode device to ground and  $V_{CC}$ . These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L and R outputs only (in TRI-STATE mode on reset).

j. **Push-Pull R**—same as f., but may be disabled. Available on R outputs only.

k. **Additional depletion pull-up**—a depletion load to  $V_{CC}$  with the same current sourcing capability as the input load a., in addition to the output drive chosen. Available on L and R outputs only. *This device cannot be disabled*; therefore, open-drain outputs with "1" output and TRI-STATE outputs do not show high-impedance characteristics. This device is useful in applications where a pull-up with low source current is desired, e.g., reading keyboards and switches.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6 respectively). Minimum and maximum current ( $I_{OUT}$  and  $V_{OUT}$ ) curves are given in Figures 11 and 12 for each of these devices to allow the designer to effectively use these I/O configurations in designing a COP440 system.



# Typical Performance Characteristics

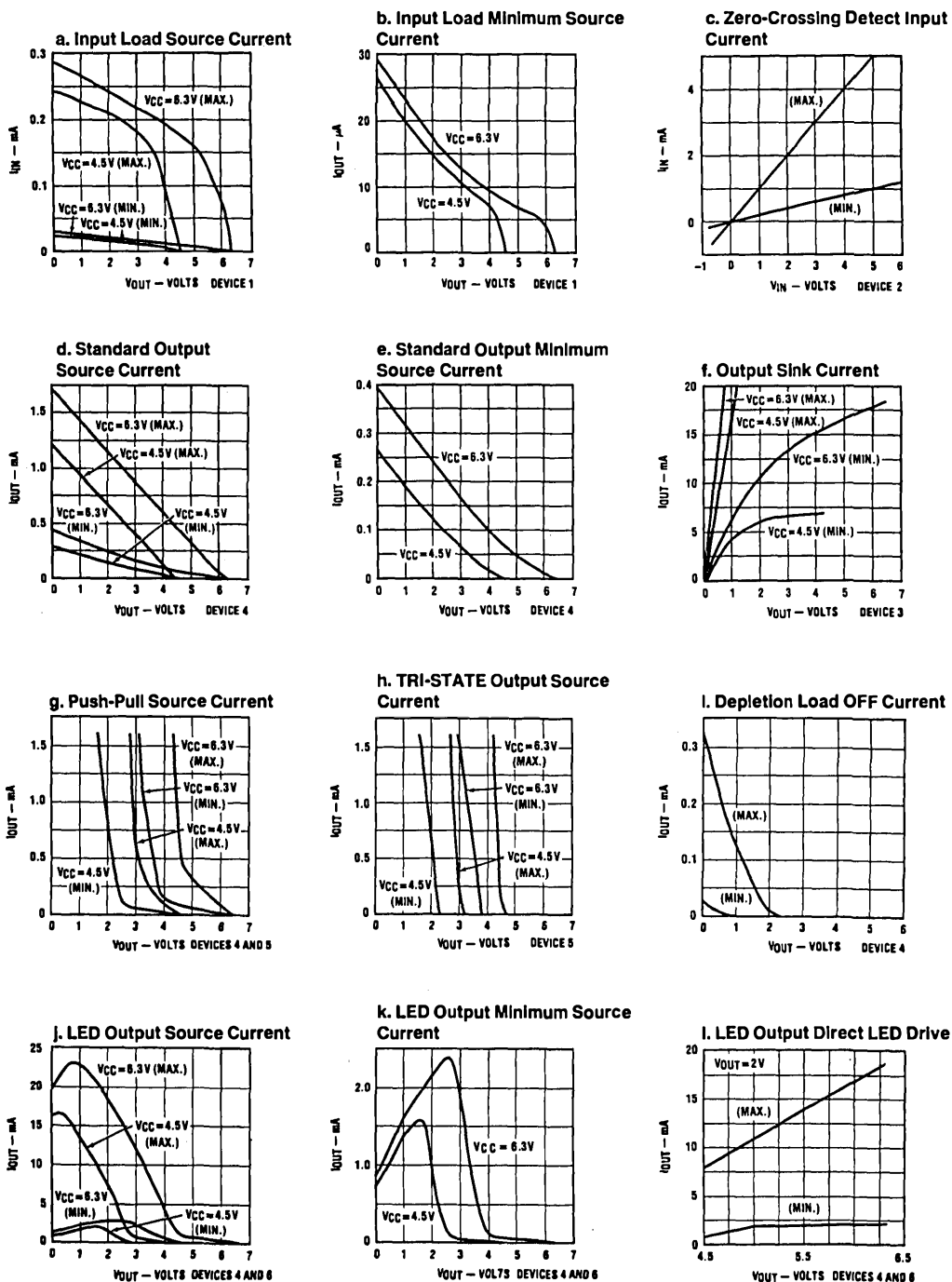


FIGURE 11. COP440/441/442 I/O Characteristics

TL/DD/6926-27

# Typical Performance Characteristics (Continued)

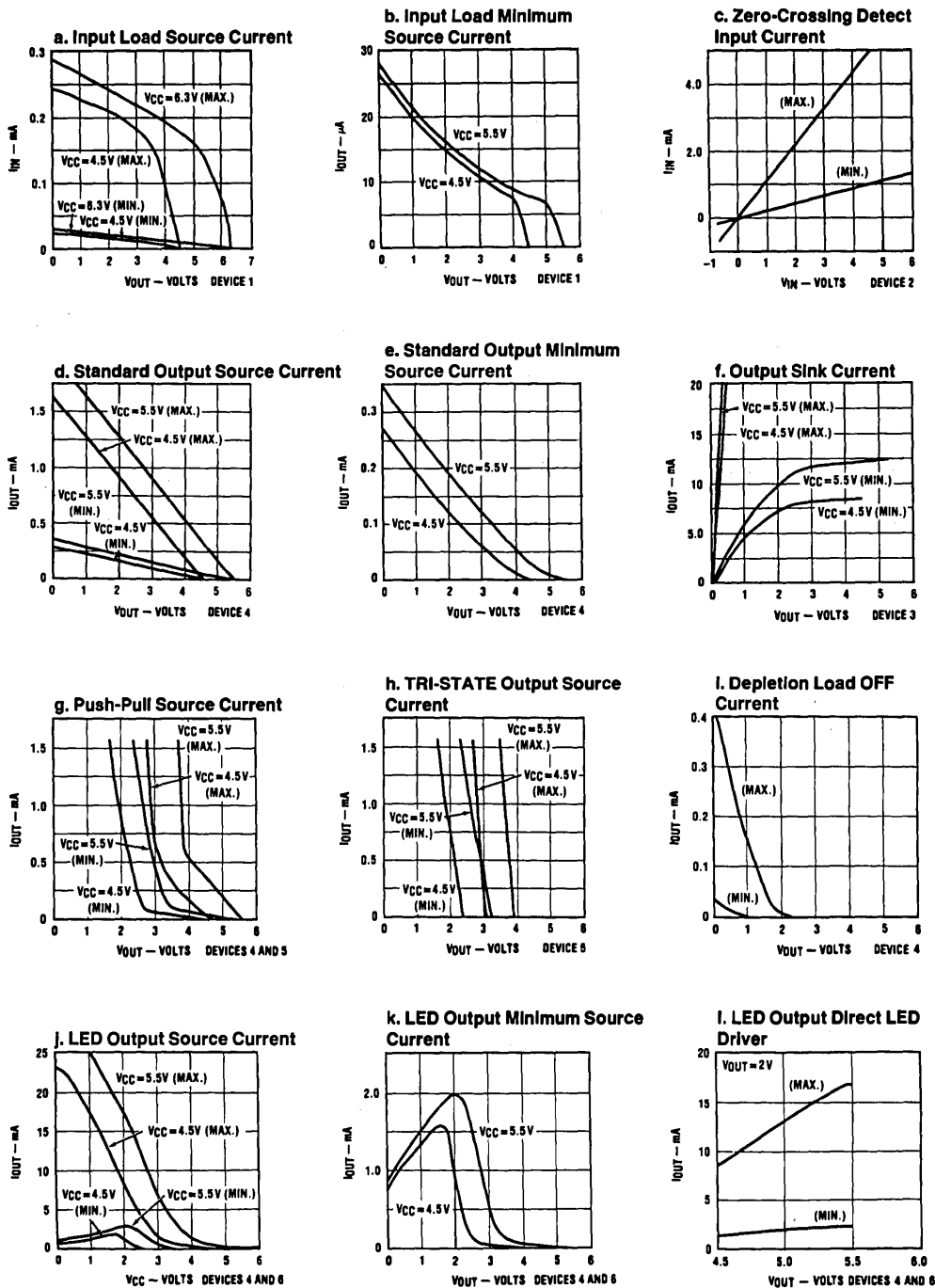


FIGURE 12. CCOP340/341/342 I/O Characteristics

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## Power Dissipation

In order not to damage the device by exceeding the absolute maximum power dissipation rating, the amount of power dissipated inside the chip must be carefully controlled. As an example, an application uses a COP440 in room temperature (25°C) environment with a  $V_{CC}$  power supply of 6V; IN and SI inputs have internal loads; G and D ports drive loads that may sink up to 2 mA into the chip; H port with standard output option reads switches; L port with the LED option drives a multiplexed seven-segment display; R, SO and SK drive MOS inputs that do not source or sink any current.

a. At 25°C, maximum power dissipation allowed = 750 mW

b. Power dissipation by chip except

$$I/O = I_{CC} \times V_{CC} = 35 \text{ mA} \times 6 \text{ V} = 210 \text{ mW}$$

c. Maximum power dissipation by IN,

$$SI = 5 \times 0.3 \text{ mA} \times 6 \text{ V} = 9 \text{ mW}$$

d. G and D ports are sinking current from external loads; maximum output voltage with 2 mA sink current is less than 0.4V. Power dissipation by G and D ports =

$$2 \text{ mA} \times 0.4 \text{ V} \times 8 = 6.4 \text{ mW}$$

e. Maximum power dissipation by H port =

$$4 \times 1.5 \text{ mA} \times 6 \text{ V} = 36 \text{ mW}$$

f. When the seven segments of the LED are turned on, the output voltage is about 2V, so that the segment current is 17 mA. Power dissipation by L port =

$$7 \times 17 \text{ mA} \times (6 \text{ V} - 2 \text{ V}) = 476 \text{ mW}$$

This power dissipation caused by driving LEDs is usually the highest among the various sources.

g. R, SO, and SK do not dissipate any significant amount of power because they do not need to source or sink any current.

Total power dissipation (TPD) inside the device is the sum of items b through g above.

$$TPD = 210 + 9 + 6 + 36 + 476 \text{ mW} = 737 \text{ mW}$$

This is within the 750 mW limit at room temperature. If this application has to operate at 70°C, then the power dissipation must be reduced to meet the limit at that temperature. Some ways to achieve this would be to limit the LED current or to use an external LED driver.

At 70°C the absolute maximum power dissipation rating drops to 400 mW. The user must be careful not to exceed this value.

### COP440 SERIES DEVICES

If the COP440 is bonded as a 28- or 24-pin device, it becomes the COP441 or COP442, respectively, as illustrated in Figure 3. Note that the COP441 and COP442 do not include H and R ports. In addition, the COP442 does not include IN inputs; use of this option precludes the use of the IN options, the interrupt feature with IN as input, the zero-crossing detect option, IN<sub>2</sub> external event counter input, and the MICROBUS option. All other options are available. COP340, COP341, and COP342 are extended temperature versions of the COP440, COP441, and COP442, respectively.

### COP440 Series Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

Table III provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP440 series instruction set.

TABLE II. COP440 Series Instruction Set Symbols

Symbol	Definition	Symbol	Definition
<b>INTERNAL ARCHITECTURE SYMBOLS</b>		<b>INSTRUCTION OPERAND SYMBOLS</b>	
A	4-bit Accumulator	d	4-bit Operand Field, 0–15 binary (RAM Digit Select)
B	8-bit RAM Address Register	r	4-bit Operand Field, 0–9 binary (RAM Register Select)
Br	Upper 4 bits of B (register address)	a	11-bit Operand Field, 0–2047 binary (ROM Address)
Bd	Lower 4 bits of B (digit address)	y	4-bit Operand Field, 0–15 binary (Immediate Data)
C	1-bit Carry Register	RAM(s)	Content of RAM location addressed by s
D	4-bit Data Output Port	RAM <sub>N</sub>	Content of RAM location addressed by stack pointer N
EN	8-bit Enable Register	ROM(t)	Content of ROM location addressed by t
G	4-bit Register to latch data for G I/O Port		
H	4-bit Register to latch data for H I/O Port		
IL	Two 1-bit Latches associated with the IN <sub>3</sub> or IN <sub>0</sub> Inputs		
IN	4-bit Input Port		
IN <sub>1</sub> Z	Zero-Crossing Input		
L	8-bit TRI-STATE I/O Port		
M	4-bit contents of RAM Memory pointed to by B Register		
N	2-bit subroutine return address stack pointer		
PC	11-bit ROM Address Register (program counter)		
Q	8-bit Register to latch data for L I/O Port		
R	8-bit Register to latch data for R TRI-STATE I/O Port		
SIO	4-bit Shift Register and Counter		
SK	Logic-Controlled Clock Output		
T	8-bit Binary Counter Register		
		<b>OPERATIONAL SYMBOLS</b>	
		+	Plus
		–	Minus
		→	Replaces
		↔	Is exchanged with
		=	Is equal to
		$\bar{A}$	The one's complement of A
		⊕	Exclusive-OR
		:	Range of values
		V	OR



## Instruction Set

**TABLE III. COP440 Series Instruction Set**

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
<b>ARITHMETIC/LOGIC INSTRUCTIONS</b>						
ASC		30	<u>0011</u> <u>0000</u>	$A + C + \text{RAM}(B) \rightarrow A$ Carry $\rightarrow C$		Add with Carry, Skip on Carry
ADD		31	<u>0011</u> <u>0001</u>	$A + \text{RAM}(B) \rightarrow A$	None	Add RAM to A
ADT		4A	<u>0100</u> <u>1010</u>	$A + 10_{10} \rightarrow A$	None	Add Ten to A
AISC	y	5-	<u>0101</u> <u>y</u>	$A + y \rightarrow A$	Carry	Add immediate, Skip on Carry (y $\neq$ 0)
CASC		10	<u>0001</u> <u>0000</u>	$\bar{A} + \text{RAM}(B) + C \rightarrow A$ Carry $\rightarrow C$	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	<u>0000</u> <u>0000</u>	$0 \rightarrow A$	None	Clear A
COMP		40	<u>0100</u> <u>0000</u>	$\bar{A} \rightarrow A$	None	One's complement of A to A
NOP		44	<u>0100</u> <u>0100</u>	None	None	No Operation
OR		33 1A	<u>0011</u> <u>0011</u> <u>0001</u> <u>1010</u>	$A \vee M \rightarrow A$	None	OR RAM with A
RC		32	<u>0011</u> <u>0010</u>	"0" $\rightarrow C$	None	Reset C
SC		22	<u>0010</u> <u>0010</u>	"1" $\rightarrow C$	None	Set C
XOR		02	<u>0000</u> <u>0010</u>	$A \oplus \text{RAM}(B) \rightarrow A$	None	Exclusive-OR RAM with A
<b>TRANSFER OF CONTROL INSTRUCTIONS</b>						
JID		FF	<u>1111</u> <u>1111</u>	ROM (PC <sub>10:8</sub> , A, M) $\rightarrow$ PC <sub>7:0</sub>	None	Jump Indirect (Note 3)
JMP	a	6- --	<u>0110</u> <u>0</u> <u>a<sub>10:8</sub></u> <u>a<sub>7:0</sub></u>	$a \rightarrow \text{PC}$	None	Jump
JP	a	-- (pages 2,3 only) or -- (all other pages)	<u>1</u> <u>a<sub>6:0</sub></u> <u>11</u> <u>a<sub>5:0</sub></u>	$a \rightarrow \text{PC}_{6:0}$ $a \rightarrow \text{PC}_{5:0}$	None	Jump within Page (Note 4)
JSRP	a	--	<u>10</u> <u>a<sub>5:0</sub></u>	$\text{PC} + 1 \rightarrow \text{RAM}_N$ $N + 1 \rightarrow N$ $00010 \rightarrow \text{PC}_{10:6}$ $a \rightarrow \text{PC}_{5:0}$	None	Jump to Subroutine Page (Note 5)
JSR	a	6- --	<u>0110</u> <u>1</u> <u>a<sub>10:8</sub></u> <u>a<sub>7:0</sub></u>	$\text{PC} + 1 \rightarrow \text{RAM}_N$ $N + 1 \rightarrow N$ $a \rightarrow \text{PC}$	None	Jump to Subroutine
RET		48	<u>0100</u> <u>1000</u>	$N - 1 \rightarrow N$ $\text{RAM}_N \rightarrow \text{PC}$	None	Return from Subroutine
RETSK		49	<u>0100</u> <u>1001</u>	$N - 1 \rightarrow N$ $\text{RAM}_N \rightarrow \text{PC}$	Always Skip on Return	Return from Subroutine then Skip

## Instruction Set (Continued)

TABLE III. COP440 Series Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description									
MEMORY REFERENCE INSTRUCTIONS															
CAME		33 1F	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0001</td><td>1111</td></tr></table>	0011	0011	0001	1111	$A \rightarrow EN_{7:4}$ $RAM(B) \rightarrow EN_{3:0}$	None	Copy A, RAM to EN					
0011	0011														
0001	1111														
CAMQ		33 3C	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0011</td><td>1100</td></tr></table>	0011	0011	0011	1100	$A \rightarrow Q_{7:4}$ $RAM(B) \rightarrow Q_{3:0}$	None	Copy A, RAM to Q					
0011	0011														
0011	1100														
CAMT		33 3F	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0011</td><td>1111</td></tr></table>	0011	0011	0011	1111	$A \rightarrow T_{7:4}$ $RAM(B) \rightarrow T_{3:0}$	None	Copy A, RAM to T					
0011	0011														
0011	1111														
CEMA		33 0F	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0000</td><td>1111</td></tr></table>	0011	0011	0000	1111	$EN_{7:4} \rightarrow RAM(B)$ $EN_{3:0} \rightarrow A$	None	Copy EN to RAM, A					
0011	0011														
0000	1111														
CQMA		33 2C	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0010</td><td>1100</td></tr></table>	0011	0011	0010	1100	$Q_{7:4} \rightarrow RAM(B)$ $Q_{3:0} \rightarrow A$	None	Copy Q to RAM, A					
0011	0011														
0010	1100														
CTMA		33 2F	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0010</td><td>1111</td></tr></table>	0011	0011	0010	1111	$T_{7:4} \rightarrow RAM(B)$ $T_{3:0} \rightarrow A$	None	Copy T to RAM, A					
0011	0011														
0010	1111														
LD	r	-5	<table><tr><td>00</td><td>r</td><td>0101</td></tr><tr><td colspan="3">r = 0:3</td></tr></table>	00	r	0101	r = 0:3			$RAM(B) \rightarrow A$ $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r			
00	r	0101													
r = 0:3															
LDD	r,d	23 --	<table><tr><td>00</td><td>10</td><td>0011</td></tr><tr><td>0</td><td>r</td><td>d</td></tr><tr><td colspan="3">r = 0:7</td></tr></table>	00	10	0011	0	r	d	r = 0:7			$RAM(r,d) \rightarrow A$	None	Load A with RAM pointed to directly by r,d
00	10	0011													
0	r	d													
r = 0:7															
LID		33 19	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0001</td><td>1001</td></tr></table>	0011	0011	0001	1001	$ROM(PC_{10:8}, A, M) \rightarrow M, A$	None	Load RAM, A Indirect					
0011	0011														
0001	1001														
LQID		BF	<table><tr><td>1011</td><td>1111</td></tr></table>	1011	1111	$ROM(PC_{10:8}, A, M) \rightarrow Q$	None	Load Q Indirect (Note 3)							
1011	1111														
RMB	0 1 2 3	4C 45 42 43	<table><tr><td>0100</td><td>1100</td></tr><tr><td>0100</td><td>0101</td></tr><tr><td>0100</td><td>0010</td></tr><tr><td>0100</td><td>0011</td></tr></table>	0100	1100	0100	0101	0100	0010	0100	0011	$0 \rightarrow RAM(B)_0$ $0 \rightarrow RAM(B)_1$ $0 \rightarrow RAM(B)_2$ $0 \rightarrow RAM(B)_3$	None	Reset RAM Bit	
0100	1100														
0100	0101														
0100	0010														
0100	0011														
SMB	0 1 2 3	4D 47 46 4B	<table><tr><td>0100</td><td>1101</td></tr><tr><td>0100</td><td>0111</td></tr><tr><td>0100</td><td>0110</td></tr><tr><td>0100</td><td>1011</td></tr></table>	0100	1101	0100	0111	0100	0110	0100	1011	$1 \rightarrow RAM(B)_0$ $1 \rightarrow RAM(B)_1$ $1 \rightarrow RAM(B)_2$ $1 \rightarrow RAM(B)_3$	None	Set RAM Bit	
0100	1101														
0100	0111														
0100	0110														
0100	1011														
STII	y	7-	<table><tr><td>0111</td><td>y</td></tr></table>	0111	y	$y \rightarrow RAM(B)$ $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd							
0111	y														
X	r	-6	<table><tr><td>00</td><td>r</td><td>0110</td></tr><tr><td colspan="3">r = 0:3</td></tr></table>	00	r	0110	r = 0:3			$RAM(B) \leftrightarrow A$ $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r			
00	r	0110													
r = 0:3															
XAD	r,d	23 --	<table><tr><td>0010</td><td>0011</td></tr><tr><td>1</td><td>r</td><td>d</td></tr><tr><td colspan="3">r = 0:7</td></tr></table>	0010	0011	1	r	d	r = 0:7			$RAM(r,d) \leftrightarrow A$	None	Exchange A with RAM pointed to directly by r,d	
0010	0011														
1	r	d													
r = 0:7															
XDS	r	-7	<table><tr><td>00</td><td>r</td><td>0111</td></tr><tr><td colspan="3">r = 0:3</td></tr></table>	00	r	0111	r = 0:3			$RAM(B) \leftrightarrow A$ $Bd - 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r			
00	r	0111													
r = 0:3															
XIS	r	-4	<table><tr><td>00</td><td>r</td><td>0100</td></tr><tr><td colspan="3">r = 0:3</td></tr></table>	00	r	0100	r = 0:3			$RAM(B) \leftrightarrow A$ $Bd + 1 \rightarrow Bd$ $Br \oplus r \rightarrow Br$	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r			
00	r	0100													
r = 0:3															

# Instruction Set (Continued)

TABLE III. COP440 Series Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
<b>REGISTER REFERENCE INSTRUCTIONS</b>						
CAB		50	0101 0000	$A \rightarrow Bd$	None	Copy A to Bd
CBA		4E	0100 1110	$Bd \rightarrow A$	None	Copy Bd to A
LBI	r,d	--	00 r (d-1) r = 0:3, d = 0,9:15 or 33 0011 0011 -- 1  r   d r = 0:7, any d	$r,d \rightarrow B$	Skip until not a LBI	Load B Immediate with r,d (Note 6)
LEI	y	33 6-	0011 0011 0110 y	$y \rightarrow EN_{3:0}$	None	Load lower half of EN Immediate
XABR		12	0001 0010	$A \leftrightarrow Br$	None	Exchange A with Br
XAN		33 0B	0011 0011 0000 1011	$A \leftrightarrow N(0,0 \rightarrow A_3, A_2)$	None	Exchange A with N
<b>TEST INSTRUCTIONS</b>						
SKC		20	0010 0000		$C = "1"$	Skip if C is True
SKE		21	0010 0001		$A = RAM(B)$	Skip if A Equals RAM
SKGZ		33 21	0011 0011 0010 0001		$G_{3:0} = 0$	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 0011	1st byte		Skip if G Bit is Zero
	0	01	0000 0001	2nd byte	$G_0 = 0$	
	1	11	0001 0001		$G_1 = 0$	
	2	03	0000 0011		$G_2 = 0$	
	3	13	0001 0011		$G_3 = 0$	
SKMBZ	0	01	0000 0001		$RAM(B)_0 = 0$	Skip if RAM Bit is Zero
	1	11	0001 0001		$RAM(B)_1 = 0$	
	2	03	0000 0011		$RAM(B)_2 = 0$	
	3	13	0001 0011		$RAM(B)_3 = 0$	
SKSZ		33	0011 0011		$SIO = 0$	Skip if SIO is Zero
		1C	0001 1100			
SKT		41	0100 0001		T counter carry has occurred since last test	Skip on Timer (Note 3)

**Instruction Set** (Continued)

TABLE III. COP440 Series Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
<b>INPUT/OUTPUT INSTRUCTIONS</b>						
CAMR		33	<u>0011</u>   <u>0011</u>	$A \rightarrow R_{7:4}$ $RAM(B) \rightarrow R_{3:0}$	None	Output A, RAM to R Port
		3D	<u>0011</u>   <u>1101</u>			
ING		33	<u>0011</u>   <u>0011</u>	$G \rightarrow A$	None	Input G Port to A
		2A	<u>0010</u>   <u>1010</u>			
INH		33	<u>0011</u>   <u>0011</u>	$H \rightarrow A$	None	Input H Port to A
		2B	<u>0010</u>   <u>1011</u>			
ININ		33	<u>0011</u>   <u>0011</u>	$IN \rightarrow A$	None	Input IN Inputs to A (Note 2)
		28	<u>0010</u>   <u>1000</u>			
INIL		33	<u>0011</u>   <u>0011</u>	$IL_3, CKO, IN_1Z, IL_0 \rightarrow A$	None	Input IL Latches to A (Note 3)
		29	<u>0010</u>   <u>1001</u>			
INL		33	<u>0011</u>   <u>0011</u>	$L_{7:4} \rightarrow RAM(B)$ $L_{3:0} \rightarrow A$	None	Input L Port to RAM, A
		2E	<u>0010</u>   <u>1110</u>			
INR		33	<u>0011</u>   <u>0011</u>	$R_{7:4} \rightarrow RAM(B)$ $R_{3:0} \rightarrow A$	None	Input R Port to RAM, A
		2D	<u>0010</u>   <u>1101</u>			
OBD		33	<u>0011</u>   <u>0011</u>	$Bd \rightarrow D$	None	Output Bd to D Port
		3E	<u>0011</u>   <u>1110</u>			
OGI	y	33	<u>0011</u>   <u>0011</u>	$y \rightarrow G$	None	Output to G Port Immediate
		5-	<u>0101</u>   <u>y</u>			
OMG		33	<u>0011</u>   <u>0011</u>	$RAM(B) \rightarrow G$	None	Output RAM to G Port
		3A	<u>0011</u>   <u>1010</u>			
OMH		33	<u>0011</u>   <u>0011</u>	$RAM(B) \rightarrow H$	None	Output RAM to H Port
		3B	<u>0011</u>   <u>1011</u>			
XAS		4F	<u>0100</u>   <u>1111</u>	$A \leftrightarrow SIO, C \rightarrow SKL$	None	Exchange A with SIO (Note 3)

**Note 1:** All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A<sub>3</sub> indicates the most significant (left-most) bit of the 4-bit A register.

**Note 2:** The ININ instruction is not available on the 24-pin COP442/COP342 since this device does not contain the IN inputs.

**Note 3:** For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

**Note 4:** The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

**Note 5:** A JSRP transfers program control to subroutine page 2 (00010 is loaded into the upper 5 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

**Note 6:** LBI is a single-byte instruction if d = 0, 9, 10, 11, 12, 13, 14, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B (Bd) with the value 9 (1001<sub>2</sub>), the lower 4 bits of the LBI instruction equal 8 (1000<sub>2</sub>). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111<sub>2</sub>).

## Description of Selected Instructions

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP440 programs.

## XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

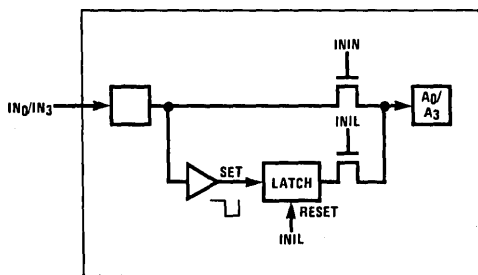
## JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 11-bit word, PC<sub>10:8</sub>. A, M, PC<sub>10</sub>, PC<sub>9</sub> and PC<sub>8</sub> are not affected by this instruction.

**Note that JID requires 2 instruction cycles if executed, 1 instruction cycle time if skipped.**

## INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL<sub>3</sub> and IL<sub>0</sub>, CKO and IN<sub>1</sub> into A (see *Figure 13*). The IL<sub>3</sub> and IL<sub>0</sub> latches are set if a low-going pulse ("1" to "0") has occurred on the IN<sub>3</sub> and IN<sub>0</sub> inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL<sub>3</sub> and IL<sub>0</sub> into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN<sub>3</sub> and IN<sub>0</sub> lines. If CKO is mask-programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. Unlike the COP420/420C/420L/444L series, INIL will input IN<sub>1</sub> into A1.



**FIGURE 13. INIL Hardware Implementation**

If zero-crossing detect is selected, the  $IN_1$  input will go through the detection logic, thus allowing the user to interrogate the input, sending a "1" if the input is above 0V and a "0" if it is below 0V. INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction. It is also useful in checking the status of the zero-crossing detect input. The general purpose inputs  $IN_3$ – $IN_6$  are input to A upon execution of an ININ instruction, and the  $IN_1$  input does not go through zero-crossing logic so that it has the same logic level as the other IN inputs for the ININ instruction (see Figure 9).

**Note:** IL latches are cleared on reset. This is different from the COP420/420C/420L/444L series.

## LOID INSTRUCTION

**LQID** (Load Q indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC<sub>10</sub>:PC<sub>9</sub>, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. Note that LQID takes two instruction cycles if executed and one instruction cycle if skipped. Unlike most other COPS processors, this instruction does not push the stack.

### LID INSTRUCTION

**LID (Load Indirect)** loads M and A with the contents of ROM pointed to by the 11-bit word PC<sub>10</sub>:PC<sub>8</sub>, A, M. Note that LID takes three instruction cycles if executed and two if skipped.

## SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter (see internal logic, above) overflow latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

## INSTRUCTION SET NOTES

- The first word of a COP440 program (ROM address 0) must be a CLRA (Clear A) instruction.
- Although skipped instructions are not executed, they are still fetched from program memory. Thus program paths take the same number of cycle times whether instructions are skipped or executed, except for LID, LQID, and JID.
- The ROM is organized into 32 pages of 64 words each. The Program Counter is an 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, LQID, or LID instruction is the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11, 15, 19, 23, 27, or 31 will access data in the next group of four pages.

## Option List

The COP440 mask-programmable options are assigned numbers which correspond with the COP440 pins.

### Option 1: L<sub>1</sub> I/O Port (see note below)

- = 0: Standard output
- = 1: Open-drain output
- = 2: LED direct drive output
- = 3: TRI-STATE output
- = 4: same as 0 with extra load device to V<sub>CC</sub>
- = 5: same as 1 with extra load device to V<sub>CC</sub>
- = 6: same as 2 with extra load device to V<sub>CC</sub>
- = 7: same as 3 with extra load device to V<sub>CC</sub>

### Option 2: L<sub>0</sub> I/O Port

(same as Option 1)

### Option 3: SI Input

- = 0: Input with load device to V<sub>CC</sub>
- = 1: Hi-Z Input

### Option 4: SO Output

- = 0: Standard output
- = 1: Open-drain output
- = 2: Push-pull output

### Option 5: SK Output

(same as Option 4)

### Option 6: IN<sub>0</sub> Input

(same as Option 3)

### Option 7: IN<sub>3</sub> Input

(same as Option 3)

### Option 8: G<sub>0</sub> I/O Port

- = 0: Standard output
- = 1: Open-drain output

### Option 9: G<sub>1</sub> I/O Port

(same as Option 8)

### Option 10: G<sub>2</sub> I/O Port

(same as Option 8)

### Option 11: G<sub>3</sub> I/O Port

(same as Option 8)

### Option 12: H<sub>0</sub> I/O Port

(same as Option 8)

### Option 13: H<sub>1</sub> I/O Port

(same as Option 8)

### Option 14: H<sub>2</sub> I/O Port

(same as Option 8)

### Option 15: H<sub>3</sub> I/O Port

(same as Option 8)

### Option 16: D<sub>3</sub> Output

(same as Option 8)

### Option 17: D<sub>2</sub> Output

(same as Option 8)

### Option 18: D<sub>1</sub> Output

(same as Option 8)

### Option 19: D<sub>0</sub> Output

(same as Option 8)

### Option 20: GND—No options available

### Option 21: CKO Pin

- = 0: Oscillator output
- = 1: RAM power supply (V<sub>R</sub>) input
- = 2: General purpose input with load device to V<sub>CC</sub>
- = 3: General purpose Hi-Z input

### Option 22: CKI Input

- = 0: Crystal input divided by 16
- = 1: Crystal input divided by 8
- = 2: Single-pin RC controlled oscillator (÷ 4)
- = 3: Schmitt trigger clock input (÷ 4)

### Option 23: $\overline{\text{RESET}}$ Input

(same as Option 3)

### Option 24: R<sub>7</sub> I/O Port (see note below)

- = 0: Standard output
- = 1: Open-drain output
- = 2: Push-pull output
- = 3: TRI-STATE output
- = 4: same as 0 with extra load device to V<sub>CC</sub>
- = 5: same as 1 with extra load device to V<sub>CC</sub>
- = 6: same as 2 with extra load device to V<sub>CC</sub>
- = 7: same as 3 with extra load device to V<sub>CC</sub>

### Option 25: R<sub>6</sub> I/O Port

(same as Option 24)

### Option 26: R<sub>5</sub> I/O Port

(same as Option 24)

### Option 27: R<sub>4</sub> I/O Port

(same as Option 24)

### Option 28: R<sub>3</sub> I/O Port

(same as Option 24)

### Option 29: R<sub>2</sub> I/O Port

(same as Option 24)

### Option 30: R<sub>1</sub> I/O Port

(same as Option 24)

### Option 31: R<sub>0</sub> I/O Port

(same as Option 24)

### Option 32: L<sub>7</sub> I/O Port

(same as Option 1)

### Option 33: L<sub>6</sub> I/O Port

(same as Option 1)

### Option 34: L<sub>5</sub> I/O Port

(same as Option 1)

### Option 35: L<sub>4</sub> I/O Port

(same as Option 1)

### Option 36: IN<sub>1</sub> Input

- = 0: Input with load device to V<sub>CC</sub>
- = 1: Hi-Z Input
- = 2: Zero-crossing detect input (Option 41 = 0)

### Option 37: IN<sub>2</sub> Input

(same as Option 3)

### Option 38: L<sub>3</sub> I/O Port

(same as Option 1)

### Option 39: L<sub>2</sub> I/O Port

(same as Option 1)

### Option 40: V<sub>CC</sub>—no options available

## Option List (Continued)

Option 41: COP Function

- = 0: Normal
- = 1: MICROBUS option

Option 42: IN Input Levels

- = 0: Standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
- = 1: Higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 43: G Input Levels

(same as Option 42)

Option 44: L Input Levels

(same as Option 42)

Option 45: CKO Input Levels

(same as Option 42)

Option 46: SI Input Levels

(same as Option 42)

Option 47: R Input Levels

(same as Option 42)

Option 48: H Input Levels

(same as Option 42)

Option 49: No option available

Option 50: COP Bonding

- = 0: COP440 (40-pin device)
- = 1: COP441 (28-pin device)
- = 2: COP442 (24-pin device)
- = 3: COP440 and COP441
- = 4: COP440 and COP442
- = 5: COP440, COP441, and COP442
- = 6: COP441 and COP442

## COP440 Option Table

The following options information is to be sent to National along with the EPROM.

OPTION 1 VALUE = \_\_\_\_\_ IS: L<sub>1</sub> I/O PORT  
 OPTION 2 VALUE = \_\_\_\_\_ IS: L<sub>0</sub> I/O PORT  
 OPTION 3 VALUE = \_\_\_\_\_ IS: SI INPUT  
 OPTION 4 VALUE = \_\_\_\_\_ IS: SO OUTPUT  
 OPTION 5 VALUE = \_\_\_\_\_ IS: SK OUTPUT  
 OPTION 6 VALUE = \_\_\_\_\_ IS: IN<sub>0</sub> INPUT  
 OPTION 7 VALUE = \_\_\_\_\_ IS: IN<sub>3</sub> INPUT  
 OPTION 8 VALUE = \_\_\_\_\_ IS: G<sub>0</sub> I/O PORT  
 OPTION 9 VALUE = \_\_\_\_\_ IS: G<sub>1</sub> I/O PORT  
 OPTION 10 VALUE = \_\_\_\_\_ IS: G<sub>2</sub> I/O PORT  
 OPTION 11 VALUE = \_\_\_\_\_ IS: G<sub>3</sub> I/O PORT  
 OPTION 12 VALUE = \_\_\_\_\_ IS: H<sub>0</sub> I/O PORT  
 OPTION 13 VALUE = \_\_\_\_\_ IS: H<sub>1</sub> I/O PORT  
 OPTION 14 VALUE = \_\_\_\_\_ IS: H<sub>2</sub> I/O PORT  
 OPTION 15 VALUE = \_\_\_\_\_ IS: H<sub>3</sub> I/O PORT  
 OPTION 16 VALUE = \_\_\_\_\_ IS: D<sub>3</sub> OUTPUT  
 OPTION 17 VALUE = \_\_\_\_\_ IS: D<sub>2</sub> OUTPUT  
 OPTION 18 VALUE = \_\_\_\_\_ IS: D<sub>1</sub> OUTPUT  
 OPTION 19 VALUE = \_\_\_\_\_ IS: D<sub>0</sub> OUTPUT  
 OPTION 20 VALUE = 0 IS: GROUND PIN  
 OPTION 21 VALUE = \_\_\_\_\_ IS: CKO PIN  
 OPTION 22 VALUE = \_\_\_\_\_ IS: CKI INPUT  
 OPTION 23 VALUE = \_\_\_\_\_ IS: RESET INPUT  
 OPTION 24 VALUE = \_\_\_\_\_ IS: R<sub>7</sub> I/O PORT  
 OPTION 25 VALUE = \_\_\_\_\_ IS: R<sub>6</sub> I/O PORT

OPTION 26 VALUE = \_\_\_\_\_ IS: R<sub>5</sub> I/O PORT  
 OPTION 27 VALUE = \_\_\_\_\_ IS: R<sub>4</sub> I/O PORT  
 OPTION 28 VALUE = \_\_\_\_\_ IS: R<sub>3</sub> I/O PORT  
 OPTION 29 VALUE = \_\_\_\_\_ IS: R<sub>2</sub> I/O PORT  
 OPTION 30 VALUE = \_\_\_\_\_ IS: R<sub>1</sub> I/O PORT  
 OPTION 31 VALUE = \_\_\_\_\_ IS: R<sub>0</sub> I/O PORT  
 OPTION 32 VALUE = \_\_\_\_\_ IS: L<sub>7</sub> I/O PORT  
 OPTION 33 VALUE = \_\_\_\_\_ IS: L<sub>6</sub> I/O PORT  
 OPTION 34 VALUE = \_\_\_\_\_ IS: L<sub>5</sub> I/O PORT  
 OPTION 35 VALUE = \_\_\_\_\_ IS: L<sub>4</sub> I/O PORT  
 OPTION 36 VALUE = \_\_\_\_\_ IS: IN<sub>1</sub> INPUT  
 OPTION 37 VALUE = \_\_\_\_\_ IS: IN<sub>2</sub> INPUT  
 OPTION 38 VALUE = \_\_\_\_\_ IS: L<sub>3</sub> I/O PORT  
 OPTION 39 VALUE = \_\_\_\_\_ IS: L<sub>2</sub> I/O PORT  
 OPTION 40 VALUE = 0 IS: V<sub>CC</sub>  
 OPTION 41 VALUE = \_\_\_\_\_ IS: COP FUNCTION  
 OPTION 42 VALUE = \_\_\_\_\_ IS: IN INPUT LEVELS  
 OPTION 43 VALUE = \_\_\_\_\_ IS: G INPUT LEVELS  
 OPTION 44 VALUE = \_\_\_\_\_ IS: L INPUT LEVELS  
 OPTION 45 VALUE = \_\_\_\_\_ IS: CKO INPUT LEVELS  
 OPTION 46 VALUE = \_\_\_\_\_ IS: SI INPUT LEVELS  
 OPTION 47 VALUE = \_\_\_\_\_ IS: R INPUT LEVELS  
 OPTION 48 VALUE = \_\_\_\_\_ IS: H INPUT LEVELS  
 OPTION 49 VALUE = \_\_\_\_\_ IS: NO OPTION  
 OPTION 50 VALUE = \_\_\_\_\_ IS: COP BONDING

### Note on L and R I/O Port Options

If L and R I/O Ports are used as inputs, the following must be observed:

- a. Open-Drain output (selection 1) is allowed only if external pull-up is provided.
- b. If L and R output ports are disabled when reading, an external pull-up is required unless selections 4, 5, 6, or 7 are chosen.
- c. If L output port is enabled, selections 3 and 7 are not allowed.
- d. If R output port is enabled, selections 2, 3, 6, and 7 are not allowed.

### Test Mode (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed COP440. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

- a. RAM and Internal Logic Test Mode (SI = 1)
- b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.