National Semiconductor

PRELIMINARY

COP888CFP/COP884CFP
Single-Chip microCMOS Microcontroller

General Description

The COP888CFP and COP884CFP are piggyback versions of the COP888CF and COP884CF. These two devices are identical except that the piggyback device has been placed permanently in ROMless mode so that program memory is only accessed externally. The device package incorporates circuitry and a socket on top of the package to accommodate a piggyback EPROM such as an NMC27C64. With the addition of the EPROM, the COP888CFP/COP884CFP perform like their masked equivalent. (Continued)

Features

- Low cost 8-bit microcontroller
- Fully static CMOS
- 1 μs instruction cycle time
- 128 bytes on-board RAM
- Single supply operation: 4.5V–5.5V
- 8-channel A/D converter with prescaler and both differential and single ended modes
- MICROWIRE/PLUS™ serial I/O
- WatchDog and Clock Monitor logic
- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)
- Versatile instruction set
- Ten multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Two Timers (each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- Package: 40 N or 28 N
  - — 40 N with 33 I/O pins
  - — 28 N with 21 I/O pins
- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Real time emulation and full program debug offered by National's Development Systems

Block Diagram

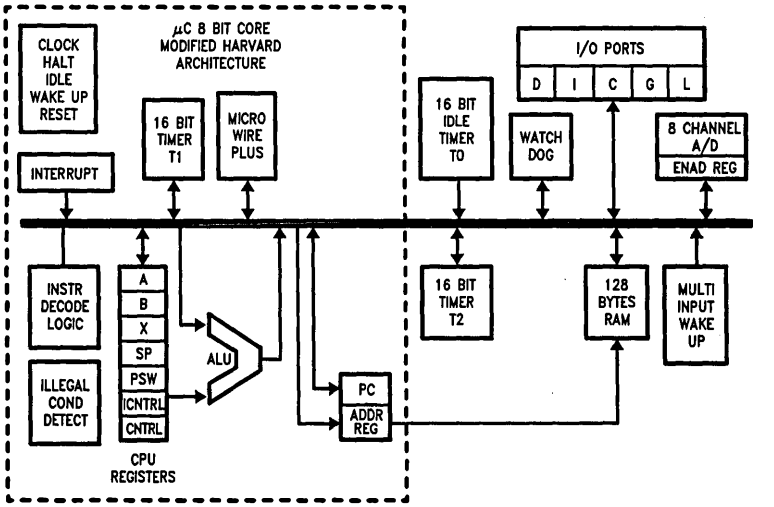

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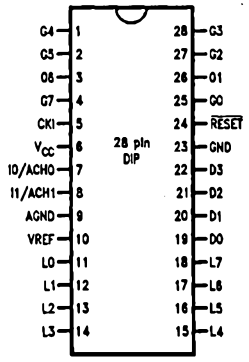
FIGURE 1. COP888CFP Block Diagram

General Description (Continued)

The COP888CFP and COP884CFP are fully static parts, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, two 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), an 8-channel, 8-bit A/D converter with both differential and single ended modes, and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The COP888CF and COP884CFP operate over a voltage range of 4.5V to 5.5V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 μs per instruction rate.

Connection Diagrams

Dual-In-Line Package



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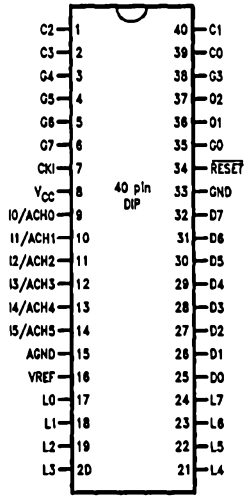
Top View

Order Number COP884CPF-XE

Dual-In-Line Package



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Top View

Order Number COP888CPF-XE

FIGURE 2. COP888CFP Connection Diagrams

COP888CFP Pinouts for 28- and 40-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.
L0	I/O	MIWU		11	17
L1	I/O	MIWU		12	18
L2	I/O	MIWU		13	19
L3	I/O	MIWU		14	20
L4	I/O	MIWU	T2A	15	21
L5	I/O	MIWU	T2B	16	22
L6	I/O	MIWU		17	23
L7	I/O	MIWU		18	24
G0	I/O	INT		25	35
G1	WDOUT			26	36
G2	I/O	T1B		27	37
G3	I/O	T1A		28	38
G4	I/O	SO		1	3
G5	I/O	SK		2	4
G6	I	SI		3	5
G7	I/CKO	HALT Restart		4	6
D0	O			19	25
D1	O			20	26
D2	O			21	27
D3	O			22	28
I0	I	ACH0		7	9
I1	I	ACH1		8	10
I2	I	ACH2			11
I3	I	ACH3			12
I4	I	ACH4			13
I5	I	ACH5			14
D4	O				29
D5	O				30
D6	O				31
D7	O				32
C0	I/O				39
C1	I/O				40
C2	I/O				1
C3	I/O				2
V_{REF}	$+V_{REF}$			10	16
AGND	AGND			9	15
V_{CC}				6	8
GND				23	33
CKI				5	7
$\overline{RESET}$				24	34

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
ESD Susceptibility (Note 4)	2000V
Total Current into V_{CC} Pin (Source)	100 mA
Total Current out of GND Pin (Sink)	110 mA
Storage Temperature Range	−65°C to +140°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 1)	Peak-to-Peak			0.1 V_{CC}	V
Supply Current (Note 2) CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			100	mA
HALT Current (Note 3)	V_{CC} = 5.5V, CKI = 0 MHz			80	mA
IDLE Current CKI = 10 MHz	V_{CC} = 5.5V, t_c = 1 μs			90	mA
Input Levels					
$\overline{RESET}$					
Logic High		0.8 V_{CC}			V
Logic Low				0.2 V_{CC}	V
CKI (External and Crystal Osc. Modes)					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
All Other Inputs					
Logic High		0.7 V_{CC}			V
Logic Low				0.2 V_{CC}	V
Hi-Z Input Leakage	V_{CC} = 5.5V	−2		+2	μA
Input Pullup Current	V_{CC} = 5.5V	40		250	μA
G and L Port Input Hysteresis			0.05 V_{CC}		V
Output Current Levels					
D Outputs					
Source	V_{CC} = 4.5V, V_{OH} = 3.3V	0.4			mA
Sink	V_{CC} = 4.5V, V_{OL} = 1V	10			mA
All Others					
Source (Weak Pull-Up Mode)	V_{CC} = 4.5V, V_{OH} = 2.7V	10		100	μA
Source (Push-Pull Mode)	V_{CC} = 4.5V, V_{OH} = 3.3V	0.4			mA
Sink (Push-Pull Mode)	V_{CC} = 4.5V, V_{OL} = 0.4V	1.6			mA
TRI-STATE Leakage		−2		+2	μA

Note 1: Rate of voltage change must be less then 0.5 V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}, L and G ports in the TRI-STATE mode and tied to ground, all outputs low and tied to ground. If the A/D is not being used and minimum standby current is desired, V_{REF} should be tied to AGND (effectively shorting the Reference resistor). The clock monitor is disabled.

Note 4: Human body model, 100 pF through 1500Ω.

DC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Allowable Sink/Source Current per Pin D Outputs (Sink) All others				 15 3	 mA mA
Maximum Input Current without Latchup (Note 7)	$T_A = 25°C$			±100	mA
RAM Retention Voltage, V_r	500 ns Rise and Fall Time (Min)	2			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

A/D Converter Specifications $V_{CC} = 5V \pm 10\%$ $(V_{SS} - 0.050V) \le$ Any input $\le (V_{CC} + 0.050V)$

Parameter	Conditions	Min	Typ	Max	Units
Resolution				8	Bits
Reference Voltage Input	AGND = 0V	3		V_{CC}	V
Absolute Accuracy	$V_{REF} = V_{CC}$			±1	LSB
Non-Linearity	$V_{REF} = V_{CC}$ Deviation from the Best Straight Line			±½	LSB
Differential Non-Linearity	$V_{REF} = V_{CC}$			±½	LSB
Input Reference Resistance		1.6		4.8	kΩ
Common Mode Input Range (Note 8)		AGND		V_{REF}	V
DC Common Mode Error				±¼	LSB
Off Channel Leakage Current			1		μA
On Channel Leakage Current			1		μA
A/D Clock Frequency (Note 6)		0.1		1.67	MHz
Conversion Time (Note 5)			12		A/D Clock Cycles

Note 5: Conversion Time includes sample and hold time.

Note 6: See Prescaler description.

Note 7: Except pin G7: −60 mA to +100 mA (sampled but not 100% tested).

Note 8: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input. The diodes will forward conduct for analog input voltages below ground or above the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (t_c)					
Crystal, Resonator	$4.5V \le V_{CC} \le 5.5V$	1		DC	μs
R/C Oscillator	$4.5V \le V_{CC} \le 5.5V$	3		DC	μs
CKI Clock Duty Cycle (Note 10)	f_r = Max	40		60	%
Rise Time (Note 10)	f_r = 10 MHz Ext Clock			5	ns
Fall Time (Note 10)	f_r = 10 MHz Ext Clock			5	ns
Inputs					
t_{SETUP}	$4.5V \le V_{CC} \le 5.5V$	200			ns
t_{HOLD}	$4.5V \le V_{CC} \le 5.5V$	60			ns
Output Propagation Delay	R_L = 2.2k, C_L = 100 pF				
t_{PD1}, t_{PD0}					
SO, SK	$4.5V \le V_{CC} \le 5.5V$			0.7	μs
All Others	$4.5V \le V_{CC} \le 5.5V$			1	μs
MICROWIRE™ Setup Time (t_{UWS})		20			ns
MICROWIRE Hold Time (t_{UWH})		56			ns
MICROWIRE Output Propagation Delay (t_{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		1			t_c
Interrupt Input Low Time		1			t_c
Timer Input High Time		1			t_c
Timer Input Low Time		1			t_c
Reset Pulse Width		1			μs

Note 10: Parameter sample but not 100% tested.

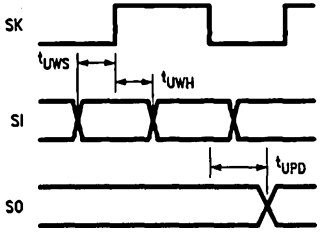

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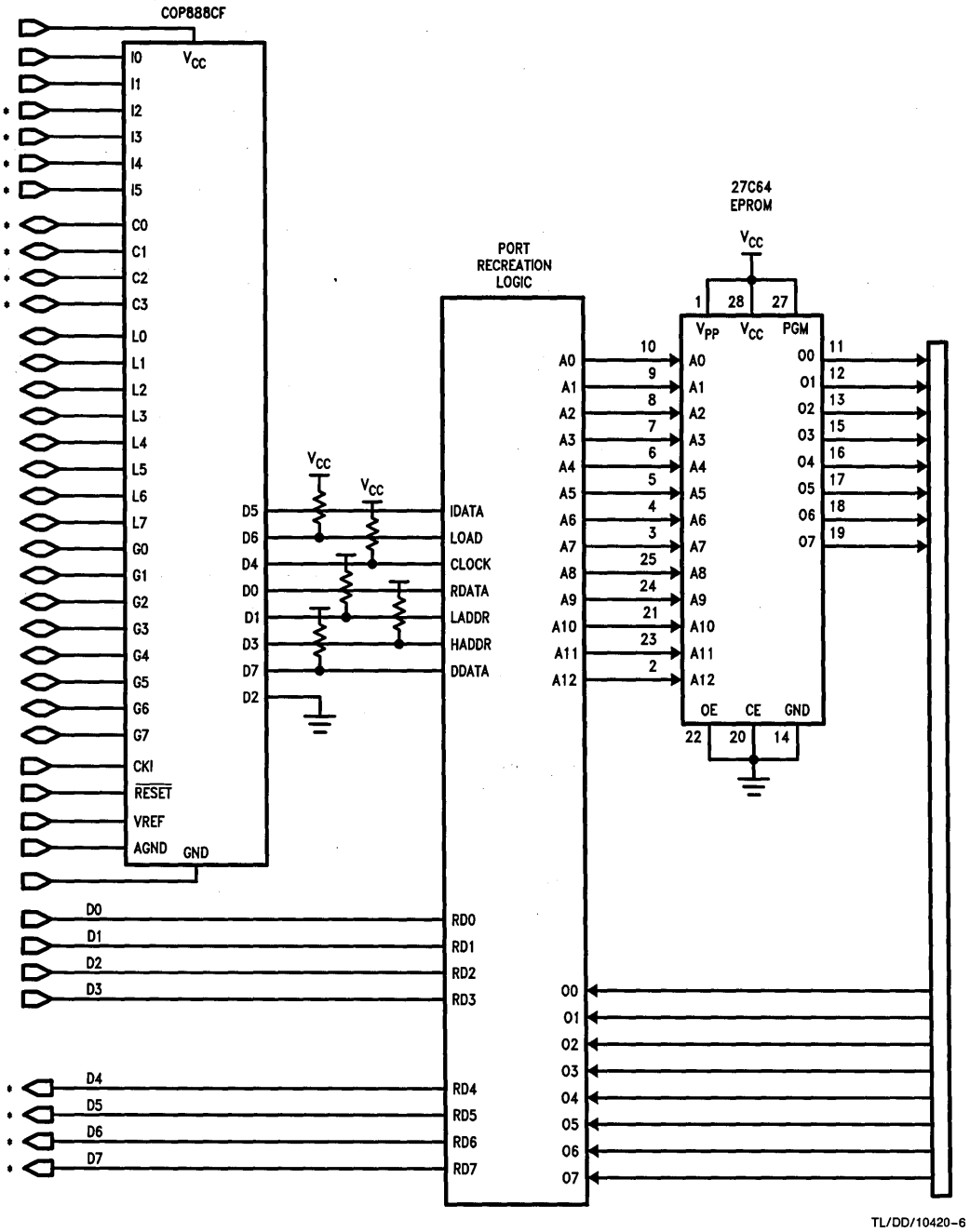
FIGURE 3. MICROWIRE/PLUS Timing

Connection Diagram



All resistors are 330Ω ±20%

(Not needed if the CKI frequency is less than 5 MHz)

*Not available on 28-pin package.

FIGURE 4

Oscillator Circuits

The chip can be driven by a clock input on the CKI input pin which can be between DC and 10 MHz. The CKO output clock is on pin G7 (crystal configuration). The CKI input frequency is divided down by 10 to produce the instruction cycle clock ($1/t_C$).

Figure 5 shows the Crystal and R/C diagrams.

CRYSTAL OSCILLATOR

CKI and CKO can be connected to make a closed loop crystal (or resonator) controlled oscillator.

Table I shows the component values required for various standard crystal values.

R/C OSCILLATOR (SPECIAL ORDER ONLY)

By selecting CKI as a single pin oscillator input, a single pin R/C oscillator circuit can be connected to it. CKO is available as a general purpose input, and/or HALT restart pin.

Table II shows the variation in the oscillator frequencies as functions of the component (R and C) values.

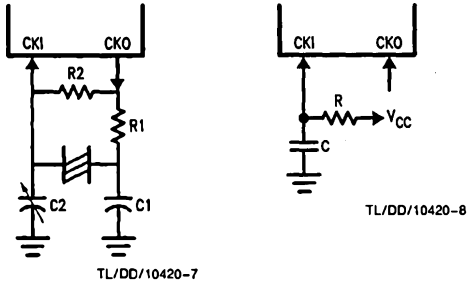


FIGURE 5. Crystal and R/C Oscillator Diagrams

TABLE I. Crystal Oscillator Configuration
T_A = 25°C, V_{CC} = 5V

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)
0	1	30	30–36	10
0	1	30	30–36	4
0	1	200	100–150	0.455

TABLE II. R/C Oscillator Configuration
T_A = 25°C, V_{CC} = 5V

R (kΩ)	C (pF)	CKI Freq (MHz)	Instr. Cycle (μs)
3.3	82	2.8 to 2.2	3.6 to 4.5
5.6	100	1.5 to 1.1	6.7 to 9
6.8	100	1.1 to 0.8	9 to 12.5

EPROM Selection

The COP888CFP and COP884CFP are the piggyback versions of the COP888CF and COP884CF microcontrollers, (see Table IV). With the addition of an EPROM this part is the functional equivalent of the masked version.

Table III lists the minimum access times for a given instruction cycle time of the microcontroller. At high speeds an NMC57C64 (an 8k byte device) or any comparable EPROM must be used.

TABLE III. EPROM Selection

EPROM Minimum Access Time	COP Instruction Cycle Time
120 ns	1.00 μs
150 ns	1.10 μs
200 ns	1.27 μs
250 ns	1.44 μs
300 ns	1.60 μs
400 ns	1.94 μs

TABLE IV. Clock Options per Package

Order Part Number	Clock Option
COP888CFP-XE	Crystal Oscillator Divide by 10 with Halt Enabled, this is identical to the masked COP888CF and COP884CF with Option 1 = 1; Option 2 = 1.

Development Support

MOLE™ DEVELOPMENT SYSTEM

The MOLE (Microcomputer On Line Emulator) is a low cost development system and emulator for all microcontroller products. These include COPs™ microcontrollers and the HPC family of products. The MOLE consists of a BRAIN Board, Personality Board and optional host software.

The purpose of the MOLE is to provide the user with a tool to write and assemble code, emulate code for the target microcontroller and assist in both software and hardware debugging of the system.

It is a self contained computer with its own firmware which provides for all system operation, emulation control, communication, PROM programming and diagnostic operations.

It contains three serial ports to optionally connect to a terminal, a host system, a printer or a modem, or to connect to other MOLEs in a multi-MOLE environment.

MOLE can be used in either a stand alone mode or in conjunction with a selected host system using PC-DOS communicating via a RS-232 port.

How to Order

To order a complete development package, select the section for the microcontroller to be developed and order the parts listed.

Development Tools Selection Table

Microcontroller	Order Part Number	Description	Includes	Manual Number
COP888	MOLE-BRAIN	Brain Board	Brain Board Users Manual	420408188-001
	MOLE-COP8-PB2	Personality Board	COP888 Personality Board Users Manual	420420084-001
	MOLE-COP8-IBM	Assembler Software for IBM	COP800 Software Users Manual and Software Disk PC-DOS Communications Software Users Manual	424410527-001 420040416-001
	420411060-001	Programmer's Manual		420411060-001

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications group. The Dial-A-Helper is an Electronic Bulletin Board Information system and additionally, provides the capability of remotely accessing the MOLE development system at a customer site.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

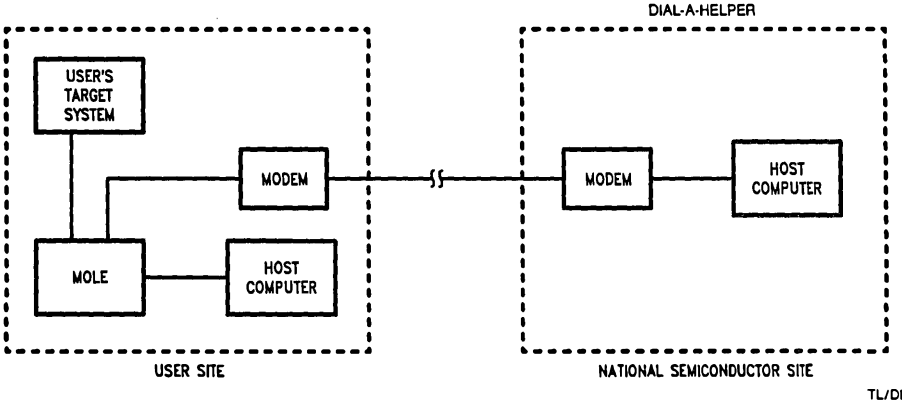
Order P/N: MOLE-DIAL-A-HLP

Information System Package Contents
- Dial-A-Helper User Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factor applications support. If a user is having difficulty in operating a MOLE, he can leave messages on our electronic bulletin board, which we will respond to, or under extraordinary circumstances he can arrange for us to actually take control of his system via modem for debugging purposes.

Voice:	(408) 721-5582	
Modem:	(408) 739-1162	
	Baud:	300 or 1200 Baud
	Set-Up:	Length: 8-Bit
		Parity: None
		Stop Bit: 1
	Operation:	24 Hours, 7 Days



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COP888CFP Dimension Diagrams

28-Pin Package

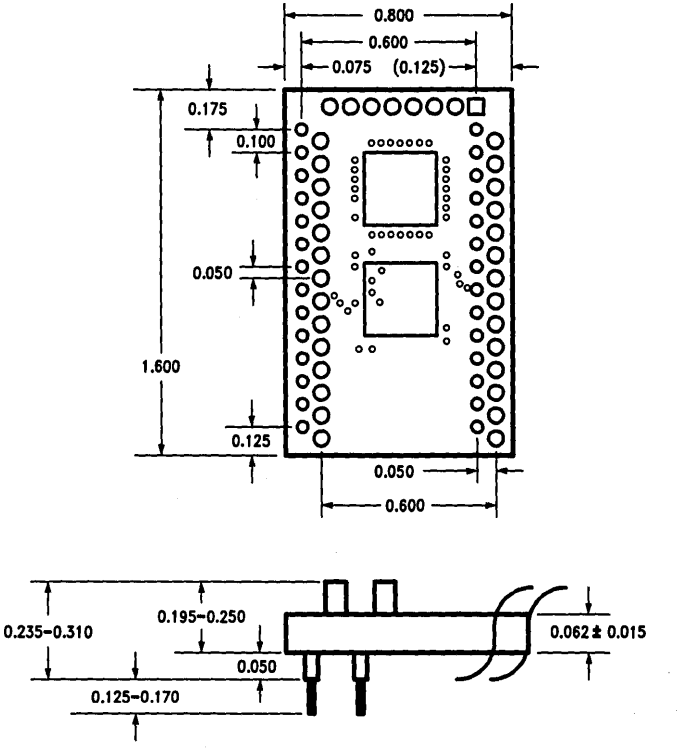

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FIGURE 6

COP888CFP Dimension Diagrams (Continued)

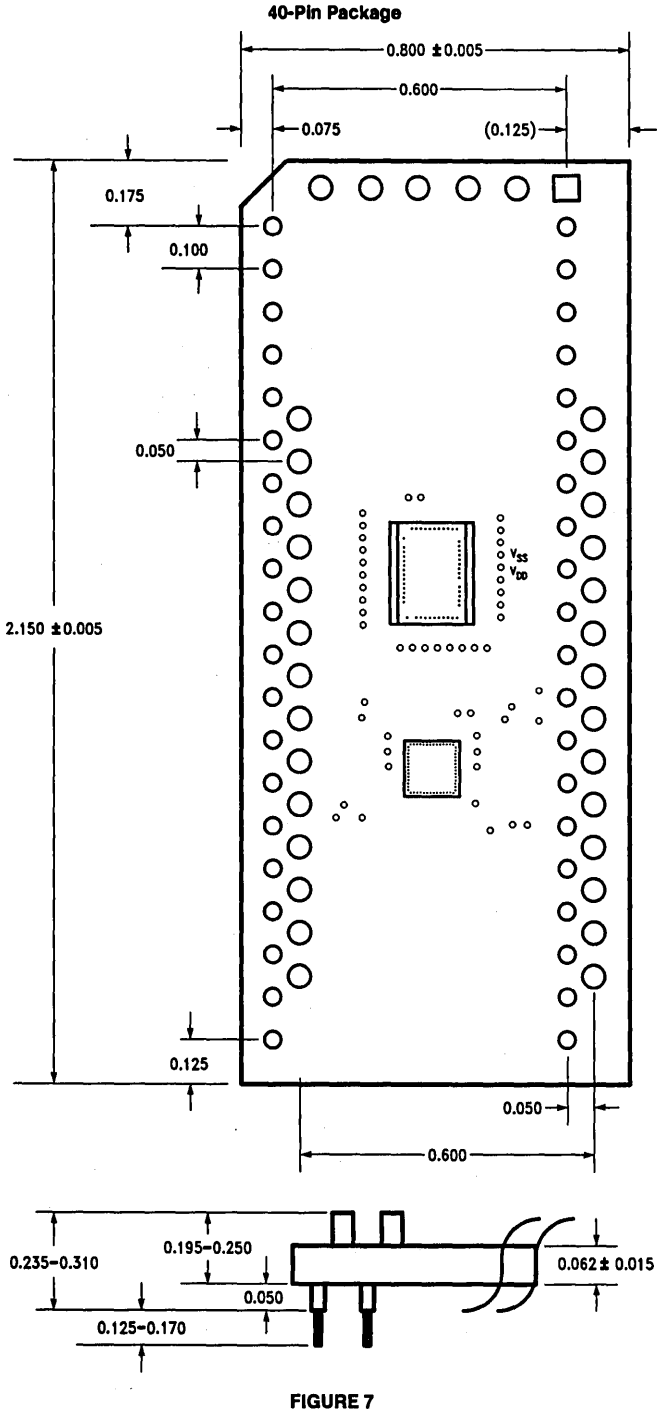

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FIGURE 7